P2I2305NZ

3.3V 1:5 Clock Buffer

ON Semiconductor®

http://onsemi.com

Functional Description

P2I2305NZ is a low cost high speed buffer designed to accept one clock input and distribute up to five clocks in mobile PC systems and desktop PC systems. The device operates at 3.3 V and outputs can run up to 133.33 MHz.

P2I2305NZ is designed for low EMI and power optimization and consumes less than 32 mA at 66.6 MHz, making it ideal for the low−power requirements of mobile systems. It is available in an 8−pin SOIC Package over Industrial temperature range.

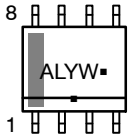
Features

- One−Input to Five−Output Buffer/Driver
- Buffers All Frequencies from DC to 133.33 MHz
- Low Power Consumption for Mobile Applications
- Less than 32 mA at 66.6 MHz with Unloaded Outputs
- Input−Output delay: 6 nS(max)
- Output−Output skew less than 250 pS
- Supply Voltage: 3.3 V ± 0.3 V
- Operating Temperature Range: −40°C to +85°C
- 8−pin SOIC Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAM



SOIC−8
D SUFFIX
CASE 751



xx	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

Block Diagram

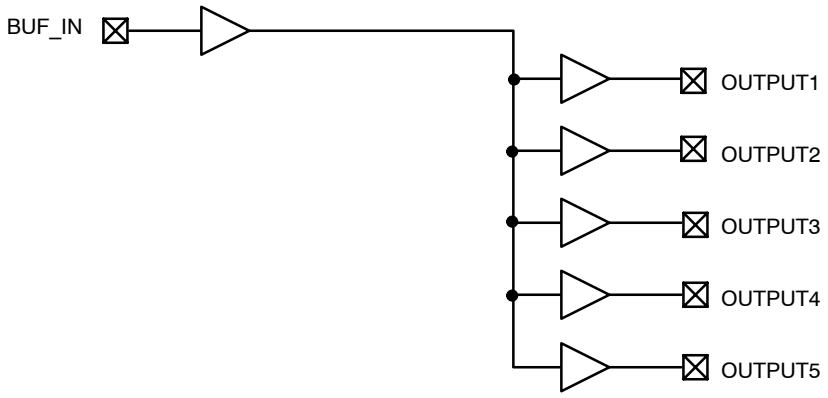


Figure 1. Block Diagram

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PIN CONFIGURATION

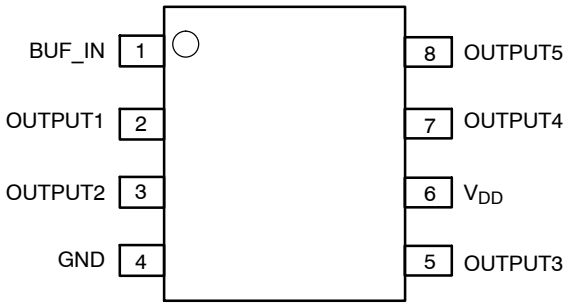


Figure 2. P2I2305NZ Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

Pin#	Pin Name	Description
6	V_{DD}	3.3 V, Supply Voltage
4	GND	Ground
1	BUF_IN	Clock Input
2, 3, 5, 7, 8	OUTPUT [1:5]	Clock Outputs

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Supply Voltage to Ground Potential	−0.5	+4.6	V
DC Input Voltage (Except REF)	−0.5	V_{DD} + 0.5	V
DC Input Voltage (REF)	−0.5	7	V
Storage Temperature	−65	+150	°C
Max. Soldering Temperature (10 sec)		260	°C
Junction Temperature		150	°C
Static Discharge Voltage (As per JEDEC STD22− A114−B)		2000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. OPERATING CONDITIONS

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature	−40	85	°C
C_L	Load Capacitance, F_{out} < 100 MHz		30	pF
	Load Capacitance, 100 MHz < F_{out} < 133.33 MHz		15	pF
C_{IN}	Input Capacitance		7	pF
BUF_IN, OUTPUT [1:5]	Operating Frequency	DC	133.33	MHz
t_{PU}	Power−up time for all V_{DD}'s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	mS

Table 4. DC CHARACTERISTICS V_{DD} = 3.0 V to 3.6 V, GND = 0 V, T_A = −40°C to +85°C

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW Voltage (Note 1)			0.8	V
V_{IH}	Input HIGH Voltage (Note 1)		2.2		V
I_{IL}	Input LOW Current	V_{IN} = 0 V		50.0	μA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		100.0	μA
V_{OL}	Output LOW Voltage (Note 2)	I_{OL} = 12 mA		0.4	V
V_{OH}	Output HIGH Voltage (Note 2)	I_{OH} = −12 mA	2.4		V
I_{DD}	Supply Current	Unloaded outputs at 66.66 MHz		32	mA

1. BUF_IN input has a threshold voltage of $V_{DD}/2$.
2. Parameter is guaranteed by design and characterization. It is not tested in production.

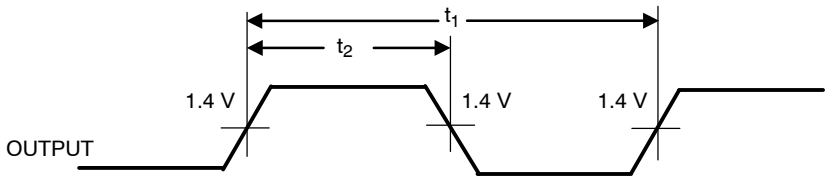
Table 5. AC CHARACTERISTICS (Note 3) V_{DD} = 3.0 V to 3.6 V, GND = 0 V, T_A = −40°C to +85°C

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_3	Rise Time (Note 4)	Measured between 0.8 V and 2.0 V		1.5	2	nS
t_4	Fall Time (Note 4)	Measured between 2.0 V and 0.8 V		1.5	2	nS
t_D	Duty Cycle (Note 4) = $t_2 \div t_1$	Measured at 1.4 V (For an Input Clock Duty Cycle 50%)	45	50	55	%
t_5	Output to Output Skew (Note 4)	All outputs equally loaded			±250	pS
t_6	Propagation Delay, BUF_IN Rising Edge to OUTPUT Rising Edge (Note 4)	Measured at $V_{DD}/2$		4	6	nS

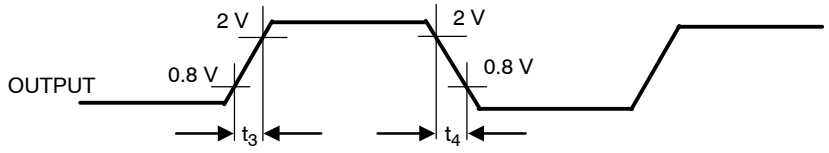
3. All parameters specified with loaded outputs.
4. Parameter is guaranteed by design and characterization. It is not tested in production.

SWITCHING WAVEFORMS

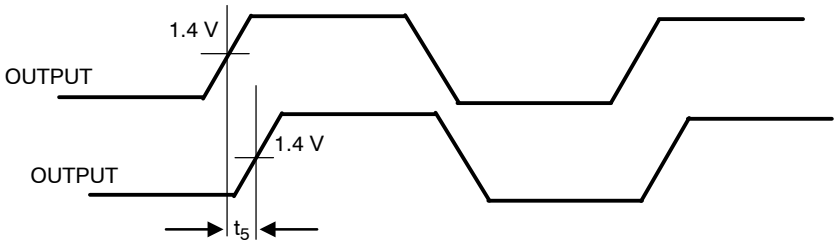
Duty Cycle Timing



All Outputs Rise/Fall Time



Output−Output Skew



Input−Output Propagation Delay

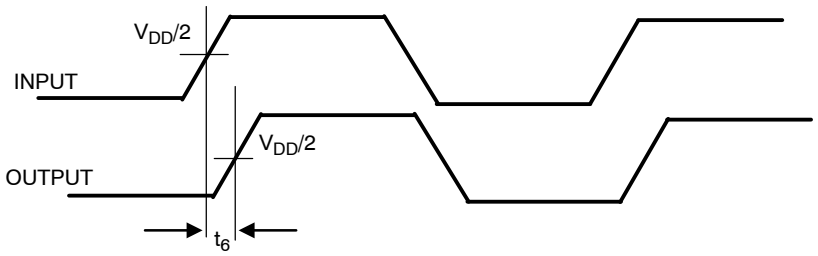


Figure 3. Switching Waveforms

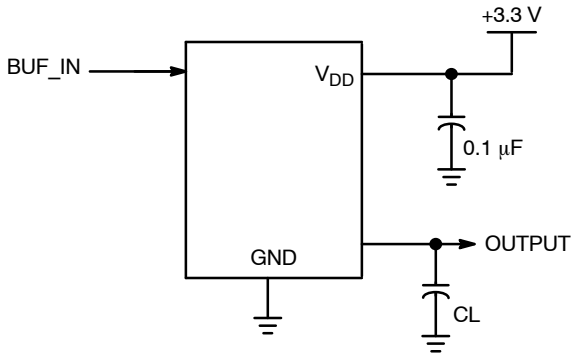


Figure 4. Test Circuit

ORDERING INFORMATION

Device	Marking	Package	Shipping†
P2I2305NZG−08SR	ADB	SOIC−8 (Pb−Free)	2500 / Tape & Reel

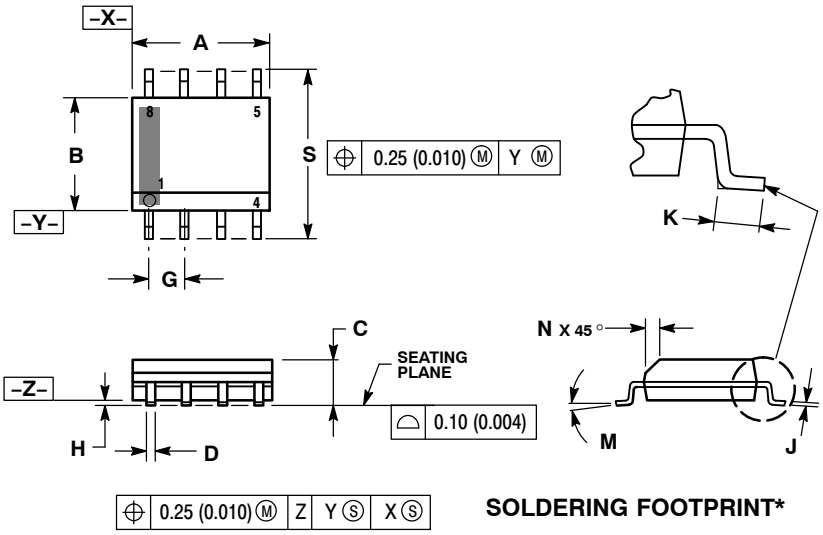
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb−Free.

P2I2305NZ

PACKAGE DIMENSIONS

SOIC−8 NB
CASE 751−07
ISSUE AK

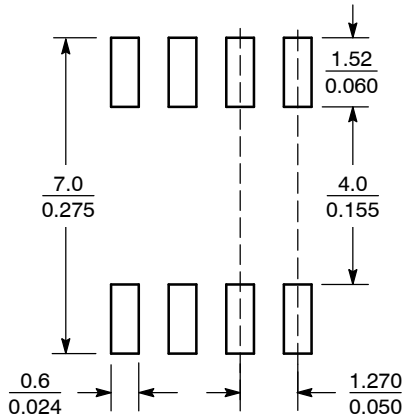


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

0.25 (0.010) M Z Y S X S

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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