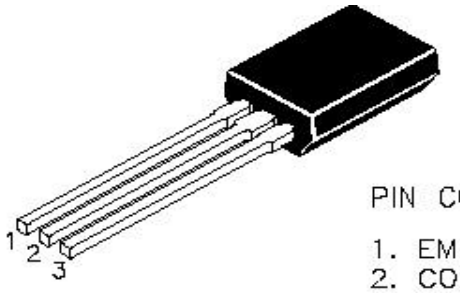
SILICON PLANAR EPITAXIAL TRANSISTORS

CSAL1013 PNP
CSCL2383 NPN

TO-92L
Plastic Package



PIN CONFIGURATION:–

1. EMITTER
2. COLLECTOR
3. BASE

Colour TV Audio output and Vertical Deflecfion Output

ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	SYMBOL	VALUE	UNITS
Collector Base Voltage	V_{CBO}	160	V
Collector Emitter Voltage	V_{CEO}	160	V
Emitter Base Voltage	V_{EBO}	6	V
Collector Current	I_C	1.0	A
Base Current	I_B	0.5	A
Collector Power Dissipation @ T_a=25ºC	P_C	0.9	W
Junction Temperature	T_j	150	ºC
Storage Temperature	T_{stg}	- 55 to +150	ºC

ELECTRICAL CHARACTERISTICS (T_a=25ºC unless specified otherwise)

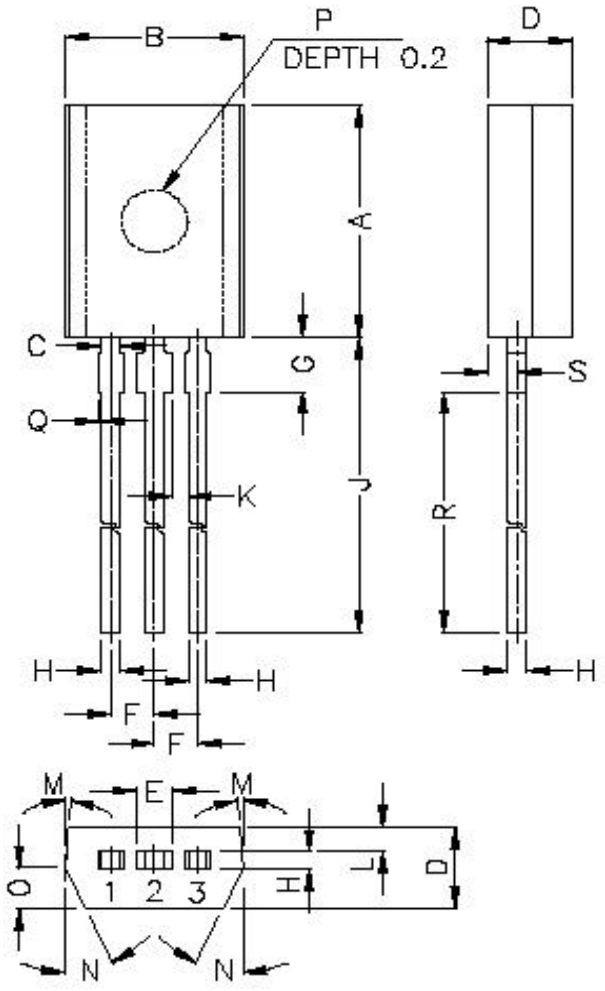
DESCRIPTION	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Collector Cut Off Current	I_{CBO}	V_{CB}=150V, I_E = 0			1.0	µA
Emitter Cut Off Current	I_{EBO}	V_{EB}=6V, I_C = 0			1.0	µA
Collector Emitter Voltage	V_{CEO}	I_C=10mA, I_B=0	160			V
DC Current Gain	*h_{FE}	V_{CE}=5V, I_C=200mA	60		320	
Collector Emitter Saturation Voltage	*$V_{CE\ (sat)}$	I_C=500mA, I_B=50mA			1.5	V
Base Emitter On Voltage	$V_{BE\ (on)}$	I_C=5mA, V_{CE}=5V	0.45		0.75	V
Transition Frequency	f_T	I_C=200mA, V_{CE}=5V **NPN**	20			MHz
		PNP	15			MHz
Output Capacitance	C_{ob}	I_E=0, V_{CB}=10V, f=1MHz **NPN**			20	pF
		PNP			35	pF

h_{FE} Classification	R : 60 - 120, O : 100 - 200 , Y : 160 - 320

CSAL1013_CSCL2383Rev_1 130105E

***Pulse Test: Pulse Width ≤300ms, Duty Cycle≤2%**

PACKAGE TO–92L



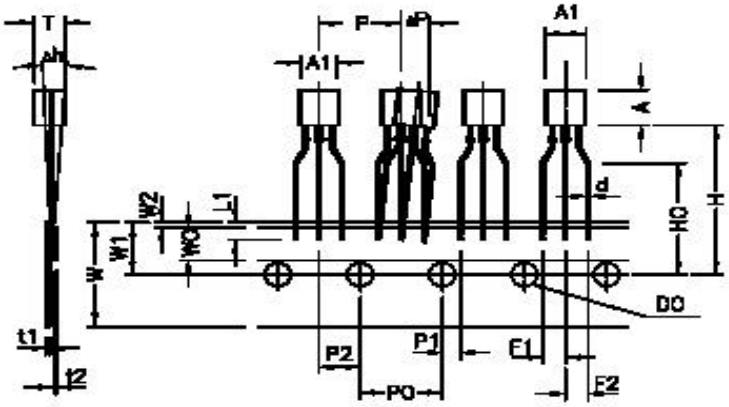
DIMENSIONS			
REF DIM	MIN	NOM	MAX
A	–	–	7.20
B	–	–	5.20
C	–	–	0.60
D	–	–	2.50
E	–	–	1.15
F	–	1.27	–
G	–	–	1.70
H	–	–	0.55
J	13.50	–	14.50
K	0.35	–	–
L	0.65	–	0.85
M	–	4°	–
N	–	25°	–
O	–	1.25	–
P	–	ø1.50	–
Q	–	–	0.10
R	12.00	–	13.00
S	–	1.00	–

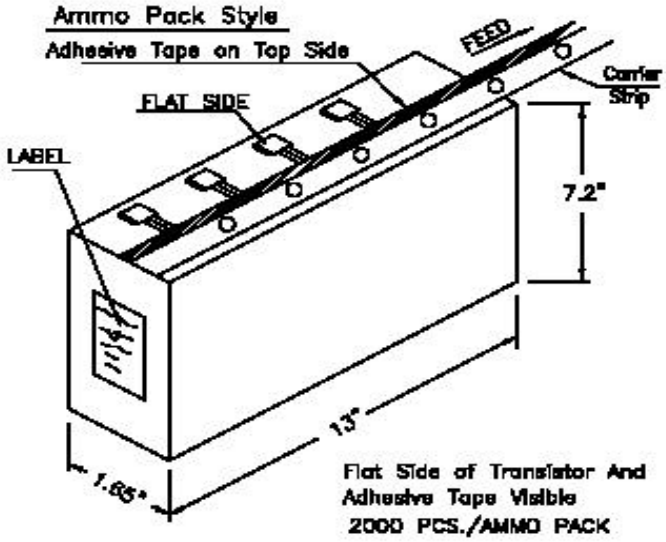
ALL DIMENSIONS ARE IN M.M.

PIN CONFIGURATION:–

1. EMITTER
2. COLLECTOR
3. BASE

TO−92L TRANSISTOR ON TAPE AND AMMO PACK





ITEM	SYMBOL	VALUE & TOLERANCE
BODY WIDTH	A1	4.9 ±0.2
BODY HEIGHT	A	8.0 ±0.2
BODY THICKNESS	T	3.9 ±0.2
LEAD WIRE DIAMETER	d	0.45 ±0.05
PITCH OF COMPONENT	P	12.7 ±0.3
FEED HOLE PITCH	P0	12.7 ±0.2
HOLE CENTER TO COMPONENT CENTER	P2	6.35 ±0.3
LEAD TO LEAD DISTANCE	F1,F2	2.5 ±0.3
COMPONENT ALIGNMENT,F−R	Δh	0 ±1.0
TYPE WIDTH	W	18.0 +1.0,−0.5
HOLE DOWN TAPE WIDTH	W0	6.0 ±0.5
HOLE POSITION	W1	9.0 ±0.5
HOLE DOWN TAPE POSITION	W2	1.0 MAX.
HEIGHT OF COMPONENT FROM TAPE CENTER	H	19.0 +2.0,−0
LEAD WIRE CLINCH HEIGHT	HO	16.0 ±0.5
LEAD WIRE (TAPE PORTION)	L1	2.5 MIN
FEED HOLE DIAMETER	D0	4.0 ±0.2
TAPED LEAD THICKNESS	t1	0.4 ±0.05
CARRIER TAPE THICKNESS	t2	0.2 ±0.05
POSITION OF HOLE	P1	3.85 ±0.3
COMPONENT ALIGNMENT	ΔP	0 ±1.0

NOTES:−

1. MAXIMUM ALIGNMENT DEVIATION BETWEEN LEADS NOT TO BE GREATER THAN 0.2 mm
2. MAXIMUM NON−CUMULATIVE VARIATION BETWEEN TAPE FEED HOLES SHALL NOT EXCEED 1 mm IN 20 PITCHES.
3. HOLDDOWN TAPE NOT TO EXCEED BEYOND THE EDGE(S) OF CARRIER TAPE AND THERE SHALL BE NO EXPOSURE OF ADHESIVE.
4. NO MORE THAN 3 CONSECUTIVE MISSING COMPONENTS IS PERMITTED.
5. A TAPE TRAILER, HAVING AT LEAST THREE FEED HOLES IS REQUIRED AFTER THE LAST COMPONENT.
6. SPLICES SHALL NOT INTERFERE WITH THE SPROCKET FEED HOLES.

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.

2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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CSAL1013_CSCL2383Rev_1 130105E