



STD20NF06

N-channel 60V - 0.032Ω - 24A - DPAK
STripFET™ II Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STD20NF06	60V	<0.040Ω	24A

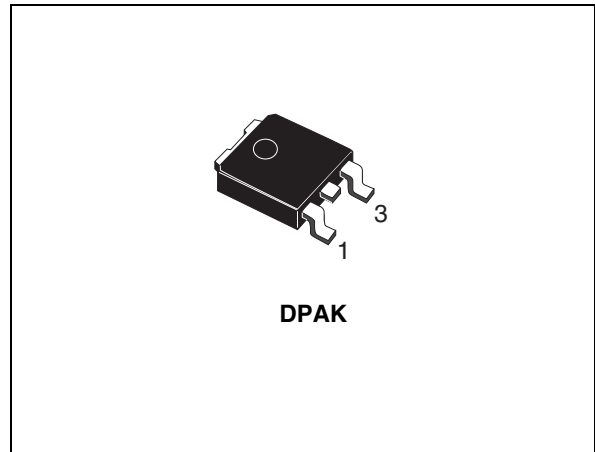
- Exceptional dv/dt capability
- Application oriented characterization
- 100% avalanche tested

Description

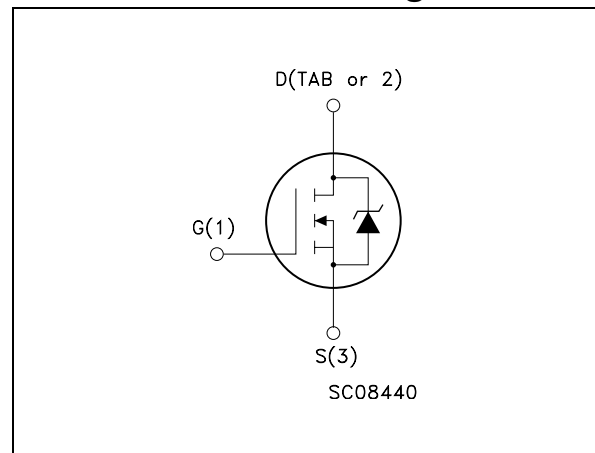
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

- Switching application



Internal schematic diagram



Order code

Part number	Marking	Package	Packaging
STD20NF06T4	D20NF06	DPAK	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	60	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20\text{ k}\Omega$)	60	V
V_{GS}	Gate- source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	24	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	17	A
$I_{DM}^{(1)}$	Drain current (pulsed)	96	A
P_{tot}	Total dissipation at $T_C = 25^\circ\text{C}$	60	W
	Derating Factor	0.4	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery avalanche energy	10	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	300	mJ
T_{stg}	Storage temperature	-55 to 175	$^\circ\text{C}$
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 24\text{A}$, $di/dt \leq 100\text{A}/\mu\text{s}$, $V_{DD} = V_{(BR)DSS}$, $T_j \leq T_{JMAX}$
3. Starting $T_j = 25^\circ\text{C}$, $I_D = 10\text{A}$, $V_{DD} = 45\text{V}$

Table 2. Thermal data

$R_{thj-case}$	Thermal resistance junction-case max	2.5	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-to ambient max	100	$^\circ\text{C}/\text{W}$
T_J	Maximum lead temperature for soldering purpose ⁽¹⁾	275	$^\circ\text{C}$

1. 1.6 mm from case, for 10 sec.

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0$	60			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 12\text{A}$		0.032	0.040	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 25\text{V}$, $I_D = 12\text{A}$		15		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$		690 170 68		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 30\text{V}$, $I_D = 10\text{A}$ $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ (see Figure 13)		10 30 30 8		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 30\text{V}$, $I_D = 20\text{A}$, $V_{GS} = 10\text{V}$, $R_G = 4.7\Omega$ (see Figure 14)		23 5 7.5	31	nC nC nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				24 96	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 24A$, $V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 20A$, $di/dt = 100A/\mu s$, $V_{DD} = 30V$, $T_j = 150^\circ C$ (see Figure 15)		65 150 4.6		ns nC A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

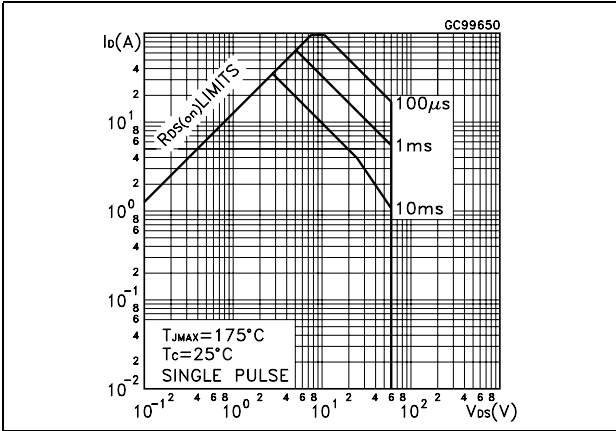


Figure 2. Thermal impedance

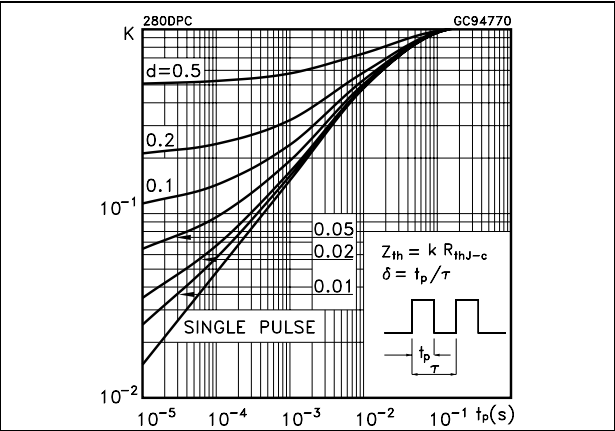


Figure 3. Output characteristics

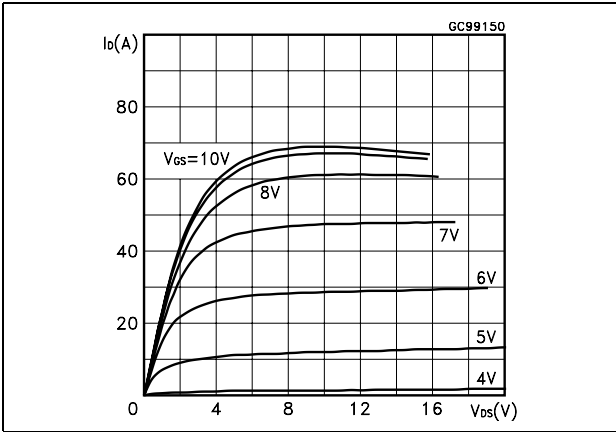


Figure 4. Transfer characteristics

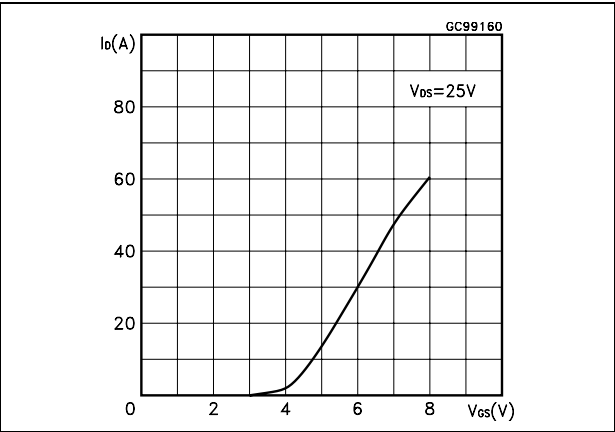


Figure 5. Transconductance

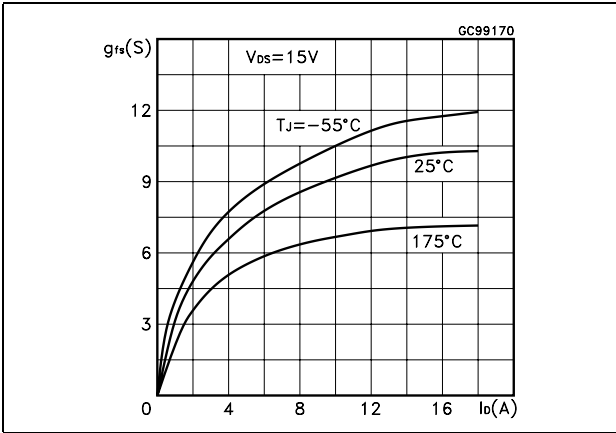


Figure 6. Static drain-source on resistance

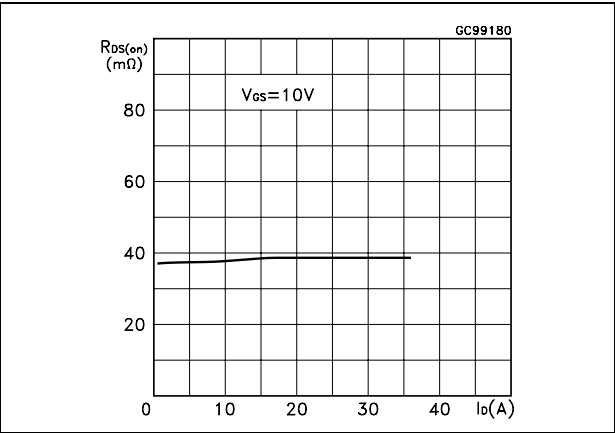


Figure 7. Gate charge vs. gate-source voltage Figure 8. Capacitance variations

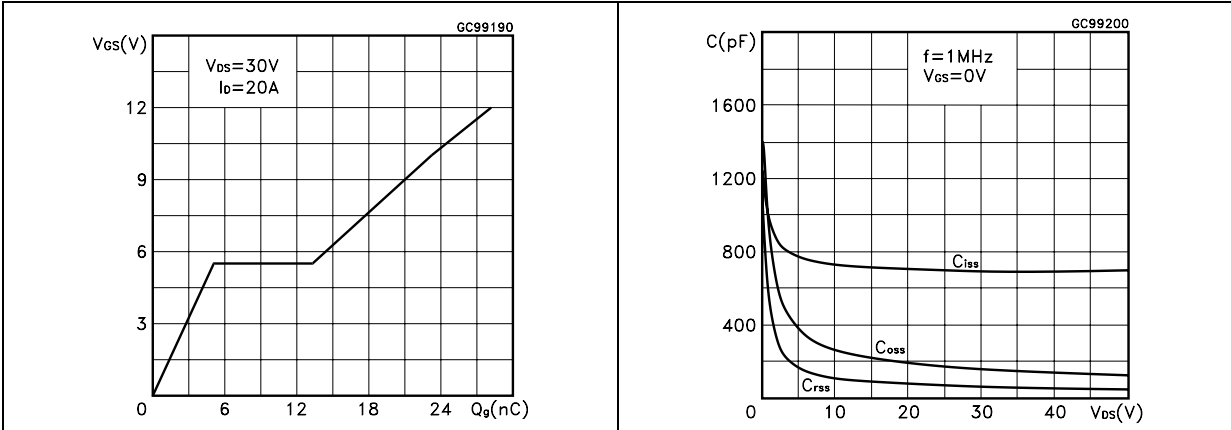


Figure 9. Normalized gate threshold voltage vs. temperature Figure 10. Normalized on resistance vs. temperature

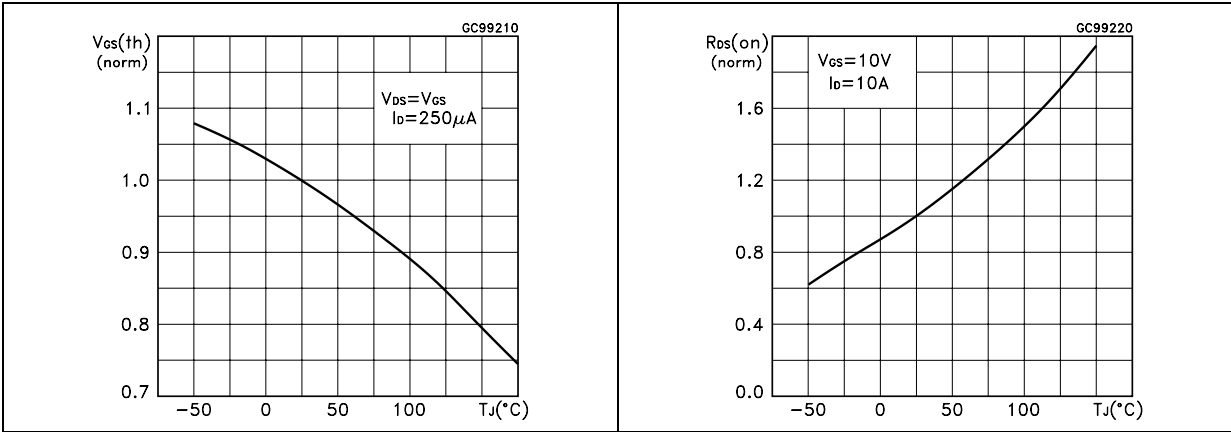
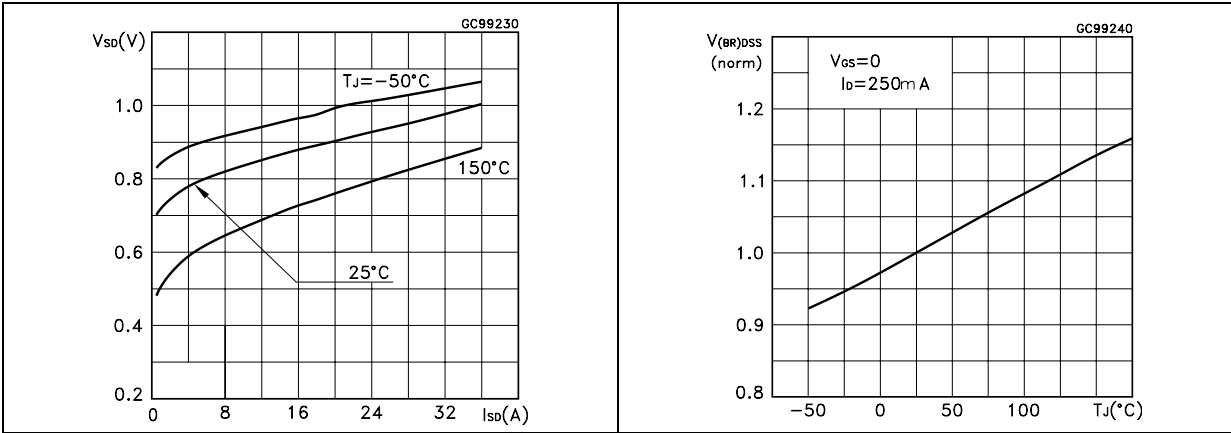


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized breakdown voltage vs. temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

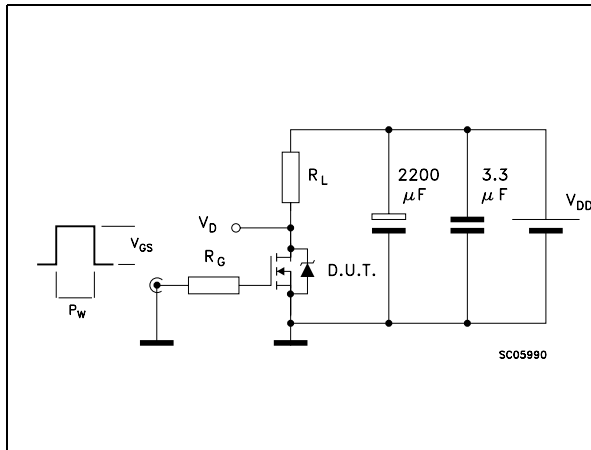


Figure 14. Gate charge test circuit

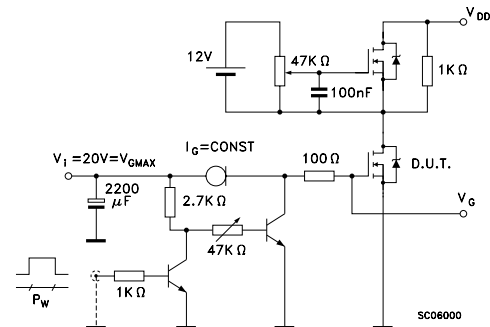


Figure 15. Test circuit for inductive load switching and diode recovery times

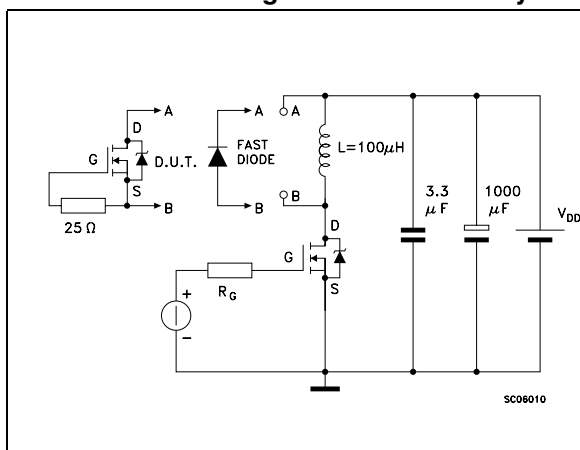


Figure 16. Unclamped Inductive load test circuit

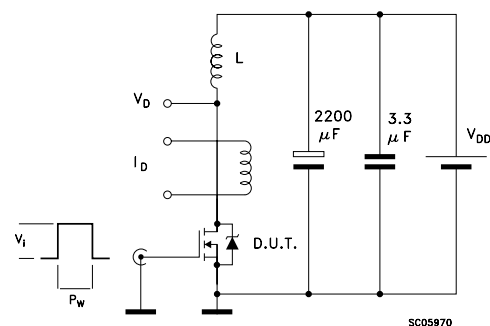


Figure 17. Unclamped inductive waveform

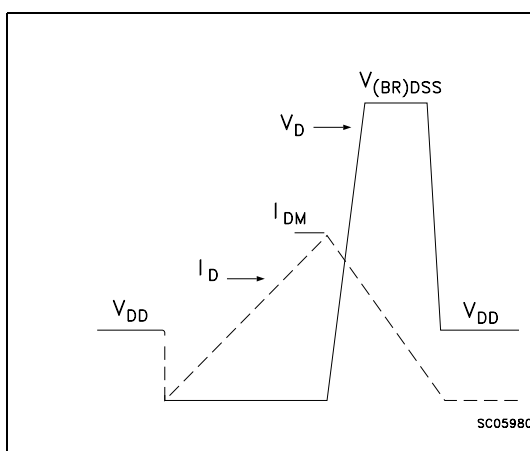
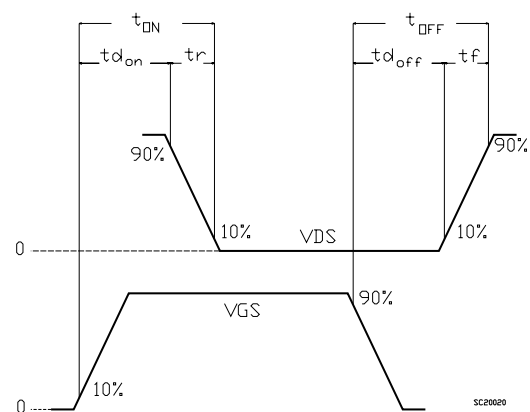


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

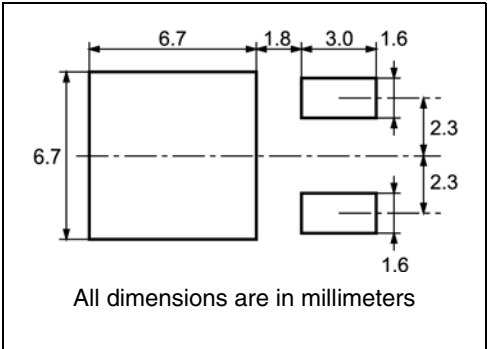
DPAK MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°

The diagram illustrates the mechanical specifications of the STD20NF06 DPAK package. It includes a top view showing dimensions A, A1, A2, B, b4, C, C2, D, D1, E, E1, e, e1, H, L, (L1), L2, L4, R, and V2. A side view shows dimensions A, A1, A2, B, b4, C, C2, D, D1, E, E1, e, e1, H, L, (L1), L2, L4, R, and V2. A detail view shows the thermal pad and the seating plane. The dimensions are defined in the table above.

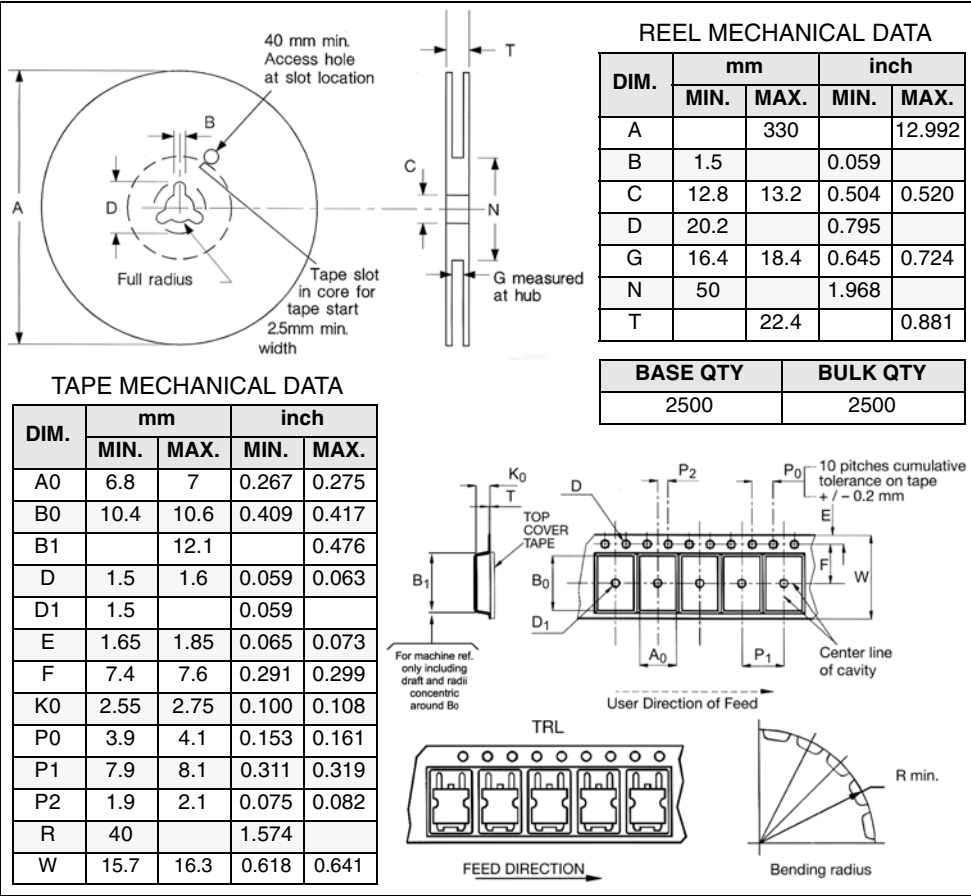
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5 Packing mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 6. Revision history

Date	Revision	Changes
22-Jun-2004	1	First release
16-Jul-2004	2	Change status from preliminary to definitive datasheet
09-Sep-2004	3	Typing error
03-Jul-2006	4	New template, no content change
20-Feb-2007	5	Typo mistake on page 1

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