S-24C02D/04D/08D/16D

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2-WIRE SERIAL E^{2}PROM

Rev.3.0_02_U

This IC is a 2-wire, low current consumption and wide range operation serial E^{2}PROM. This IC has the capacity of 2 K-bit, 4 K-bit, 8-K bit and 16 K-bit, and the organization is 256 words × 8-bit, 512 words × 8-bit, 1024 words × 8-bit and 2048 words × 8-bit, respectively. Page write and sequential read are available.

Caution **This product is intended to use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to ABLIC Inc. is indispensable.**

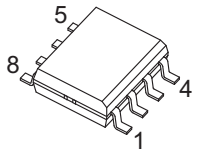
■ Features

- Operation voltage range
  Read: 1.7 V to 5.5 V
  Write: 1.7 V to 5.5 V
- Operation frequency:
  1.0 MHz max. (V_{CC} = 2.5 V to 5.5 V)
  400 kHz max. (V_{CC} = 1.7 V to 5.5 V)
- Write time: 5.0 ms max.
- Page write
  S-24C02D: 8 bytes / page
  S-24C04D: 16 bytes / page
  S-24C08D: 16 bytes / page
  S-24C16D: 16 bytes / page
- Sequential read
- Noise suppression:
  Schmitt trigger and noise filter on input pins (SCL, SDA)
- Write protect function during low power supply voltage
- Endurance: 10^6 cycle / word*1 (Ta = +25°C)
- Data retention: 100 years (Ta = +25°C)
- Memory capacity
  S-24C02D: 2 K-bit
  S-24C04D: 4 K-bit
  S-24C08D: 8 K-bit
  S-24C16D: 16 K-bit
- Write protect: 100%
- Initial delivery state: FFh
- Operation temperature range: Ta = –40°C to +85°C
- Lead-free (Sn 100%), halogen-free

***1.** For each address (Word: 8-bit)

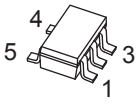
■ Packages

- 8-Pin SOP (JEDEC)



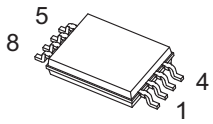
(5.0 × 6.0 × t1.75 mm)

- SOT-23-5



(2.8 × 2.9 × t1.3 mm)

- 8-Pin TSSOP

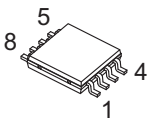


(3.0 × 6.4 × t1.1 mm)

- DFN-8(2030)

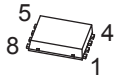
(3.0 × 2.0 × t0.5 mm)

- TMSOP-8



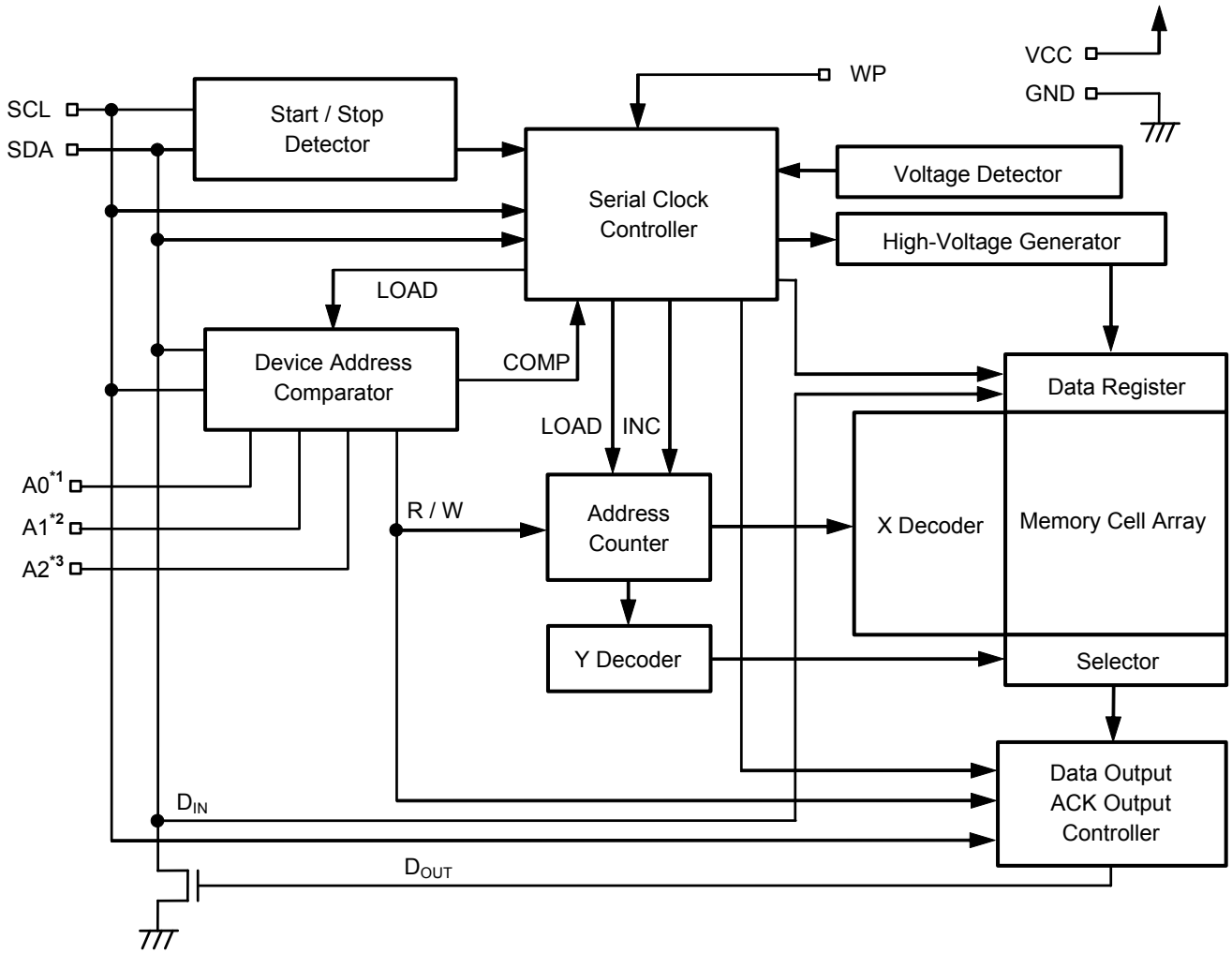
(2.9 × 4.0 × t0.8 mm)

- SNT-8A



(2.5 × 2.0 × t0.5 mm)

■ Block Diagram



***1.** This pin is not available for the S-24C04D/08D/16D.
***2.** This pin is not available for the S-24C08D/16D.
***3.** This pin is not available for the S-24C16D.

Remark The A0 pin, the A1 pin and the A2 pin are no connection in the product with SOT-23-5 package.

■ Product Name Structure

1. Product name

S-24CxxD I - xxxx U 5

Environmental code
- U: Lead-free (Sn 100%), halogen-free

Package name (abbreviation) and IC packing specification*1
- J8T1: 8-Pin SOP (JEDEC), Tape
- T8T1: 8-Pin TSSOP, Tape
- K8T3: TMSOP-8, Tape
- M5T1: SOT-23-5, Tape
- A8T1: DFN-8(2030), Tape
- I8T1: SNT-8A, Tape

Operation temperature
- I: Ta = −40°C to +85°C

Product name
- S-24C02D: 2 K-bit
- S-24C04D: 4 K-bit
- S-24C08D: 8 K-bit
- S-24C16D: 16 K-bit

***1.** Refer to the tape drawing.

2. Packages

Package Name	Dimension	Tape	Reel	Land
8-Pin SOP (JEDEC)	FJ008-Z-P-SD	FJ008-Z-C-SD	FJ008-Z-R-SD	–
8-Pin TSSOP	FT008-Z-P-SD	FT008-Z-C-SD	FT008-Z-R-SD	–
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD	–
SOT-23-5	MP005-A-P-SD	MP005-B-C-SD	MP005-B-R-SD	–
DFN-8(2030)	PP008-A-P-S1	PP008-A-C-SD	PP008-A-R-SD	PP008-A-L-SD
SNT-8A	PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD

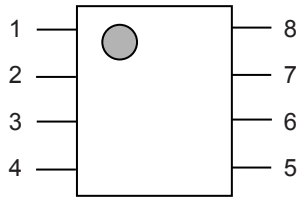
3. Product name list

Product Name	Capacity	Package Name
S-24C02DI-J8T1U5	2 K-bit	8-Pin SOP (JEDEC)
S-24C02DI-T8T1U5	2 K-bit	8-Pin TSSOP
S-24C02DI-K8T3U5	2 K-bit	TMSOP-8
S-24C02DI-M5T1U5	2 K-bit	SOT-23-5
S-24C02DI-A8T1U5	2 K-bit	DFN-8(2030)
S-24C02DI-I8T1U5	2 K-bit	SNT-8A
S-24C04DI-J8T1U5	4 K-bit	8-Pin SOP (JEDEC)
S-24C04DI-T8T1U5	4 K-bit	8-Pin TSSOP
S-24C04DI-K8T3U5	4 K-bit	TMSOP-8
S-24C04DI-M5T1U5	4 K-bit	SOT-23-5
S-24C04DI-A8T1U5	4 K-bit	DFN-8(2030)
S-24C04DI-I8T1U5	4 K-bit	SNT-8A
S-24C08DI-J8T1U5	8 K-bit	8-Pin SOP (JEDEC)
S-24C08DI-T8T1U5	8 K-bit	8-Pin TSSOP
S-24C08DI-K8T3U5	8 K-bit	TMSOP-8
S-24C08DI-M5T1U5	8 K-bit	SOT-23-5
S-24C08DI-A8T1U5	8 K-bit	DFN-8(2030)
S-24C08DI-I8T1U5	8 K-bit	SNT-8A
S-24C16DI-J8T1U5	16 K-bit	8-Pin SOP (JEDEC)
S-24C16DI-T8T1U5	16 K-bit	8-Pin TSSOP
S-24C16DI-K8T3U5	16 K-bit	TMSOP-8
S-24C16DI-M5T1U5	16 K-bit	SOT-23-5
S-24C16DI-A8T1U5	16 K-bit	DFN-8(2030)
S-24C16DI-I8T1U5	16 K-bit	SNT-8A

■ Pin Configurations

1. 8-Pin SOP (JEDEC), 8-Pin TSSOP, TMSOP-8, DFN-8(2030), SNT-8A

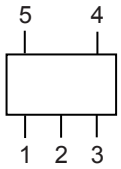
Top view



Pin No.	Symbol				Description
	S-24C02D	S-24C04D	S-24C08D	S-24C16D	
1	A0	NC*2	NC*2	NC*2	Slave address input
2	A1	A1	NC*2	NC*2	Slave address input
3	A2	A2	A2	NC*2	Slave address input
4	GND	GND	GND	GND	Ground
5	SDA*1	SDA*1	SDA*1	SDA*1	Serial data I/O
6	SCL*1	SCL*1	SCL*1	SCL*1	Serial clock input
7	WP	WP	WP	WP	Write protect input Connected to V_{CC}: Protection valid Open or connected to GND: Protection invalid
8	VCC	VCC	VCC	VCC	Power supply

2. SOT-23-5

Top view



Pin No.	Symbol	Description
1	SCL*1	Serial clock input
2	GND	Ground
3	SDA*1	Serial data I/O
4	VCC	Power supply
5	WP	Write protect input Connected to V_{CC}: Protection valid Open or connected to GND: Protection invalid

***1.** Do not use it in "High-Z".
***2.** The NC is no connection.

Remark For DFN-8(2030) package, connect the heatsink of back side to the board, and set electric potential open or GND. However, do not use it as the function of electrode.

■ Absolute Maximum Ratings

Table 1

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V_{CC}	−0.3 to +6.5	V
Input voltage	V_{IN}	−0.3 to +6.5	V
Output voltage	V_{OUT}	−0.3 to +6.5	V
Operation ambient temperature	T_{opr}	−40 to +85	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operating Conditions

Table 2

Item	Symbol	Condition	Ta = −40°C to +85°C		Unit
			Min.	Max.	
Power supply voltage	V_{CC}	Read	1.7	5.5	V
		Write	1.7	5.5	V
High level input voltage	V_{IH}	V_{CC} = 1.7 V to 5.5 V	0.7 × V_{CC}	5.5	V
Low level input voltage	V_{IL}	V_{CC} = 1.7 V to 5.5 V	−0.3	0.3 × V_{CC}	V

■ Pin Capacitance

Table 3

(Ta = +25°C, f = 1.0 MHz, V_{CC} = 5.0 V)

Item	Symbol	Condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V (S-24C02D: SCL, A0, A1, A2, WP)	−	8	pF
		V_{IN} = 0 V (S-24C04D: SCL, A1, A2, WP)	−	8	pF
		V_{IN} = 0 V (S-24C08D: SCL, A2, WP)	−	8	pF
		V_{IN} = 0 V (S-24C16D: SCL, WP)	−	8	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V (SDA)	−	8	pF

■ Endurance

Table 4

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Endurance	N_W	Ta = +25°C	10^6	−	cycle / word[*1]

***1.** For each address (Word: 8-bit)

■ Data Retention

Table 5

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Data retention	−	Ta = +25°C	100	−	year

■ DC Electrical Characteristics

Table 6

Item	Symbol	Condition	Ta = –40°C to +85°C				Unit
			V_{CC} = 2.5 V to 5.5 V f_{SCL} = 1.0 MHz		V_{CC} = 1.7 V to 5.5 V f_{SCL} = 400 kHz		
			Min.	Max.	Min.	Max.	
Current consumption (READ)	I_{CC1}	–	–	1.0	–	0.8	mA

Table 7

Item	Symbol	Condition	Ta = –40°C to +85°C				Unit
			V_{CC} = 2.5 V to 5.5 V f_{SCL} = 1.0 MHz		V_{CC} = 1.7 V to 5.5 V f_{SCL} = 400 kHz		
			Min.	Max.	Min.	Max.	
Current consumption (WRITE)	I_{CC2}	–	–	2.0	–	2.0	mA

Table 8

Item	Symbol	Condition	Ta = –40°C to +85°C				Unit
			V_{CC} = 2.5 V to 5.5 V		V_{CC} = 1.7 V to 2.5 V		
			Min.	Max.	Min.	Max.	
Standby current consumption	I_{SB}	V_{IN} = V_{CC} or GND	–	1.0	–	1.0	μA
Input leakage current 1	I_{LI1}	SCL, SDA V_{IN} = GND to V_{CC}	–	1.0	–	1.0	μA
Input leakage current 2	I_{LI2}	A0, A1, A2 V_{IN} > 0.7 × V_{CC}	–	1.0	–	1.0	μA
Output leakage current	I_{LO}	SDA V_{OUT} = GND to V_{CC}	–	1.0	–	1.0	μA
Input current 1	I_{IL}	WP V_{IN} < 0.3 × V_{CC}	–	50.0	–	50.0	μA
Input current 2	I_{IH}	WP V_{IN} > 0.7 × V_{CC}	–	2.0	–	2.0	μA
Input Impedance 1	Z_{IL}	WP V_{IN} = 0.3 × V_{CC}	30	–	30	–	kΩ
Input Impedance 2	Z_{IH}	WP V_{IN} = 0.7 × V_{CC}	500	–	500	–	kΩ
Low level output voltage	V_{OL}	I_{OL} = 3.2 mA	–	0.4	–	–	V
		I_{OL} = 1.5 mA	–	0.3	–	0.3	V
		I_{OL} = 0.7 mA	–	0.2	–	0.2	V

■ AC Electrical Characteristics

Table 9 Measurement Conditions

Input pulse voltage	$0.2 \times V_{CC}$ to $0.8 \times V_{CC}$
Input pulse rising / falling time	20 ns or less
Output reference voltage	$0.3 \times V_{CC}$ to $0.7 \times V_{CC}$
Output load	100 pF

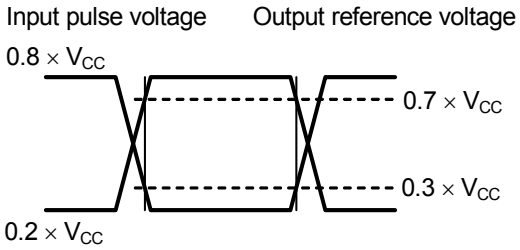


Figure 1 Input / Output Waveform during AC Measurement

Table 10

Item	Symbol	Ta = −40°C to +85°C				Unit
		V_{CC} = 2.5 V to 5.5 V		V_{CC} = 1.7 V to 5.5 V		
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	1000	0	400	kHz
SCL clock time "L"	t_{LOW}	0.4	–	1.3	–	µs
SCL clock time "H"	t_{HIGH}	0.3	–	0.6	–	µs
SDA output delay time	t_{AA}	0.1	0.5	0.1	0.9	µs
SDA output hold time	t_{DH}	50	–	50	–	ns
Start condition setup time	$t_{SU.STA}$	0.25	–	0.6	–	µs
Start condition hold time	$t_{HD.STA}$	0.25	–	0.6	–	µs
Data input setup time	$t_{SU.DAT}$	80	–	100	–	ns
Data input hold time	$t_{HD.DAT}$	0	–	0	–	ns
Stop condition setup time	$t_{SU.STO}$	0.25	–	0.6	–	µs
SCL, SDA rising time	t_R	–	0.3	–	0.3	µs
SCL, SDA falling time	t_F	–	0.3	–	0.3	µs
WP setup time	t_{WS1}	0	–	0	–	µs
WP hold time	t_{WH1}	0	–	0	–	µs
WP release setup time	t_{WS2}	0	–	0	–	µs
WP release hold time	t_{WH2}	0	–	0	–	µs
Bus release time	t_{BUF}	0.5	–	1.3	–	µs
Noise suppression time	t_I	–	50	–	50	ns
Write time	t_{WR}	–	5.0	–	5.0	ms

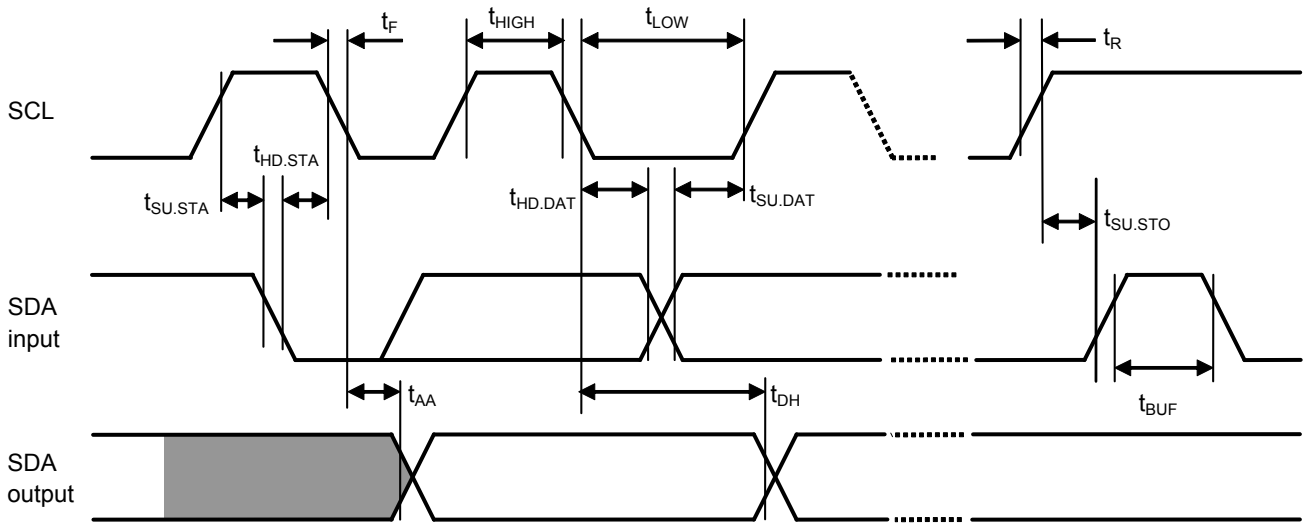


Figure 2 Bus Timing

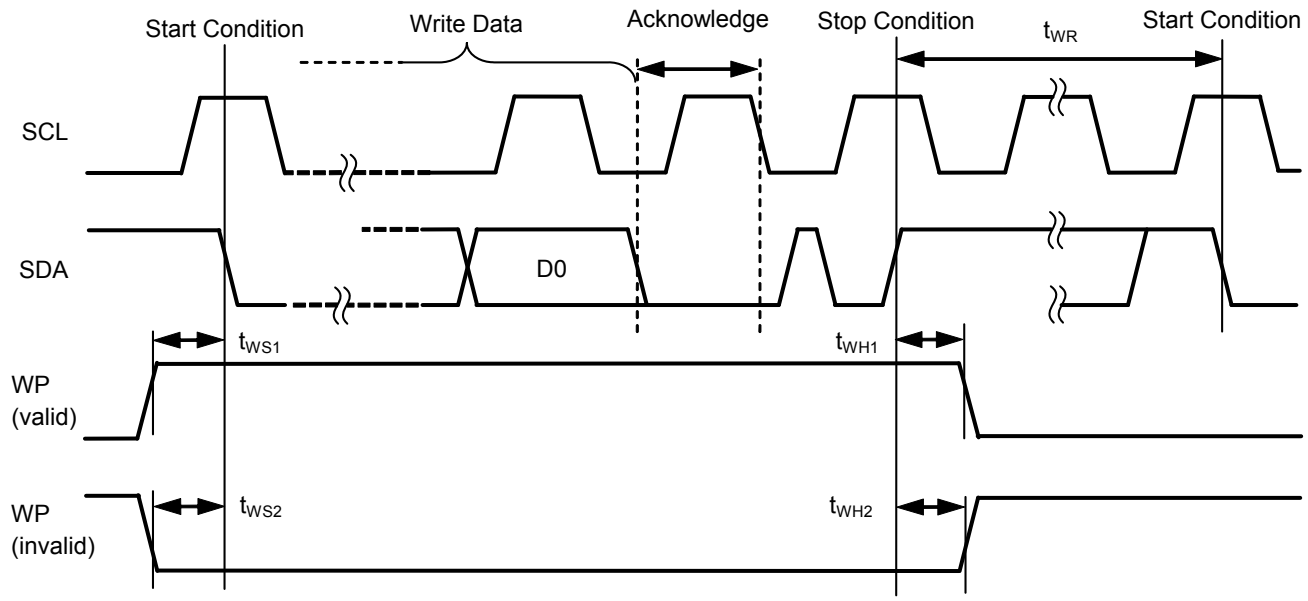


Figure 3 Write Cycle Timing

■ Pin Functions

1. VCC (Power supply) pin

The VCC pin is used to apply positive supply voltage. Regarding the applied voltage value, refer to "■ **Recommended Operating Conditions**". Set a bypass capacitor of about 0.1 μF between the VCC pin and the GND pin to make the power supply voltage stable.

2. A0, A1 and A2 (Slave address input) pins

In the S-24C02D, to set the slave address, connect each of A0 pin, A1 pin and A2 pin to the GND pin or the VCC pin. Therefore the users can set 8 types of slave address by a combination of A0, A1, A2 pins.
In the S-24C04D, to set the slave address, connect each of A1 pin and A2 pin to the GND pin or the VCC pin. Therefore the users can set 4 types of slave address by a combination of A1, A2 pins.
In the S-24C08D, to set the slave address, connect A2 pin to the GND pin or the VCC pin. Therefore the users can set 2 types of slave address.
In the S-24C16D, the slave address can not be assigned.
Comparing the slave address transmitted from the master device and one that you set, makes possible to select one slave address from other devices connected onto the bus.
Each of A0 pin, A1 pin and A2 pin has a built-in pull-down resistor. In open, the pin is set to the same status as it connected to the GND pin.

In the case of the products with SOT-23-5, set the slave address transmitting from the master device to "0".

3. SDA (Serial data I/O) pin

The SDA pin is used for the bi-directional transmission of serial data. This pin is a signal input pin, and an Nch open-drain output pin.
In use, generally, connect the SDA line to any other device which has the open-drain or open-collector output with Wired-OR connection by pulling up to V_{CC} by a resistor. **Figure 4** shows the relation with an output load.

4. SCL (Serial clock input) pin

The SCL pin is used for the serial clock input. Since the signals are processed at a rising or falling edge of the SCL clock, pay attention to the rising and falling time and comply with the specification.

5. WP (Write protect input) pin

The write protect is enabled by connecting the WP pin to V_{CC}. When not using the write protect, connect this pin to the GND pin or set in open.

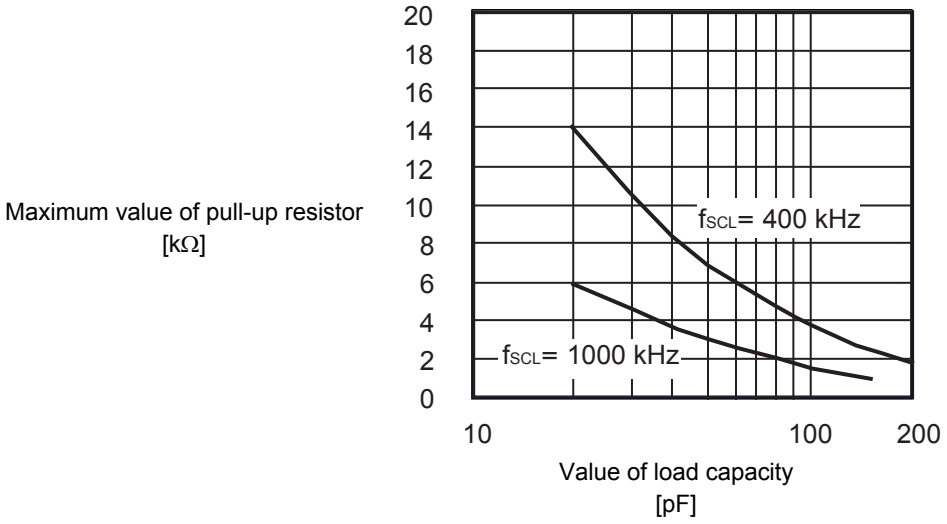


Figure 4 Output Load

■ Initial Delivery State

Initial delivery state of all addresses is "FFh".

■ Operation

1. Initialization operation after power-on

By a power-on-clear circuit, this IC initializes the internal circuit at the time of power-on. Perform the beginning (start condition) of the instruction transmission to this IC after the initialization by the power-on-clear circuit. Regarding the datails of power-on-clear, refer to "**5. Power-on-clear circuit**" in "**■ Usage**".

2. Start condition

Start is identified by a "H" to "L" transition of the SDA line while the SCL line is stable at "H".
Every operation begins from a start condition.

3. Stop condition

Stop is identified by a "L" to "H" transition of the SDA line while the SCL line is stable at "H".
When a device receives a stop condition during a read sequence, the read operation is interrupted, and the device enters standby mode.
When a device receives a stop condition during a write sequence, the reception of the write data is halted, and this IC initiates a write cycle.

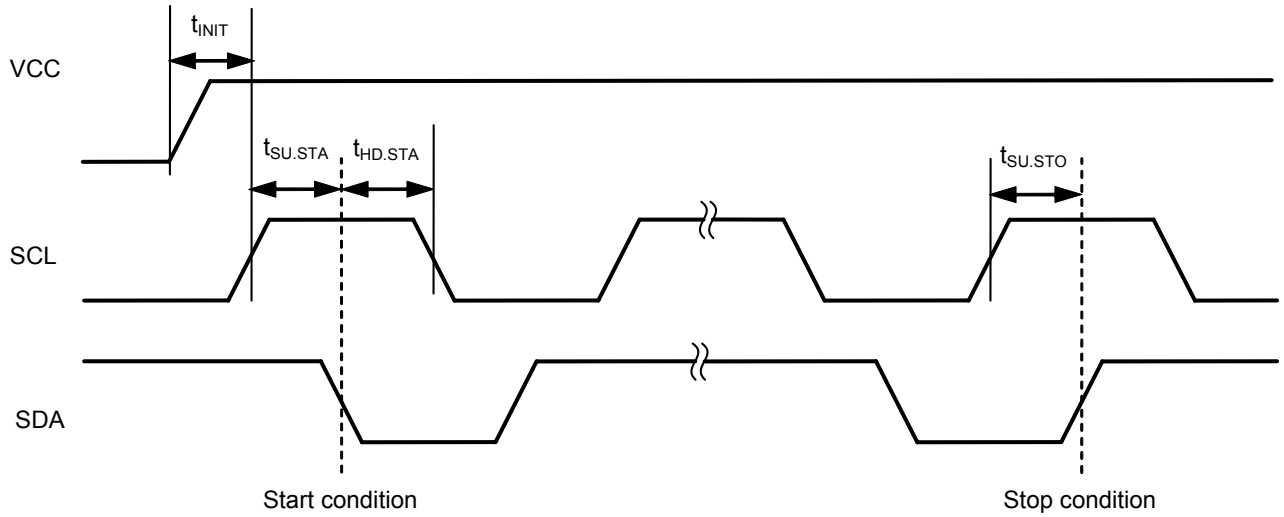


Figure 5 Start / Stop Conditions after Power-on

4. Data transmission

Changing the SDA line while the SCL line is "L", data is transmitted.
Changing the SDA line while the SCL line is "H", a start or stop condition is recognized.

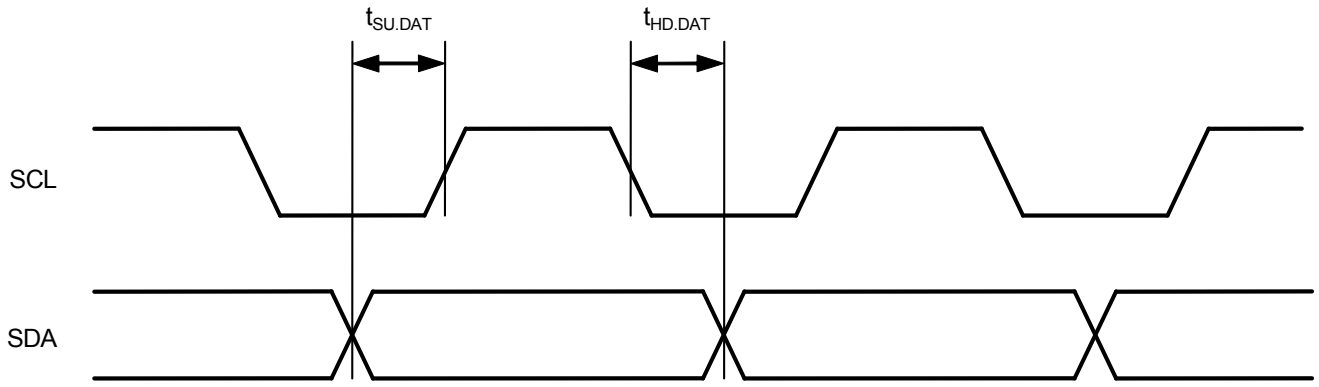


Figure 6 Data Transmission Timing

5. Acknowledge

The unit of data transmission is 8 bits. During the 9th clock cycle period the receiver on the bus pulls down the SDA line to acknowledge the receipt of the 8-bit data.
When an internal write cycle is in progress, the device does not generate an acknowledge.

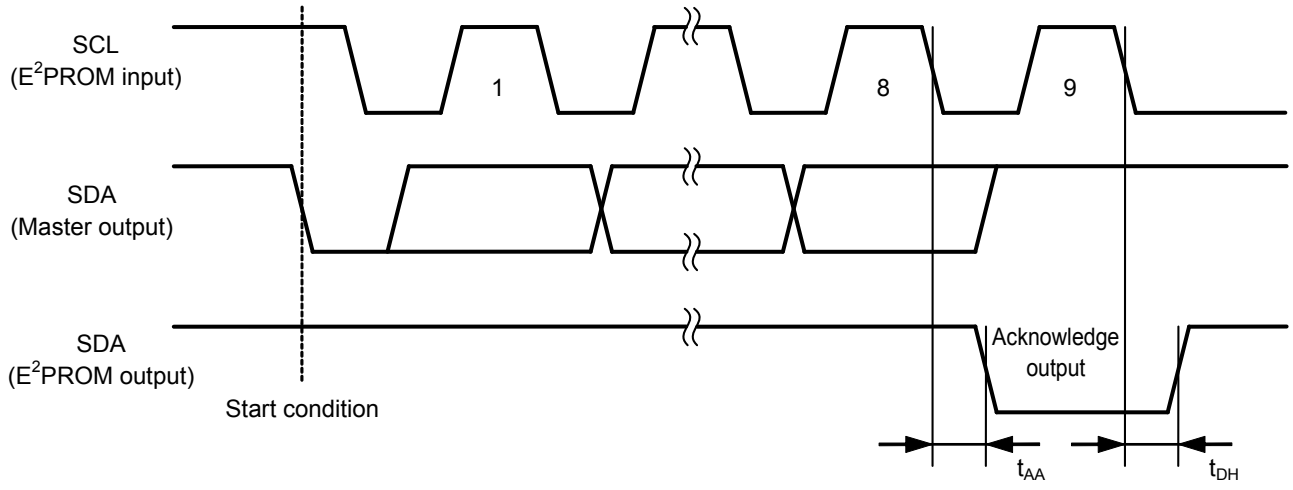


Figure 7 Acknowledge Output Timing

6. Device addressing

To start communication, the master device on the system generates a start condition to the bus line. Next, the master device sends 7-bit device address and a 1-bit read / write instruction code on to the SDA bus.
The higher 4 bits of the device address are the "Device Code", and are fixed to "1010".

In the S-24C02D, successive 3 bits are the "Slave Address". These 3 bits are used to identify a device on the system bus and are compared with the predetermined value which is defined by the address input pins (A2, A1, A0). When the comparison result matches, the slave device responds with an acknowledge during the 9th clock cycle.

In the S-24C04D, successive 2 bits are the "Slave Address". These 2 bits are used to identify a device on the system bus and are compared with the predetermined value which is defined by the address input pins (A2, A1). When the comparison result matches, the slave device responds with an acknowledge during the 9th clock cycle.
The successive 1 bit (P0) is used to define a page address and choose the two 256-byte memory blocks (Address 000h to 0FFh, 100h to 1FFh).

In the S-24C08D, successive 1 bit is called the "Slave Addrdess". This 1 bit is used to identify a device on the system bus and is compared with the predetermined value which is defined by the address input pin (A2). When the comparison result matches, the slave device responds with an acknowledge during the 9th clocks cycle.
The successive 2 bits (P1, P0) are used to define a page address and choose the four 256-byte memory blocks (Address 000h to 0FFh, 100h to 1FFh, 200h to 2FFh , 300h to 3FFh).

In the S-24C16D, successive 3 bits (P2, P1, P0) are "Page Address". Choose the 8 memory blocks of 256-byte (Adress 000h to 0FFh, 100h to 1FFh, 200h to 2FFh, 300h to 3FFh, 400h to 4FFh, 500h to 5FFh, 600h to 6FFh, 700h to 7FFh).

In the case of the product with SOT-23-5, set the slave address transmitting from the master device to "0".

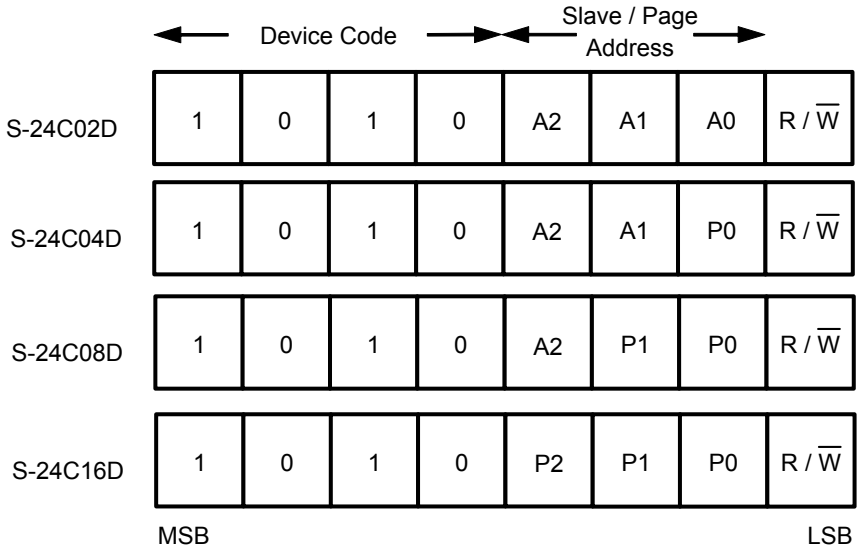
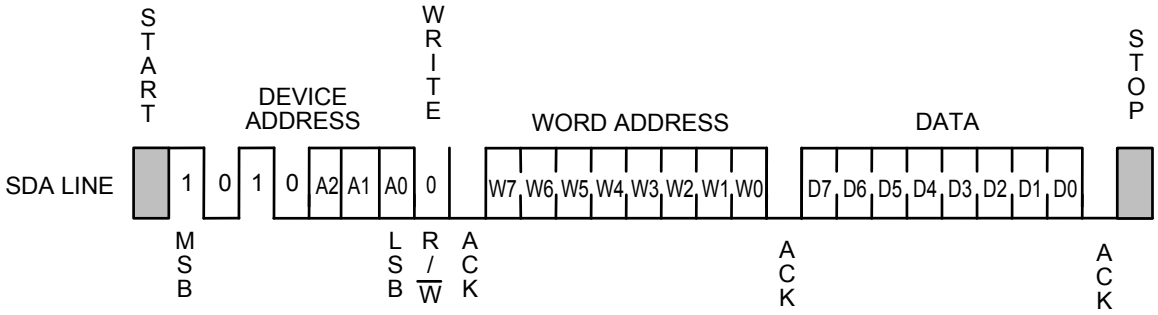


Figure 8 Device Address

7. Write

7. 1 Byte write

When the master sends a 7-bit device address and a 1-bit read / write instruction code set to "0", following a start condition, this IC acknowledges it.
This IC then receives an 8-bit word address and responds with an acknowledge. After this IC receives 8-bit write data and responds with an acknowledge, it receives a stop condition and that initiates the write cycle at the addressed memory.
During the write cycle all operations are forbidden and no acknowledge is generated.

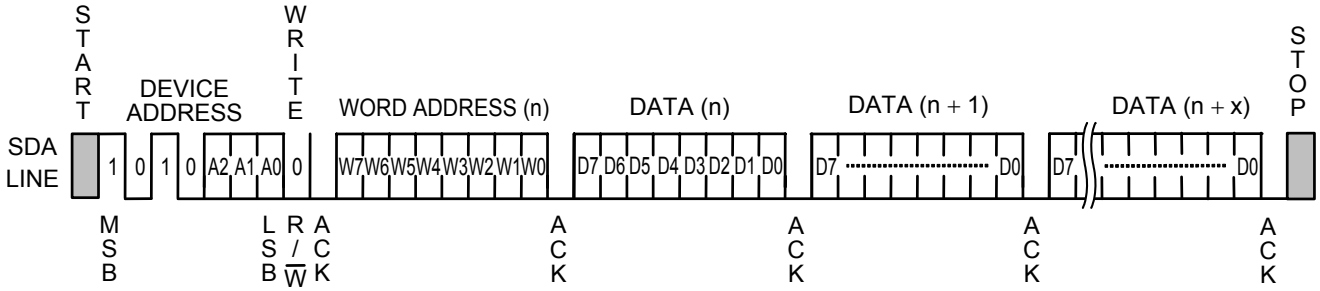


Remark A0 is P0 in the S-24C04D/08D/16D.
A1 is P1 in the S-24C08D/16D.
A2 is P2 in the S-24C16D.
Set A0, A1, A2 to "0" in the product with SOT-23-5 package.

Figure 9 Byte Write

7. 2 Page write

The page write mode allows up to 8 bytes to be written in a single write operation in the S-24C02D.
The page write mode allows up to 16 bytes to be written in a single write operation in the S-24C04D/08D/16D.
Its basic process to transmit data is as same as byte write, but it operates page write by sequentially receiving 8-bit write data as much data as the page size has.
When this IC receives a 7-bit device address and a 1-bit read / write instruction code set to "0", following a start condition, it generates an acknowledge. Then this IC receives an 8-bit word address, and responds with an acknowledge. After this IC receives 8-bit write data and responds with an acknowledge, it receives 8-bit write data corresponding to the next word address, and generates an acknowledge. This IC repeats reception of 8-bit write data and generation of acknowledge in succession. This IC can receive as many write data as the maximum page size.
Receiving a stop condition initiates a write cycle of the area starting from the designated memory address and having the page size equal to the received write data.



Remark A0 is P0 in the S-24C04D/08D/16D.
A1 is P1 in the S-24C08D/16D.
A2 is P2 in the S-24C16D.
Set A0, A1, A2 to "0" in the product with SOT-23-5 package.

Figure 10 Page Write

In the S-24C02D, the lower 3 bits of the word address are automatically incremented every time when the S-24C02D receives 8-bit write data. If the size of the write data exceeds 8 bytes, the higher 5 bits (W7 to W3) of the word address remain unchanged, and the lower 3 bits are rolled over and the last 8-byte data that the S-24C02D received will be overwritten.

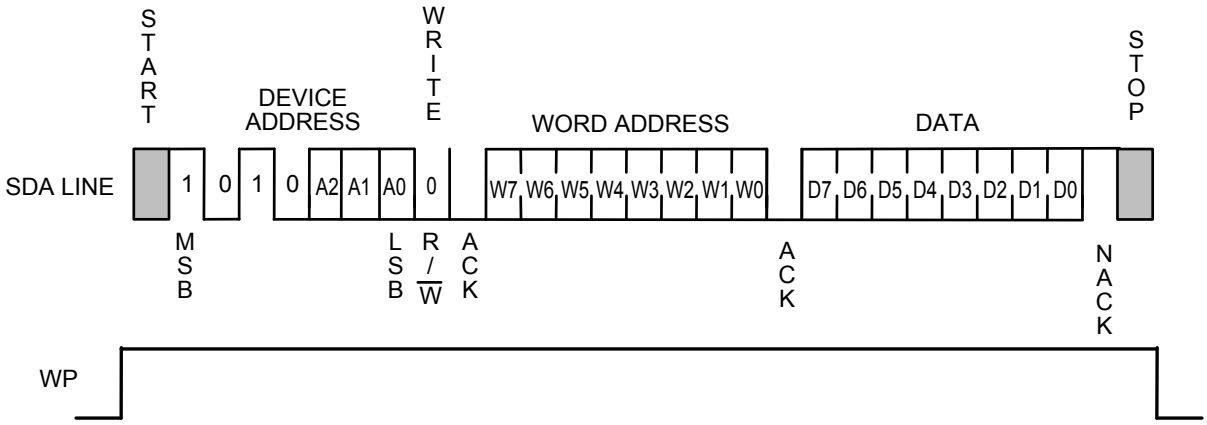
In the S-24C04D, the lower 4 bits of the word address are automatically incremented every time when the S-24C04D receives 8-bit write data. If the size of the write data exceeds 16 bytes, the higher 4 bits (W7 to W4) of the word address and page address (P0) remain unchanged, and the lower 4 bits are rolled over and the last 16-byte data that the S-24C04D received will be overwritten.

In the S-24C08D, the lower 4 bits of the word address are automatically incremented every time when the S-24C08D receives 8-bit write data. If the size of the write data exceeds 16 bytes, the higher 4 bits (W7 to W4) of the word address and page address (P1, P0) remain unchanged, and the lower 4 bits are rolled over and the last 16-byte data that the S-24C08D received will be overwritten.

In the S-24C16D, the lower 4 bits of the word address are automatically incremented every time when the S-24C16D receives 8-bit write data. If the size of the write data exceeds 16 bytes, the higher 4 bits (W7 to W4) of the word address and page address (P2, P1, P0) remain unchanged, and the lower 4 bits are rolled over and the last 16-byte data that the S-24C16D received will be overwritten.

7. 3 Write protect

Write protect is available in this IC. When the WP pin is connected to the VCC pin, write operation to memory area is forbidden at all.
When the WP pin is connected to the GND pin or set in open, the write protect is invalid, and write operation in all memory area is available.
Fix the level of the WP pin from start condition in the write operation (byte write, page write) until stop condition. If the WP pin changes during this time, the address data being written at this time is not guaranteed. Regarding the timing of write protect, refer to "**Figure 3 Write Cycle Timing**".
When not using the write protect, connect the WP pin to the GND pin or set in open. The write protect is valid in the range of operation power supply voltage.
As seen in **Figure 11** when the write protect is valid, this IC does not generate an acknowledgel after data input.



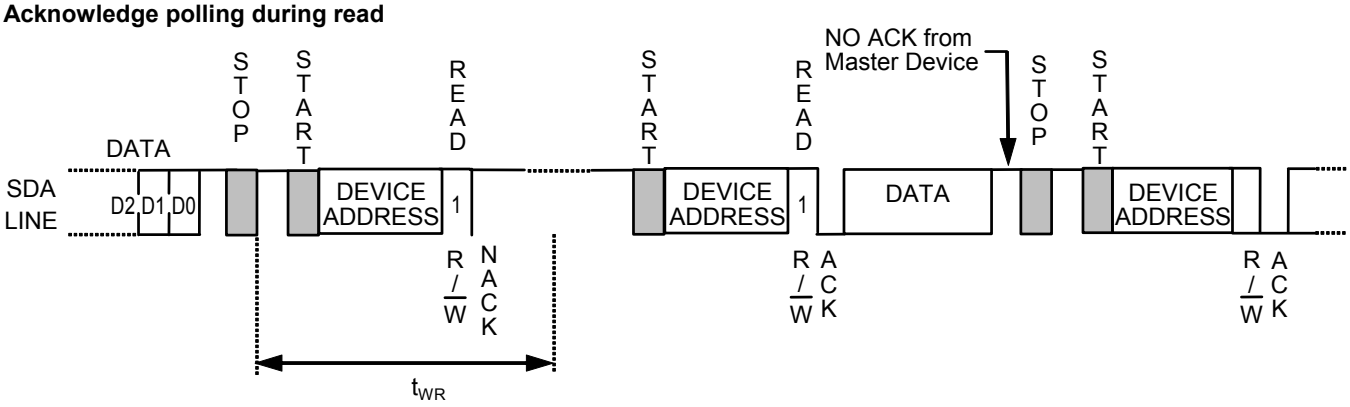
Remark A0 is P0 in the S-24C04D/08D/16D.
A1 is P1 in the S-24C08D/16D.
A2 is P2 in the S-24C16D.
Set A0, A1, A2 to "0" in the product with SOT-23-5 package.

Figure 11 Write Protect

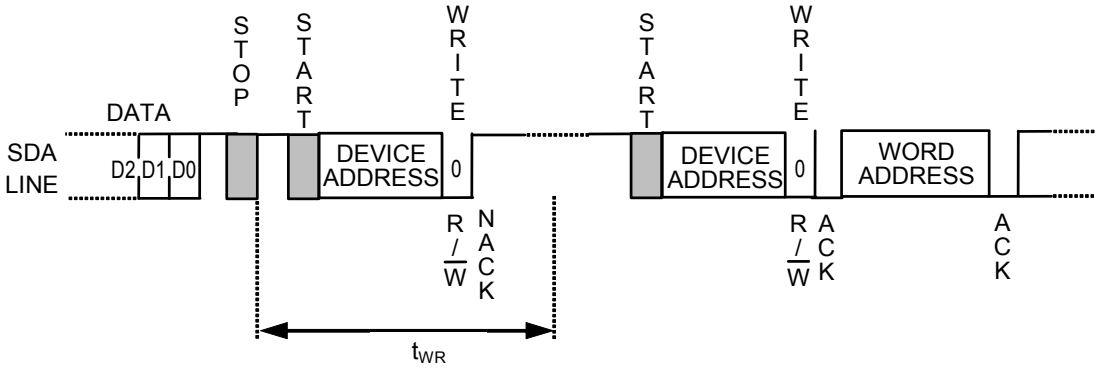
7. 4 Acknowledge polling

Acknowledge polling is used to know the completion of the write cycle in this IC.
After this IC receives a stop condition and once starts the write cycle, all operations are forbidden and no response is made to the signal transmitted by the master device.
Accordingly the master device can recognize the completion of the write cycle in this IC by detecting a response from the slave device after transmitting the start condition, the device address and the read / write instruction code to this IC, namely to the slave devices.
That is, if this IC does not generate an acknowledge, the write cycle is in progress and if this IC generates an acknowledge, the write cycle has been completed.
It is recommended to use the read instruction "1" as the read / write instruction code transmitted by the master device.

Acknowledge polling during read



Acknowledge polling during write



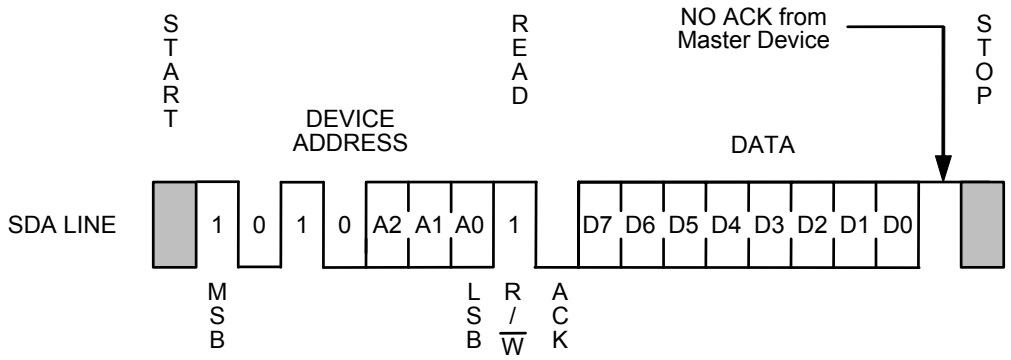
Remark Users are able to read data after acknowledge output in acknowledge polling during read.
Users are able to input word address and data after acknowledge output in acknowledge polling during write.
However, after that users input the write instruction, a start condition may not be input during data output. Input a stop condition and the next instruction after data output and acknowledge output.

Figure 12 Usage Example of Acknowledge Polling

8. Read

8. 1 Current address read

Either in writing or in reading this IC holds the last accessed memory address. The memory address is maintained when the instruction transmission is not interrupted, and the memory address is maintained as long as the power voltage does not decrease less than the operating voltage.
The master device can read the data at the memory address of the current address pointer without assigning the word address as a result, when it recognizes the position of the address pointer in this IC. This is called "Current Address Read".
In the following the address counter in this IC is assumed to be "n".
When this IC receives a 7-bit device address and a 1-bit read / write instruction code set to "1" following a start condition, it responds with an acknowledge.
Next an 8-bit data at the address "n" is sent from this IC synchronous to the SCL clock. The address counter is incremented and the content of the address counter becomes n + 1. The master device outputs stop condition not an acknowledge, the reading of this IC is ended.



Remark In the S-24C04D/08D/16D, A0 = Don't care.
In the S-24C08D/16D, A1 = Don't care.
In the S-24C16D, A2 = Don't care.
Set A0, A1, A2 to "0" in the product with SOT-23-5 package.

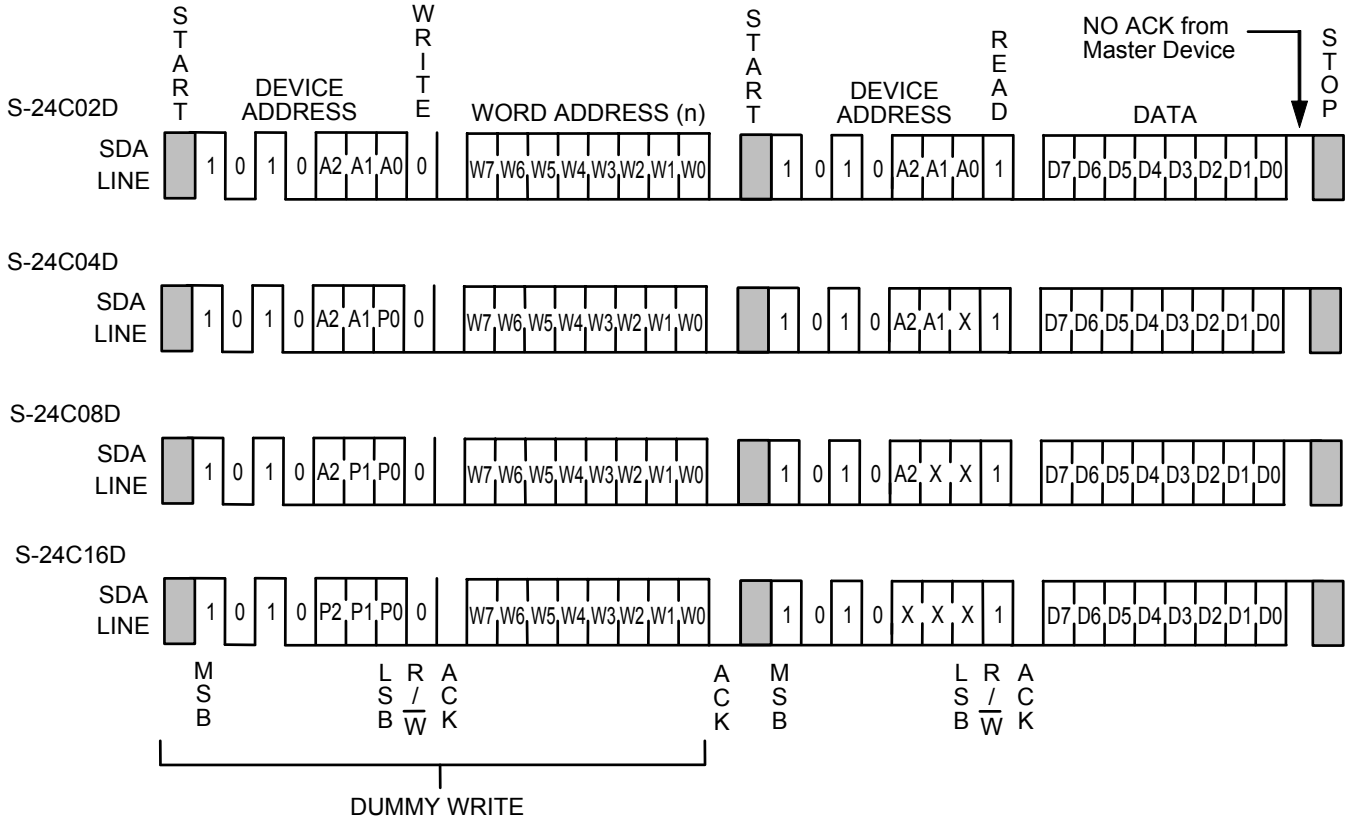
Figure 13 Current Address Read

Attention should be paid to the following point on the recognition of the address pointer in this IC.
In Read, the memory address counter in this IC is automatically incremented after output of the 8th bit of the data. In Write, on the other hand, the higher bits of the memory address (the higher bits of the word address and the page address[*1]) are left unchanged and are not incremented.

***1.** In the S-24C02D, the higher 5 bits (W7 to W3) of the word address.
In the S-24C04D, the higher 4 bits (W7 to W4) of the word address and the page address (P0).
In the S-24C08D, the higher 4 bits (W7 to W4) of the word address and the page address (P1, P0).
In the S-24C16D, the higher 4bits (W7 to W4) of the word address and the page address (P2, P1, P0).

8. 2 Random read

Random read is used to read the data at an arbitrary memory address.
A dummy write is performed to load the memory address into the address counter.
When this IC receives a 7-bit device address and a 1-bit read / write instruction code set to "0" following a start condition, it responds with an acknowledge.
This IC then receives an 8-bit word address and responds with an acknowledge. The memory address is loaded to the address counter in this IC by these operations. Reception of write data does not follow in a dummy write whereas reception of write data follows in byte write and in page write.
Since the memory address is loaded into the memory address counter by dummy write, the master device can read the data starting from the arbitrary memory address by transmitting a new start condition and performing the same operation in the current address read.
That is, when this IC receives a 7-bit device address and a 1-bit read / write instruction code set to "1", following a start condition signal, it responds with an acknowledge. Next, 8-bit data is transmitted from this IC in synchronous to the SCL clock. The master device outputs stop condition not an acknowledge, the reading of this IC is ended.



Remark 1. X = Don't care
2. Set A0, A1, A2 to "0" in the product with SOT-23-5 package.

Figure 14 Random Read

8. 3 Sequential read

When this IC receives a 7-bit device address and a 1-bit read / write instruction code set to "1" following a start condition both in current address read and random read, it responds with an acknowledge.
When an 8-bit data is output from this IC synchronous to the SCL clock, the address counter is automatically incremented.
When the master device responds with an acknowledge, the data at the next memory address is transmitted. Response with an acknowledge by the master device has the memory address counter in this IC incremented and makes it possible to read data in succession. This is called sequential read.
The master device outputs stop condition not an acknowledge, the reading of this IC is ended.
Data can be read in succession in the sequential read mode. When the memory address counter reaches the last word address, it rolls over to the first word address.

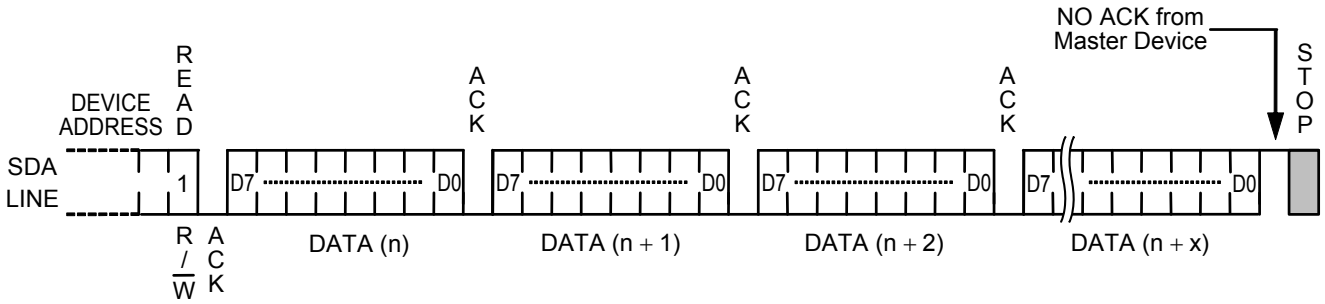


Figure 15 Sequential Read

■ Usage

1. A pull-up resistor to SDA I/O pin and SCL input pin

In consideration of I²C-bus protocol function, the SDA I/O pin should be connected with a pull-up resistor. This IC cannot transmit normally without using a pull-up resistor.

In case that the SCL input pin of this IC is connected to the Nch open-drain output pin of the master device, connect the SCL pin with a pull-up resistor. As well, in case the SCL input pin of this IC is connected to the tri-state output pin of the master device, connect the SCL pin with a pull-up resistor in order not to set it in "High-Z". This prevents this IC from error caused by an uncertain output (High-Z) from the tri-state pin when resetting the master device during the voltage drop.

2. Equivalent circuits of input pin and I/O pin

The SCL pin and the SDA pin of this IC does not have a built-in pull-down or pull-up resistor. Each of A0 pin, A1 pin, A2 pin and WP pin has a built-in pull-down resistor. The SDA pin is an open-drain output. The followings are equivalent circuits of the pins.

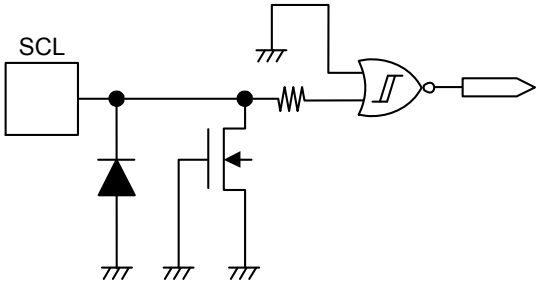


Figure 16 SCL Pin

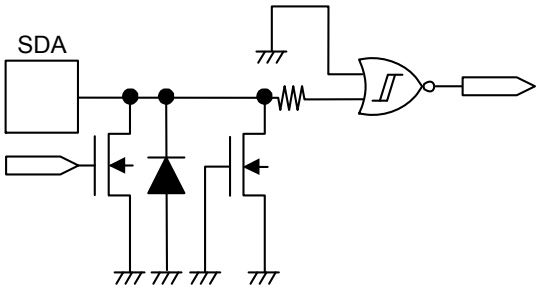


Figure 17 SDA Pin

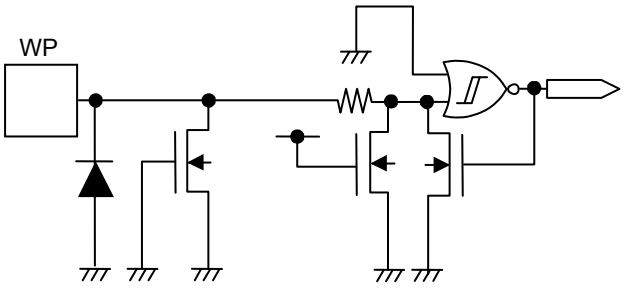


Figure 18 WP Pin

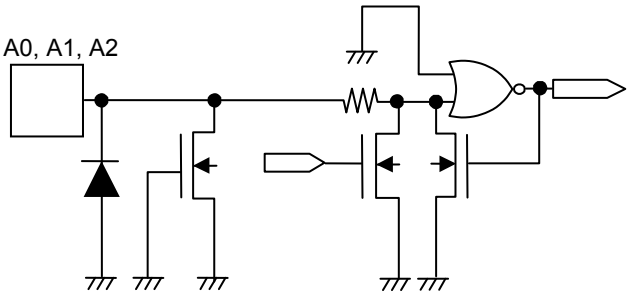


Figure 19 A0, A1, A2 Pin

Remark In the S-24C04D/08D/16D, A0 pin is not available.
In the S-24C08D/16D, A1 pin is not available.
In the S-24C16D, A2 pin is not available.
The A0 pin, the A1 pin and the A2 pin are no connection in the product with SOT-23-5 package.

3. Phase adjustment of the I²C-bus product

The I²C-bus product does not have a pin to reset (the internal circuit). The users cannot forcibly reset it externally. If the communication interrupted, the users need to handle it as you do for software.
In this IC, users are able to reset the internal circuit by inputting a start condition and a stop condition.
Although the reset signal is input to the master device, this IC's internal circuit does not go in reset, but it does by inputting a stop condition to this IC. This IC keeps the same status thus cannot do the next operation. Especially, this case corresponds to that only the master device is reset when the power supply voltage drops.
If the power supply voltage restored in this status, input the instruction after resetting (adjusting the phase with the master device) this IC. How to reset is shown below.

[How to reset this IC]

This IC is able to be reset by a start and stop instructions. When this IC is reading data "0" or is outputting the acknowledgment signal, outputs "0" to the SDA line. In this status, the master device cannot output an instruction to the SDA line. In this case, terminate the acknowledgment output operation or the Read operation, and then input a start condition.
Figure 20 shows this procedure.
First, input a start condition. Then transmit 9 clocks (dummy clock) of SCL. During this time, the master device sets the SDA line to "H". By this operation, this IC interrupts the acknowledgment output operation or data output, so input a start condition*1. When a start condition is input, this IC is reset. To make doubly sure, input the stop condition to this IC. The normal operation is then possible.

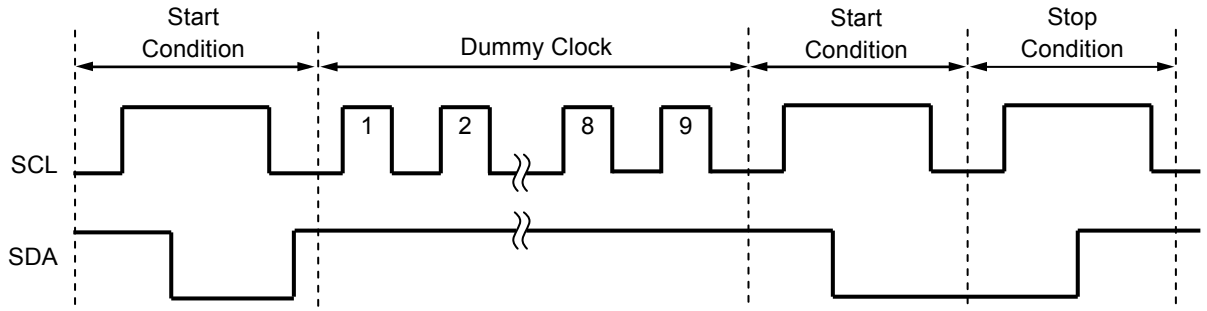


Figure 20 Resetting Method

***1.** After 9 clocks (dummy clock), if the SCL clock continues to being output without inputting a start condition, this IC may go in the write operation when it receives a stop condition. To prevent this, input a start condition after 9 clocks (dummy clock).

Remark Regarding this reset procedure with dummy clock, it is recommended to perform at the system initialization after applying the power supply voltage.

4. Acknowledge check

The I²C-bus protocol includes an acknowledge check function as a handshake function to prevent a communication error. This function allows detection of a communication failure during data communication between the master device and this IC. This function is effective to prevent malfunction, so it is recommended to perform an acknowledge check with the master device.

5. Power-on-clear circuit

By power-on-clear circuit, this IC initializes at the same time when the power supply voltage is raised. After the initialization by the power-on-clear circuit is completed, this IC becomes standby state.
In order to use this IC safely, raise the power supply voltage depending on the following conditions.

5. 1 Initialization time

This IC initializes at the same time when the power supply voltage is raised. Input instructions to this IC after initialization. This IC does not accept any instruction during initialization.
Figure 21 shows the initialization time of this IC.

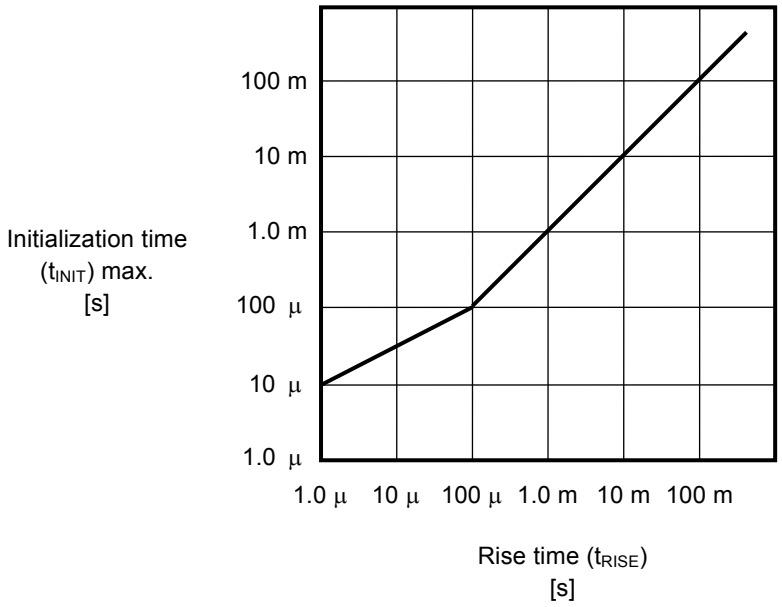


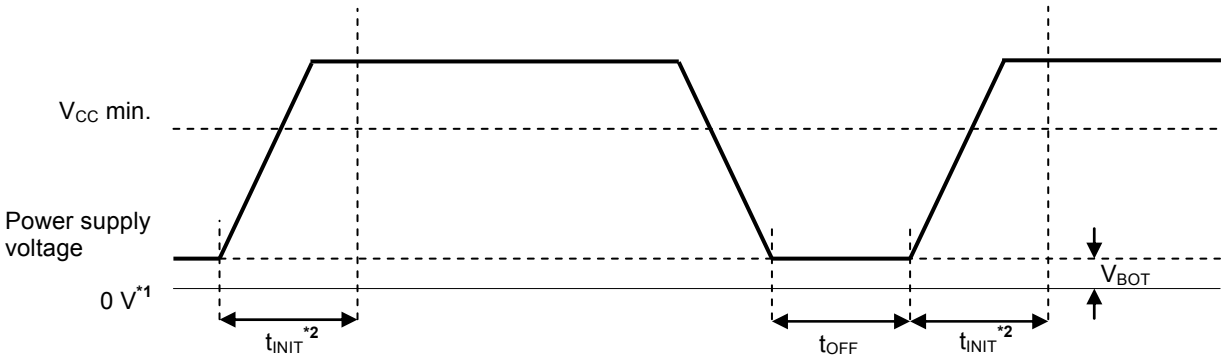
Figure 21 Initialization Time

5. 2 Caution when raising the power supply voltage

The internal circuit of this IC is reset by the power-on-clear circuit. In order for the power-on-clear circuit to operate normally, the condition showed in **Table 11** must be obeyed for raising the power supply voltage.
Due to the voltage drop, this IC may not perform normal communication if the power-on-clear operation condition is not fulfilled, even when the master device is reset.
However, the interface of this IC is reset normally and the master device can make normal communication if phase adjustment is performed, even when the power-on-clear operation condition of this IC is not fulfilled.

Table 11

Item	Symbol	Min.	Max.	Unit
Power-off time	t_{OFF}	100	–	μs
Power-off voltage	V_{BOT}	–	0.6	V



***1.** 0 V means that there is no potential difference between the VCC pin and the GND pin of this IC.
***2.** t_{INIT} is the time to initialize the internal IC. This IC does not accept any instruction during the initialization time.

Figure 22 Caution When Raising the Power Supply Voltage

6. Write protect function during the low power supply voltage

This IC has a built-in detection circuit which operates with the low power supply voltage, cancels Write when the power supply voltage drops and power-on. Its detection and release voltages are 1.3 V typ. (refer to **Figure 23**).
This IC cancels Write by detecting a low power supply voltage when it receives a stop condition. In the data trasmission and the Write operation, data in the address written during the low power supply voltage is not assurable.

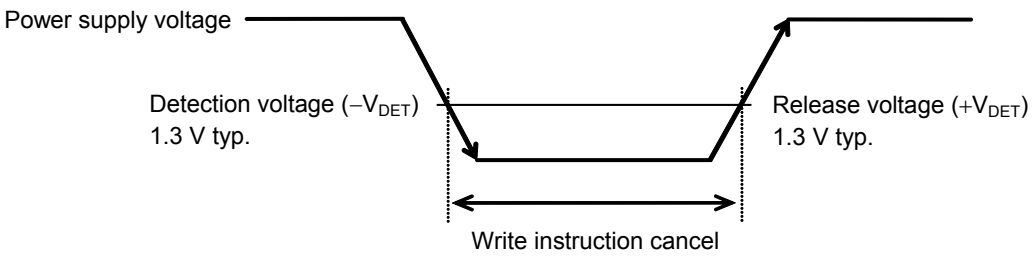


Figure 23 Operation during Low Power Supply Voltage

7. Data hold time ($t_{HD.DAT}$ = 0 ns)

If SCL and SDA of this IC are changed at the same time, it is necessary to prevent a start / stop condition from being mistakenly recognized due to the effect of noise.
This IC may error if it does not recognize a start / stop condition correctly during transmission.
In this IC, it is recommended to set the delay time of 0.3 μs minimum from a falling edge of SCL for the SDA.
This is to prevent this IC from going in a start / stop condition due to the time lag caused by the load of the bus line.

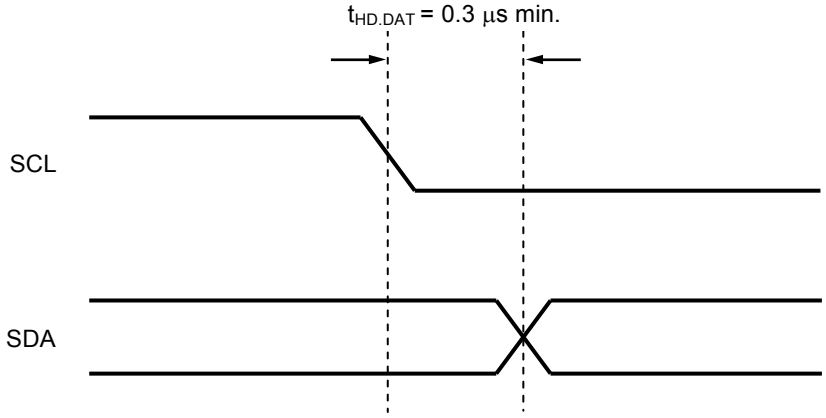


Figure 24 Data Hold Time

8. SDA pin and SCL pin noise suppression time

This IC includes a built-in low-pass filter at the SDA pin and the SCL pin to suppress noise. If the power supply voltage is 5.0 V, this suppression time can be suppressed noise with a pulse width of approx. 80 ns.
For details of the assurable value, refer to noise suppression time (t_I) in **Table 10** in "■ **AC Electrical Characteristics**".

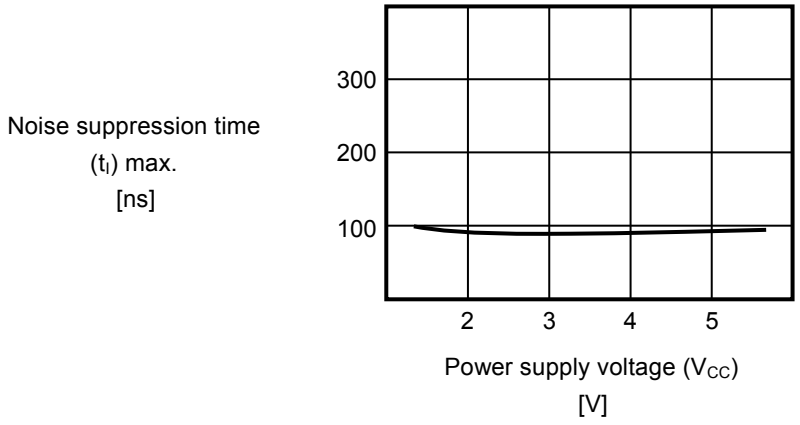
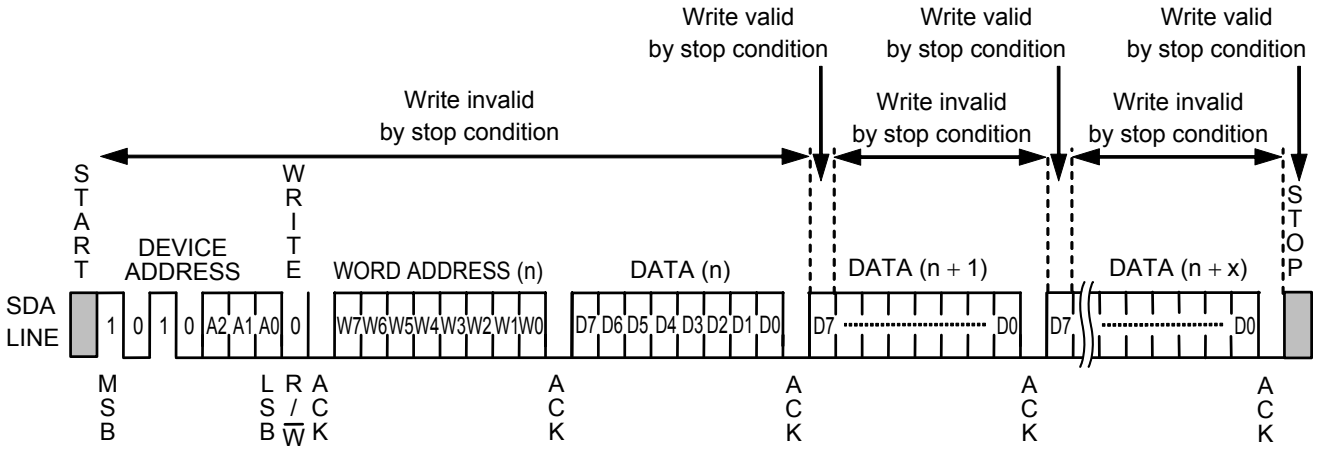


Figure 25 Noise Suppression Time for SDA Pin and SCL Pin

9. Operation when input stop condition during input write data

This IC does the write operation only when it receives data of 1 byte or more and receives a stop condition immediately after acknowledge output.
Refer to **Figure 26** regarding details.



Remark A0 is P0 in the S-24C04D/08D/16D.
A1 is P1 in the S-24C08D/16D.
A2 is P2 in the S-24C16D.
Set A0, A1, A2 to "0" in the product with SOT-23-5 package.

Figure 26 Write Operation by Inputting Stop Condition during Write

10. Command cancel by start condition

By a start condition, users are able to cancel command which is being input. However, adjust the phase while this IC is outputting "L" because users are not able to input a start condition. When users cancel the command, there may be a case that the address will not be identified. Use random read for the read operation, not current address read.

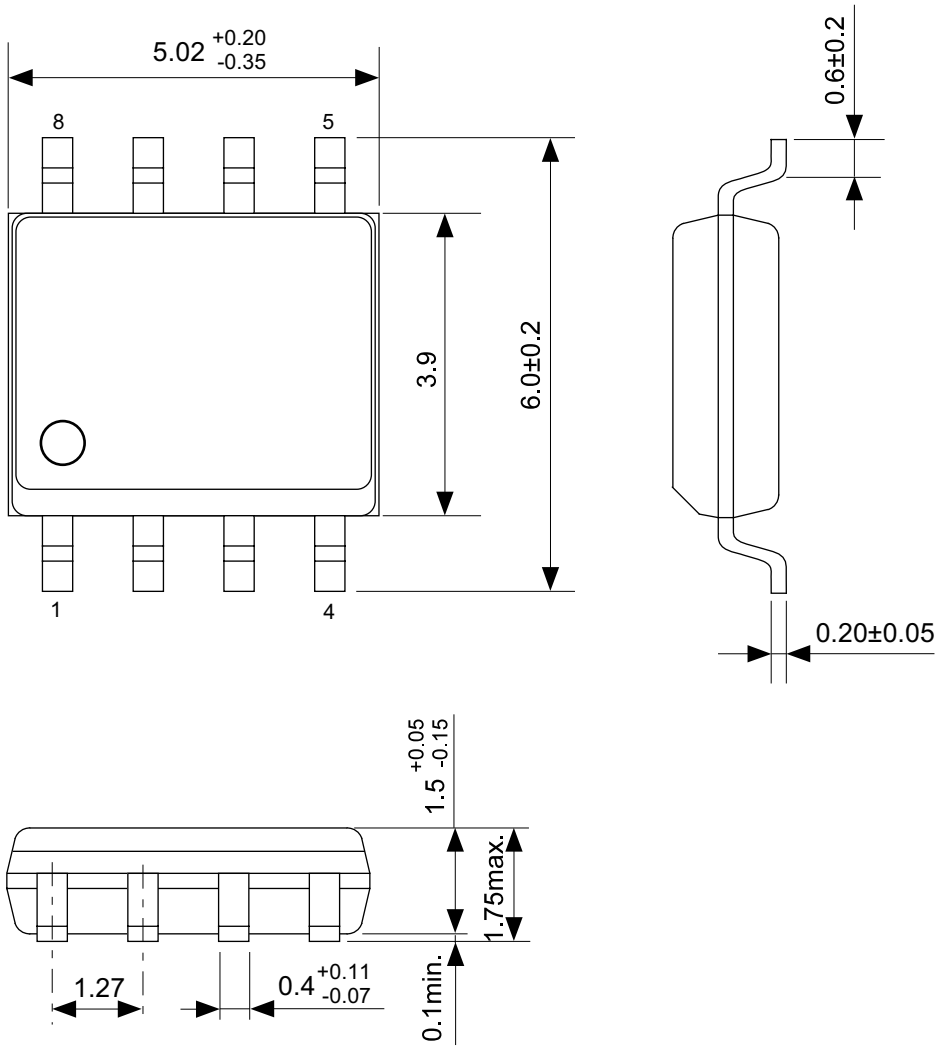
■ Precautions

- Do not operate these ICs in excess of the absolute maximum ratings. Attention should be paid to the power supply voltage, especially. The surge voltage which exceeds the absolute maximum ratings can cause latch-up and malfunction. Perform operations after confirming the detailed operation condition in the data sheet.

- Operations with moisture on this IC's pins may occur malfunction by short-circuit between pins. Especially, in occasions like picking this IC up from low temperature tank during the evaluation. Be sure that not remain frost on this IC's pin to prevent malfunction by short-circuit.
  Also attention should be paid in using on environment, which is easy to dew for the same reason.

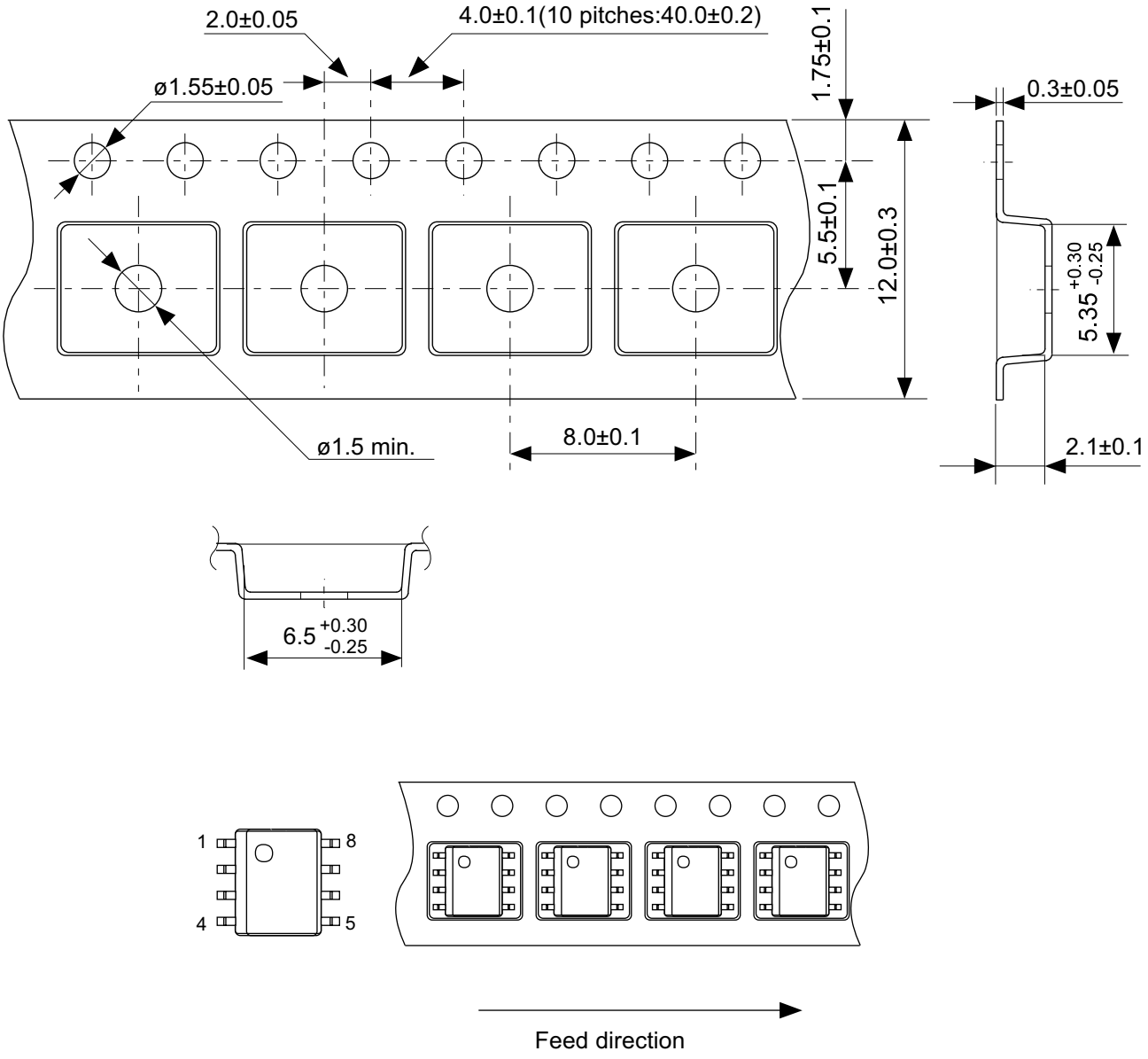
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.



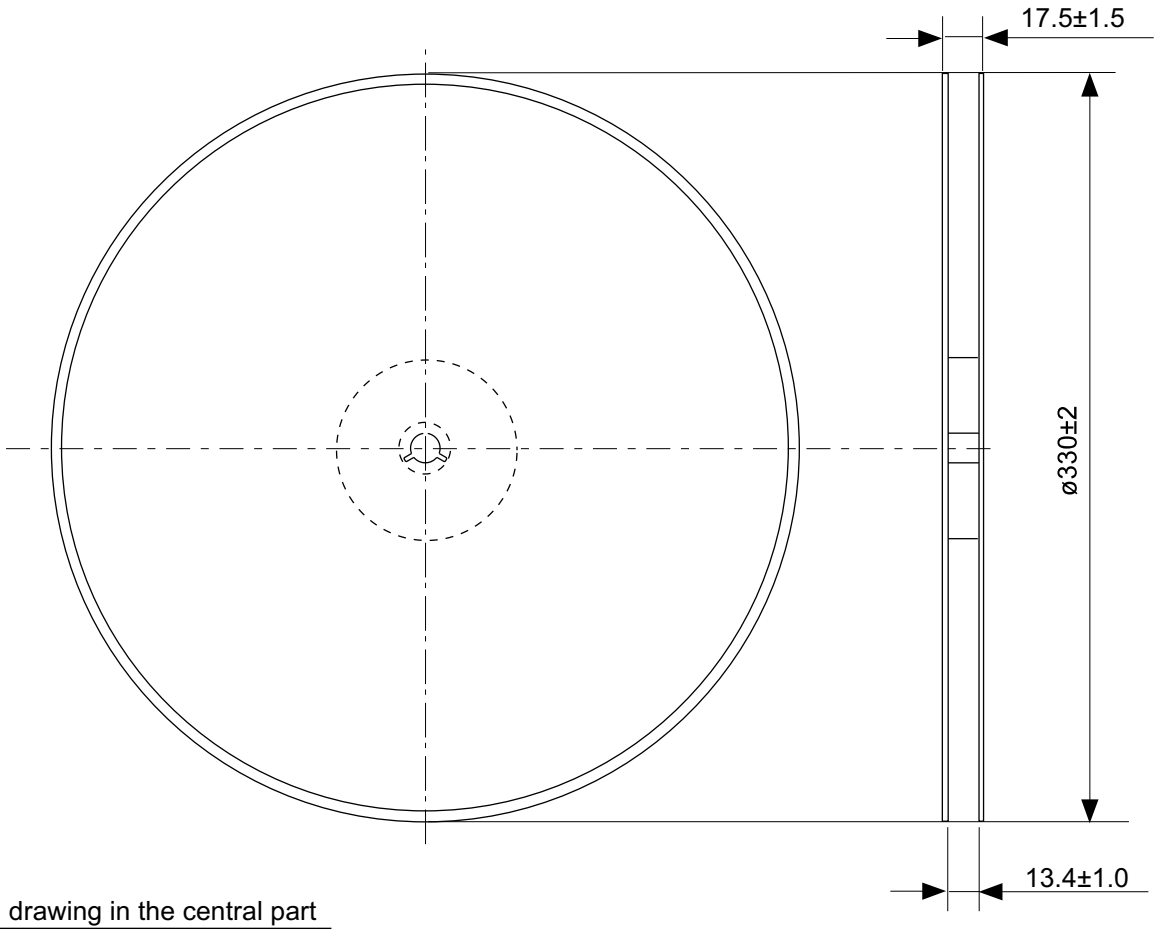
No. FJ008-Z-P-SD-2.1

TITLE	SOP8J-Z-PKG Dimensions
No.	FJ008-Z-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

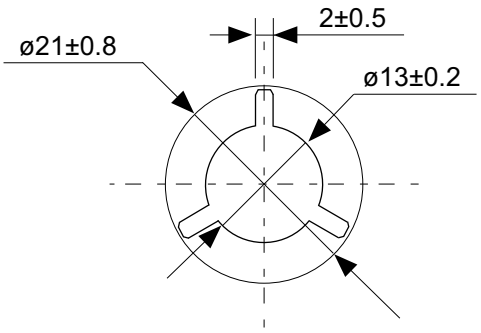


No. FJ008-Z-C-SD-1.0

TITLE	SOP8J-Z-Carrier Tape
No.	FJ008-Z-C-SD-1.0
ANGLE	
UNIT	mm
	ABLIC Inc.

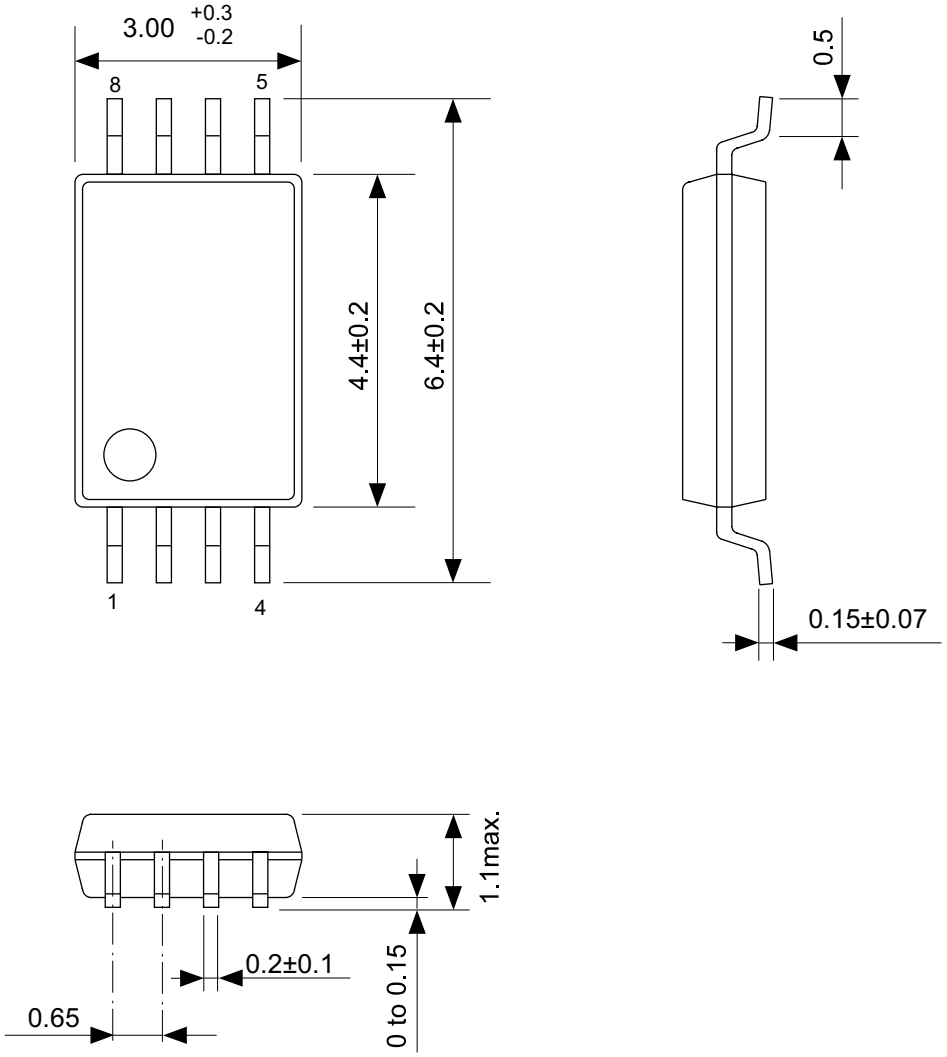


Enlarged drawing in the central part



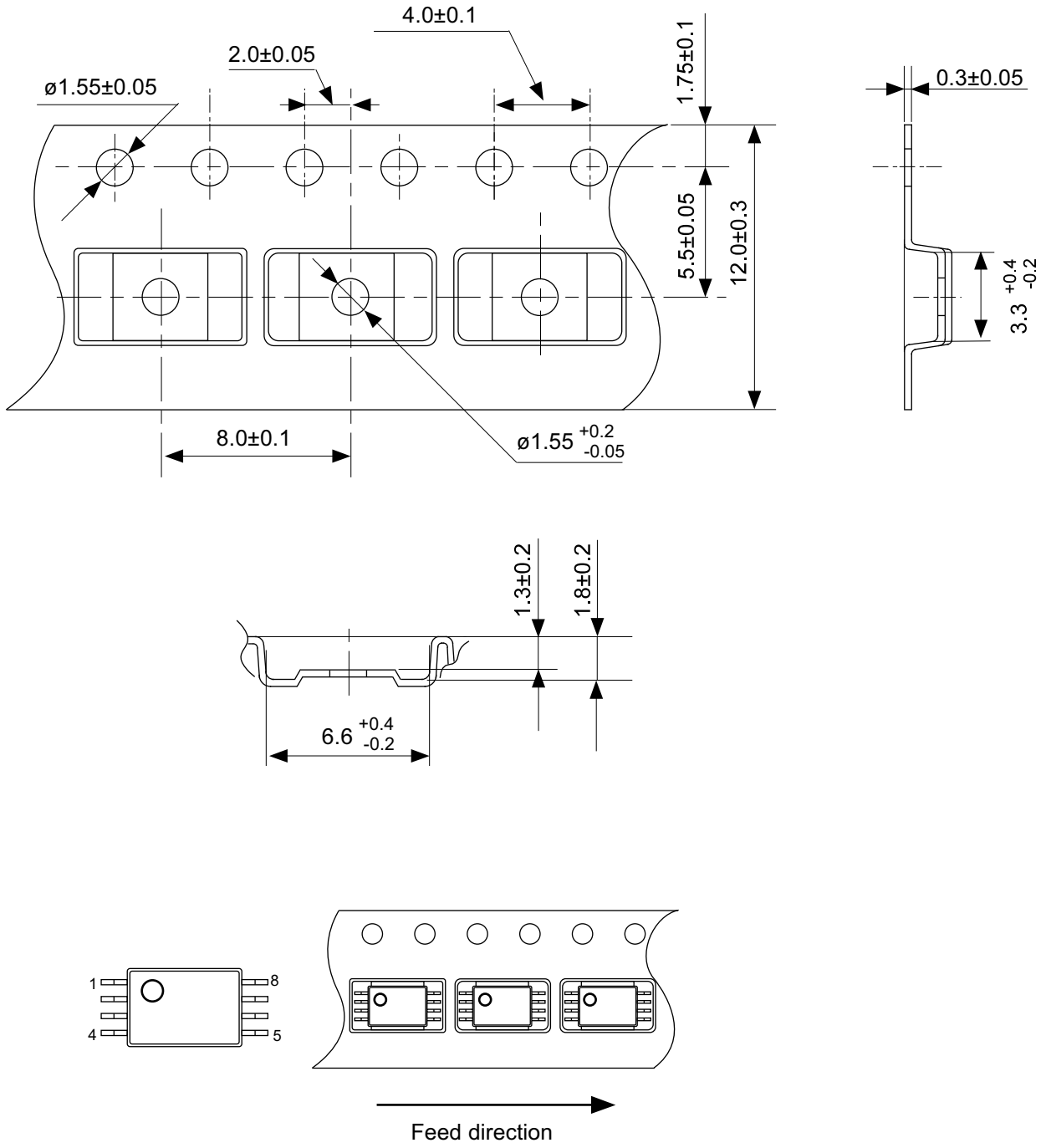
No. FJ008-Z-R-SD-1.0

TITLE	SOP8J-Z-Reel		
No.	FJ008-Z-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			



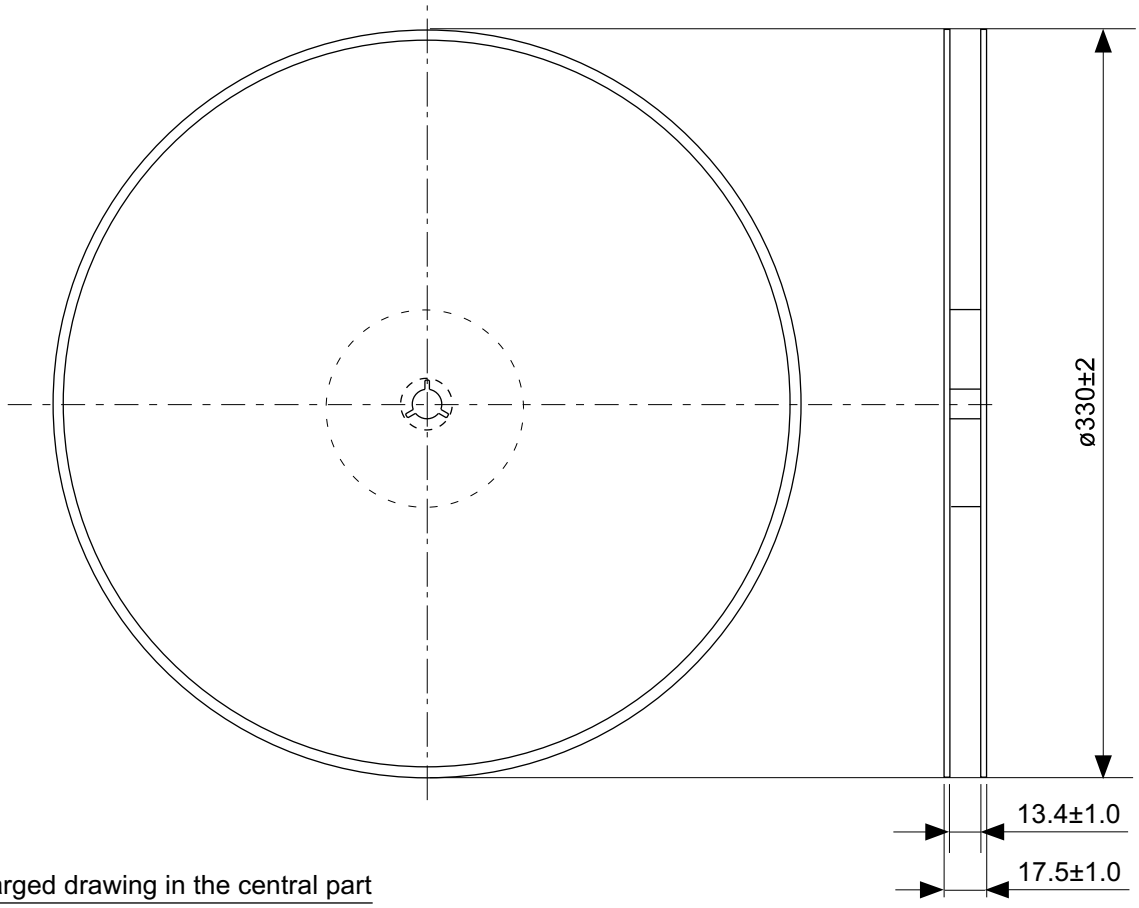
No. FT008-Z-P-SD-1.2

TITLE	TSSOP8-Z-PKG Dimensions
No.	FT008-Z-P-SD-1.2
ANGLE	
UNIT	mm
ABLIC Inc.	

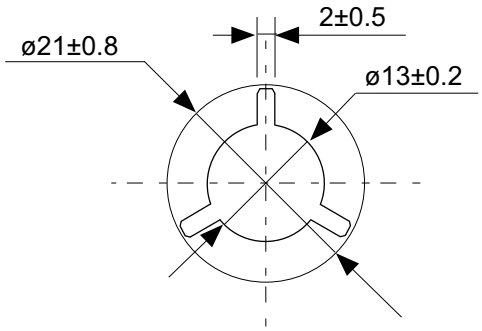


No. FT008-Z-C-SD-1.0

TITLE	TSSOP8-Z-Carrier Tape
No.	FT008-Z-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

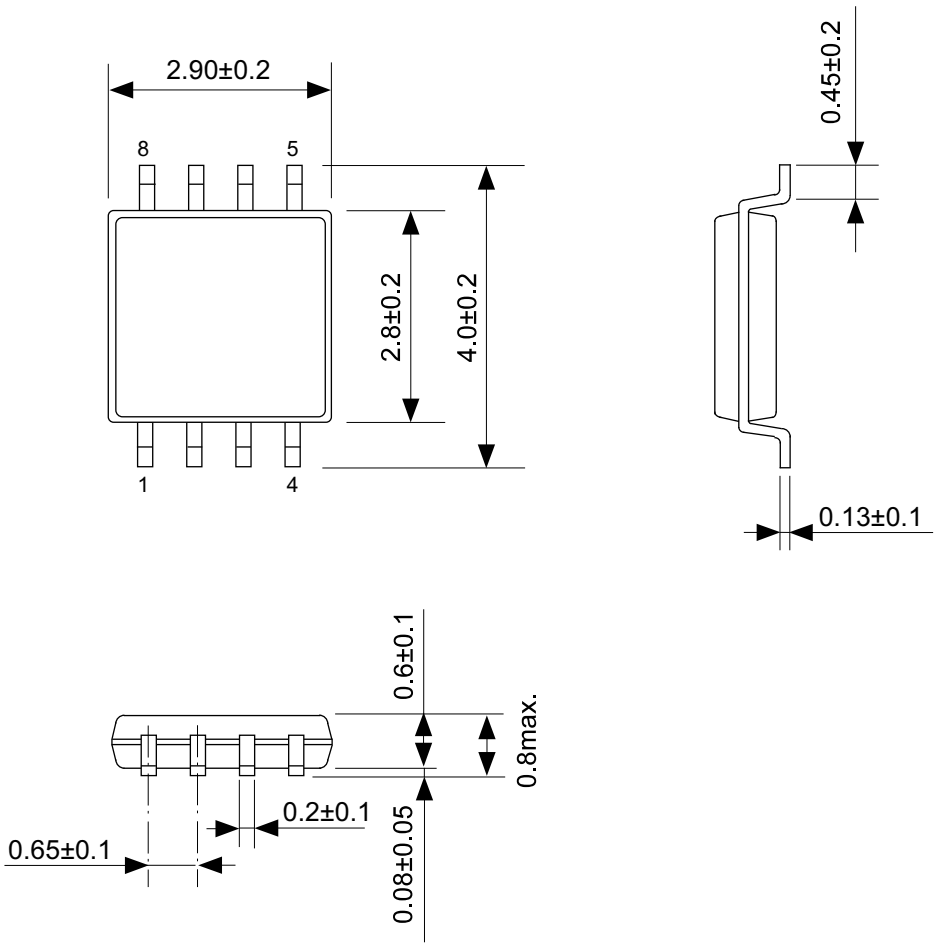


Enlarged drawing in the central part



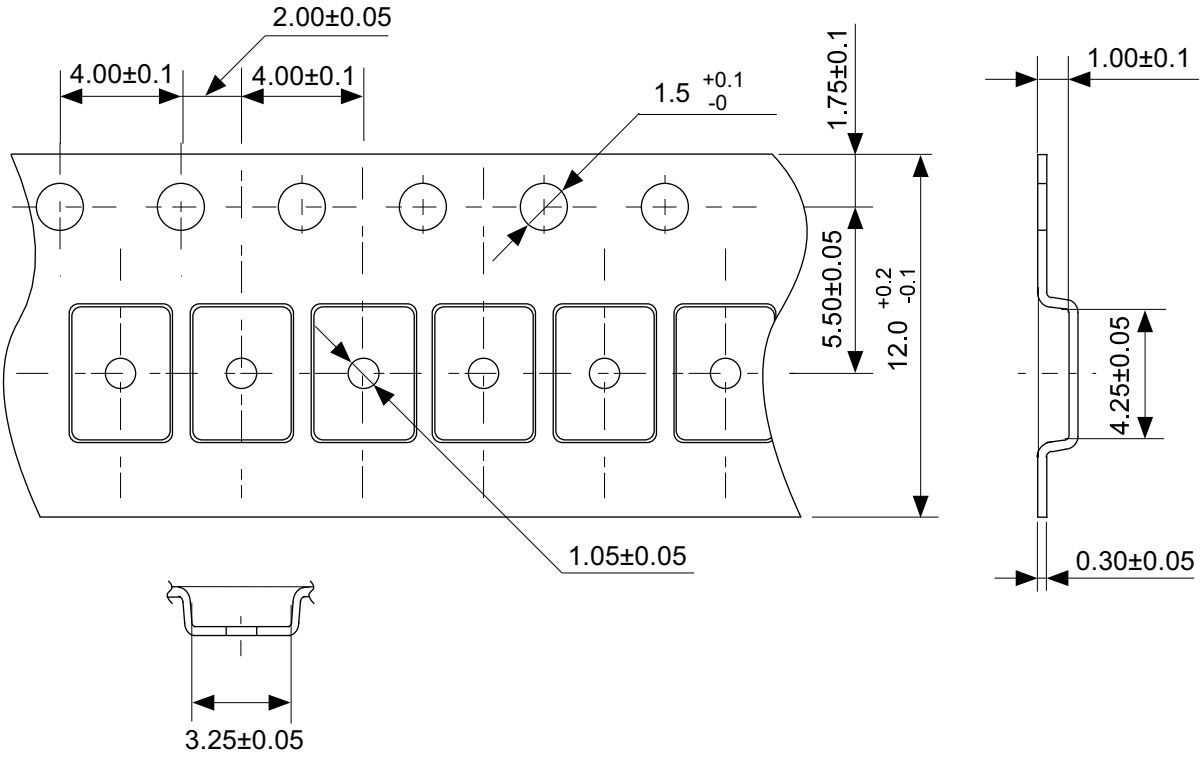
No. FT008-Z-R-SD-1.0

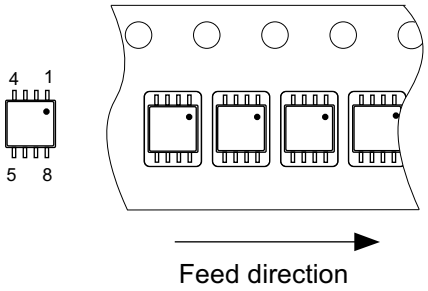
TITLE	TSSOP8-Z-Reel		
No.	FT008-Z-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
	ABLIC Inc.		



No. FM008-A-P-SD-1.2

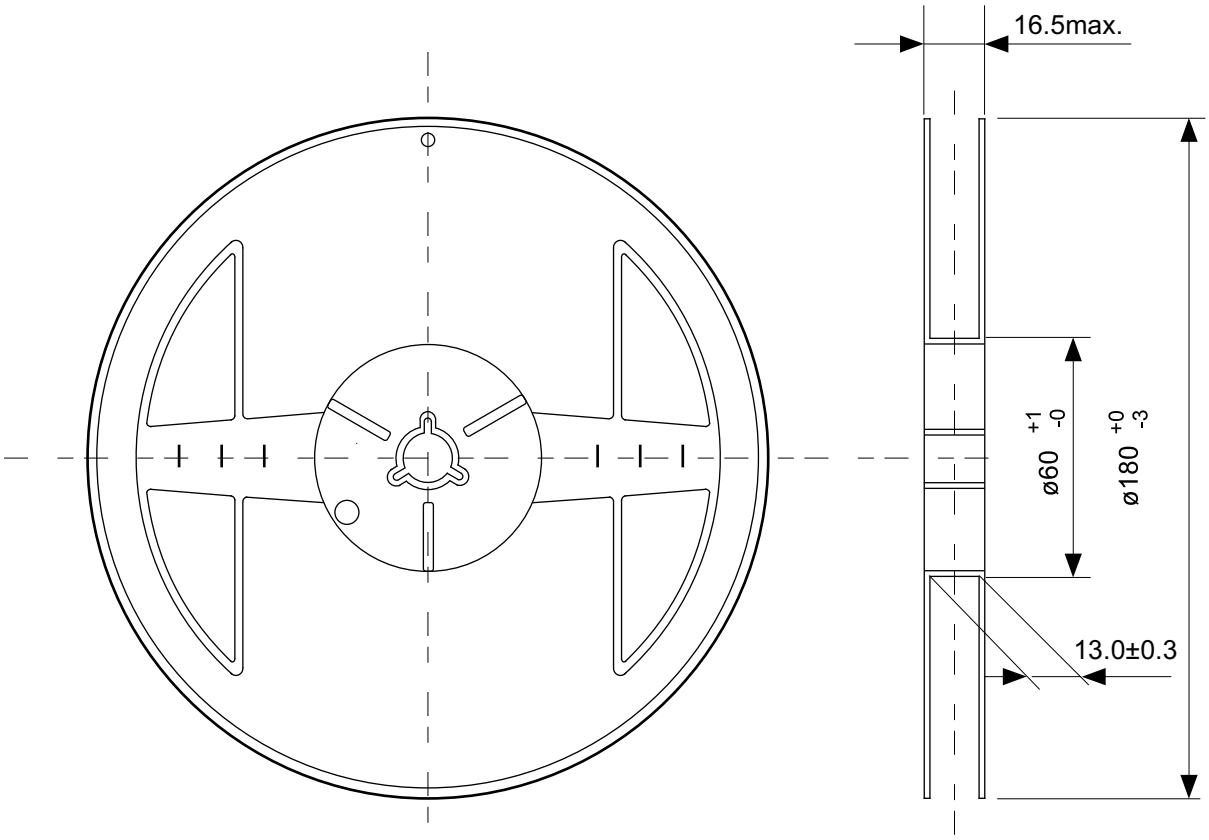
TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm
ABLIC Inc.	



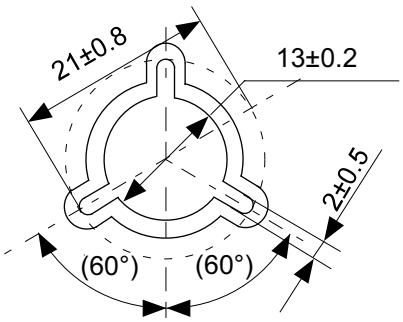


No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

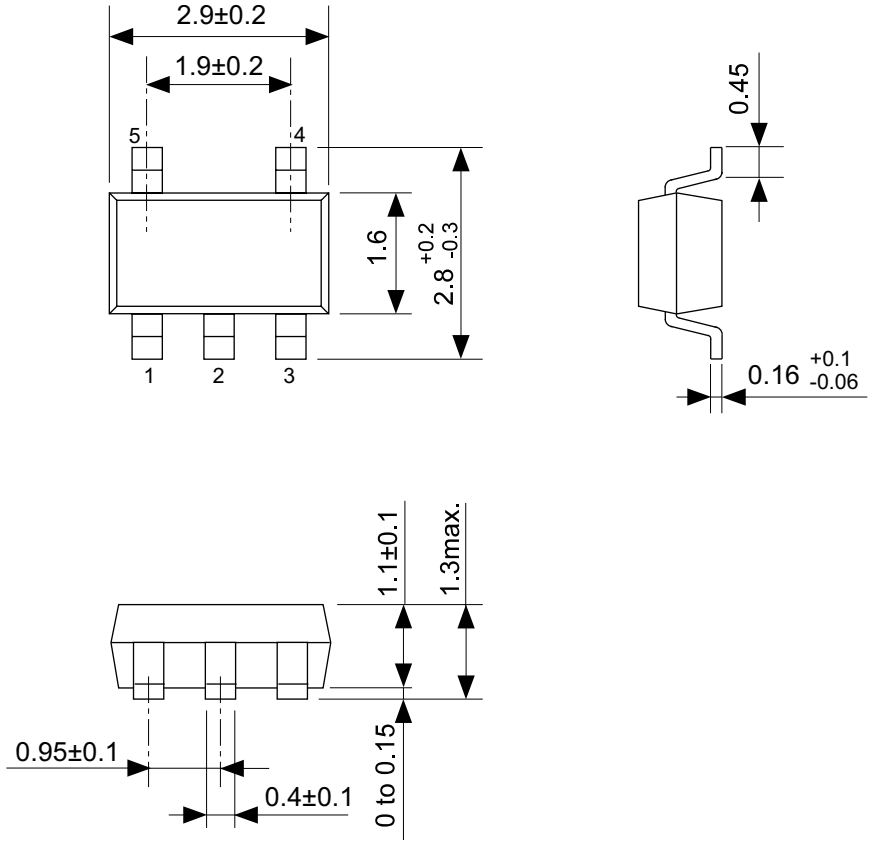


Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

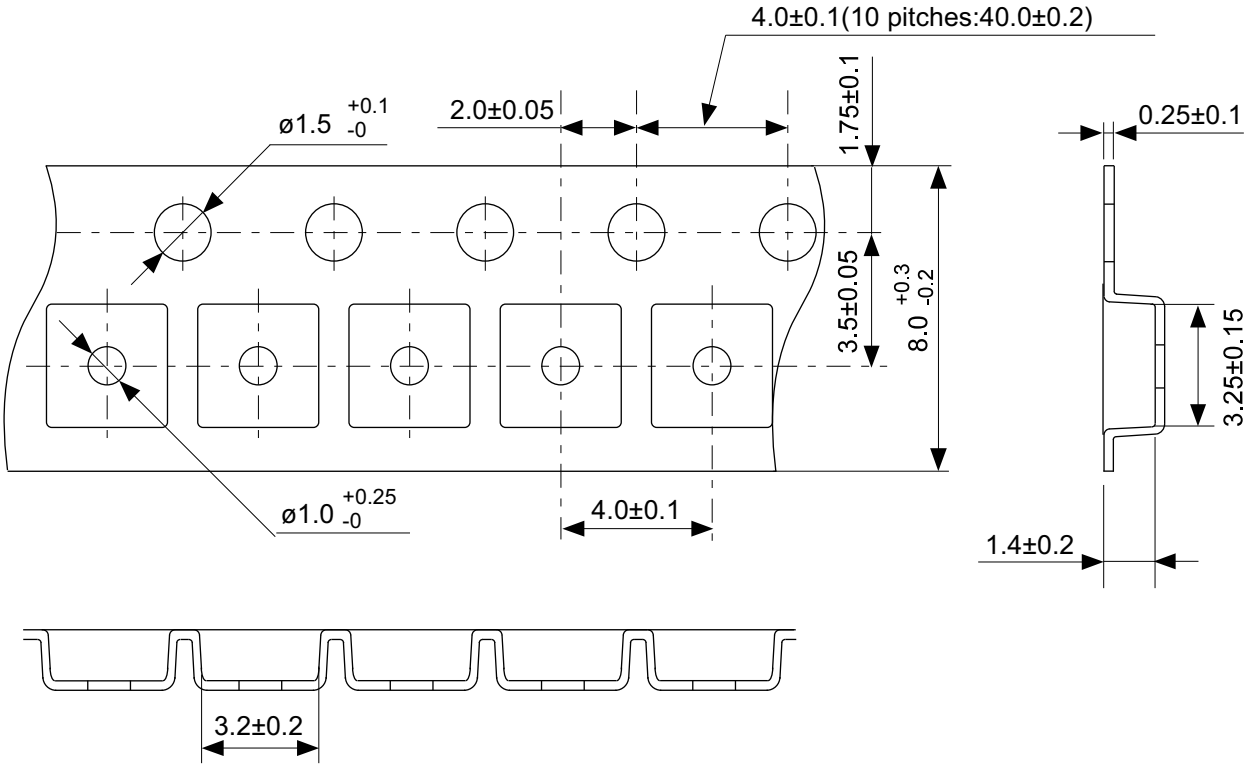
TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

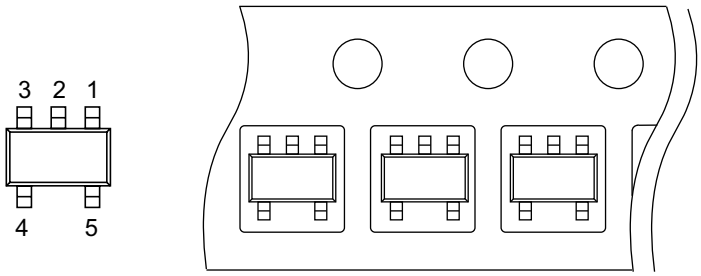


No. MP005-A-P-SD-1.3

TITLE	SOT235-B-PKG Dimensions
No.	MP005-A-P-SD-1.3
ANGLE	
UNIT	mm

ABLIC Inc.

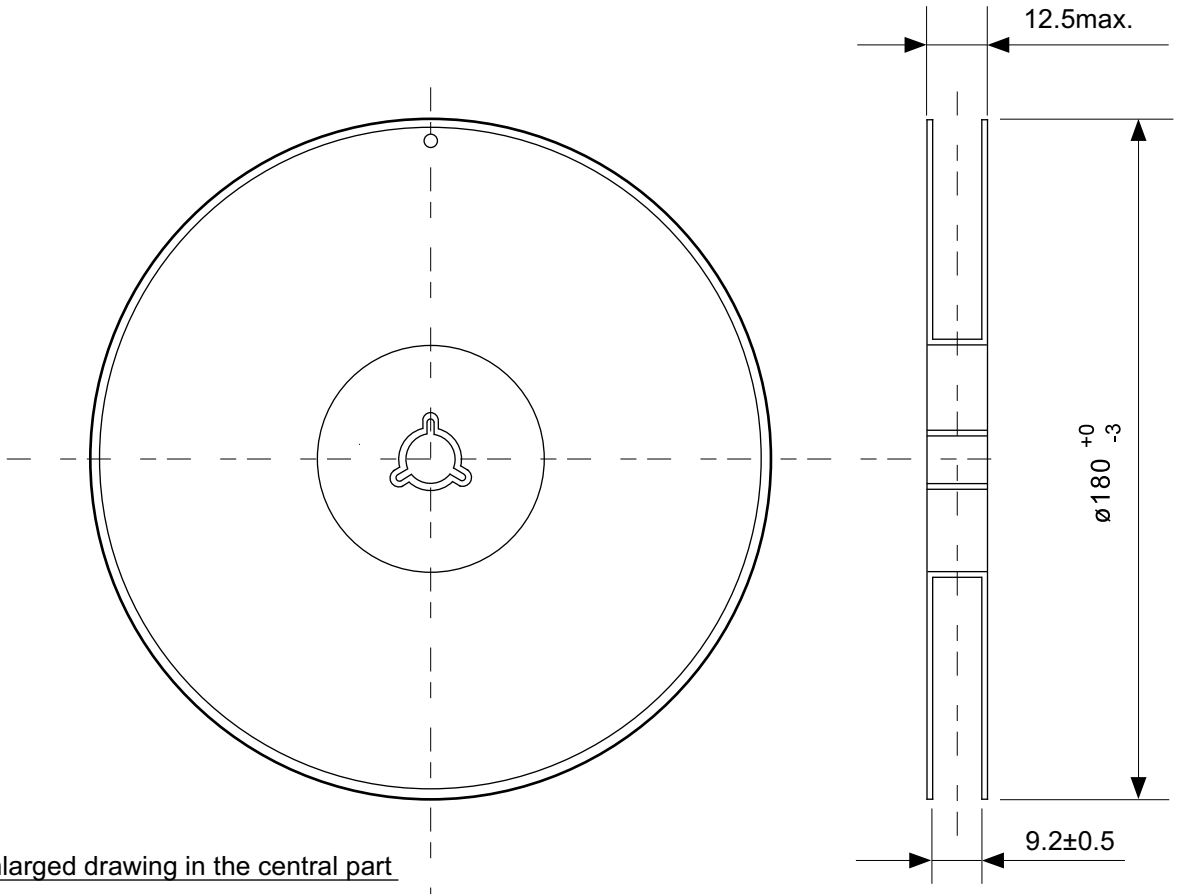




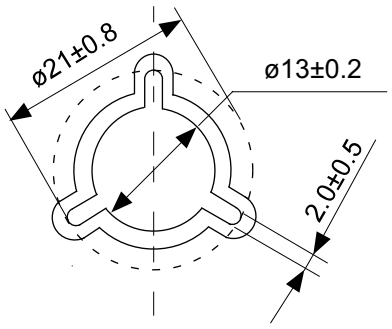
Feed direction

No. MP005-B-C-SD-1.0

TITLE	SOT235-B-Carrier Tape
No.	MP005-B-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

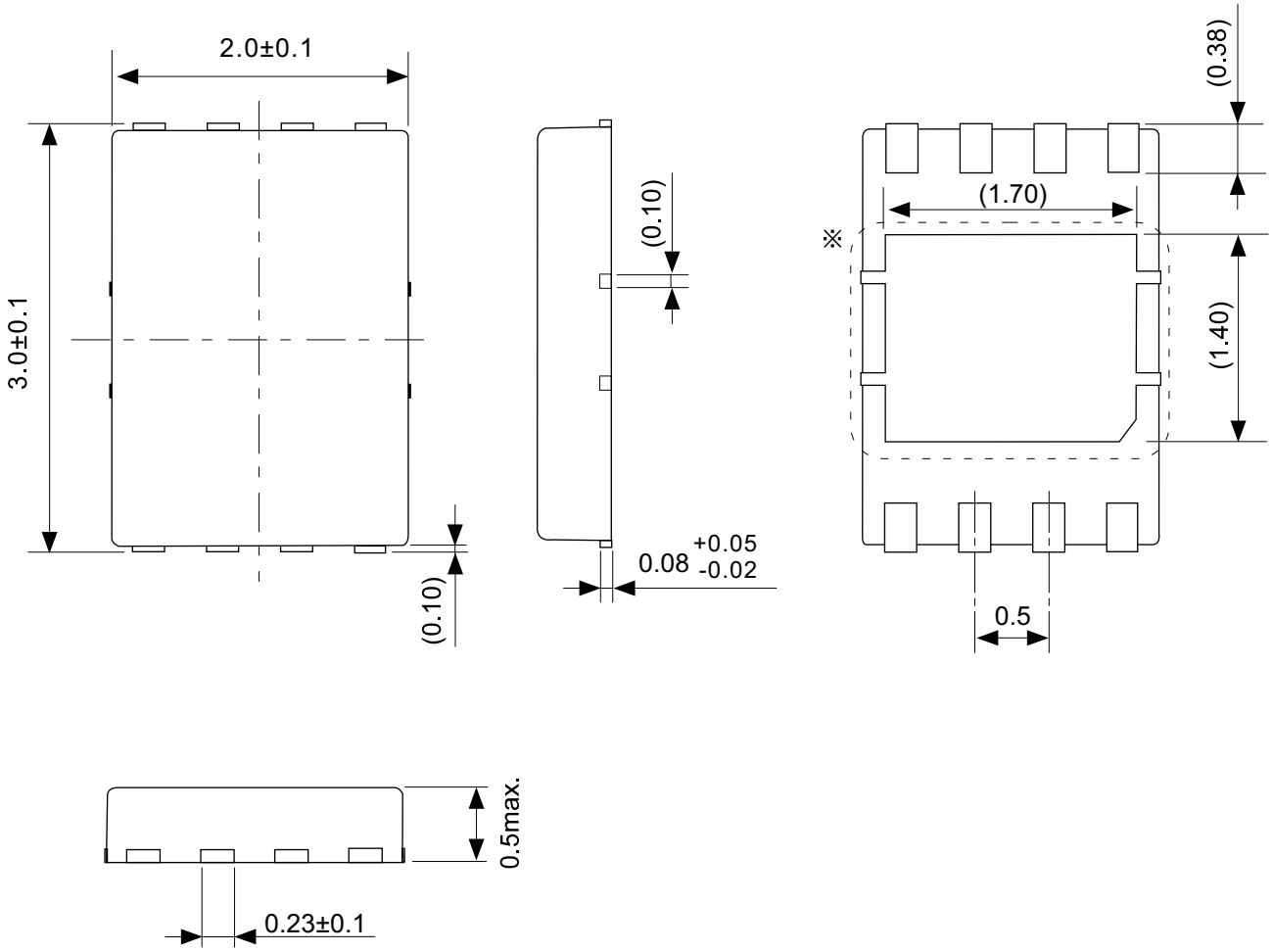


Enlarged drawing in the central part



No. MP005-B-R-SD-1.0

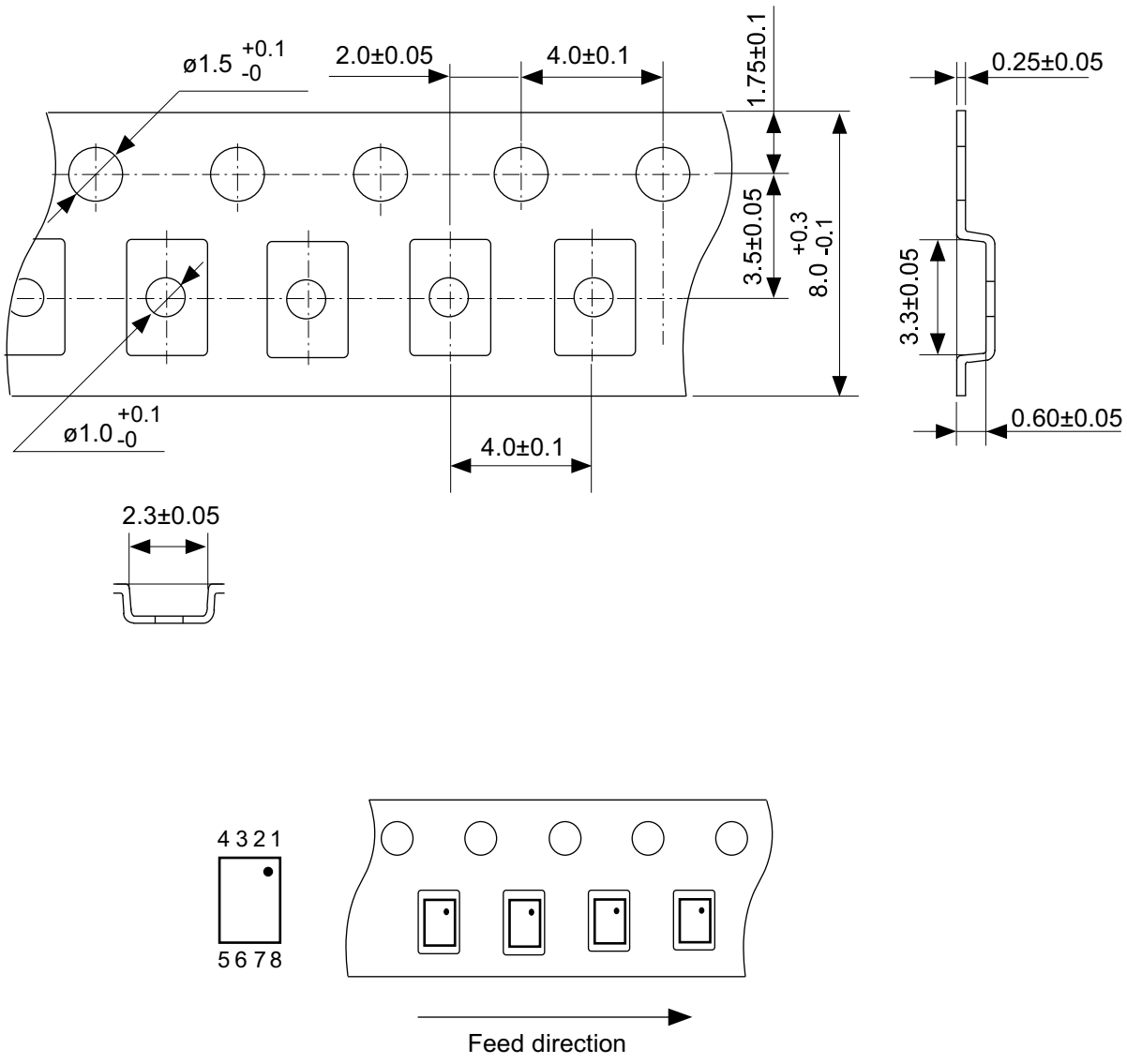
TITLE	SOT235-B-Reel		
No.	MP005-B-R-SD-1.0		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			



※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

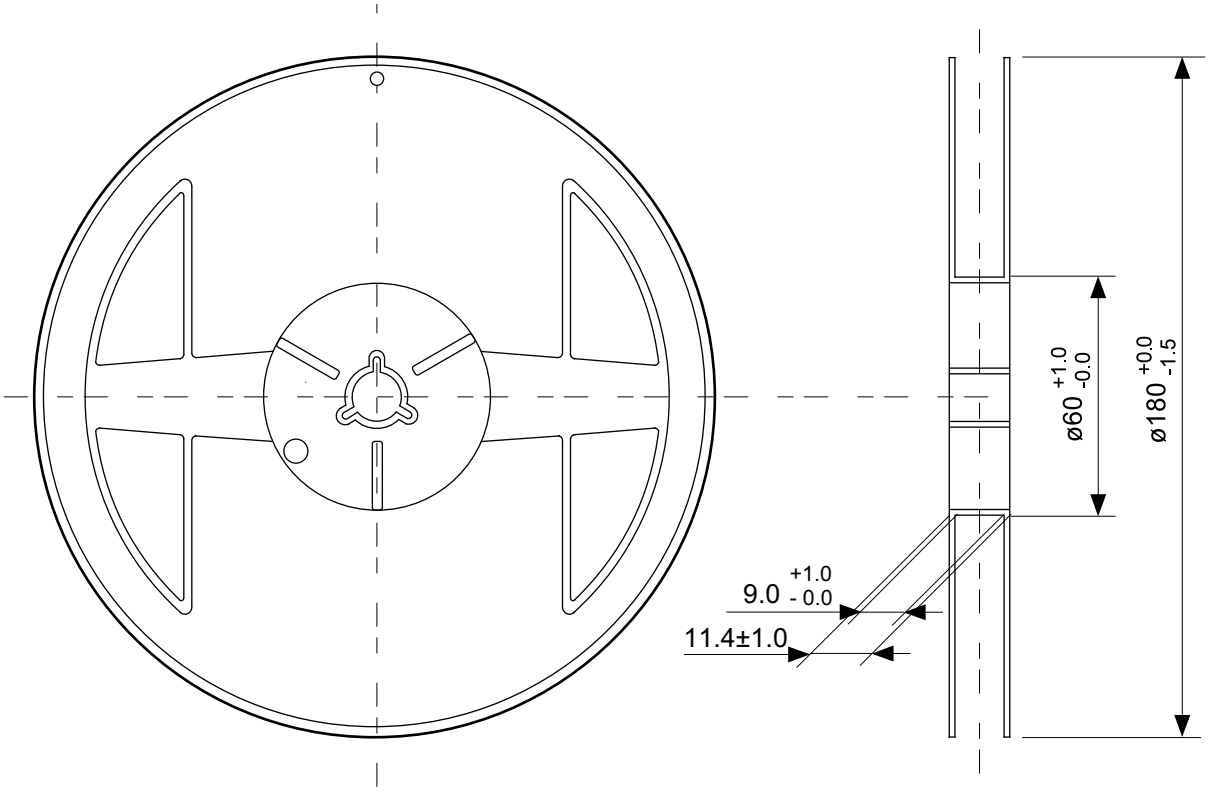
No. PP008-A-P-S1-2.0

TITLE	DFN-8/HSNT-8-A-PKG Dimensions
No.	PP008-A-P-S1-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

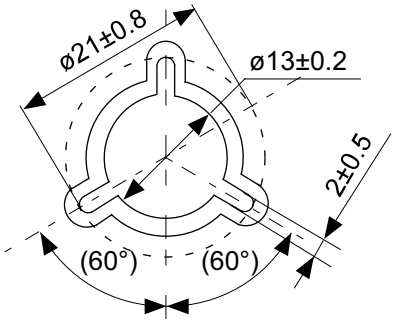


No. PP008-A-C-SD-1.0

TITLE	DFN-8/HSNT-8-A-Carrier Tape
No.	PP008-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

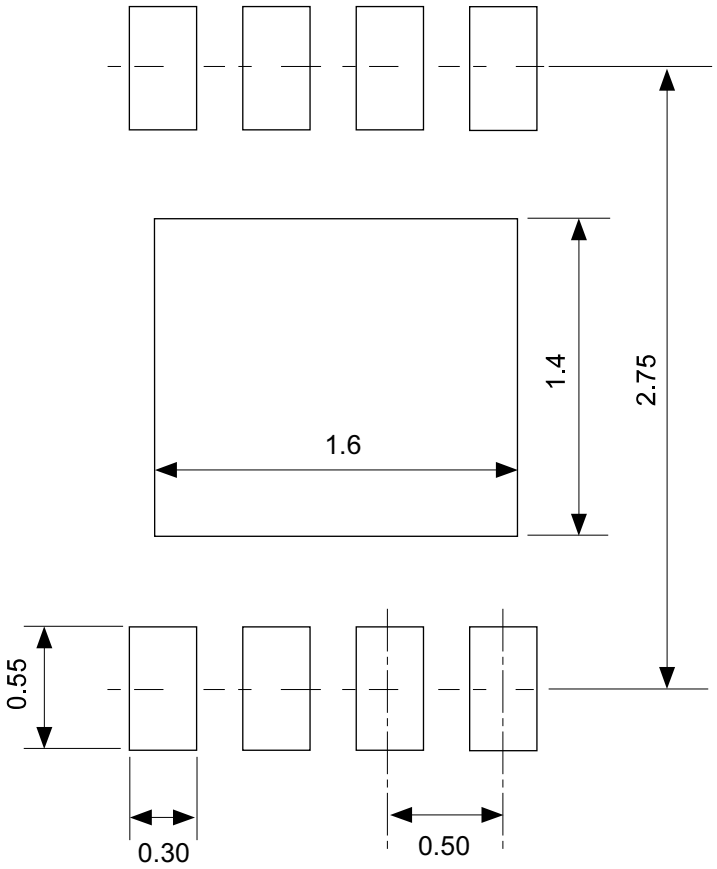


Enlarged drawing in the central part



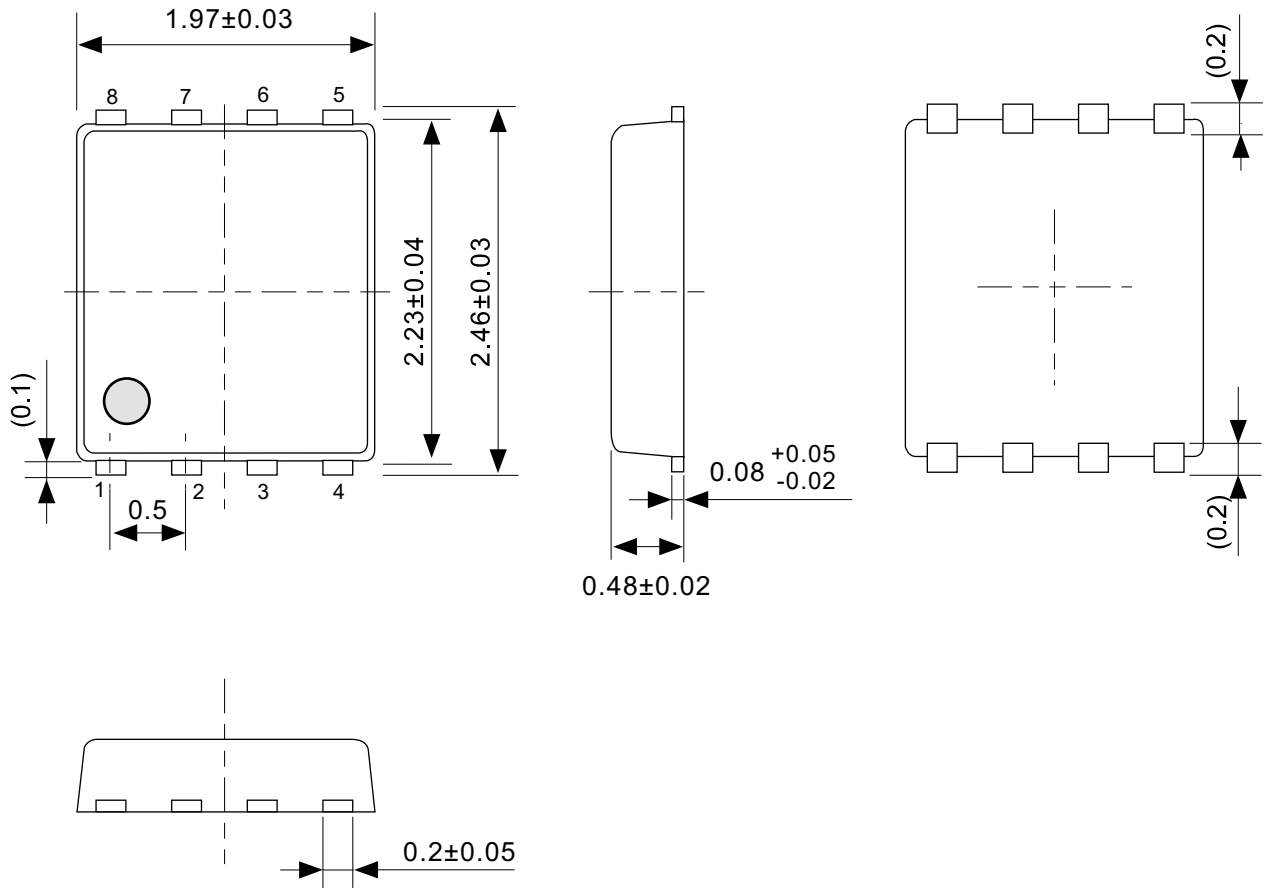
No. PP008-A-R-SD-1.0

TITLE	DFN-8/HSNT-8-A-Reel		
No.	PP008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



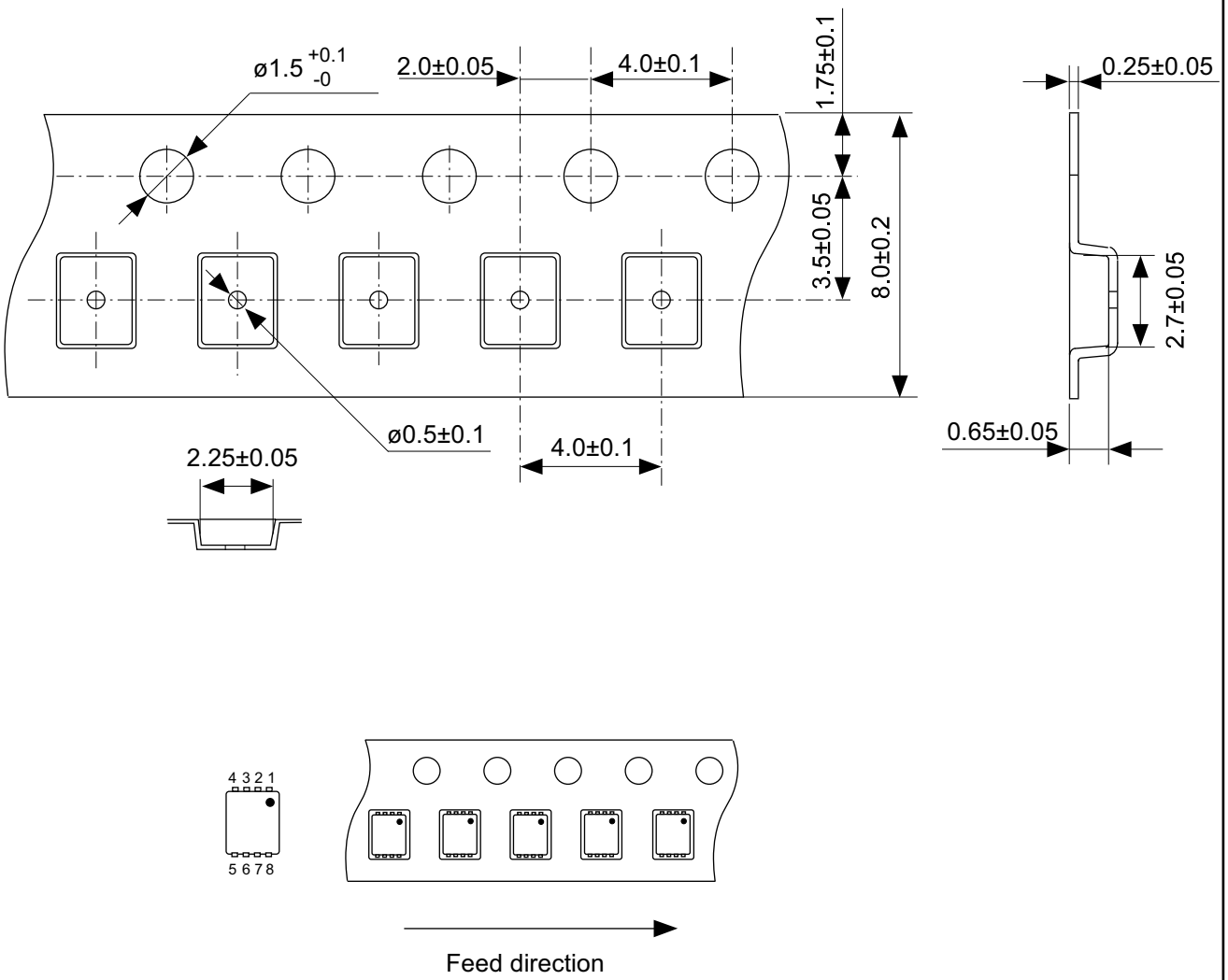
No. PP008-A-L-SD-1.0

TITLE	DFN-8/HSNT-8-A -Land Recommendation
No.	PP008-A-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



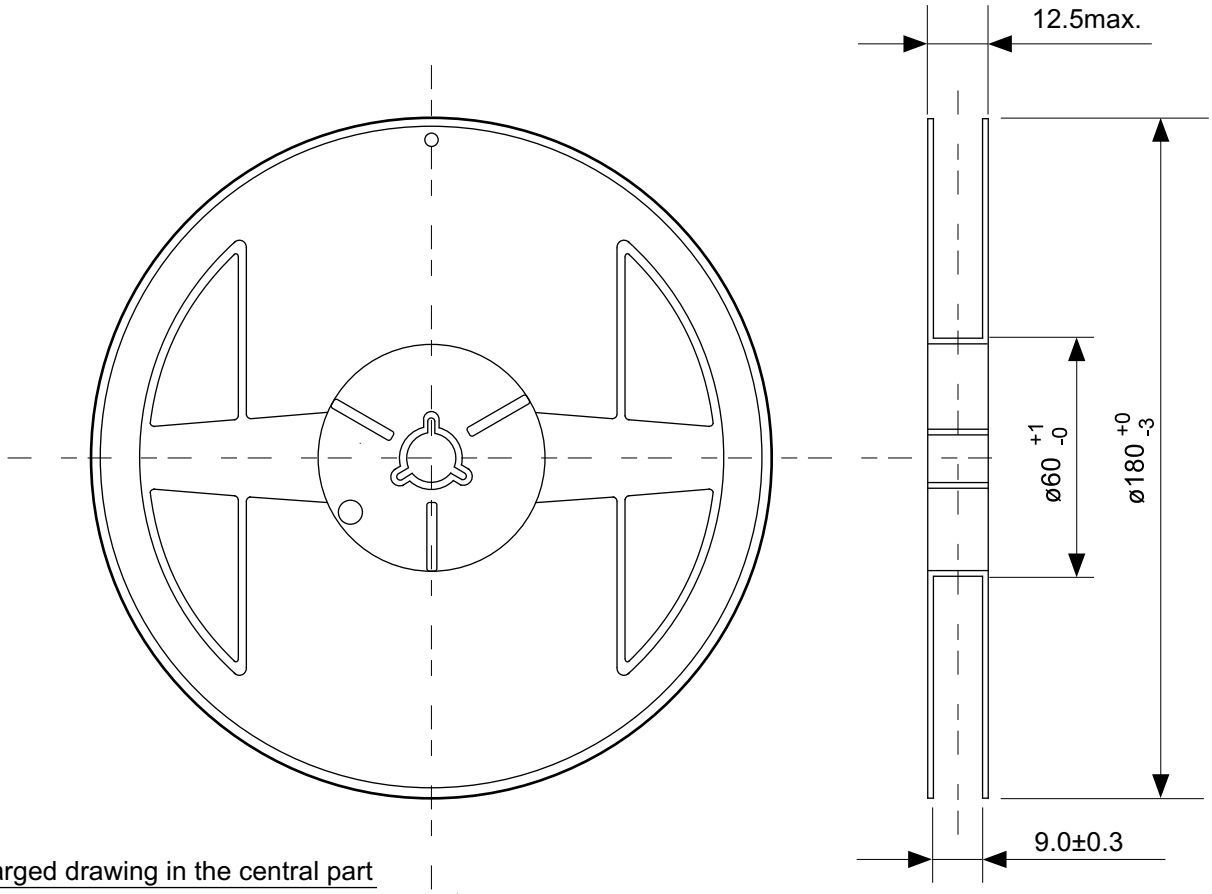
No. PH008-A-P-SD-2.1

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

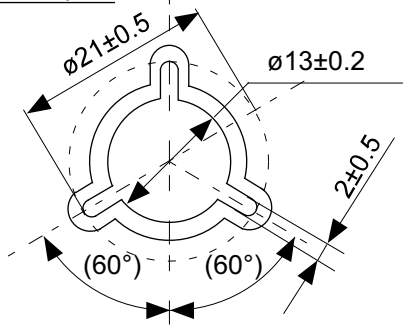


No. PH008-A-C-SD-2.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

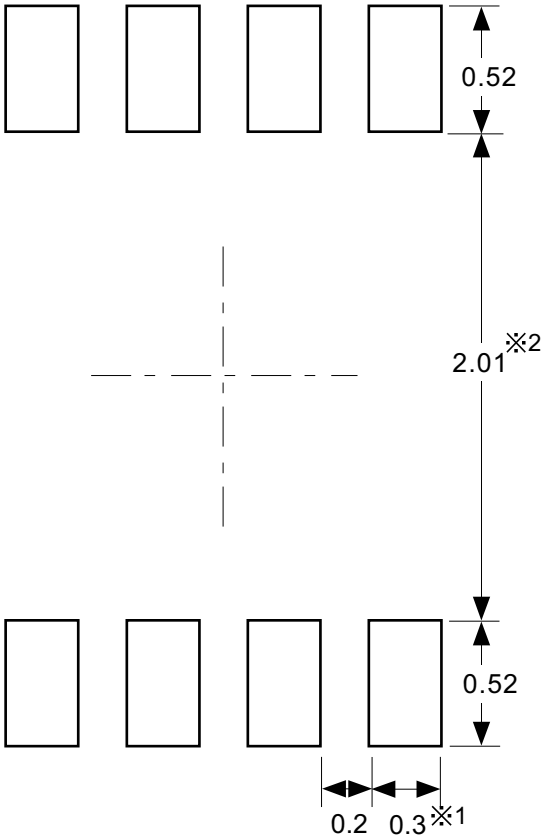


Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

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2.4-2019.07