Product Brief
July 2008
Revision 1.1

WPCN384U
Legacy-Reduced SuperI/O with Two Serial Ports, Parallel Port and GPIOs for Notebook and Docking Applications

General Description

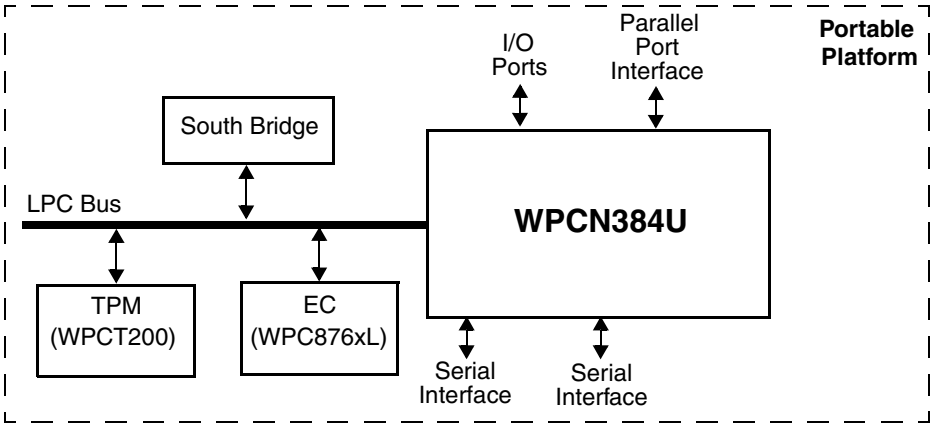
The WPCN384U, a member of the Nuvoton LPC SuperI/O family, is targeted for a wide range of notebook and docking applications. The WPCN384U is PC2001 and ACPI compliant, and features two Serial Ports, Parallel Port and General-Purpose Input/Output (GPIO) support for a total of 21 ports.

The WPCN384U is an optimized solution for notebook systems requiring no FIR Port, and for LPC-based docking stations implementing an on-board SuperI/O.

Outstanding Features

- Pin and software compatible with the Nuvoton 87384
- Two Serial Ports
- LPC bus interface, based on Intel's *LPC Interface Specification* Revision 1.1, August 2002 (supports CLKRUN and LPCPD signals)
- PC2001 and ACPI Revision 3.0 compliant
- IEEE 1284 Parallel Port
- 21 GPIO ports, including 14 with IRQ assertion capability
- Two testability modes (XOR Tree and TRI-STATE® device pins).
- 5V tolerant and back-drive protected pins (except LPC bus pins)
- 64-pin TQFP package

System Block Diagram

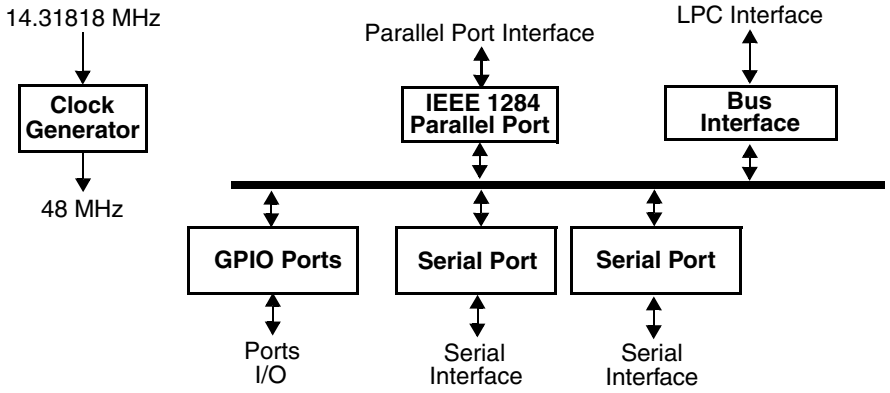


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Features

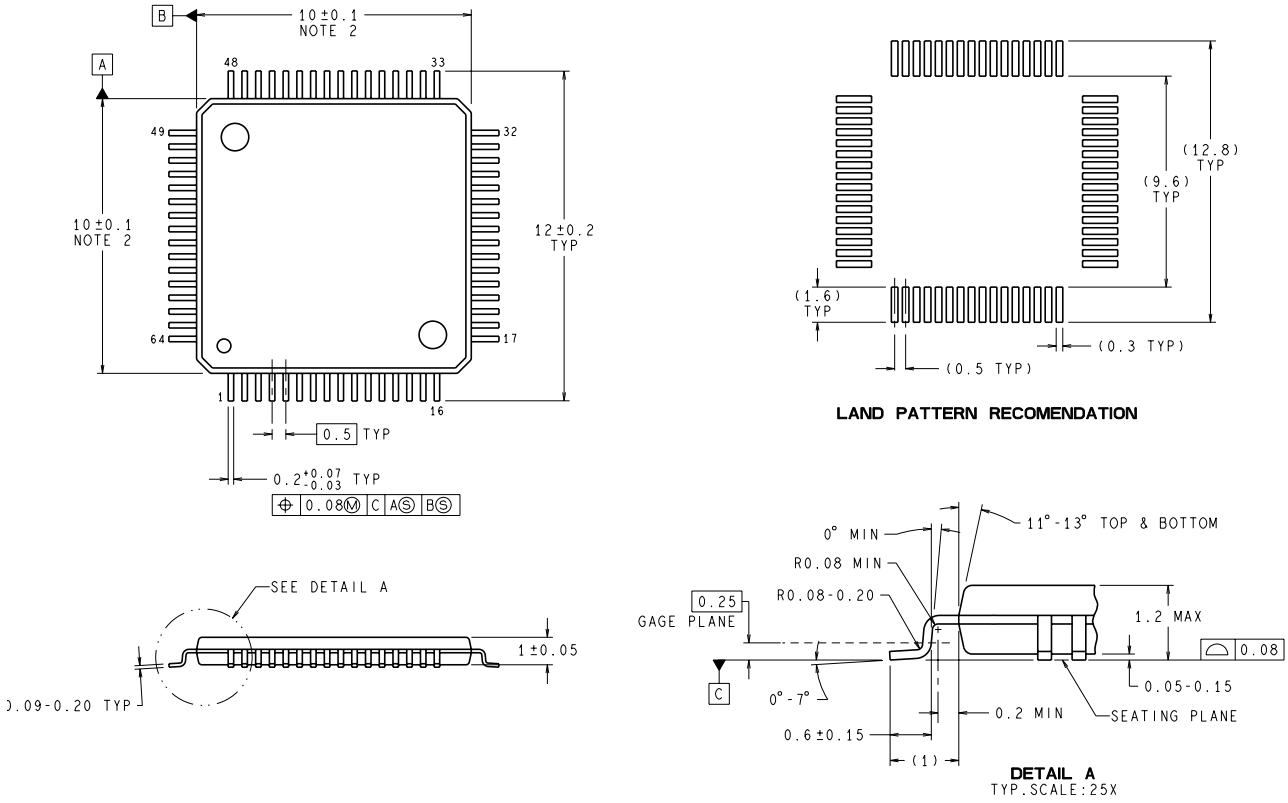
- Two Serial Ports (SP1 and SP2)
  - Software compatible with the 16550A and the 16450
  - Shadow register support for write-only bit monitoring
  - UART data rates up to 1.5 Mbaud
- IEEE 1284-Compliant Parallel Port
  - ECP, with Level 2 (14 mA sink and source output buffers)
  - Software or hardware control
  - Enhanced Parallel Port (EPP) compatible with EPP 1.7 and EPP 1.9
  - Supports EPP as mode 4 of the Extended Control Register (ECR)
  - Selection of internal pull-up or pull-down resistor for Paper End (PE) pin
  - Supports a demand DMA mode mechanism and a DMA fairness mechanism for improved bus utilization
  - Protection circuit that prevents damage to the parallel port when a printer connected to it is powered up or is operated at high voltages (in both cases, even if the WPCN384U is in power-down state)
- 21 General-Purpose I/O (GPIO) Ports
  - Supports IRQ assertion
  - Programmable drive type for each output pin (open-drain, push-pull or output disable)
  - Programmable option for internal pull-up resistor on each input pin
  - Output lock option
  - Input debounce mechanism
- LPC System Interface
  - 8-bit I/O cycles
  - $\overline{\text{LPCPD}}$ and $\overline{\text{CLKRUN}}$ support
  - Implements PCI mobile design guide recommendation (*PCI Mobile Design Guide 1.1, Dec. 18, 1998)*
- PC2001 and ACPI 3.0 Compliant
  - PnP Configuration Register structure
  - Flexible resource allocation for all logical devices
    - Relocatable base address
    - 15 IRQ routing options
    - Optional 8-bit DMA channels (where applicable) selected from four possible DMA channels
- Clock Sources
  - 14.318 MHz or 48 MHz clock input
  - LPC clock, 0 or 30 MHz to 33 MHz
- Strap Configuration
  - Base Address (BADDR) strap to determine the base address of the Index-Data register pair
  - Strap Inputs to select testability mode
- Power Supply
  - 3.3V supply operation
  - All pins are 5V tolerant, except LPC bus pins
  - All pins are back-drive protected, except LPC bus pins
- Testability
  - XOR Tree
  - TRI-STATE device pins

Internal Block Diagram



Physical Dimensions

All dimensions are in millimeters



64-Pin Thin Quad Flatpack (TQFP)
Order Number WPCN384U_0MG
(Replace "_" with chip revision: A, B, and so on)

Important Notice

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