Advanced

CAT25C03/05/09/17/33

2K/4K/8K/16K/32K SPI Serial CMOS E²PROM

FEATURES

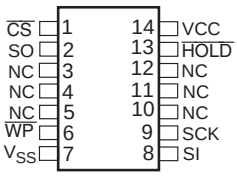
- 10 MHz SPI Compatible
- 1.8 to 6.0 Volt Operation
- Hardware and Software Protection
- Zero Standby Current
- Low Power CMOS Technology
- SPI Modes (0,0 &1,1)
- Commercial, Industrial and Automotive Temperature Ranges
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Self-Timed Write Cycle
- 8-Pin DIP/SOIC, 16-Pin SOIC and 14-Pin TSSOP
- Page Write Buffer
- Write Protection
  – Protect First Page, Last Page, Any 1/4 Array or Lower 1/2 Array

DESCRIPTION

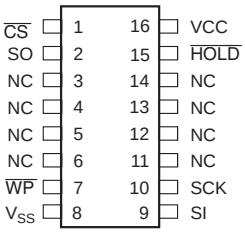
The CAT25C03/05/09/17/33 is a 2K/4K/8K/16K/32K-Bit SPI Serial CMOS E²PROM internally organized as 256x8/512x8/1024x8/2048x8/4096x8 bits. Catalyst's advanced CMOS Technology substantially reduces device power requirements. The CAT25C03/05 features a 16-byte page write buffer. The 25C09/17/33 features a 32-byte page write buffer.The device operates via the SPI bus serial interface and is enabled though a Chip Select ($\overline{CS}$). In addition to the Chip Select, the clock input (SCK), data in (SI) and data out (SO) are required to access the device. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence. The CAT25C03/05/09/17/33 is designed with software and hardware write protection features. The device is available in 8-pin DIP, 8-pin SOIC, 16-pin SOIC, 8-pin TSSOP and 14-pin TSSOP packages.

PIN CONFIGURATION

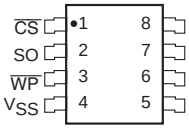
TSSOP Package (U14)



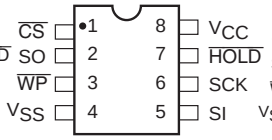
SOIC Package (S16)



SOIC Package (S)



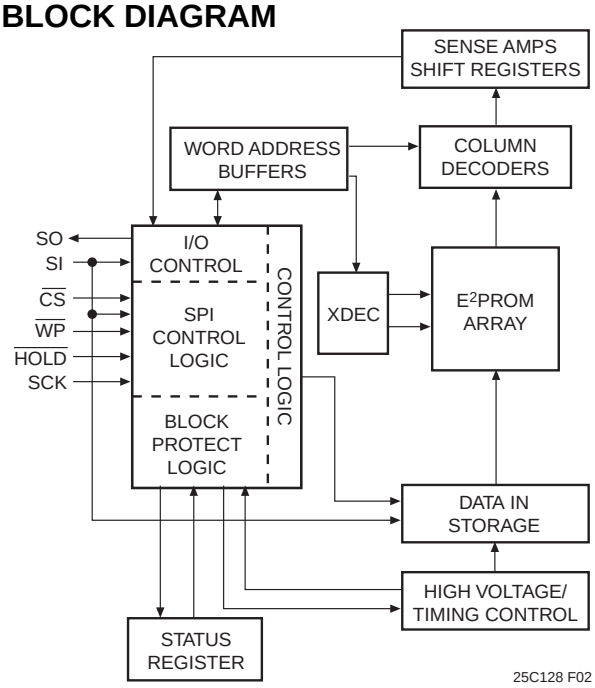
DIP Package (P)



TSSOP Package (U)



BLOCK DIAGRAM



PIN FUNCTIONS

Pin Name	Function
SO	Serial Data Output
SCK	Serial Clock
$\overline{WP}$	Write Protect
V_{CC}	+1.8V to +6.0V Power Supply
V_{SS}	Ground
$\overline{CS}$	Chip Select
SI	Serial Data Input
$\overline{HOLD}$	Suspends Serial Input
NC	No Connect

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Doc. No. 25068-00 2/98

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) ..... 100 mA

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	1,000,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

V_{CC} = +1.8V to +6.0V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}	Power Supply Current (Operating Write)			5	mA	V_{CC} = 5V @ 5MHz SO=open; CS=Vss
I_{CC2}	Power Supply Current (Operating Read)			0.4	mA	V_{CC} = 5.5V F_{CLK} = 5MHz
I_{SB}	Power Supply Current (Standby)			0	µA	$\overline{CS}$ = V_{CC} V_{IN} = V_{SS} or V_{CC}
I_{LI}	Input Leakage Current			2	µA	
I_{LO}	Output Leakage Current			3	µA	V_{OUT} = 0V to V_{CC}, CS = 0V
V_{IL}(3)	Input Low Voltage	-1		V_{CC} x 0.3	V	
V_{IH}(3)	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL1}	Output Low Voltage			0.4	V	4.5V≤V_{CC}<5.5V I_{OL} = 3.0mA I_{OH} = -1.6mA
V_{OH1}	Output High Voltage	V_{CC} - 0.8			V	
V_{OL2}	Output Low Voltage			0.2	V	1.8V≤V_{CC}<2.7V I_{OL} = 150µA I_{OH} = -100µA
V_{OH2}	Output High Voltage	V_{CC}-0.2			V	

Note:

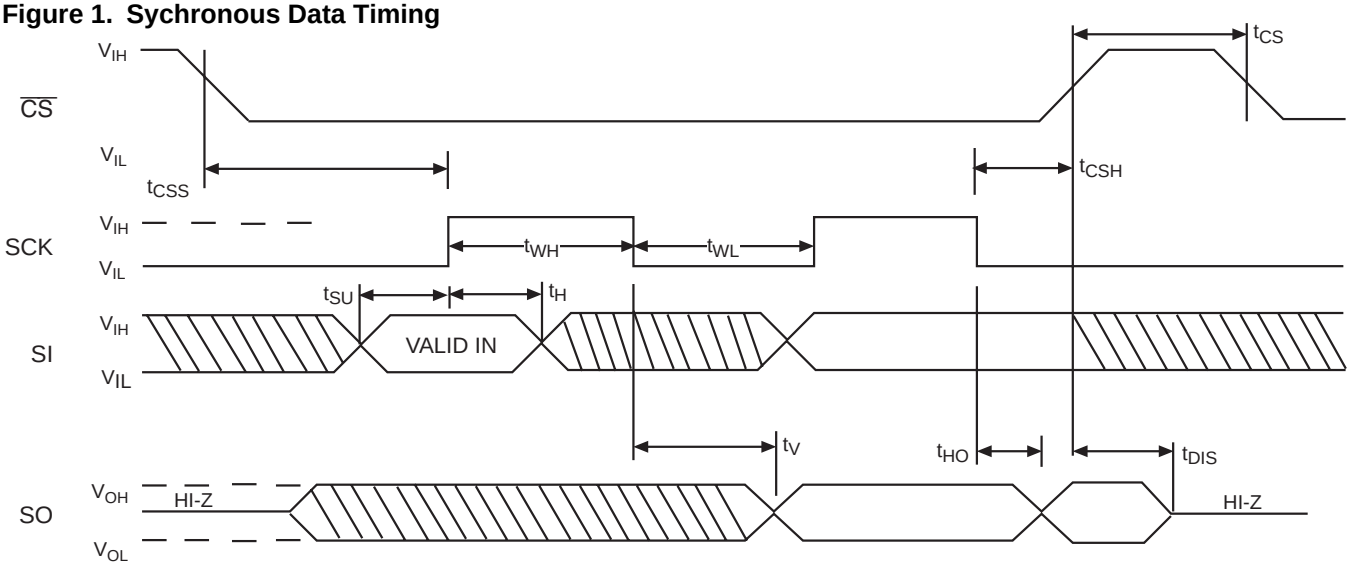
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.

(2) Output shorted for no more than one second. No more than one output shorted at a time.

(3) This parameter is tested initially and after a design or process change that affects the parameter.

(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

Figure 1. Sychronous Data Timing



A.C. CHARACTERISTICS

SYMBOL	PARAMETER	Limits				UNITS	Test Conditions
		1.8, 2.5		4.5V-5.5V			
		Min.	Max.	Min.	Max.		
t_{SU}	Data Setup Time	50		10		ns	C_L = 50pF
t_H	Data Hold Time	50		20		ns	
t_{WH}	SCK High Time	200		40		ns	
t_{WL}	SCK Low Time	200		40		ns	
f_{SCK}	Clock Frequency	DC	2	DC	10	MHz	
t_{LZ}	$\overline{HOLD}$ to Output Low Z		50		50	ns	
t_{RI}(1)	Input Rise Time		2		2	µs	
t_{FI}(1)	Input Fall Time		2		2	µs	
t_{HD}	$\overline{HOLD}$ Setup Time	100		40		ns	
t_{CD}	$\overline{HOLD}$ HOLD Time	100		40		ns	
t_{WC}	Write Cycle Time		10		5	ms	
t_V	Output Valid from Clock Low		200		80	ns	
t_{HO}	Output HOLD Time	0		0		ns	
t_{DIS}	Output Disable Time		250		75	ns	
t_{HZ}	$\overline{HOLD}$ to Output High Z		100		50	ns	
t_{CS}	$\overline{CS}$ High Time	250		100		ns	
t_{CSS}	$\overline{CS}$ Setup Time	250		100		ns	
t_{CSH}	$\overline{CS}$ HOLD Time	250		100		ns	

NOTE:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

FUNCTIONAL DESCRIPTION

The CAT25C03/05/09/17/33 supports the SPI bus data transmission protocol. The synchronous Serial Peripheral Interface (SPI) helps the CAT25C03/05/09/17/33 to interface directly with many of today's popular microcontrollers. The CAT25C03/05/09/17/33 contains an 8-bit instruction register. (The instruction set and the operation codes are detailed in the instruction set table)

After the device is selected with $\overline{CS}$ going low, the first byte will be received. The part is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The first byte contains one of the six op-codes that define the operation to be performed.

PIN DESCRIPTION

SI: Serial Input
SI is the serial data input pin. This pin is used to input all opcodes, byte addresses, and data to be written to the 25C03/05/09/17/33. Input data is latched on the rising edge of the serial clock.

SO: Serial Output
SO is the serial data output pin. This pin is used to transfer data out of the 25C03/05/09/17/33. During a read cycle, data is shifted out on the falling edge of the serial clock.

SCK: Serial Clock
SCK is the serial clock pin. This pin is used to synchronize the communication between the microcontroller and the 25C03/05/09/17/33. Opcodes, byte addresses, or data present on the SI pin are latched on the rising edge of the SCK. Data on the SO pin is updated on the falling edge of the SCK.

$\overline{CS}$: Chip Select

$\overline{CS}$ is the Chip select pin. $\overline{CS}$ low enables the CAT25C03/05/09/17/33 and $\overline{CS}$ high disables the CAT25C03/05/09/17/33. $\overline{CS}$ high takes the SO output pin to high impedance and forces the devices into a Standby Mode (unless an internal write operation is underway) The CAT25C03/05/09/17/33 draws ZERO current in the Standby mode. A high to low transition on $\overline{CS}$ is required prior to any sequence being initiated. A low to high transition on $\overline{CS}$ after a valid write sequence is what initiates an internal write cycle.

$\overline{WP}$: Write Protect
$\overline{WP}$ is the Write Protect pin. The Write Protect pin will allow normal read/write operations when held high. When $\overline{WP}$ is tied low, all write operations to the device are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the status register.

$\overline{HOLD}$: Hold

$\overline{HOLD}$ is the HOLD pin. The $\overline{HOLD}$ pin is used to pause transmission to the CAT25C03/05/09/17/33 while in the middle of a serial sequence without having to re-transmit entire sequence at a later time. To pause, $\overline{HOLD}$ must be

INSTRUCTION SET

Instruction	Opcode	Operation
WREN	0000 0110	Enable Write Operations
WRDI	0000 0100	Disable Write Operations
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 X011(1)	Read Data from Memory
WRITE	0000 X010(1)	Write Data to Memory

Power-Up Timing(2)(3)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Note:
(1) X=O for 25C03, 25C09, 25C17 and 25C33. X=A8 for 25C05
(2) This parameter is tested initially and after a design or process change that affects the parameter.
(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

brought low while SCK is low. The SO pin is in a high impedance state during the time the part is paused, and transitions on the SI pins will be ignored. To resume communication, $\overline{HOLD}$ is brought high, while SCK is low. ($\overline{HOLD}$ should be held high any time this function is not being used.) $\overline{HOLD}$ may be tied high directly to V_{CC} or tied to V_{CC} through a resistor. Figure 9 illustrates hold timing sequence.

STATUS REGISTER

The status register defines the protection status of the device. The register features three protection bits which allow the user to protect the desirable part of the memory array. There are seven different variations for the protection mechanism. The protection can vary from one page to as much as half of the entire array. These areas and associated address ranges are protected by configuring the protection bits of the status register through WRSR instruction. Once the three protection bits are set, the associated memory can be read but not written until the protection bits are reset.

STATUS REGISTER

7	6	5	4	3	2	1	0
0	0	0	0	0	IDL2	IDL1	IDL0

MEMORY PROTECTION

IDL2	IDL1	IDL0	
0	0	0	Non-Protection
0	0	1	Q1 Protected
0	1	0	Q2 Protected
0	1	1	Q3 Protected
1	0	0	Q4 Protected
1	0	1	H1 Protected
1	1	0	P0 Protected
1	1	1	Pn Protected

	25C03	25C05	25C09	25C17	25C33
Q1	00-3F	000-07F	000-0FF	000-1FF	000-3FF
Q2	40-7F	080-0FF	100-1FF	200-3FF	400-7FF
Q3	80-BF	100-17F	200-2FF	400-5FF	800-BFF
Q4	C0-FF	180-1FF	300-3FF	600-7FF	C00-FFF
H1	00-7F	000-0FF	000-1FF	000-3FF	000-7FF
P0	00-0F	000-00F	000-01F	000-01F	000-01F
Pn	F0-FF	1F0-1FF	3E0-3FF	7E0-7FF	FE0-FFF

DEVICE OPERATION

Write Enable and Disable

The CAT25C03/05/09/17/33 contains a write enable latch. This latch must be set before any write operation. The device powers up in a write disable state when V_{CC} is applied. WREN instruction will enable writes (set the latch) to the device. WRDI instruction will disable writes (reset the latch) to the device. Disabling writes will protect the device against inadvertent writes.

READ Sequence

The part is selected by pulling $\overline{CS}$ low. The 8-bit read instruction is transmitted to the CAT25C03/05/09/17/33, followed by the 16-bit address for 25C09/17/33 (only 10-bit addresses are used for 25C09, 11-bit addresses are used for 25C17, and 12-bit addresses are used for 25C33. The rest of the bits are don't care bits) and 8-bit address for 25C03/05 (for the 25C05, bit 3 of the read data instruction contains address A8).

After the correct read instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by pulling the $\overline{CS}$ high. Read sequece is illustrated in Figure 4. Reading status register is illustrated in Figure 5. To read the status register, RDSR instruction should be sent. The contents of the status register are shifted out on the SO line. If a non-volatile write is in progress, the RDSR instruction returns a high on SO. When the non-volatile write cycle is completed, the status register data is read out.

Figure 2. WREN Instruction Timing

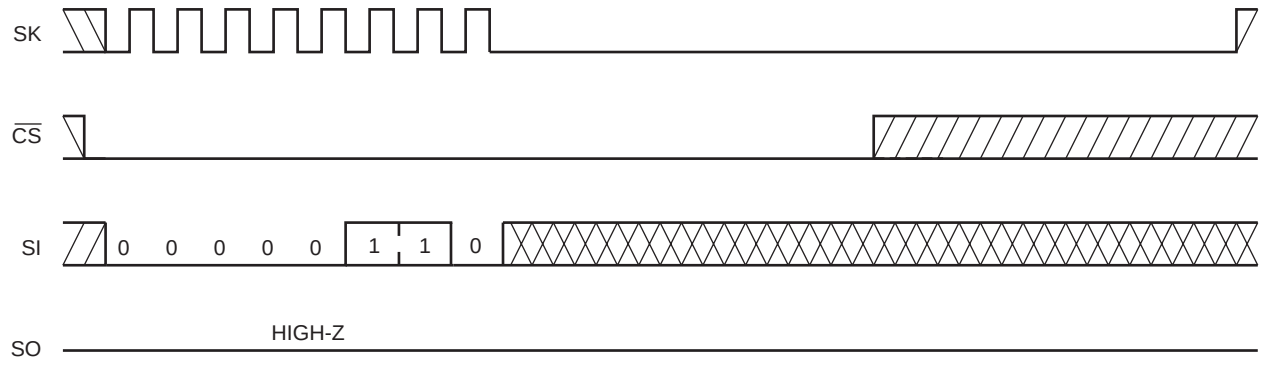
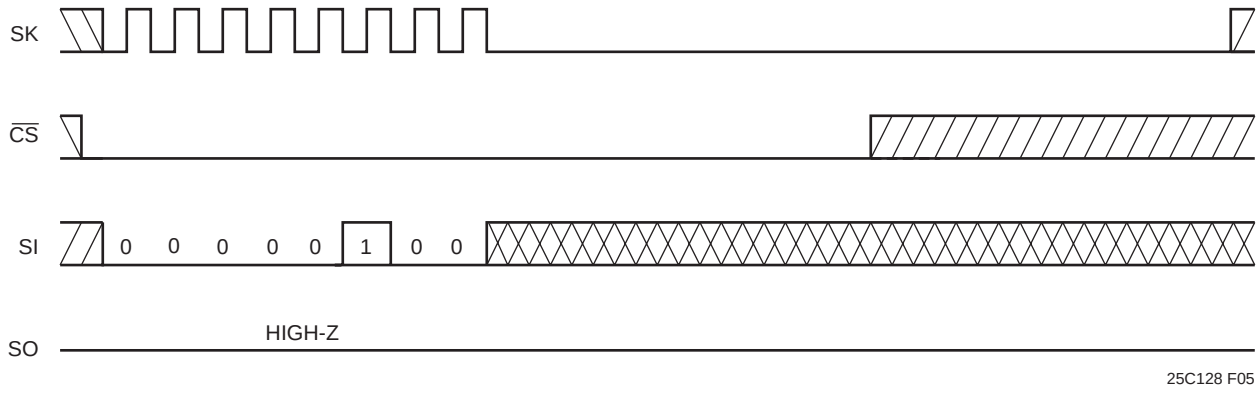


Figure 3. WRDI Instruction Timing



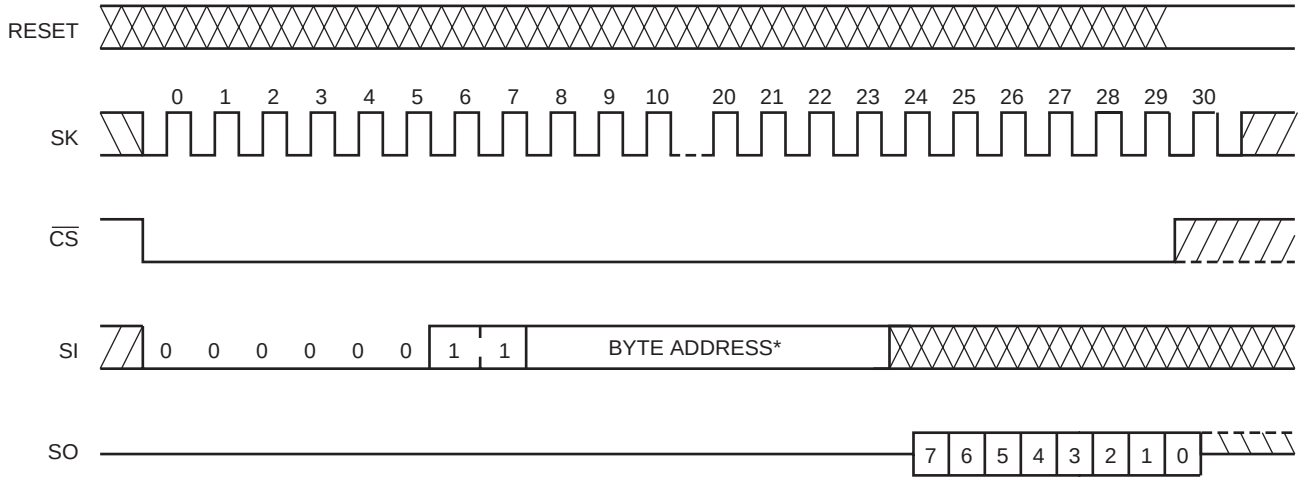
WRITE Sequence

The CAT25C03/05/09/17/33 powers up in a Write Disable state. Prior to any write instructions, the WREN instruction must be sent to CAT25C03/05/09/17/33. The device goes into Write enable state by pulling the $\overline{CS}$ low and then clocking the WREN instruction into CAT25C03/05/09/17/33. The $\overline{CS}$ must be brought high after the WREN instruction to enable writes to the device. If the write operation is initiated immediately after the WREN instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set. Also, for a successful write operation the address of the memory location(s) to be programmed must be outside the protected address field.

Byte Write

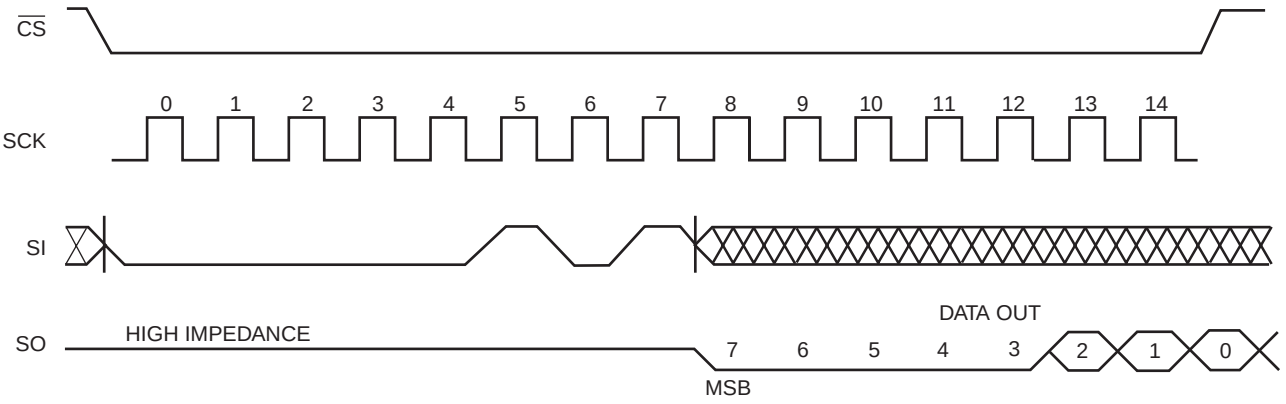
Once the device is in a Write Enable state, the user may proceed with a write sequence by setting the $\overline{CS}$ low, issuing a write instruction via the SI line, followed by the 16-bit address for 25C09/17/33. (only 10-bit addresses are used for 25C09, 11-bit addresses are used for 25C17, and 12-bit addresses are used for 25C33. The rest of the bits are don't care bits) and 8-bit address for 25C03/05 (for the 25C05, bit 3 of the read data instruction contains address A8). Programming will start after the $\overline{CS}$ is brought high. The low to high transition of the $\overline{CS}$ pin must occur during the SCK low time, immediately after clocking the least significant bit of the data. Figure 6 illustrates byte write sequence.

Figure 4. Read Instruction Timing



*Please check the instruction set table for address

Figure 5. RDSR Timing



25C03 F09

Page Write

The CAT25C03/05/09/17/33 features page write capability. After the initial byte, the host may continue to write up to 16 bytes of data to the CAT25C03/05 and 32 bytes of data for 25C09/17/33. After each byte of data received, lower order address bits are internally incremented by one; the high order bits of address willremain constant.The only restriction is that the X (X=16 for 25C03/05 and X=32 for 25C09/17/33) bytes must reside on the same page. If the address counter reaches the end of the page and clock continues, the counter will "roll over" to the first address of the page and overwrite any data that may have been written. The CAT25C03/05/09/17/33 is automatically returned to the write disable state at the completion of the write cycle. Figure 8 illustrates the page write sequence.

To write to the status register, the WRSR instruction should be sent. Figure 7 illustrates the sequence of writing to status register.

Figure 6. Write Instruction Timing

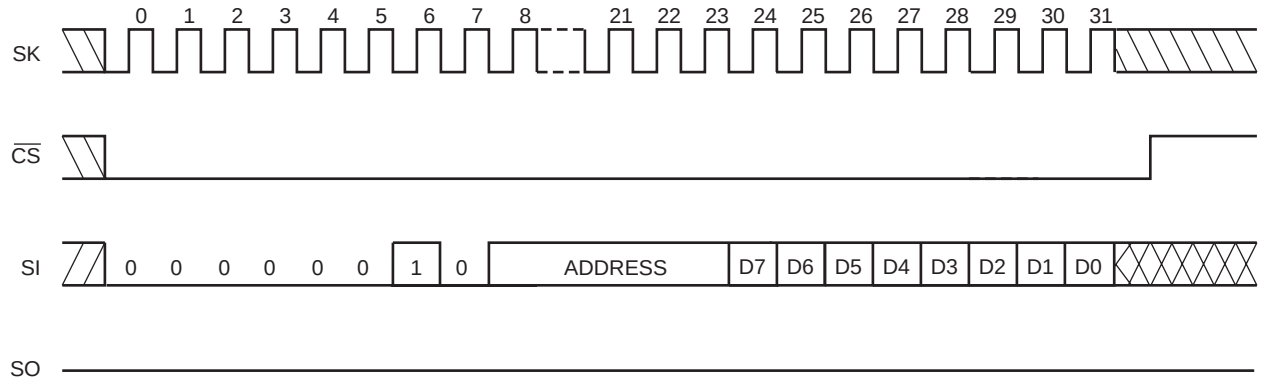
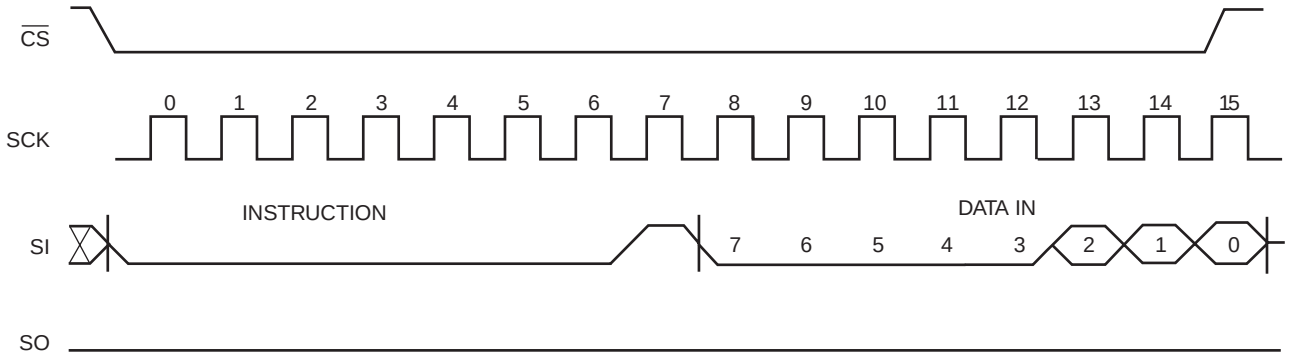


Figure 7. WRSR Timing



DESIGN CONSIDERATIONS

The CAT25C03/05/09/17/33 powers up in a write disable state and in a low power standby mode. A WREN instruction must be issued to perform any writes to the device after power up. Also,on power up $\overline{CS}$ should be brought low to enter a ready state and receive an instruction. After a successful byte/page write or status register write the CAT25C03/05/09/17/33 goes into a write disable mode. $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle. Access to the array during an internal write cycle is ignored and programming is continued. On power up, SO is in a high impedance. If an invalid op code is received, no data will be shifted into the CAT25C03/05/09/17/33, and the serial output pin (SO) will remain in a high impedance state until the falling edge of $\overline{CS}$ is detected again.

Figure 8. Page Write Instruction Timing

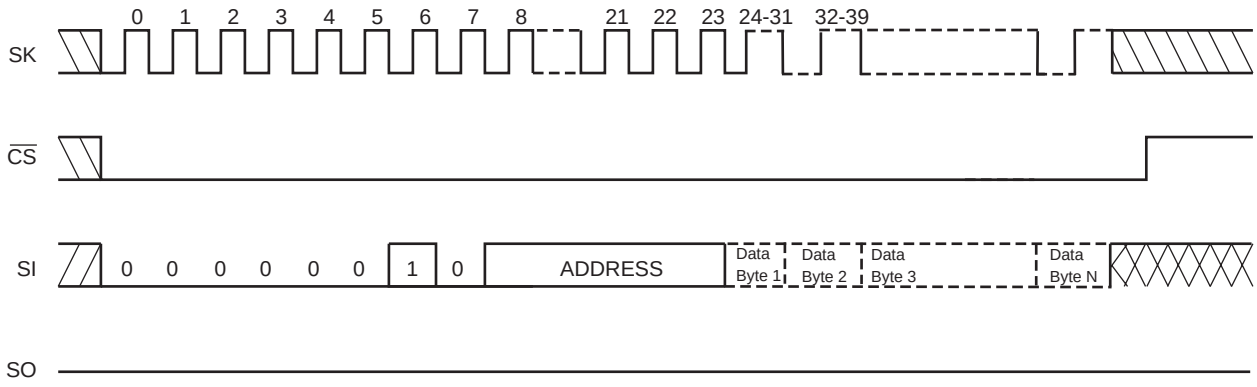
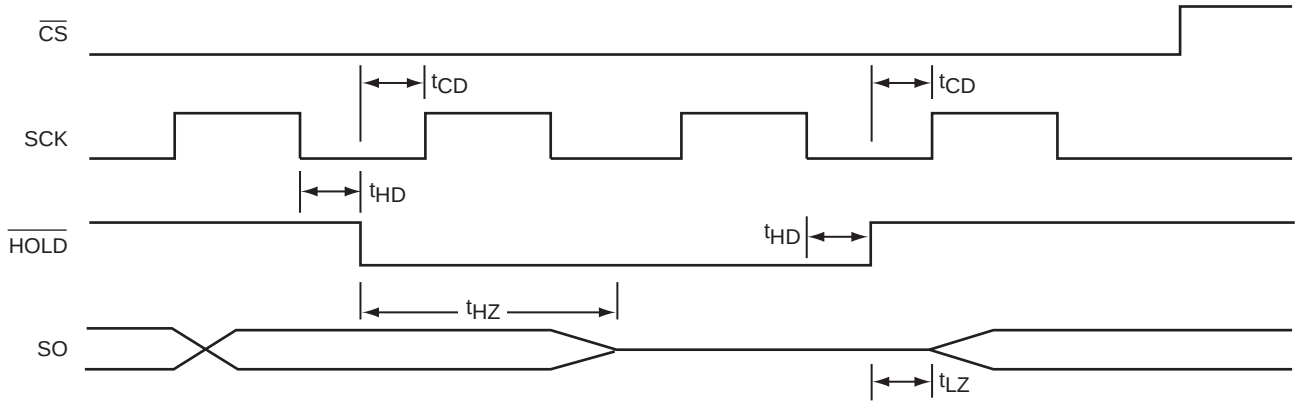
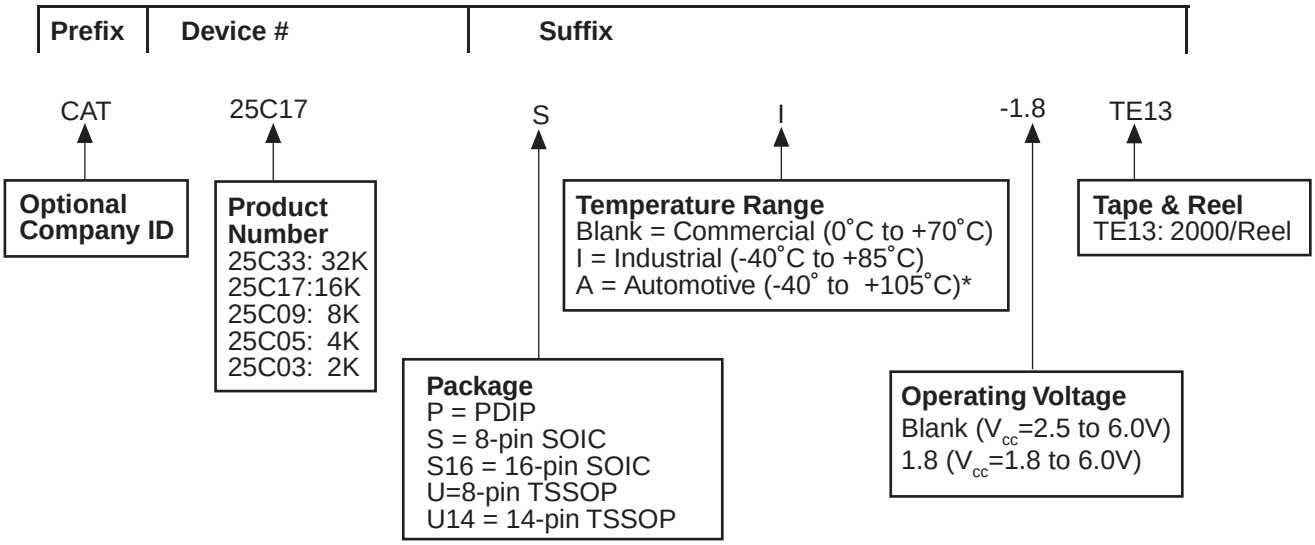


Figure 9. HOLD Timing



25C128 F10

ORDERING INFORMATION



* -40˚C to +125˚C is available upon request

Notes:
(1) The device used in the above example is a 25C17SI-1.8TE13 (SOIC, Industrial Temperature, 1.8 Volt to 6 Volt Operating Voltage, Tape & Reel)