National Semiconductor

August 2000

DS3884A
BTL Handshake Transceiver

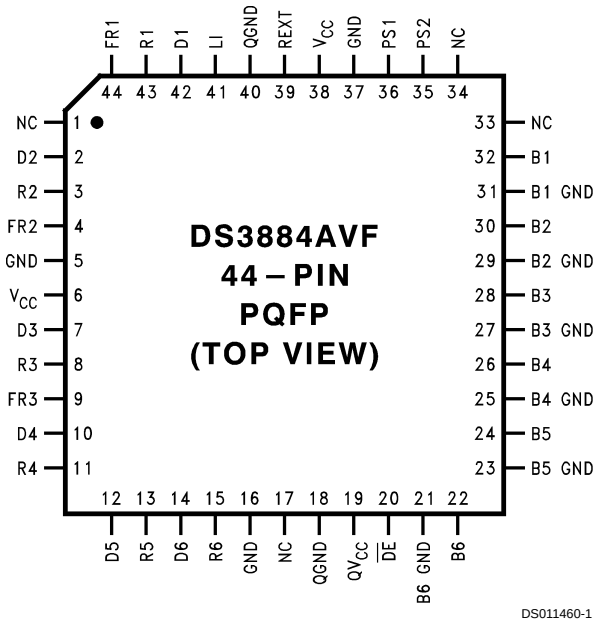
General Description

The DS3884A is one in a series of transceivers designed specifically for the implementation of high performance Futurebus+ and proprietary bus interfaces. The DS3884A is a BTL 6-bit Handshake Transceiver designed to conform to IEEE 1194.1 (Backplane Transceiver Logic — BTL) as specified in the IEEE 896.2 Futurebus+ specification.

Features

- Fast propagation delay (3 ns typ)
- 6-bit BTL transceiver
- Selective receiver glitch filtering (FR1–FR3)
- Meets 1194.1 Standard on Backplane Transceiver Logic (BTL)
- Supports live insertion
- Glitch free power-up/down protection
- Typically less than 5 pF bus-port capacitance
- Low Bus-port voltage swing (typically 1V) at 80 mA
- TTL compatible driver and control inputs
- Separate TTL I/O
- Open collector bus-port outputs allow Wired-OR connection
- Controlled rise and fall time to reduce noise coupling to adjacent lines
- Built in Bandgap reference with separate QV_{CC} and QGND pins for precise receiver thresholds
- Exceeds 2 kV ESD testing (Human Body Model)
- Individual Bus-port ground pins
- Product offered in PQFP package styles

Connection Diagram



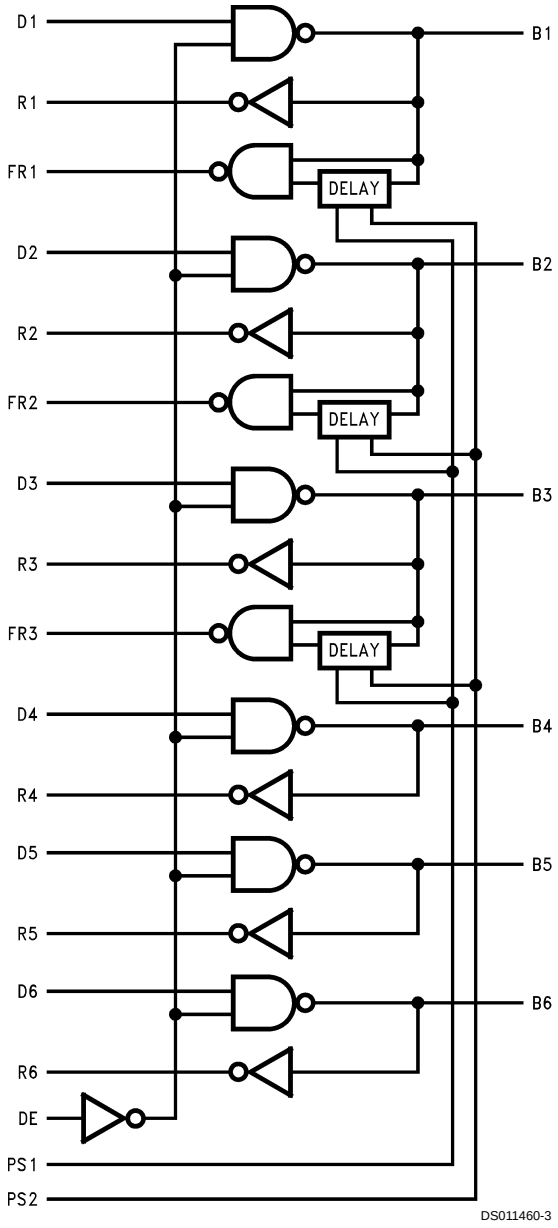
DS011460-1

Order Number DS3884AVF
See NS Package VF44B

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Logic Diagram



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6.5V
Control Input Voltage	6.5V
Driver Input and Receiver Output	5.5V
Receiver Input Current	±15 mA
Bus Termination Voltage	2.4V
Power Dissipation at 25˚C	
PQFP	1.3W
Derate PQFP Package	11.1 mW/˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature	
(Soldering, 4 seconds):	260˚C

Recommended Operating Conditions

Supply Voltage, V_{CC}	4.5V–5.5V
Bus Termination Voltage (V_T)	2.06V–2.14V
Operating Free Air Temperature	0˚C to 70˚C

DC Electrical Characteristics (Notes 2, 3)

T_A = 0 to +70˚C, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AND CONTROL INPUT: (Dn, DE*, PS1 and PS2)						
V_{IH}	Minimum Input High Voltage		2.0			V
V_{IL}	Maximum Input Low Voltage				0.8	V
I_I	Input Leakage Current	$V_{IN} = V_{CC} = 5.5V$			100	µA
I_{IH}	Input High Current	V_{IN} = 2.4V			40	µA
I_{IL}	Input Low Current	V_{IN} = 0.5V			−100	µA
V_{CL}	Input Diode Clamp Voltage	I_{CLAMP} = −12 mA			−1.2	V
DRIVER OUTPUT/RECEIVER INPUT: (Bn)						
V_{OLB}	Output Low Bus Voltage (Note 5)	Dn = 2.4V, DE* = 0V, I_{OL} = 80 mA	0.75	1.0	1.1	V
I_{OLBZ}	Output Low Bus Current	Dn = 0.5V, DE* = 2.4V, Bn = 0.75V			100	µA
I_{OHBZ}	Output High Bus Current	Dn = 0.5V, DE* = 2.4V, Bn = 2.1V			100	µA
I_{OLB}	Output Low Bus Current	Dn = 0.5V, DE* = 0V, Bn = 0.75V			220	µA
I_{OHB}	Output High Bus Current	Dn = 0.5V, DE* = 0V, Bn = 2.1V			350	µA
V_{TH}	Receiver Input Threshold	DE* = 2.4V	1.47	1.55	1.62	V
V_{CLP}	Positive Clamp Voltage	V_{CC} = Max or 0V, I_{Bn} = 1 mA	2.4	3.4	4.5	V
		V_{CC} = Max or 0V, I_{Bn} = 10 mA	2.9	3.9	5.0	V
V_{CLN}	Negative Clamp Voltage	I_{CLAMP} = −12 mA			−1.2	V
RECEIVER OUTPUT: (FRn and Rn)						
V_{OH}	Voltage Output High	Bn = 1.1V, DE* = 2.4V, I_{OH} = −2 mA	2.4	3.2		V
V_{OL}	Voltage Output Low	Bn = 2.1V, DE* = 2.4V, I_{OL} = 24 mA		0.35	0.5	V
		Bn = 2.1V, DE* = 2.4V, I_{OL} = 8 mA		0.35	0.4	V
I_{OS}	Output Short Circuit Current	Bn = 1.1V, DE* = 2.4V (Note 4)	−40	−70	−100	mA
SUPPLY CURRENT						
I_{CC}	Supply Current: Includes V_{CC}, QV_{CC} and LI	DE* = 0.5V, All Dn = 2.4V		50	70	mA
		DE* = 2.4V, All Bn = 2.1V		50	70	mA
I_{LI}	Live Insertion Current	DE* = 2.4V, All Dn = 0.5V		1	3	mA
		DE* = 0.5V, All Dn = 2.4V		2	5	mA

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All input and/or output pins shall not exceed V_{CC} plus 0.5V and shall not exceed the absolute maximum rating at anytime, including power-up and power-down. This prevents the ESD structure from being damaged due to excessive currents flowing from the input and/or output pins to QV_{CC} and V_{CC}. There is a diode between each input and/or output to V_{CC} which is forward biased when incorrect sequencing is applied. Alternatively, a current limiting resistor can be used when pulling-up the inputs to prevent damage. The current into any input/output pin shall be no greater than 50 mA. Exception, LI and Bn pins do not have power sequencing requirements with respect to V_{CC} and QV_{CC}. Furthermore, the difference between V_{CC} and QV_{CC} should never be greater than 0.5V at any time including power-up.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified. All typical values are specified under these conditions.: V_{CC} = 5V and T_A = 25˚C unless otherwise stated.

Note 4: Only one output should be shorted at a time, and duration of the short should not exceed one second.

Note 5: Referenced to appropriate signal ground. Do not exceed maximum power dissipation of package.

AC Electrical Characteristics (Note 6)

T_A = 0˚C to +70˚C, V_{CC} = 5V ±10%

Symbol	Parameter		Conditions	Min	Typ	Max	Units
DRIVER							
t_{PHL}	Dn to Bn	Prop. Delay	DE* = 0V	1	3	5	ns
t_{PLH}			(*Figure 1*, *Figure 2*)	1	3	5	ns
t_{PHL}	DE* to Bn	Enable Time	Dn = 3V	2	4	6	ns
t_{PLH}		Disable Time	(*Figure 1*, *Figure 3*)	2	4	6	ns
t_r	Transition Time—Rise/Fall		(*Figure 1*, *Figure 2*)	1	2	3.5	ns
t_f	20% to 80%			1	2	3.5	ns
SR	Skew Rate is Calculated from 1.3V to 1.8V		(Note 11)			0.5	V/ns
t_{skew}	Skew between Drivers in the Same Package		(Note 7)		1	3	ns
RECEIVER							
t_{PHL}	Bn to Rn	Prop. Delay	DE* = 3V	2	4	5	ns
t_{PLH}			(*Figure 4*, *Figure 5*)	2	4	6	ns
t_{skew}	Skew between Receivers in Same Package		(Note 7)		1	3	ns
FILTERED RECEIVER							
t_{PHL}	Bn to FRn	Prop. Delay	PS1 = 0V PS2 = 0V DE* = 3V (*Figure 4*, *Figure 5*), R_{EXT} = 13 kΩ	6	12	16	ns
			PS1 = 0V PS2 = 3V DE* = 3V (*Figure 4*, *Figure 5*), R_{EXT} = 13 kΩ	11	16	21	ns
			PS1 = 3V PS2 = 0V DE* = 3V (*Figure 4*, *Figure 5*), R_{EXT} = 13 kΩ	15	21	27	ns
			PS1 = 3V PS2 = 3V DE* = 3V (*Figure 4*, *Figure 5*), R_{EXT} = 13 kΩ	25	33	45	ns
t_{PLH}	Bn to FRn	Prop. Delay	DE* = 3V (*Figure 4*, *Figure 5*) (Note 8) R_{EXT} = 13 kΩ	2	5	7	ns
t_{GR}	Glitch Rejection		PS1 = 0V PS2 = 0V DE* = 3V (*Figure 4*, *Figure 6*), R_{EXT} = 13 kΩ	5	9	16	ns
			PS1 = 0V PS2 = 3V DE* = 3V (*Figure 4*, *Figure 6*), R_{EXT} = 13 kΩ	10	13	18	ns
			PS1 = 3V PS2 = 0V DE* = 3V (*Figure 4*, *Figure 6*), R_{EXT} = 13 kΩ	14	18	24	ns
			PS1 = 3V PS2 = 3V DE* = 3V (*Figure 4*, *Figure 6*), R_{EXT} = 13 kΩ	24	31	42	ns
FILTERED RECEIVER TIMING REQUIREMENTS							
t_s	PSn to Bn	Set-Up Time	(*Figure 7*), R_{EXT} = 13 kΩ	250			ns
PARAMETERS NOT TESTED							
Coutput	Capacitance at Bn		(Note 9)		5		pF
t_{NR}	Noise Rejection		(Note 10)		1		ns

Note 6: Input waveforms shall have a rise/fall time of 3 ns.

Note 7: t_{skew} is an absolute value defined as differences seen in propagation delays between drivers in the same package with identical load conditions.

Note 8: Filtered receiver t_{PLH} is independent of filter setting.

Note 9: The parameter is tested using TDR techniques described in P1194.0 BTL Backplane Design Guide.

Note 10: This parameter is tested during device characterization. The measurements revealed that the part will reject 1 ns pulse width.

Note 11: Futurebus+ transceivers are required to limit bus signal rise and fall times to no faster than 0.5V/ns, measured between 1.3V and 1.8V (approximately 20% to 80% of nominal voltage swing). The rise and fall times are measured with a transceiver loading equivalent to 12.5Ω tied to +2.1V DC.

Pin Descriptions

Pin Name	Number of Pins	Input/ Output	Description
B1–B6	6	I/O	BTL receiver input and driver output
B1GND–B6GND	6	NA	Driver output ground reduces bounce due to high current switching of driver outputs (Note 12)
DE*	1	I	Driver Enable Low
D1–D6	6	I	TTL Driver Input
FR1–FR3	3	O	TTL Filtered Receiver Output
GND	3	NA	Ground reference for switching circuits. (Note 12)
LI	1	NA	Power supply for live insertion. Boards that require live insertion should connect LI to the live insertion pin on the connector. (Note 13)
NC	4	NA	No Connect
PS1, PS2	2	I	Pulse Width Selection pin determines glitch filter setting (Note 14)
R1–R6	6	O	TTL Receiver Output
REXT	1	NA	External Resistor pin. External resistor is used for internal biasing of filter circuitry. The 13 kΩ resistor shall be connected between REXT and GND. The resistor shall have a tolerance of 1% and a temperature coefficient of 100 ppm/°C or better.
QGND	2	NA	Ground reference for receiver input bandgap reference and non-switching circuits (Note 12)
QV_{CC}	1	NA	V_{CC} supply for bandgap reference and non-switching circuits (Note 13)
V_{CC}	2	NA	V_{CC} supply for switching circuits (Note 13)

Note 12: the multiplicity of grounds reduces the effective inductance of bonding wires and leads, which then reduces the noise caused by transients on the ground path. The various ground pins can be tied together provided that the external ground has low inductance (i.e., ground plane with power pins and many signal pins connected to the backplane ground). If the external ground floats considerably during transients, precautionary steps should be taken to prevent QGND from moving with reference to the backplane ground. The receiver threshold should have the same ground reference as the signal coming from the backplane. A voltage offset between their grounds will degrade the noise margin.

Note 13: The same considerations for ground are used for V_{CC} in reducing lead inductance (see Note 12). QV_{CC} and V_{CC} should be tied together externally. If live insertion is not supported, the LI pin can be tied together with QV_{CC} and V_{CC}.

Note 14: See AC characteristics for filter setting.

Pin Descriptions (Continued)

DE*	Dn	FRn	Rn	Bn
H	X	H	H	L
H	X	L	L	H
L	H	H	H	L
L	L	L	L	H

X: High or low logic state
L: Low state
H: High state
L-H: Low to high transition

Glitch Filter Table

PS1	PS2	Filter Setting
L	L	5 ns
L	H	10 ns
H	L	14 ns
H	H	24 ns

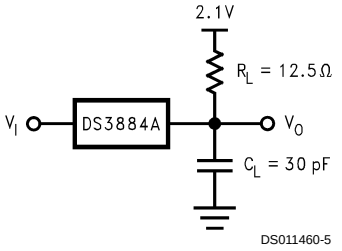


FIGURE 1. Driver Propagation Delay Set-Up

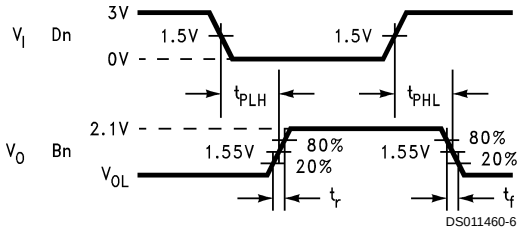


FIGURE 2. Driver: Dn to Bn

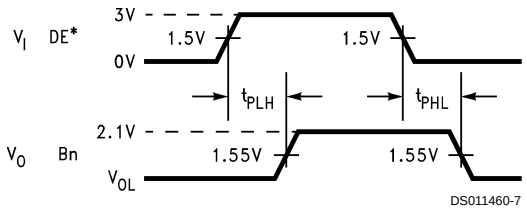
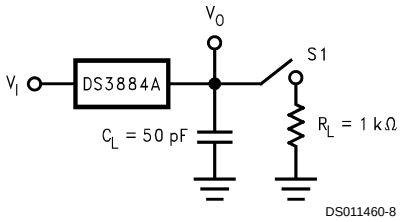


FIGURE 3. Driver: DE* to Bn



	Switch Position	
	t_{PLH}	t_{PHL}
S1	open	close

FIGURE 4. Receiver Propagation Delay Set-Up

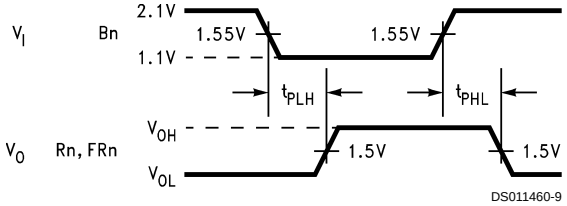


FIGURE 5. Receiver: Bn to FRn, Bn to Rn

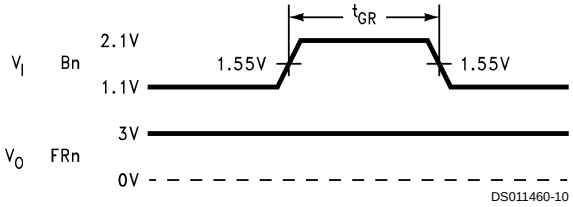


FIGURE 6. Receiver: t_{GR}, FRn(min) = 2V

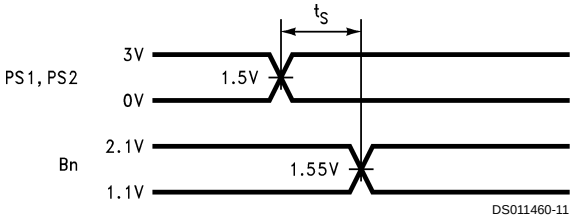


FIGURE 7. Receiver: PSn to Bn

Application Information

The DS3884A is pin to pin and functionally compatible with the DS3884. The DS3884A is a speed and power enhanced version of the DS3884. There are two minor differences between the DS3884 and DS3884A.

The external resistor used in the DS3884A is different from that used in the DS3884. REXT for the DS3884 is 6.2k while REXT for the DS3884A is 13k. The available filter settings for the DS3884A are 5 ns, 10 ns, 14 ns, 24 ns, while the settings for the DS3884 are 5 ns, 7.5 ns, 15 ns, and 25 ns.

Utilization of the DS3884A simplifies the implementation of all handshake signals which require Wired-OR glitch filtering. Three of the six bits have an additional parallel Wired-OR filtered receive output giving a total of nine receiver outputs.

Application Information (Continued)

In Wired-OR applications, the glitch generated as drivers are released from the bus, is dependent upon the backplane and parasitic wiring components causing the characteristics of the glitch to vary in pulse width and amplitude. To accommodate this variation the DS3884A features two pins defined as PS1 and PS2 which allow selection of a 5 ns, 10 ns, 14 ns and 24 ns filter setting to optimize glitch filtering for a given situation. The REXT pin is issued in conjunction with the filtering circuitry and requires a 13 kΩ resistor to ground. For additional information on Wired-OR glitch, reference Application Note AN-774.

The DS3884A driver output configuration is an NPN open collector which allows Wired-OR connection on the bus. Each driver output incorporates a Schottky diode in series with its collector to isolate the transistor output capacitance from the bus thus reducing the bus loading in the inactive state. The combined output capacitance of the driver and receiver input is typically less than 5 pF. The driver also has high sink current capability to comply with the bus loading requirements defined within IEEE 1194.1 BTL specification.

Backplane Transceiver Logic (BTL) is a signaling standard that was invented and first introduced by National Semiconductor, then developed by the IEEE to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. The BTL standard eliminates settling time delays that severely limit TTL bus performance, and thus provide significantly higher bus transfer rates. The backplane bus is intended to be operated with termination resistors (selected to match the bus impedance) connected to 2.1V at both ends. The low voltage is typically 1V.

Separate ground pins are provided for each BTL output to minimize induced ground noise during simultaneous switching.

The device's unique driver circuitry meets a maximum slew rate of 0.5V/ns which allows controlled rise and fall times to reduce noise coupling to adjacent lines.

The transceiver's high impedance control and driver inputs are fully TTL compatible.

The receiver is a high speed comparator that utilizes a bandgap reference for precision threshold control allowing maximum noise immunity to the BTL 1V signaling level.

Separate QV_{CC} and QGND pins are provided to minimize the effects of high current switching noise. Output pins FR1–FR3 are the filtered outputs and R1–R6 are the unfiltered outputs. All receiver outputs are fully TTL compatible.

The DS3884A supports live insertion as defined for Futurebus+ through the LI (Live Insertion) pin. To implement live insertion the LI pin should be connected to the live insertion power connector. If this function is not supported the LI pin must be tied to the V_{CC} pin. The DS3884A also provides power up/down glitch free protection during power sequencing.

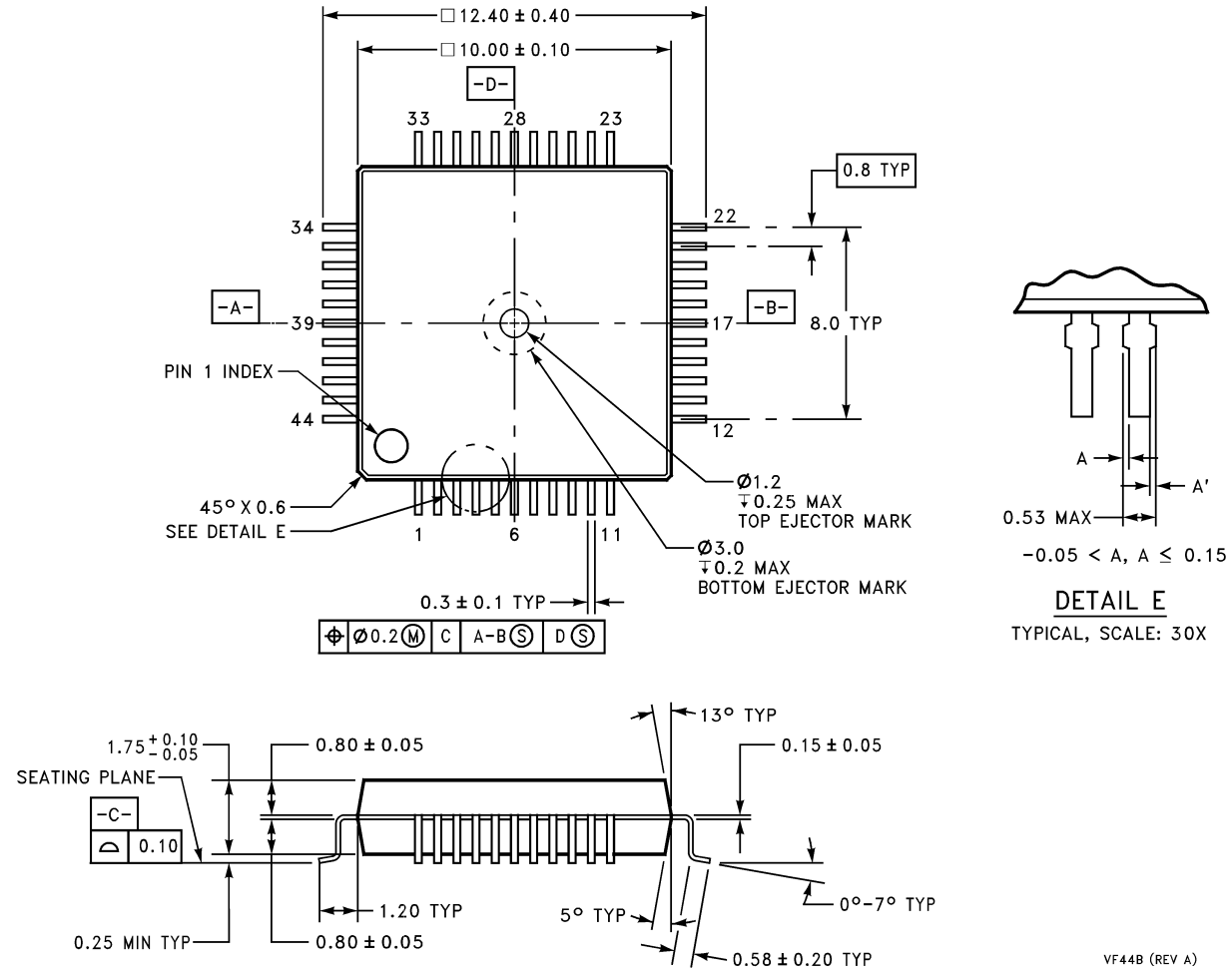
The DS3884A has two types of power connections in addition to the LI pin. They are the Logic V_{CC} (V_{CC}) and the Quiet V_{CC} (QV_{CC}). There are two V_{CC} pins on the DS3884A that provide the supply voltage for the logic and control circuitry. Multiple connections are provided to reduce the effects of package inductance and thereby minimize switching noise. As these pins are common to the V_{CC} bus internal to the device, a voltage difference should never exist between these pins and the voltage difference between V_{CC} and QV_{CC} should never exceed ±0.5V because of ESD circuitry. Additionally, the ESD circuitry between the V_{CC} pins and all other pins except for BTL I/O's and LI pins requires that any voltage on these pins should not exceed the voltage on V_{CC} + 0.5V.

There are three different types of ground pins on the DS3884A. They are the logic ground (GND), BTL grounds (B1GND–B6GND) and the Bandgap reference ground (QGND). All of these ground reference pins are isolated within the chip to minimize the effects of high current switching transients. For optimum performance the QGND should be returned to the connector through a quiet channel that does not carry transient switching current. The GND and B1GND–B6GND should be connected to the nearest backplane ground pin with the shortest possible path.

Since many different grounding schemes could be implemented and ESD circuitry exist on the DS3884A, it is important to note that any voltage difference between ground pins, QGND, GND or B1GND–B6GND should not exceed ±5V including power up/down sequencing.

Additional transceivers included in the Futurebus+ / BTL family are; the DS3883A BTL 9-bit Transceiver, and the DS3886A BTL 9-bit Latching Data Transceiver featuring edge triggered latches in the driver which may be bypassed during a fall-through mode and a transparent latch in the receiver.

Physical Dimensions inches (millimeters) unless otherwise noted



44-Pin PQFP
Order Number DS3884AVF
NS Package VF44B

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