Standard Products

ACT8510 64-Channel Analog Multiplexer Module Radiation Tolerant & ESD Protected

www.aeroflex.com/mux

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FEATURES

- 64-Channels provided by six 16-channel multiplexers
- Radiation performance
  - Total dose: 150 krads(Si), Dose rate = 50 - 300 rads(Si)/s
  - SEU: Immune up to 90 MeV-cm^2/mg
  - SEL: Immune by process design
- Full military temperature range
- Low power consumption < 90mW
- Two address busses (A0-3 & B0-3) and four enable lines afford flexible organization.
- All channel inputs are protected by ±20V nominal Transorbs.
- Fast access time < 500ns typical
- Break-Before-Make switching
- High analog input impedance (power on or off)
- Designed for aerospace and high reliability space applications
- Packaging – Hermetic ceramic
  - 96 leads, 1.32"Sq x 0.20"Ht quad flat pack
  - Typical Weight 15 grams
- DSCC SMD 5962-09202 pending

Note: Aeroflex Plainview does not currently have a DSCC certified Radiation Hardened Assurance Program.

GENERAL DESCRIPTION

Aeroflex's ACT8510 is a radiation tolerant, 64 channel multiplexer MCM (multi-chip module) with electrostatic discharge (ESD) protection on all channel inputs.

The ACT8510 has been specifically designed to meet exposure to radiation environments. It is available in a 96 lead High Temperature Co-Fired Ceramic (HTCC) Quad Flatpack (CQFP). It is guaranteed operational from -55°C to +125°C. Available screened in accordance with MIL-PRF-38534, the ACT8510 is ideal for demanding military and space applications.

ORGANIZATION AND APPLICATION

The ACT8510 consists of six 16 channel multiplexers arranged as shown in the Block Diagram. The ACT8510 design is inherently radiation tolerant.

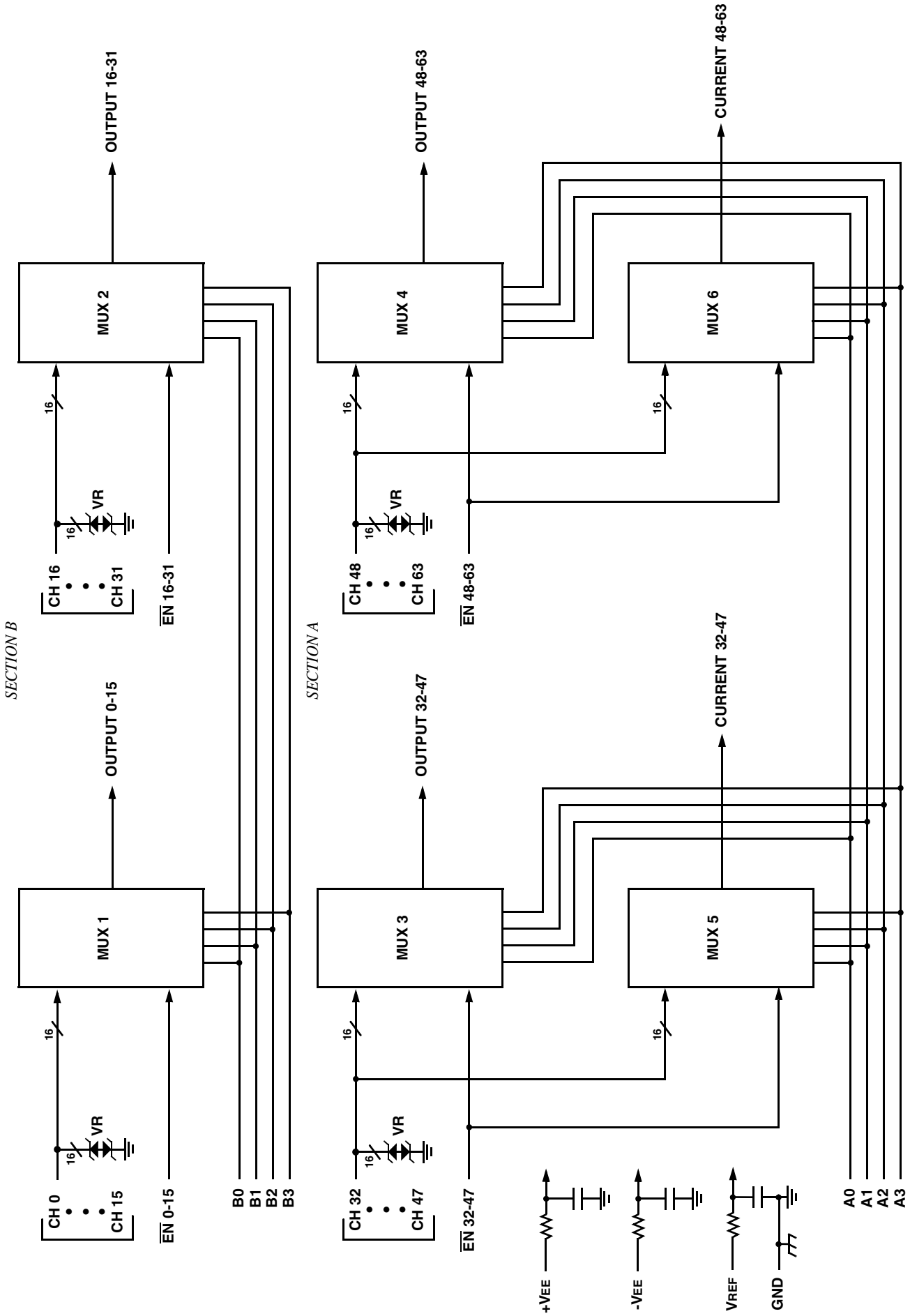
A SECTION

Thirty-two (32) channels addressable by bus A_0~A_3, in two 16 channel blocks, each block enabled separately. Each block connects the addressed channel to two outputs, "Output" and "Current". This technique enables selecting and reading a remote resistive sensor without the multiplexer resistance being part of the measurement. For grounded sensors, this is done by passing current to the sensor by means of the "Current" pin and reading the resultant voltage (proportional to the sensor resistance) at the "Output" pin.

B SECTION

Thirty-two (32) channels addressable by bus B_0~B_3, in two 16 channel blocks, each block enabled separately. Each block connects the addressed channel to one output. By paralleling the channel inputs and enables, this section can be converted to act like one of the 16 channel blocks of the A section.

ACT8510 64 – CHANNEL ANALOG MUX BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS 1/

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	°C
Storage Temperature Range	-65 to +150	°C
Supply Voltage +VEE (Pin 44) -VEE (Pin 46) VREF (Pin 48)	 +20 -20 +7.5	 V V V
Digital Input Overvoltage VEN (Pins 5, 6, 91, 92), VA (Pins 1, 3, 93, 95), VB (Pins 2, 4, 94, 96)	< VREF +0.5 > GND -0.5	V V
Analog Input Over Voltage VS	±18V	V

Notes:
1/ All measurements are made with respect to ground.

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may affect device reliability.

RECOMMENDED OPERATING CONDITIONS 1/

Symbol	Parameter	Typical	Units
+VEE	+15V Power Supply Voltage	+15.0	V
-VEE	-15V Power Supply Voltage	-15.0	V
VREF	Reference Voltage	+5.00	V
VAL	Logic Low Level	+0.8	V
VAH	Logic High Level	+4.0	V

Notes:
1/ Power Supply turn-on sequence shall be as follows: -VEE, VREF, followed by +VEE.

DC ELECTRICAL PERFORMANCE CHARACTERISTICS 1/

(Tc = -55°C to +125°C, -VEE = -15V, VREF = +5.0V, +VEE = +15V - Unless otherwise specified)

Parameter	Symbol	Conditions	Min	Max	Units
Supply Current	+IEE	VEN(0-63) = VA(0-3)A = VA(0-3)B = 0	0	3	mA
	-IEE		-3	0	mA
	+ISBY	VEN(0-63) = 4V, VA(0-3)A = VA(0-3)B = 0 7/	0	3	mA
	-ISBY		-3	0	mA
Address Input Current	IAL(0-3)A	VA = 0V	-4	4	µA
	IAH(0-3)A	VA = 5V	-4	4	µA
	IAL(0-3)B	VB = 0V	-2	2	µA
	IAH(0-3)B	VB = 5V	-2	2	µA
Enable Input Current	IENL(0-15)	VEN(0-15) = 0V	-1	1	µA
	IENH(0-15)	VEN(0-15) = 5V	-1	1	µA
	IENL(16-31)	VEN(16-31) = 0V	-1	1	µA
	IENH(16-31)	VEN(16-31) = 5V	-1	1	µA
	IENL(32-47)	VEN(32-47) = 0V	-2	2	µA
	IENH(32-47)	VEN(32-47) = 5V	-2	2	µA
	IENL(48-63)	VEN(48-63) = 0V	-2	2	µA
	IENH(48-63)	VEN(48-63) = 5V	-2	2	µA

DC ELECTRICAL PERFORMANCE CHARACTERISTICS 1/ (continued)

(Tc = -55°C to +125°C, -VEE = -15V, VREF = +5.0V, +VEE = +15V - Unless otherwise specified)

Parameter	Symbol	Conditions		Min	Max	Units
Positive Input Leakage Current CH0-CH63	+ISOFFOUTPUT	VIN = +10V, VEN = 4V, output and all unused MUX inputs under test = -10V 2/, 3/		-100	+1000	nA
	+ISOFFCURRENT			-100	+1000	nA
Negative Input Leakage Current CH0-CH63	-ISOFFOUTPUT	VIN = -10V, VEN = 4V, output and all unused MUX inputs under test = +10V 2/, 3/		-100	+1000	nA
	-ISOFFCURRENT			-100	+1000	nA
Output Leakage Current OUTPUTS (pins 25, 26, 68 & 70) CURRENTS (pins 67 & 69)	+IDOFFOUTPUT	VOUT = +10V, VEN = 4V, output and all unused MUX inputs under test = -10V 3/, 4/		-100	+100	nA
	+IDOFFCURRENT			-100	+100	nA
Output Leakage Current OUTPUTS (pins 25, 26, 68 & 70) CURRENTS (pins 67 & 69)	-IDOFFOUTPUT	VOUT = -10V, VEN = 4V, output and all unused MUX inputs under test = +10V 3/, 4/		-100	+100	nA
	-IDOFFCURRENT			-100	+100	nA
Input Clamped Voltage CH0 - CH63	+VCLMP	VEN = 4V, all unused MUX inputs under test are open. 3/	+25°C +125°C -55°C	18.0 18.0 17.5	23.0 23.5 22.5	V V V
Input Clamped Voltage CH0 - CH63	-VCLMP		+25°C +125°C -55°C	-23.0 -23.5 -22.5	-18.0 -18.0 -17.5	V V V
Switch ON Resistance OUTPUTS (pins 25, 26, 68 & 70) 6/	$R_{DS(ON)(0\text{-}63)_A}$	VIN = +15V, VEN = 0.8V, IOUT = -1mA 2/, 3/, 5/		200	1000	Ω
	$R_{DS(ON)(0\text{-}63)_B}$	VIN = +5V, VEN = 0.8V, IOUT = -1mA 2/, 3/, 5/		200	1500	Ω
	$R_{DS(ON)(0\text{-}63)_C}$	VIN = -5V, VEN = 0.8V, IOUT = +1mA 2/, 3/, 5/		200	2500	Ω
Switch ON Resistance CURRENTS (pins 67 & 69) 6/	$R_{DS(ON)(32\text{-}63)_A}$	VIN = +15V, VEN = 0.8V, IOUT = -1mA 2/, 3/, 5/		200	1000	Ω
	$R_{DS(ON)(32\text{-}63)_B}$	VIN = +5V, VEN = 0.8V, IOUT = -1mA 2/, 3/, 5/		200	1500	Ω
	$R_{DS(ON)(32\text{-}63)_C}$	VIN = -5V, VEN = 0.8V, IOUT = +1mA 2/, 3/, 5/		200	2500	Ω

Notes:

1/ Measure inputs sequentially. Ground all unused inputs of the device under test. VA is the applied input voltage to the address lines A(0-3). VB is the applied input voltage to the address lines B(0-3).

2/ VIN is the applied input voltage to the input channels CH0-CH63.

3/ VEN is the applied input voltage to the enable lines En(0-15), En(16-31), En(32-47) and En(48-63).

4/ VOUT is the applied input voltage to the output lines OUTPUT(0-15), OUTPUT(16-31), OUTPUT(32-47), OUTPUT(48-63), CURRENT(32-47) and CURRENT(48-63).

5/ Negative current is the current flowing out of each of the MUX pins. Positive current is the current flowing into each MUX pin.

6/ The ACT8510 cannot be operated with analog inputs from -15 to -5 volts.

7/ Not tested, guaranteed to the specified limits.

SWITCHING CHARACTERISTICS

(Tc = -55°C to +125°C, -VEE = -15V, VREF = +5.0V, +VEE = +15V -- Unless otherwise specified)

Parameter	Symbol	Conditions	Min	Max	Units
Switching Test MUX	t_AHL	RL = 10KΩ, CL = 50pF	10	1000	ns
	t_ALH		10	1000	ns
	$t_{ON}EN$	RL = 1KΩ, CL = 50pF	10	1000	ns
	$t_{OFF}EN$		10	1000	ns

TRUTH TABLE (CH0 – CH15)

B3	B2	B1	B0	EN(0-15)	"ON" CHANNEL 1/
X	X	X	X	H	NONE
L	L	L	L	L	CH0
L	L	L	H	L	CH1
L	L	H	L	L	CH2
L	L	H	H	L	CH3
L	H	L	L	L	CH4
L	H	L	H	L	CH5
L	H	H	L	L	CH6
L	H	H	H	L	CH7
H	L	L	L	L	CH8
H	L	L	H	L	CH9
H	L	H	L	L	CH10
H	L	H	H	L	CH11
H	H	L	L	L	CH12
H	H	L	H	L	CH13
H	H	H	L	L	CH14
H	H	H	H	L	CH15

1/ Between CH0-15 and OUTPUT (0-15)

TRUTH TABLE (CH16 – CH31)

B3	B2	B1	B0	EN(16-31)	"ON" CHANNEL 1/
X	X	X	X	H	NONE
L	L	L	L	L	CH16
L	L	L	H	L	CH17
L	L	H	L	L	CH18
L	L	H	H	L	CH19
L	H	L	L	L	CH20
L	H	L	H	L	CH21
L	H	H	L	L	CH22
L	H	H	H	L	CH23
H	L	L	L	L	CH24
H	L	L	H	L	CH25
H	L	H	L	L	CH26
H	L	H	H	L	CH27
H	H	L	L	L	CH28
H	H	L	H	L	CH29
H	H	H	L	L	CH30
H	H	H	H	L	CH31

1/ Between CH16-31 and OUTPUT (16-31)

TRUTH TABLE (CH32 – CH47)

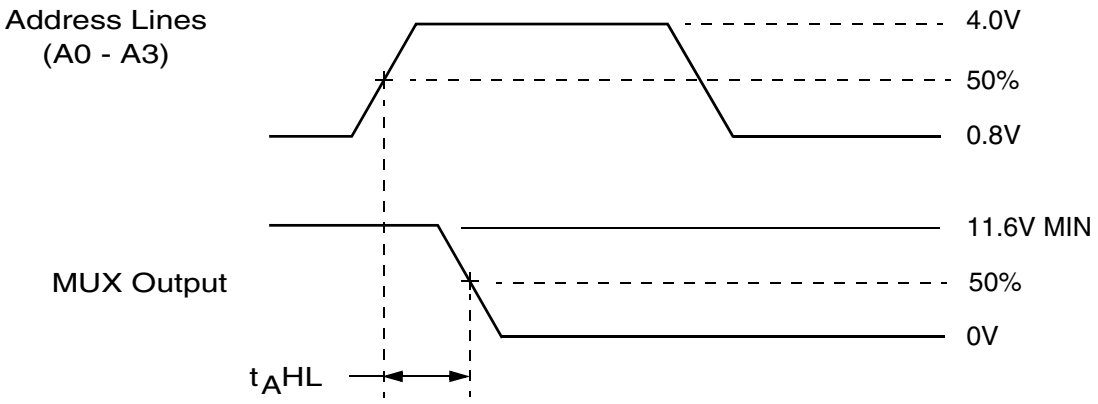
A3	A2	A1	A0	EN(32-47)	"ON" CHANNEL 1/
X	X	X	X	H	NONE
L	L	L	L	L	CH32
L	L	L	H	L	CH33
L	L	H	L	L	CH34
L	L	H	H	L	CH35
L	H	L	L	L	CH36
L	H	L	H	L	CH37
L	H	H	L	L	CH38
L	H	H	H	L	CH39
H	L	L	L	L	CH40
H	L	L	H	L	CH41
H	L	H	L	L	CH42
H	L	H	H	L	CH43
H	H	L	L	L	CH44
H	H	L	H	L	CH45
H	H	H	L	L	CH46
H	H	H	H	L	CH47

1/ Between CH32-47 and OUTPUT (32-47) and CURRENT (32-47)

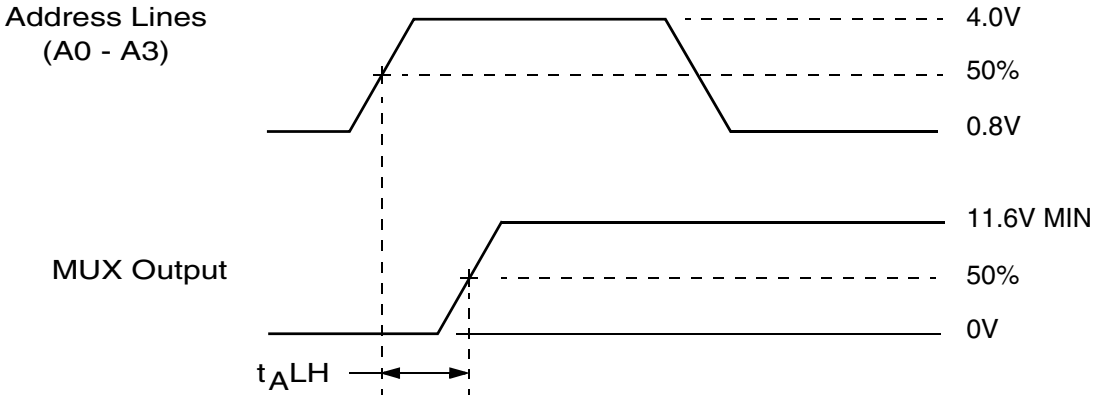
TRUTH TABLE (CH48 – CH63)

A3	A2	A1	A0	EN(48-63)	"ON" CHANNEL 1/
X	X	X	X	H	NONE
L	L	L	L	L	CH48
L	L	L	H	L	CH49
L	L	H	L	L	CH50
L	L	H	H	L	CH51
L	H	L	L	L	CH52
L	H	L	H	L	CH53
L	H	H	L	L	CH54
L	H	H	H	L	CH55
H	L	L	L	L	CH56
H	L	L	H	L	CH57
H	L	H	L	L	CH58
H	L	H	H	L	CH59
H	H	L	L	L	CH60
H	H	L	H	L	CH61
H	H	H	L	L	CH62
H	H	H	H	L	CH63

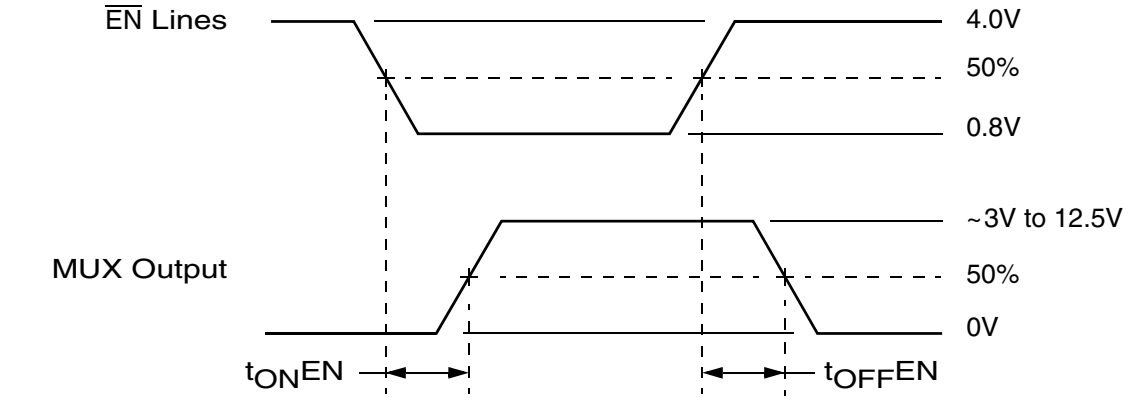
1/ Between CH48-63 and OUTPUT (48-63) and CURRENT (48-63)



Definition of t_AHL



Definition of t_ALH



Definition of $t_{ON}EN$ and $t_{OFF}EN$

NOTE: f = 10KHz, Duty cycle = 50%.

ACT8510 SWITCHING DIAGRAMS

PIN NUMBERS & FUNCTIONS

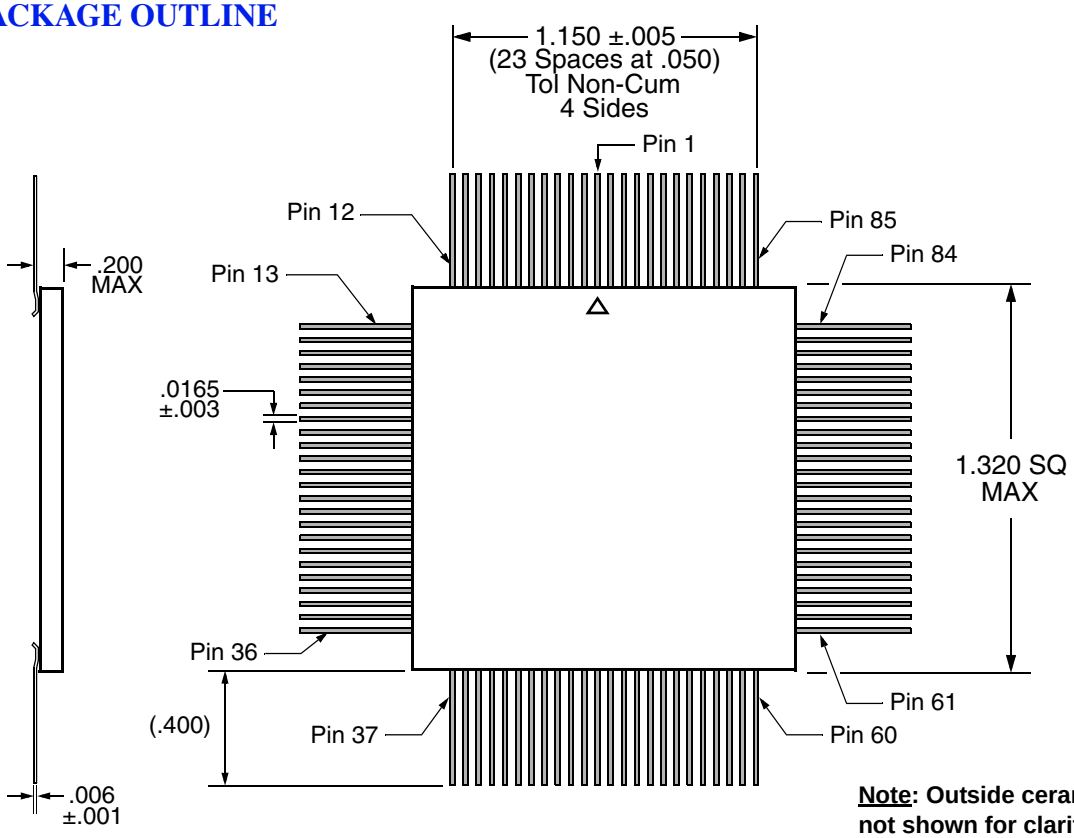
ACT8510 – 96 Leads Ceramic QUAD Flat Pack					
Pin #	**Function**	**Pin #**	**Function**	**Pin #**	**Function**
1	A2	33	CH11	65	CH49
2	B2	34	CH27	66	CH48
3	A3	35	CH12	67	Output I(48-63)
4	B3	36	CH28	68	Output V(48-63)
5	$\overline{EN}$ 0-15	37	CH13	69	Output I(32-47)
6	$\overline{EN}$ 16-31	38	CH29	70	Output V(32-47)
7	CH0	39	CH14	71	GND
8	CH16	40	CH30	72	GND
9	CH1	41	CH15	73	CH47
10	CH17	42	CH31	74	CH46
11	CH2	43	NC	75	CH45
12	CH18	44	+VEE	76	CH44
13	CH3	45	NC	77	CH43
14	CH19	46	-VEE	78	CH42
15	CH4	47	NC	79	CH41
16	CH20	48	VREF	80	CH40
17	CH5	49	NC	81	CH39
18	CH21	50	CASE GND	82	CH38
19	CH6	51	CH63	83	CH37
20	CH22	52	CH62	84	CH36
21	CH7	53	CH61	85	CH35
22	CH23	54	CH60	86	CH34
23	GND	55	CH59	87	CH33
24	GND	56	CH58	88	CH32
25	Output V(0-15)	57	CH57	89	GND
26	Output V(16-31)	58	CH56	90	GND
27	CH8	59	CH55	91	$\overline{EN}$ 48-63
28	CH24	60	CH54	92	$\overline{EN}$ 32-47
29	CH9	61	CH53	93	A0
30	CH25	62	CH52	94	B0
31	CH10	63	CH51	95	A1
32	CH26	64	CH50	96	B1

NOTE: It is recommended that all "NC or "no connect pin" be grounded. This eliminates or minimizes any ESD or static buildup.

ORDERING INFORMATION

Model Number	Screening	DSCC SMD #	Package
ACT8510-S	Military Temperature, -55°C to +125°C, Screened in accordance with MIL-PRF-38534, Class K	NA	QUAD Flat Pack
ACT8510-7	Commercial Flow, +25°C testing only		
ACT8510-201-1S	In accordance with DSCC SMD	5962-0920201KXC	

FLAT PACKAGE OUTLINE



Note: Outside ceramic tie bars not shown for clarity. Contact factory for details.

EXPORT CONTROL:

This product is controlled for export under the International Traffic in Arms Regulations (ITAR). A license from the U.S. Department of State is required prior to the export of this product from the United States.

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PLAINVIEW, NEW YORK
Toll Free: 800-THE-1553
Fax: 516-694-6715

INTERNATIONAL
Tel: 805-778-9229
Fax: 805-778-1980

NORTHEAST
Tel: 603-888-3975
Fax: 603-888-4585

SE AND MID-ATLANTIC
Tel: 321-951-4164
Fax: 321-951-4254

WEST COAST
Tel: 949-362-2260
Fax: 949-362-2266

CENTRAL
Tel: 719-594-8017
Fax: 719-594-8468

www.aeroflex.com info-ams@aeroflex.com

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