**Freescale Semiconductor**
Data Sheet: Technical Data

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# MC9S08PT16

# MC9S08PT16 Series

## Support: MC9S08PT16 and MC9S08PT8

### Features

- 8-Bit S08 central processor unit (CPU)
  - Up to 20 MHz bus at 2.7 V to 5.5 V across temperature range of -40 °C to 105 °C
  - Supporting up to 40 interrupt/reset sources
  - Supporting up to four-level nested interrupt
  - On-chip memory
  - Up to 16 KB flash read/program/erase over full operating voltage and temperature
  - Up to 256 byte EEPROM; 2-byte erase sector; program and erase while executing flash
  - Up to 2048 byte random-access memory (RAM)
  - Flash and RAM access protection

- Power-saving modes
  - One low-power stop mode; reduced power wait mode
  - Peripheral clock enable register can disable clocks to unused modules, reducing currents; allows clocks to remain enabled to specific peripherals in stop3 mode

- Clocks
  - Oscillator (XOSC) - loop-controlled Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 39.0625 kHz or 4 MHz to 20 MHz
  - Internal clock source (ICS) - containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allowing 1% deviation across temperature range of 0 °C to 70 °C and 2% deviation across temperature range of -40 °C to 105 °C; up to 20 MHz

- System protection
  - Watchdog with independent clock source
  - Low-voltage detection with reset or interrupt; selectable trip points
  - Illegal opcode detection with reset
  - Illegal address detection with reset

- Development support
  - Single-wire background debug interface
  - Breakpoint capability to allow three breakpoints setting during in-circuit debugging
  - On-chip in-circuit emulator (ICE) debug module containing two comparators and nine trigger modes

- Peripherals
  - ACMP - one analog comparator with both positive and negative inputs; separately selectable interrupt on rising and falling comparator output; filtering
  - ADC - 12-channel, 12-bit resolution; 2.5 µs conversion time; data buffers with optional watermark; automatic compare function; internal bandgap reference channel; operation in stop mode; optional hardware trigger
  - CRC - programmable cyclic redundancy check module
  - FTM - two flex timer modulators modules including one 6-channel and one 2-channel ones; 16-bit counter; each channel can be configured for input capture, output compare, edge- or center-aligned PWM mode
  - IIC - One inter-integrated circuit module; up to 400 kbps; multi-master operation; programmable slave address; supporting broadcast mode and 10-bit addressing
  - MTIM - One modulo timer with 8-bit prescaler and overflow interrupt
  - RTC - 16-bit real timer counter (RTC)
  - SCI - two serial communication interface (SCI/UART) modules optional 13-bit break; full duplex non-return to zero (NRZ); LIN extension support
  - SPI - one 8-bit serial peripheral interface (SPI) modules; full-duplex or single-wire bidirectional; master or slave mode
  - TSI - supporting up to 16 external electrodes; configurable software or hardware scan trigger; fully support freescale touch sensing software library; capability to wake MCU from stop3 mode

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- Input/Output
  - 37 GPIOs including one output-only pin
  - One 8-bit keyboard interrupt module (KBI)
  - Two true open-drain output pins
  - Four, ultra-high current sink pins supporting 20 mA source/sink current

- Package options
  - 44-pin LQFP
  - 32-pin LQFP
  - 20-pin SOIC; 20-pin TSSOP
  - 16-pin TSSOP

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# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device numbers: PT16 and PT8.

# 2 Part identification

## 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 2.2 Format

Part numbers for this device have the following format:

MC 9 S08 PT AA B CC

## 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description | Values |
|---|---|---|
| MC | Qualification status | • MC = fully qualified, general market flow |
| 9 | Memory | • 9 = flash based |
| S08 | Core | • S08 = 8-bit CPU |
| PT | Device family | • PT |
| AA | Approximate flash size in KB | • 16 = 16 KB<br>• 8 = 8 KB |
| B | Temperature range (°C) | • V = –40 to 105 |

*Table continues on the next page...*

| Field | Description | Values |
|---|---|---|
| CC | Package designator | • LD = 44-LQFP<br>• LC = 32-LQFP<br>• TJ = 20-TSSOP<br>• WJ = 20-SOIC<br>• TG = 16-TSSOP |

## 2.4 Example

This is an example part number:

MC9S08PT16VLD

# 3 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

**Table 1. Parameter Classifications**

| | |
|---|---|
| P | Those parameters are guaranteed during production testing on each individual device. |
| C | Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. |
| T | Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category. |
| D | Those parameters are derived mainly from simulations. |

**NOTE**

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

# 4 Ratings

## 4.1 Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | –55 | 150 | °C | 1 |
| $T_{SDR}$ | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.2 Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.3 ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{HBM}$ | Electrostatic discharge voltage, human body model | -6000 | +6000 | V | 1 |
| $V_{CDM}$ | Electrostatic discharge voltage, charged-device model | -500 | +500 | V | 2 |
| $I_{LAT}$ | Latch-up current at ambient temperature of 105°C | -100 | +100 | mA | |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

## 4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in below table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either $V_{SS}$ or $V_{DD}$) or the programmable pullup resistor associated with the pin is enabled.

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | –0.3 | 5.8 | V |
| $I_{DD}$ | Maximum current into $V_{DD}$ | — | 120 | mA |

*Table continues on the next page...*

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DIO}$ | Digital input voltage (except $\overline{RESET}$, EXTAL, and XTAL) | –0.3 | $V_{DD}$ + 0.3 | V |
| $V_{AIO}$ | Analog[1], $\overline{RESET}$, EXTAL, and XTAL input voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_D$ | Instantaneous maximum current single pin limit (applies to all port pins) | –25 | 25 | mA |
| $V_{DDA}$ | Analog supply voltage | $V_{DD}$ – 0.3 | $V_{DD}$ + 0.3 | V |

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

# 5 General

## 5.1 Nonswitching electrical specifications

### 5.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

**Table 2. DC characteristics**

| Symbol | C | Descriptions | | | Min | Typical[1] | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| — | — | Operating voltage | | — | 2.7 | — | 5.5 | V |
| $V_{OH}$ | P | Output high voltage | All I/O pins, low-drive strength | 5 V, $I_{load}$ = -2 mA | $V_{DD}$ - 1.5 | — | — | V |
| | C | | | 3 V, $I_{load}$ = -0.6 mA | $V_{DD}$ - 0.8 | — | — | V |
| | P | | High current drive pins, high-drive strength[2] | 5 V, $I_{load}$ = -20 mA | $V_{DD}$ - 1.5 | — | — | V |
| | C | | | 3 V, $I_{load}$ = -6 mA | $V_{DD}$ - 0.8 | — | — | V |
| $I_{OHT}$ | D | Output high current | Max total $I_{OH}$ for all ports | 5 V | — | — | -100 | mA |
| | | | | 3 V | — | — | -60 | |
| $V_{OL}$ | P | Output low voltage | All I/O pins, low-drive strength | 5 V, $I_{load}$ = 2 mA | — | — | 1.5 | V |
| | C | | | 3 V, $I_{load}$ = 0.6 mA | — | — | 0.8 | V |
| | P | | High current drive pins, high-drive strength[2] | 5 V, $I_{load}$ =20 mA | — | — | 1.5 | V |
| | C | | | 3 V, $I_{load}$ = 6 mA | — | — | 0.8 | V |
| $I_{OLT}$ | D | Output low current | Max total $I_{OL}$ for all ports | 5 V | — | — | 100 | mA |
| | | | | 3 V | — | — | 60 | |

*Table continues on the next page...*

## Table 2. DC characteristics (continued)

| Symbol | C | Descriptions | | | Min | Typical[1] | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | P | Input high voltage | All digital inputs | $V_{DD}$>4.1V | 0.70 × $V_{DD}$ | — | — | V |
| | | | | $V_{DD}$>2.7V | 0.85 × $V_{DD}$ | — | — | |
| $V_{IL}$ | P | Input low voltage | All digital inputs | $V_{DD}$>4.1V | — | — | 0.35 × $V_{DD}$ | V |
| | | | | $V_{DD}$>2.7V | — | — | 0.30 × $V_{DD}$ | |
| $V_{hys}$ | C | Input hysteresis | All digital inputs | — | 0.06 × $V_{DD}$ | — | — | mV |
| $\lvert I_{In}\rvert$ | P | Input leakage current | All input only pins (per pin) | $V_{IN}$ = $V_{DD}$ or $V_{SS}$ | — | 0.1 | 1 | µA |
| $\lvert I_{OZ}\rvert$ | P | Hi-Z (off-state) leakage current | All input/output (per pin) | $V_{IN}$ = $V_{DD}$ or $V_{SS}$ | — | 0.1 | 1 | µA |
| $\lvert I_{OZTOT}\rvert$ | C | Total leakage combined for all inputs and Hi-Z pins | All input only and I/O | $V_{IN}$ = $V_{DD}$ or $V_{SS}$ | — | — | 2 | µA |
| $R_{PU}$ | P | Pullup resistors | All digital inputs, when enabled (all I/O pins other than PTA5/ IRQ/TCLK/RESET | — | 17.5 | — | 52.5 | kΩ |
| $R_{PU}$[3] | P | Pullup resistors | PTA5/IRQ/TCLK/ RESET | — | 17.5 | — | 52.5 | kΩ |
| $I_{IC}$ | D | DC injection current[4, 5, 6] | Single pin limit | $V_{IN}$ < $V_{SS}$, $V_{IN}$ > $V_{DD}$ | -0.2 | — | 2 | mA |
| | | | Total MCU limit, includes sum of all stressed pins | | -5 | — | 25 | |
| $C_{In}$ | C | Input capacitance, all pins | | — | — | — | 8 | pF |
| $V_{RAM}$ | C | RAM retention voltage | | — | 2.0 | — | — | V |

1. Typical values are measured at 25 °C. Characterized, not tested.
2. Only PTB4, PTB5, PTD0, PTD1 support ultra high current output.
3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
4. All functional non-supply pins, except for PTA5, are internally clamped to $V_{SS}$ and $V_{DD}$.
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the large one.
6. Power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In}$ > $V_{DD}$) is higher than $I_{DD}$, the injection current may flow out of $V_{DD}$ and could result in external power supply going out of regulation. Ensure that external $V_{DD}$ load will shunt current higher than maximum injection current when the MCU is not consuming power, such as no system clock is present, or clock rate is very low (which would reduce overall power consumption).

## Table 3. LVD and POR Specification

| Symbol | C | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{POR}$ | D | POR re-arm voltage[1] | 1.5 | 1.75 | 2.0 | V |
| $V_{LVDH}$ | C | Falling low-voltage detect threshold - high range (LVDV = 1)[2] | 4.2 | 4.3 | 4.4 | V |

*Table continues on the next page...*

## Table 3. LVD and POR Specification (continued)

| Symbol | C | Description | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{LVW1H}$ | C | Falling low-voltage warning threshold - high range | Level 1 falling (LVWV = 00) | 4.3 | 4.4 | 4.5 | V |
| $V_{LVW2H}$ | C | | Level 2 falling (LVWV = 01) | 4.5 | 4.5 | 4.6 | V |
| $V_{LVW3H}$ | C | | Level 3 falling (LVWV = 10) | 4.6 | 4.6 | 4.7 | V |
| $V_{LVW4H}$ | C | | Level 4 falling (LVWV = 11) | 4.7 | 4.7 | 4.8 | V |
| $V_{HYSH}$ | C | High range low-voltage detect/warning hysteresis | | — | 100 | — | mV |
| $V_{LVDL}$ | C | Falling low-voltage detect threshold - low range (LVDV = 0) | | 2.56 | 2.61 | 2.66 | V |
| $V_{LVDW1L}$ | C | Falling low-voltage warning threshold - low range | Level 1 falling (LVWV = 00) | 2.62 | 2.7 | 2.78 | V |
| $V_{LVDW2L}$ | C | | Level 2 falling (LVWV = 01) | 2.72 | 2.8 | 2.88 | V |
| $V_{LVDW3L}$ | C | | Level 3 falling (LVWV = 10) | 2.82 | 2.9 | 2.98 | V |
| $V_{LVDW4L}$ | C | | Level 4 falling (LVWV = 11) | 2.92 | 3.0 | 3.08 | V |
| $V_{HYSDL}$ | C | Low range low-voltage detect hysteresis | | — | 40 | — | mV |
| $V_{HYSWL}$ | C | Low range low-voltage warning hysteresis | | — | 80 | — | mV |
| $V_{BG}$ | P | Buffered bandgap output [3] | | 1.14 | 1.16 | 1.18 | V |

1. Maximum is highest voltage that POR is guaranteed.
2. Rising thresholds are falling threshold + hysteresis.
3. voltage Factory trimmed at $V_{DD}$ = 5.0 V, Temp = 25 °C

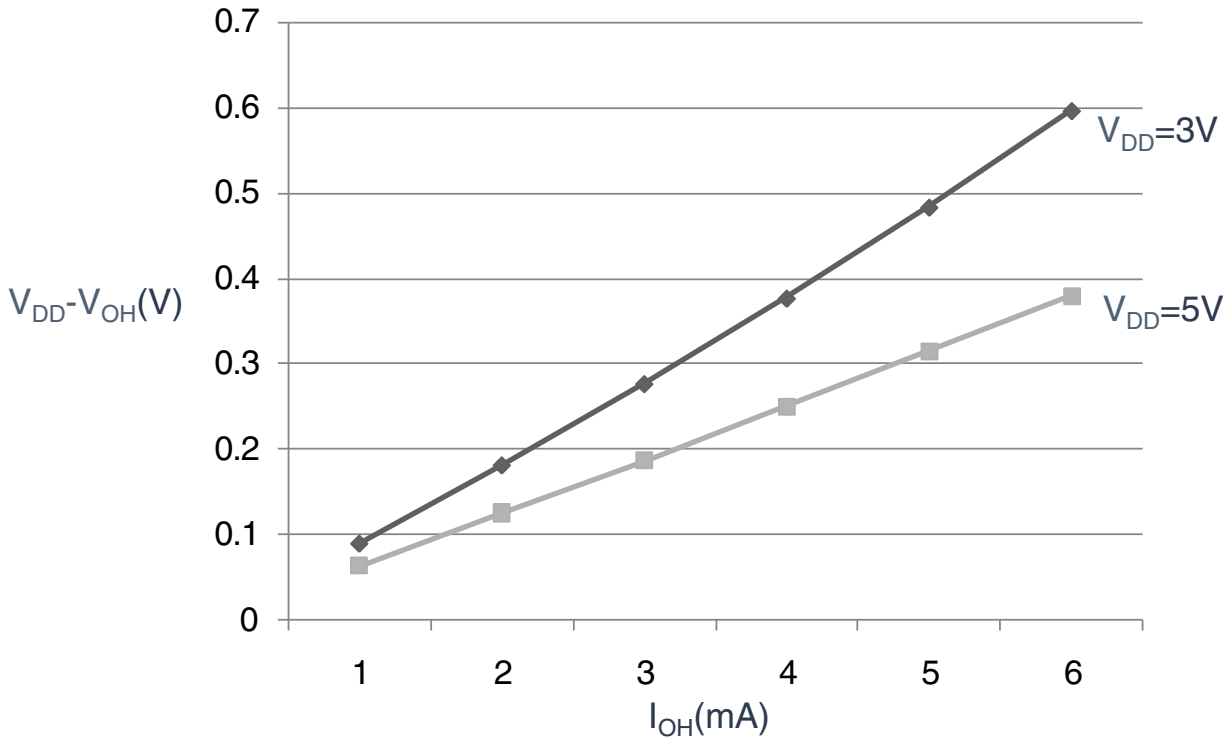



**Figure 1. Typical $I_{OH}$ Vs. $V_{DD}$-$V_{OH}$**

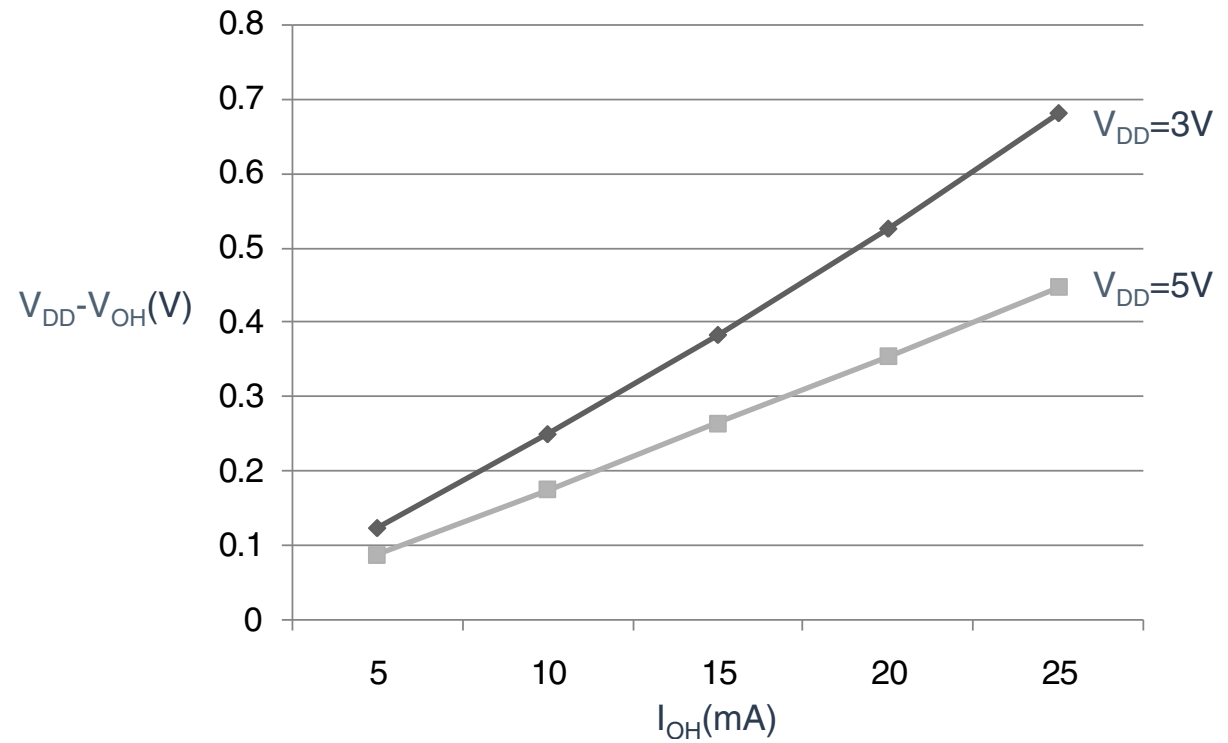



**Figure 2. Typical $I_{OH}$ Vs. $V_{DD}$-$V_{OH}$ (High current drive)**

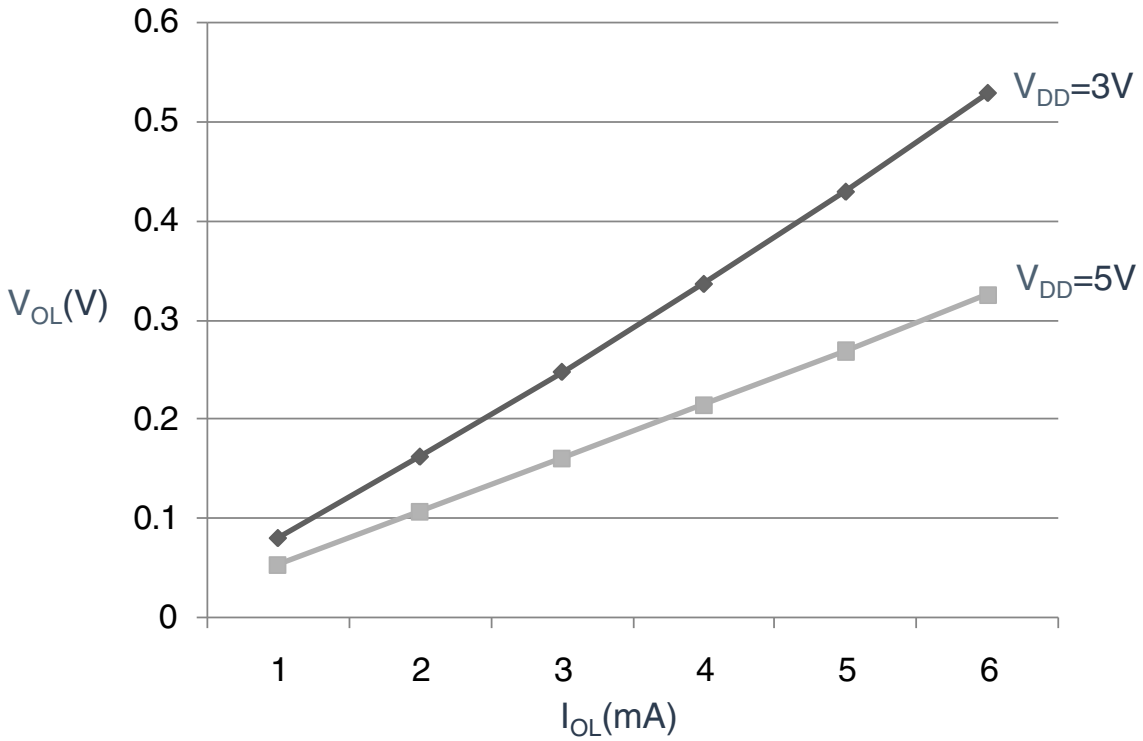



**Figure 3. Typical $I_{OL}$ Vs. $V_{OL}$**

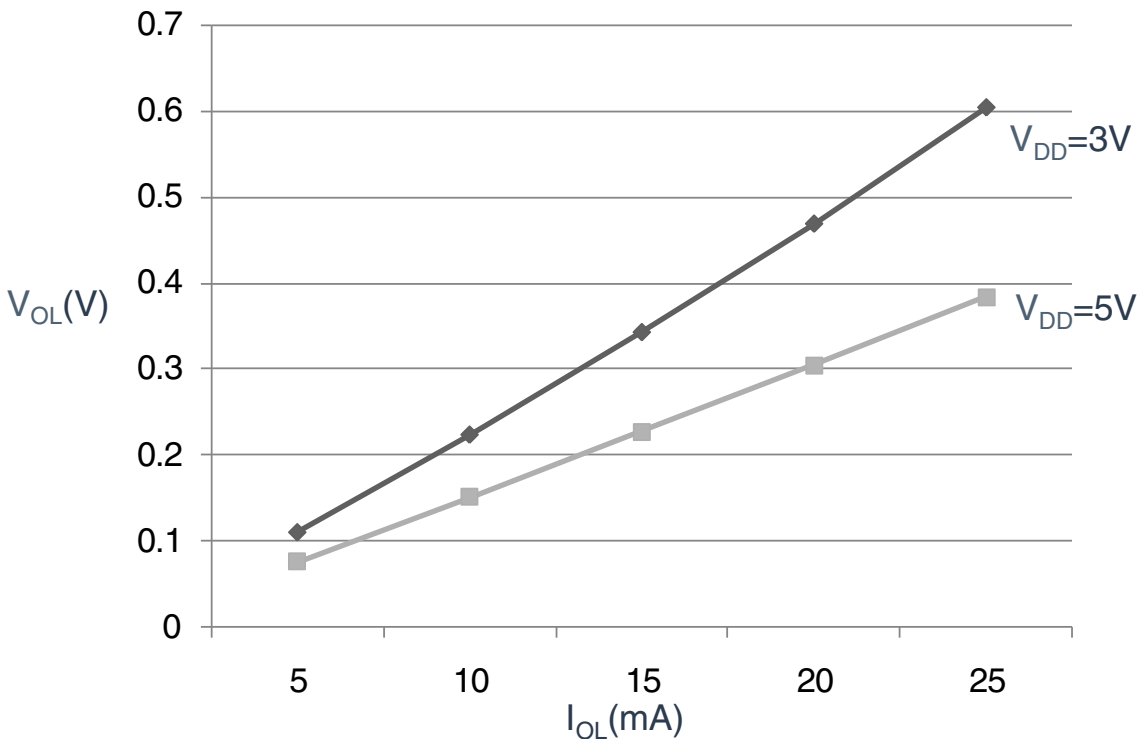



**Figure 4. Typical $I_{OL}$ Vs. $V_{OL}$ (High current drive)**

## 5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

**Table 4. Supply current characteristics**

| Num | C | Parameter | Symbol | Bus Freq | $V_{DD}$ (V) | Typical[1] | Max | Unit | Temp |
|---|---|---|---|---|---|---|---|---|---|
| 1 | C | Run supply current FEI mode, all modules on; run from flash | $RI_{DD}$ | 20 MHz | 5 | 7.60 | — | mA | -40 to 105 °C |
| | C | | | 10 MHz | | 4.65 | — | | |
| | | | | 1 MHz | | 1.90 | — | | |
| | C | | | 20 MHz | 3 | 7.05 | — | | |
| | C | | | 10 MHz | | 4.40 | — | | |
| | | | | 1 MHz | | 1.85 | — | | |
| 2 | C | Run supply current FEI mode, all modules off & gated; run from flash | $RI_{DD}$ | 20 MHz | 5 | 5.88 | — | mA | -40 to 105 °C |
| | C | | | 10 MHz | | 3.70 | — | | |
| | | | | 1 MHz | | 1.85 | — | | |
| | C | | | 20 MHz | 3 | 5.35 | — | | |
| | C | | | 10 MHz | | 3.42 | — | | |
| | | | | 1 MHz | | 1.80 | — | | |
| 3 | P | Run supply current FBE mode, all modules on; run from RAM | $RI_{DD}$ | 20 MHz | 5 | 10.9 | 14.0 | mA | -40 to 105 °C |
| | C | | | 10 MHz | | 6.10 | — | | |
| | | | | 1 MHz | | 1.69 | — | | |
| | C | | | 20 MHz | 3 | 8.18 | — | | |
| | | | | 10 MHz | | 5.14 | — | | |
| | | | | 1 MHz | | 1.44 | — | | |
| 4 | P | Run supply current FBE mode, all modules off & gated; run from RAM | $RI_{DD}$ | 20 MHz | 5 | 8.50 | 13.0 | mA | -40 to 105 °C |
| | C | | | 10 MHz | | 5.07 | — | | |
| | | | | 1 MHz | | 1.59 | — | | |
| | C | | | 20 MHz | 3 | 6.11 | — | | |
| | | | | 10 MHz | | 4.10 | — | | |
| | | | | 1 MHz | | 1.34 | — | | |
| 5 | C | Wait mode current FEI mode, all modules on | $WI_{DD}$ | 20 MHz | 5 | 5.95 | — | mA | -40 to 105 °C |
| | | | | 10 MHz | | 3.50 | — | | |
| | | | | 1 MHz | | 1.24 | — | | |
| | C | | | 20 MHz | 3 | 5.45 | — | | |
| | | | | 10 MHz | | 3.25 | — | | |
| | | | | 1 MHz | | 1.20 | — | | |
| 6 | C | Stop3 mode supply current no clocks active (except 1kHz LPO clock) | $S3I_{DD}$ | — | 5 | 4.6 | — | µA | -40 to 105 °C |
| | C | | | — | 3 | 4.5 | — | | -40 to 105 °C |

*Table continues on the next page...*

**Table 4. Supply current characteristics (continued)**

| Num | C | Parameter | Symbol | Bus Freq | $V_{DD}$ (V) | Typical[1] | Max | Unit | Temp |
|---|---|---|---|---|---|---|---|---|---|
| 7 | C | ADC adder to stop3 | — | — | 5 | 40 | — | µA | -40 to 105 °C |
| | C | ADLPC = 1<br>ADLSMP = 1<br>ADCO = 1<br>MODE = 10B<br>ADICLK = 11B | | | 3 | 39 | — | | |
| 8 | C | TSI adder to stop3[2] | — | — | 5 | 121 | — | µA | -40 to 105 °C |
| | C | PS = 010B<br>NSCN = 0x0F<br>EXTCHRG = 0<br>REFCHRG = 0<br>DVOLT = 01B | | | 3 | 120 | — | | |
| 9 | C | LVD adder to stop3[3] | — | — | 5 | 128 | — | µA | -40 to 105 °C |
| | C | | | | 3 | 124 | — | | |

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. The current varies with TSI configuration and capacity of touch electrode. Please refer toTSI electrical specifications.
3. LVD is periodically woken up from stop3 by 5% duty cycle. The period is equal to or less than 2 ms.

### 5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

## 5.2 Switching specifications

### 5.2.1 Control timing

**Table 5. Control timing**

| Num | C | Rating | Symbol | Min | Typical[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | P | Bus frequency ($t_{cyc} = 1/f_{Bus}$) | $f_{Bus}$ | DC | — | 20 | MHz |
| 2 | C | Internal low power oscillator frequency | $f_{LPO}$ | — | 1.0 | — | KHz |

*Table continues on the next page...*

## Table 5. Control timing (continued)

| Num | C | Rating | | Symbol | Min | Typical[1] | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| 3 | D | External reset pulse width[2] | | $t_{extrst}$ | 1.5 × $t_{Self_reset}$ | — | — | ns |
| 4 | D | Reset low drive | | $t_{rstdrv}$ | 34 × $t_{cyc}$ | — | — | ns |
| 5 | D | BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes | | $t_{MSSU}$ | 500 | — | — | ns |
| 6 | D | BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes[3] | | $t_{MSH}$ | 100 | — | — | ns |
| 7 | D | IRQ pulse width | Asynchronous path[2] | $t_{ILIH}$ | 100 | — | — | ns |
| | D | | Synchronous path[4] | $t_{IHIL}$ | 1.5 × $t_{cyc}$ | — | — | ns |
| 8 | D | Keyboard interrupt pulse width | Asynchronous path[2] | $t_{ILIH}$ | 100 | — | — | ns |
| | D | | Synchronous path | $t_{IHIL}$ | 1.5 × $t_{cyc}$ | — | — | ns |
| 9 | C | Port rise and fall time - Normal drive strength (HDRVE_PTXx = 0) (load = 50 pF)[5] | — | $t_{Rise}$ | — | 10.2 | — | ns |
| | C | | | $t_{Fall}$ | — | 9.5 | — | ns |
| | C | Port rise and fall time - Extreme high drive strength (HDRVE_PTXx = 1) (load = 50 pF)[5] | — | $t_{Rise}$ | — | 5.4 | — | ns |
| | C | | | $t_{Fall}$ | — | 4.6 | — | ns |

1. Typical values are based on characterization data at $V_{DD}$ = 5.0 V, 25 °C unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a reset pin request.
3. To enter BDM mode following a POR, BKGD/MS must be held low during the powerup and for a hold time of $t_{MSH}$ after $V_{DD}$ rises above $V_{LVD}$.
4. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
5. Timing is shown with respect to 20% $V_{DD}$ and 80% $V_{DD}$ levels. Temperature range -40 °C to 105 °C.

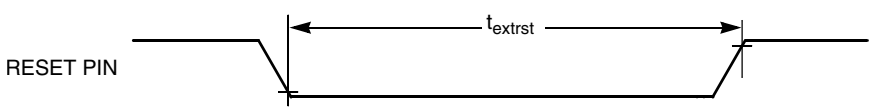



**Figure 5. Reset timing**

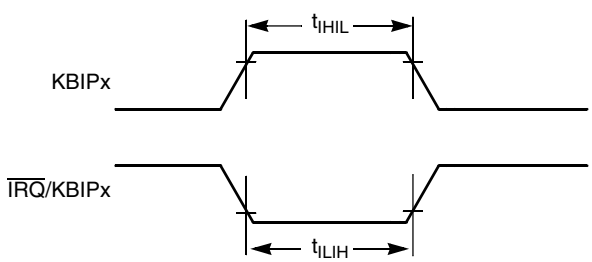



**Figure 6. IRQ/KBIPx timing**

## 5.2.2 Debug trace timing specifications

**Table 6. Debug trace operating behaviors**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{cyc}$ | Clock period | Frequency dependent | | MHz |
| $t_{wl}$ | Low pulse width | 2 | — | ns |
| $t_{wh}$ | High pulse width | 2 | — | ns |
| $t_r$ | Clock and data rise time | — | 3 | ns |
| $t_f$ | Clock and data fall time | — | 3 | ns |
| $t_s$ | Data setup | 3 | — | ns |
| $t_h$ | Data hold | 2 | — | ns |

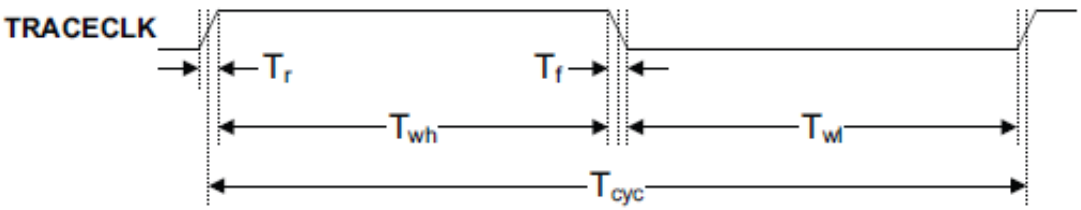



**Figure 7. TRACE_CLKOUT specifications**

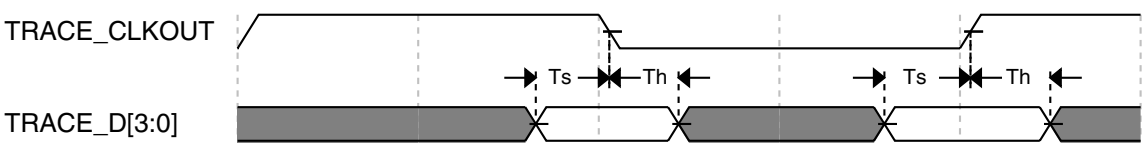



**Figure 8. Trace data specifications**

## 5.2.3 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

**Table 7. FTM input timing**

| No. | C | Function | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | D | External clock frequency | $f_{TCLK}$ | 0 | $f_{Bus}/4$ | Hz |

*Table continues on the next page...*

**Table 7. FTM input timing (continued)**

| No. | C | Function | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 2 | D | External clock period | $t_{TCLK}$ | 4 | — | $t_{cyc}$ |
| 3 | D | External clock high time | $t_{clkh}$ | 1.5 | — | $t_{cyc}$ |
| 4 | D | External clock low time | $t_{clkl}$ | 1.5 | — | $t_{cyc}$ |
| 5 | D | Input capture pulse width | $t_{ICPW}$ | 1.5 | — | $t_{cyc}$ |

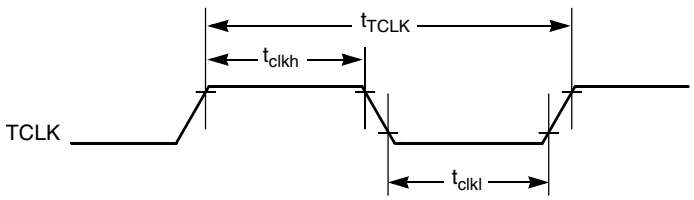



**Figure 9. Timer external clock**

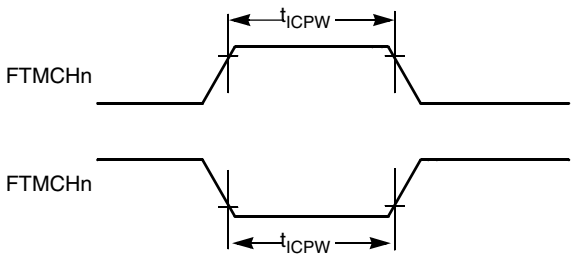



**Figure 10. Timer input capture pulse**

## 5.3 Thermal specifications

### 5.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and $V_{SS}$ or $V_{DD}$ and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and $V_{SS}$ or $V_{DD}$ will be very small.

**Table 8. Thermal characteristics**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Operating temperature range (packaged) | $T_A$ | $T_L$ to $T_H$ -40 to 105 | °C |
| Junction temperature range | $T_J$ | -40 to 150 | °C |
| Thermal resistance single-layer board | | | |
| 44-pin LQFP | $\theta_{JA}$ | 76 | °C/W |
| 32-pin LQFP | $\theta_{JA}$ | 88 | °C/W |
| 20-pin SOIC | $\theta_{JA}$ | 82 | °C/W |
| 20-pin TSSOP | $\theta_{JA}$ | 116 | °C/W |
| 16-pin TSSOP | $\theta_{JA}$ | 130 | °C/W |
| Thermal resistance four-layer board | | | |
| 44-pin LQFP | $\theta_{JA}$ | 54 | °C/W |
| 32-pin LQFP | $\theta_{JA}$ | 59 | °C/W |
| 20-pin SOIC | $\theta_{JA}$ | 54 | °C/W |
| 20-pin TSSOP | $\theta_{JA}$ | 76 | °C/W |
| 16-pin TSSOP | $\theta_{JA}$ | 87 | °C/W |

The average chip-junction temperature ($T_J$) in °C can be obtained from:

$T_J = T_A + (P_D \times \theta_{JA})$

Where:

$T_A$ = Ambient temperature, °C

$\theta_{JA}$ = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between $P_D$ and $T_J$ (if $P_{I/O}$ is neglected) is:

$P_D = K \div (T_J + 273\ °C)$

Solving the equations above for K gives:

$K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (P_D)^2$

where K is a constant pertaining to the particular part. K can be determined by measuring $P_D$ (at equilibrium) for an known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ can be obtained by solving the above equations iteratively for any value of $T_A$.

# 6 Peripheral operating requirements and behaviors

## 6.1 External oscillator (XOSC) and ICS characteristics

**Table 9. XOSC and ICS specifications (temperature range = -40 to 105 °C ambient)**

| Num | C | Characteristic | | Symbol | Min | Typical[1] | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| 1 | C | Oscillator crystal or resonator | Low range (RANGE = 0) | $f_{lo}$ | 32 | — | 40 | kHz |
| | C | | High range (RANGE = 1) FEE or FBE mode[2] | $f_{hi}$ | 4 | — | 20 | MHz |
| | C | | High range (RANGE = 1), high gain (HGO = 1), FBELP mode | $f_{hi}$ | 4 | — | 20 | MHz |
| | C | | High range (RANGE = 1), low power (HGO = 0), FBELP mode | $f_{hi}$ | 4 | — | 20 | MHz |
| 2 | D | Load capacitors | | C1, C2 | See Note[3] | | | |
| 3 | D | Feedback resistor | Low Frequency, Low-Power Mode[4] | $R_F$ | — | — | — | MΩ |
| | | | Low Frequency, High-Gain Mode | | — | 10 | — | MΩ |
| | | | High Frequency, Low-Power Mode | | — | 1 | — | MΩ |
| | | | High Frequency, High-Gain Mode | | — | 1 | — | MΩ |
| 4 | D | Series resistor - Low Frequency | Low-Power Mode [4] | $R_S$ | — | — | — | kΩ |
| | | | High-Gain Mode | | — | 200 | — | kΩ |
| 5 | D | Series resistor - High Frequency | Low-Power Mode[4] | $R_S$ | — | — | — | kΩ |
| | D | Series resistor - High Frequency, High-Gain Mode | 4 MHz | | — | 0 | — | kΩ |
| | D | | 8 MHz | | — | 0 | — | kΩ |
| | D | | 16 MHz | | — | 0 | — | kΩ |
| 6 | C | Crystal start-up time Low range = 32.768 KHz crystal; High range = 20 MHz crystal[5, 6] | Low range, low power | $t_{CSTL}$ | — | 1000 | — | ms |
| | C | | Low range, high power | | — | 800 | — | ms |
| | C | | High range, low power | $t_{CSTH}$ | — | 3 | — | ms |
| | C | | High range, high power | | — | 1.5 | — | ms |
| 7 | T | Internal reference start-up time | | $t_{IRST}$ | — | 20 | 50 | µs |
| 8 | D | Square wave input clock frequency | FEE or FBE mode[2] | $f_{extal}$ | 0.03125 | — | 5 | MHz |
| | D | | FBELP mode | | 0 | — | 20 | MHz |
| 9 | P | Average internal reference frequency - trimmed | | $f_{int_t}$ | — | 32.768 | — | kHz |
| 10 | P | DCO output frequency range - trimmed | | $f_{dco_t}$ | 16 | — | 20 | MHz |

*Table continues on the next page...*

## Table 9. XOSC and ICS specifications (temperature range = -40 to 105 °C ambient) (continued)

| Num | C | Characteristic | | Symbol | Min | Typical[1] | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| 11 | P | Total deviation of DCO output from trimmed frequency[5] | Over full voltage and temperature range | $\Delta f_{dco_t}$ | — | — | ±2.0 | $\%f_{dco}$ |
| | C | | Over fixed voltage and temperature range of 0 to 70 °C | | | | ±1.0 | |
| 12 | C | FLL acquisition time[5, 7] | | $t_{Acquire}$ | — | — | 2 | ms |
| 13 | C | Long term jitter of DCO output clock (averaged over 2 ms interval)[8] | | $C_{Jitter}$ | — | 0.02 | 0.2 | $\%f_{dco}$ |

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3. See crystal or resonator manufacturer's recommendation.
4. Load capacitors ($C_1$,$C_2$), feedback resistor ($R_F$) and series resistor ($R_S$) are incorporated internally when RANGE = HGO = 0.
5. This parameter is characterized and not tested on each device.
6. Proper PC board layout procedures must be followed to achieve specifications.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{Bus}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via $V_{DD}$ and $V_{SS}$ and variation in crystal oscillator frequency increase the $C_{Jitter}$ percentage for a given interval.

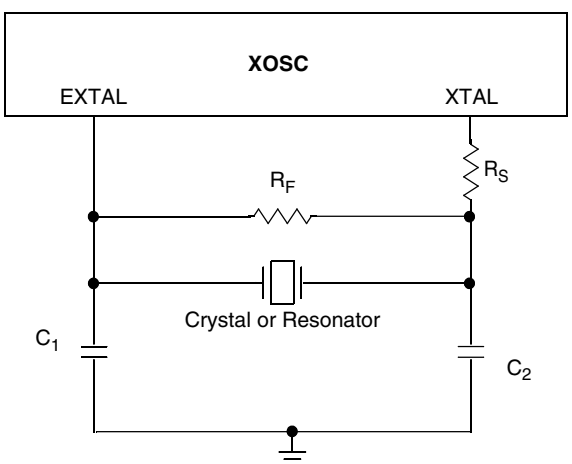



**Figure 11. Typical crystal or resonator circuit**

## 6.2 NVM specifications

This section provides details about program/erase times and program-erase endurance for the flash and EEPROM memories.

**Table 10. Flash characteristics**

| C | Characteristic | Symbol | Min[1] | Typical[2] | Max[3] | Unit[4] |
|---|---|---|---|---|---|---|
| D | Supply voltage for program/erase -40 °C to 105 °C | $V_{prog/erase}$ | 2.7 | — | 5.5 | V |
| D | Supply voltage for read operation | $V_{Read}$ | 2.7 | — | 5.5 | V |
| D | NVM Bus frequency | $f_{NVMBUS}$ | 1 | — | 25 | MHz |
| D | NVM Operating frequency | $f_{NVMOP}$ | 0.8 | — | 1.05 | MHz |
| D | Erase Verify All Blocks | $t_{VFYALL}$ | — | — | 17030 | $t_{cyc}$ |
| D | Erase Verify Flash Block | $t_{RD1BLK}$ | — | — | 16977 | $t_{cyc}$ |
| D | Erase Verify EEPROM Block | $t_{RD1BLK}$ | — | — | 843 | $t_{cyc}$ |
| D | Erase Verify Flash Section | $t_{RD1SEC}$ | — | — | 517 | $t_{cyc}$ |
| D | Erase Verify EEPROM Section | $t_{DRD1SEC}$ | 0.10 | 0.10 | 0.11 | ms |
| D | Read Once | $t_{RDONCE}$ | — | — | 455 | $t_{cyc}$ |
| D | Program Flash (2 word) | $t_{PGM2}$ | 0.12 | 0.12 | 0.14 | ms |
| D | Program Flash (4 word) | $t_{PGM4}$ | 0.20 | 0.21 | 0.24 | ms |
| D | Program Once | $t_{PGMONCE}$ | 0.20 | 0.21 | 0.24 | ms |
| D | Program EEPROM (1 Byte) | $t_{DPGM1}$ | 0.02 | 0.02 | 0.02 | ms |
| D | Program EEPROM (2 Byte) | $t_{DPGM2}$ | 0.17 | 0.18 | 0.20 | ms |
| D | Erase All Blocks | $t_{ERSALL}$ | 96.01 | 100.78 | 125.80 | ms |
| D | Erase Flash Block | $t_{ERSBLK}$ | 95.98 | 100.75 | 125.76 | ms |
| D | Erase Flash Sector | $t_{ERSPG}$ | 19.10 | 20.05 | 25.05 | ms |
| D | Erase EEPROM Sector | $t_{DERSPG}$ | 4.81 | 5.05 | 6.30 | ms |
| D | Unsecure Flash | $t_{UNSECU}$ | 96.01 | 100.78 | 125.80 | ms |
| D | Verify Backdoor Access Key | $t_{VFYKEY}$ | — | — | 469 | $t_{cyc}$ |
| D | Set User Margin Level | $t_{MLOADU}$ | — | — | 442 | $t_{cyc}$ |
| C | FLASH Program/erase endurance $T_L$ to $T_H$ = -40 °C to 105 °C | $n_{FLPE}$ | 10 k | 100 k | — | Cycles |
| C | EEPROM Program/erase endurance TL to TH = -40 °C to 105 °C | $n_{FLPE}$ | 50 k | 500 k | — | Cycles |
| C | Data retention at an average junction temperature of $T_{Javg}$ = 85°C after up to 10,000 program/erase cycles | $t_{D_ret}$ | 15 | 100 | — | years |

1. Minimun times are based on maxmum $f_{NVMOP}$ and maximum $f_{NVMBUS}$
2. Typical times are based on typical $f_{NVMOP}$ and maximum $f_{NVMBUS}$
3. Maximum times are based on minimum $f_{NVMOP}$ and maximum $f_{NVMBUS}$
4. $t_{cyc} = 1 / f_{NVMBUS}$

Program and erase operations do not require any special power sources other than the normal $V_{DD}$ supply. For more detailed information about program/erase operations, see the Memory section.

# 6.3 Analog

## 6.3.1 ADC characteristics

**Table 11. 5 V 12-bit ADC operating conditions**

| Characteristic | Conditions | Symb | Min | Typ[1] | Max | Unit | Comment |
|---|---|---|---|---|---|---|---|
| Supply voltage | Absolute | $V_{DDA}$ | 2.7 | — | 5.5 | V | — |
| | Delta to $V_{DD}$ ($V_{DD}$-$V_{DDAD}$) | $\Delta V_{DDA}$ | -100 | 0 | +100 | mV | |
| Ground voltage | Delta to $V_{SS}$ ($V_{SS}$-$V_{SSA}$)[2] | $\Delta V_{SSA}$ | -100 | 0 | +100 | mV | |
| Input voltage | | $V_{ADIN}$ | $V_{REFL}$ | — | $V_{REFH}$ | V | |
| Input capacitance | | $C_{ADIN}$ | — | 4.5 | 5.5 | pF | |
| Input resistance | | $R_{ADIN}$ | — | 3 | 5 | kΩ | — |
| Analog source resistance | 12-bit mode<br>• $f_{ADCK}$ > 4 MHz<br>• $f_{ADCK}$ < 4 MHz | $R_{AS}$ | —<br>— | —<br>— | 2<br>5 | kΩ | External to MCU |
| | 10-bit mode<br>• $f_{ADCK}$ > 4 MHz<br>• $f_{ADCK}$ < 4 MHz | | —<br>— | —<br>— | 5<br>10 | | |
| | 8-bit mode<br>(all valid $f_{ADCK}$) | | — | — | 10 | | |
| ADC conversion clock frequency | High speed (ADLPC=0) | $f_{ADCK}$ | 0.4 | — | 8.0 | MHz | — |
| | Low power (ADLPC=1) | | 0.4 | — | 4.0 | | |

1. Typical values assume $V_{DDA}$ = 5.0 V, Temp = 25°C, $f_{ADCK}$=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.

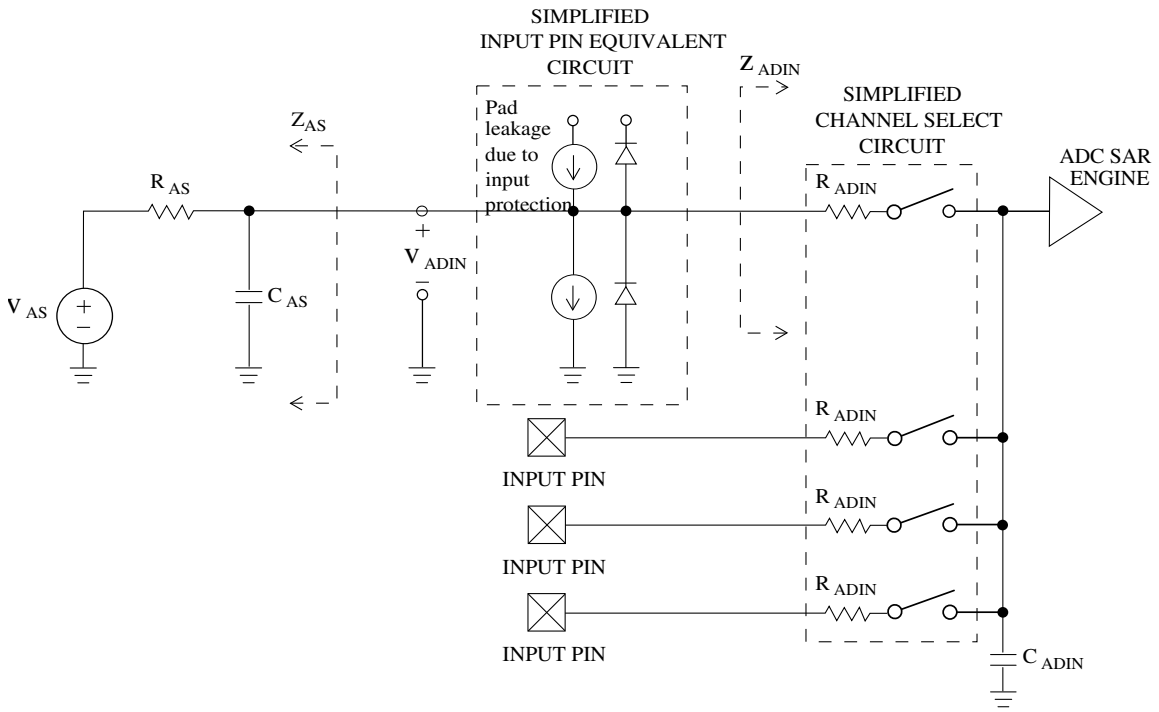



**Figure 12. ADC input impedance equivalency diagram**

**Table 12. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)**

| Characteristic | Conditions | C | Symb | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| Supply current<br>ADLPC = 1<br>ADLSMP = 1<br>ADCO = 1 | | T | $I_{DDA}$ | — | 133 | — | µA |
| Supply current<br>ADLPC = 1<br>ADLSMP = 0<br>ADCO = 1 | | T | $I_{DDA}$ | — | 218 | — | µA |
| Supply current<br>ADLPC = 0<br>ADLSMP = 1<br>ADCO = 1 | | T | $I_{DDA}$ | — | 327 | — | µA |
| Supply current<br>ADLPC = 0<br>ADLSMP = 0<br>ADCO = 1 | | T | $I_{DDAD}$ | — | 582 | 990 | µA |
| Supply current | Stop, reset, module off | T | $I_{DDA}$ | — | 0.011 | 1 | µA |

*Table continues on the next page...*

## Table 12. 12-bit ADC Characteristics ($V_{REFH}$ = $V_{DDA}$, $V_{REFL}$ = $V_{SSA}$) (continued)

| Characteristic | Conditions | C | Symb | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| ADC asynchronous clock source | High speed (ADLPC = 0) | P | $f_{ADACK}$ | 2 | 3.3 | 5 | MHz |
| | Low power (ADLPC = 1) | | | 1.25 | 2 | 3.3 | |
| Conversion time (including sample time) | Short sample (ADLSMP = 0) | T | $t_{ADC}$ | — | 20 | — | ADCK cycles |
| | Long sample (ADLSMP = 1) | | | — | 40 | — | |
| Sample time | Short sample (ADLSMP = 0) | T | $t_{ADS}$ | — | 3.5 | — | ADCK cycles |
| | Long sample (ADLSMP = 1) | | | — | 23.5 | — | |
| Total unadjusted Error[2] | 12-bit mode | T | $E_{TUE}$ | — | ±5.0 | — | LSB[3] |
| | 10-bit mode | P | | — | ±1.5 | ±2.0 | |
| | 8-bit mode | P | | — | ±0.7 | ±1.0 | |
| Differential Non-Liniarity | 12-bit mode | T | DNL | — | ±1.0 | — | LSB[3] |
| | 10-bit mode[4] | P | | — | ±0.25 | ±0.5 | |
| | 8-bit mode[4] | P | | — | ±0.15 | ±0.25 | |
| Integral Non-Linearity | 12-bit mode | T | INL | — | ±1.0 | — | LSB[3] |
| | 10-bit mode | T | | — | ±0.3 | ±0.5 | |
| | 8-bit mode | T | | — | ±0.15 | ±0.25 | |
| Zero-scale error[5] | 12-bit mode | C | $E_{ZS}$ | — | ±2.0 | — | LSB[3] |
| | 10-bit mode | P | | — | ±0.25 | ±1.0 | |
| | 8-bit mode | P | | — | ±0.65 | ±1.0 | |
| Full-scale error[6] | 12-bit mode | T | $E_{FS}$ | — | ±2.5 | — | LSB[3] |
| | 10-bit mode | T | | — | ±0.5 | ±1.0 | |
| | 8-bit mode | T | | — | ±0.5 | ±1.0 | |
| Quantization error | ≤12 bit modes | D | $E_Q$ | — | — | ±0.5 | LSB[3] |
| Input leakage error[7] | all modes | D | $E_{IL}$ | $I_{In}$ * $R_{AS}$ | | | mV |
| Temp sensor slope | -40°C– 25°C | D | m | — | 3.266 | — | mV/°C |
| | 25°C– 125°C | | | — | 3.638 | — | |
| Temp sensor voltage | 25°C | D | $V_{TEMP25}$ | — | 1.396 | — | V |

1. Typical values assume $V_{DDA}$ = 5.0 V, Temp = 25°C, $f_{ADCK}$=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization
3. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
4. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
5. $V_{ADIN} = V_{SSA}$
6. $V_{ADIN} = V_{DDA}$
7. $I_{In}$ = leakage current (refer to DC characteristics)

### 6.3.2 Analog comparator (ACMP) electricals

**Table 13. Comparator electrical specifications**

| C | Characteristic | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| D | Supply voltage | $V_{DDA}$ | 2.7 | — | 5.5 | V |
| T | Supply current (Operation mode) | $I_{DDA}$ | — | 10 | 20 | µA |
| D | Analog input voltage | $V_{AIN}$ | $V_{SS}$ - 0.3 | — | $V_{DDA}$ | V |
| P | Analog input offset voltage | $V_{AIO}$ | — | — | 40 | mV |
| C | Analog comparator hysteresis (HYST=0) | $V_H$ | — | 15 | 20 | mV |
| C | Analog comparator hysteresis (HYST=1) | $V_H$ | — | 20 | 30 | mV |
| T | Supply current (Off mode) | $I_{DDAOFF}$ | — | 60 | — | nA |
| C | Propagation Delay | $t_D$ | — | 0.4 | 1 | µs |

## 6.4 Communication interfaces

### 6.4.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20% $V_{DD}$ and 70% $V_{DD}$, unless noted, and 100 pF load on all SPI pins. All timing assumes slew rate control is disabled and high drive strength is enabled for SPI output pins.

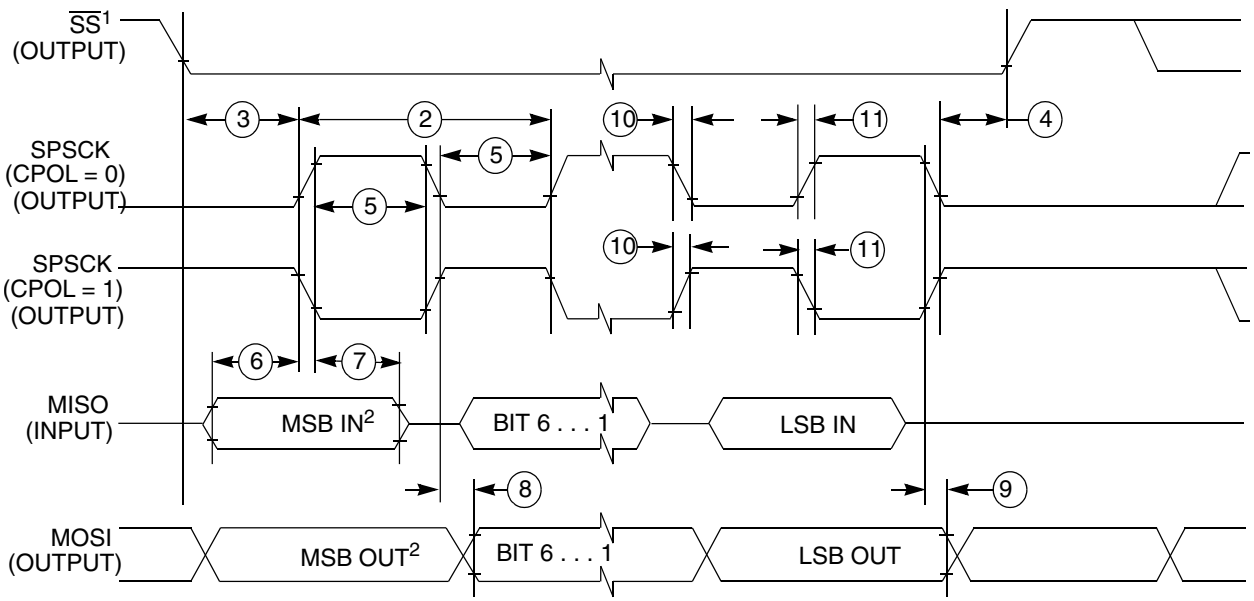
**Table 14. SPI master mode timing**

| Num. | Symbol | Description | Min. | Max. | Unit | Comment |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | $f_{Bus}$/2048 | $f_{Bus}$/2 | Hz | $f_{Bus}$ is the bus clock |
| 2 | $t_{SPSCK}$ | SPSCK period | 2 x $t_{Bus}$ | 2048 x $t_{Bus}$ | ns | $t_{Bus} = 1/f_{Bus}$ |
| 3 | $t_{Lead}$ | Enable lead time | 1/2 | — | $t_{SPSCK}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1/2 | — | $t_{SPSCK}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{Bus}$ - 30 | 1024 x $t_{Bus}$ | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 15 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 0 | — | ns | — |
| 8 | $t_v$ | Data valid (after SPSCK edge) | — | 25 | ns | — |
| 9 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |

*Table continues on the next page...*

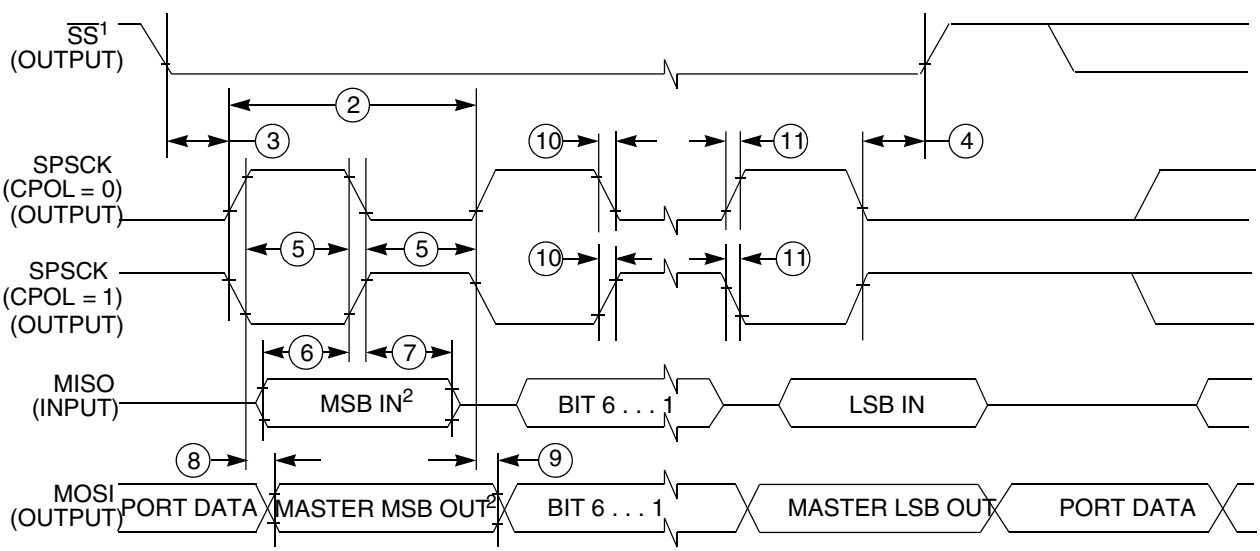
**Table 14. SPI master mode timing (continued)**

| Num. | Symbol | Description | Min. | Max. | Unit | Comment |
|---|---|---|---|---|---|---|
| 10 | $t_{RI}$ | Rise time input | — | $t_{Bus}$ - 25 | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 11 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |




1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 13. SPI master mode timing (CPHA=0)**



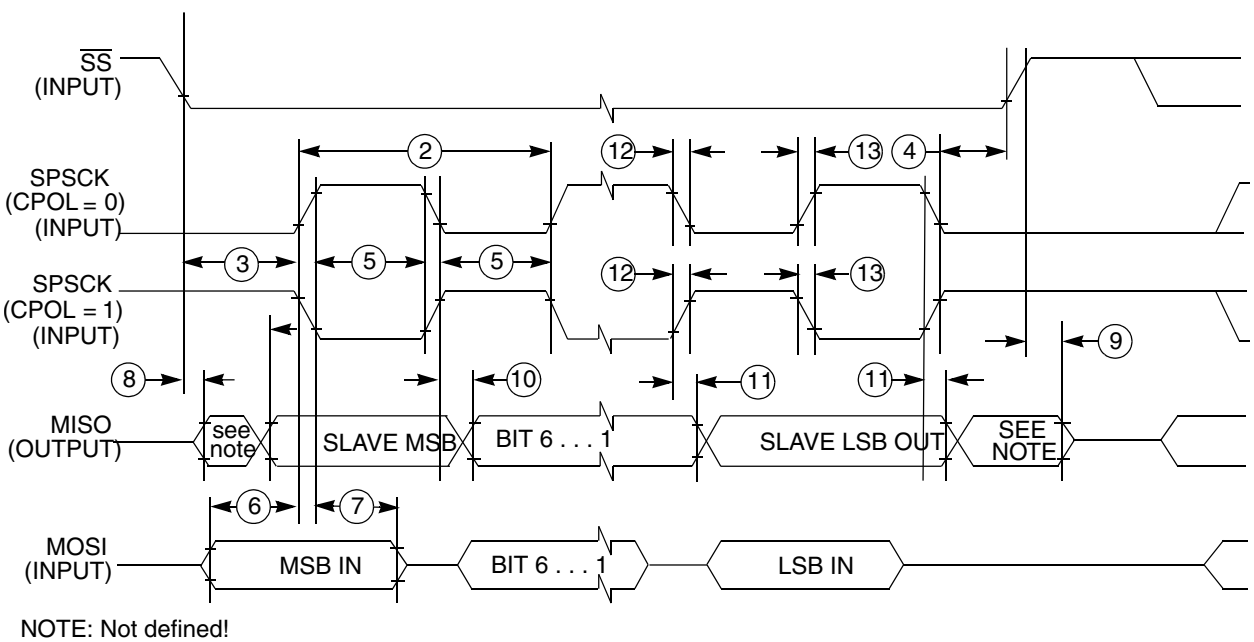

1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 14. SPI master mode timing (CPHA=1)**

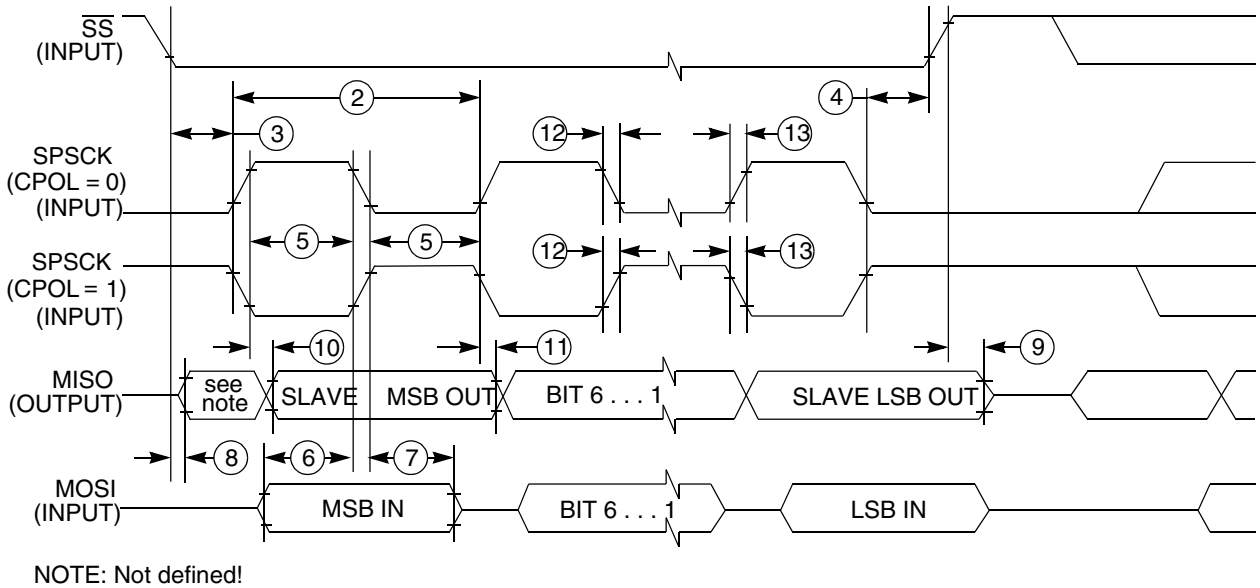
## Table 15. SPI slave mode timing

| Num. | Symbol | Description | Min. | Max. | Unit | Comment |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | 0 | $f_{Bus}/4$ | Hz | $f_{Bus}$ is the bus clock as defined in . |
| 2 | $t_{SPSCK}$ | SPSCK period | 4 x $t_{Bus}$ | — | ns | $t_{Bus} = 1/f_{Bus}$ |
| 3 | $t_{Lead}$ | Enable lead time | 1 | — | $t_{Bus}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1 | — | $t_{Bus}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{Bus}$ - 30 | — | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 15 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 25 | — | ns | — |
| 8 | $t_a$ | Slave access time | — | $t_{Bus}$ | ns | Time to data active from high-impedance state |
| 9 | $t_{dis}$ | Slave MISO disable time | — | $t_{Bus}$ | ns | Hold time to high-impedance state |
| 10 | $t_v$ | Data valid (after SPSCK edge) | — | 25 | ns | — |
| 11 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 12 | $t_{RI}$ | Rise time input | — | $t_{Bus}$ - 25 | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 13 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |




NOTE: Not defined!

**Figure 15. SPI slave mode timing (CPHA = 0)**




NOTE: Not defined!

**Figure 16. SPI slave mode timing (CPHA=1)**

## 6.5 Human-machine interfaces (HMI)

### 6.5.1 TSI electrical specifications

**Table 16. TSI electrical specifications**

| Symbol | Description | Min. | Type | Max | Unit |
|---|---|---|---|---|---|
| TSI_RUNF | Fixed power consumption in run mode | — | 100 | — | µA |
| TSI_RUNV | Variable power consumption in run mode (depends on oscillator's current selection) | 1.0 | — | 128 | µA |
| TSI_EN | Power consumption in enable mode | — | 100 | — | µA |
| TSI_DIS | Power consumption in disable mode | — | 1.2 | — | µA |
| TSI_TEN | TSI analog enable time | — | 66 | — | µs |
| TSI_CREF | TSI reference capacitor | — | 1.0 | — | pF |
| TSI_DVOLT | Voltage variation of VP & VM around nominal values | -10 | — | 10 | % |

# 7 Dimensions

## 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|---|---|
| 16-pin TSSOP | 98ASH70247A |
| 20-pin SOIC | 98ASB42343B |
| 20-pin TSSOP | 98ASH70169A |
| 32-pin LQFP | 98ASH70029A |
| 44-pin LQFP | 98ASS23225W |

# 8 Pinout

## 8.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

**Table 17. Pin availability by package pin-count**

| Pin Number | | | | Lowest Priority <-- --> Highest | | | | |
|---|---|---|---|---|---|---|---|---|
| 44-LQFP | 32-LQFP | 20-TSSOP | 16-TSSOP | Port Pin | Alt 1 | Alt 2 | Alt 3 | Alt 4 |
| 1 | 1 | — | — | PTD1[1] | — | FTM2CH3 | — | — |
| 2 | 2 | — | — | PTD0[1] | — | FTM2CH2 | — | — |
| 3 | — | — | — | PTE4 | — | TCLK2 | — | — |
| 4 | — | — | — | PTE3 | — | BUSOUT | — | — |
| 5 | 3 | 3 | 3 | — | — | — | — | $V_{DD}$ |
| 6 | 4 | — | — | — | — | — | $V_{DDA}$ | $V_{REFH}$ |
| 7 | 5 | — | — | — | — | — | $V_{SSA}$ | $V_{REFL}$ |
| 8 | 6 | 4 | 4 | — | — | — | — | $V_{SS}$ |
| 9 | 7 | 5 | 5 | PTB7 | — | — | SCL | EXTAL |
| 10 | 8 | 6 | 6 | PTB6 | — | — | SDA | XTAL |
| 11 | — | — | — | — | — | — | — | Vss |
| 12 | 9 | 7 | 7 | PTB5[1] | — | FTM2CH5 | SS0 | — |
| 13 | 10 | 8 | 8 | PTB4[1] | — | FTM2CH4 | MISO0 | — |
| 14 | 11 | 9 | — | PTC3 | — | FTM2CH3 | ADP11 | TSI9 |
| 15 | 12 | 10 | — | PTC2 | — | FTM2CH2 | ADP10 | TSI8 |
| 16 | — | — | — | PTD7 | — | — | — | — |
| 17 | — | — | — | PTD6 | — | — | — | — |

*Table continues on the next page...*

**Table 17. Pin availability by package pin-count (continued)**

| Pin Number | | | | Lowest Priority <-- --> Highest | | | | |
|---|---|---|---|---|---|---|---|---|
| 44-LQFP | 32-LQFP | 20-TSSOP | 16-TSSOP | Port Pin | Alt 1 | Alt 2 | Alt 3 | Alt 4 |
| 18 | — | — | — | PTD5 | — | — | — | — |
| 19 | 13 | 11 | — | PTC1 | — | FTM2CH1 | ADP9 | TSI7 |
| 20 | 14 | 12 | — | PTC0 | — | FTM2CH0 | ADP8 | TSI6 |
| 21 | 15 | 13 | 9 | PTB3 | KBI0P7 | MOSI0 | ADP7 | TSI5 |
| 22 | 16 | 14 | 10 | PTB2 | KBI0P6 | SPSCK0 | ADP6 | TSI4 |
| 23 | 17 | 15 | 11 | PTB1 | KBI0P5 | TXD0 | ADP5 | TSI3 |
| 24 | 18 | 16 | 12 | PTB0 | KBI0P4 | RXD0 | ADP4 | TSI2 |
| 25 | 19 | — | — | PTA7 | — | FTM2FAULT2 | ADP3 | TSI1 |
| 26 | 20 | — | — | PTA6 | — | FTM2FAULT1 | ADP2 | TSI0 |
| 27 | — | — | — | — | — | — | — | Vss |
| 28 | — | — | — | — | — | — | — | $V_{DD}$ |
| 29 | — | — | — | PTD4 | — | — | — | — |
| 30 | 21 | — | — | PTD3 | — | — | — | TSI15 |
| 31 | 22 | — | — | PTD2 | — | — | — | TSI14 |
| 32 | 23 | 17 | 13 | PTA3[2] | KBI0P3 | TXD0 | SCL | — |
| 33 | 24 | 18 | 14 | PTA2[2] | KBI0P2 | RXD0 | SDA | — |
| 34 | 25 | 19 | 15 | PTA1 | KBI0P1 | FTM0CH1 | ACMP1 | ADP1 |
| 35 | 26 | 20 | 16 | PTA0 | KBI0P0 | FTM0CH0 | ACMP0 | ADP0 |
| 36 | 27 | — | — | PTC7 | — | TxD1 | — | TSI13 |
| 37 | 28 | — | — | PTC6 | — | RxD1 | — | TSI12 |
| 38 | — | — | — | PTE2 | — | MISO0 | — | — |
| 39 | — | — | — | PTE1 | — | MOSI0 | — | — |
| 40 | — | — | — | PTE0 | — | SPSCK0 | — | — |
| 41 | 29 | — | — | PTC5 | — | FTM0CH1 | — | TSI11 |
| 42 | 30 | — | — | PTC4 | — | FTM0CH0 | — | TSI10 |
| 43 | 31 | 1 | 1 | PTA5 | IRQ | TCLK0 | — | RESET |
| 44 | 32 | 2 | 2 | PTA4 | — | ACMPO | BKGD | MS |

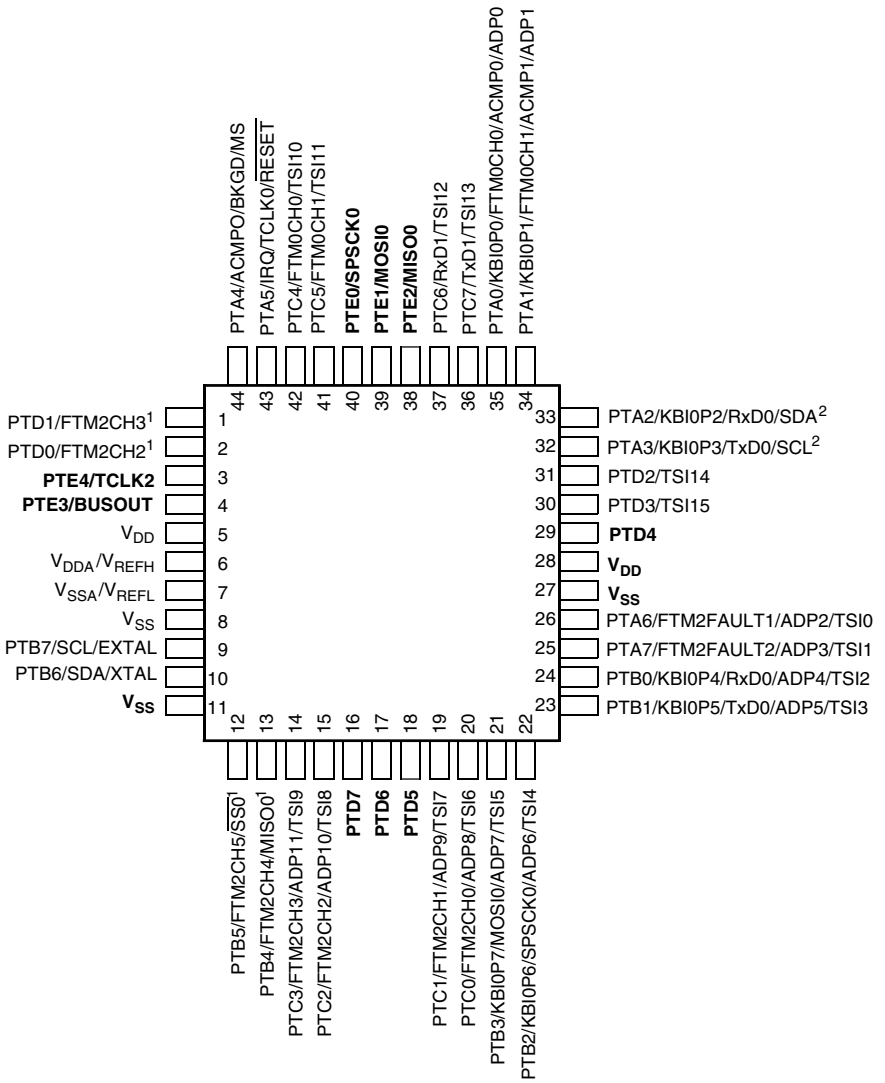
1. This is a high current drive pin when operated as output.
2. This is a true open-drain pin when operated as output.

## Note

When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. The table above illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function

already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

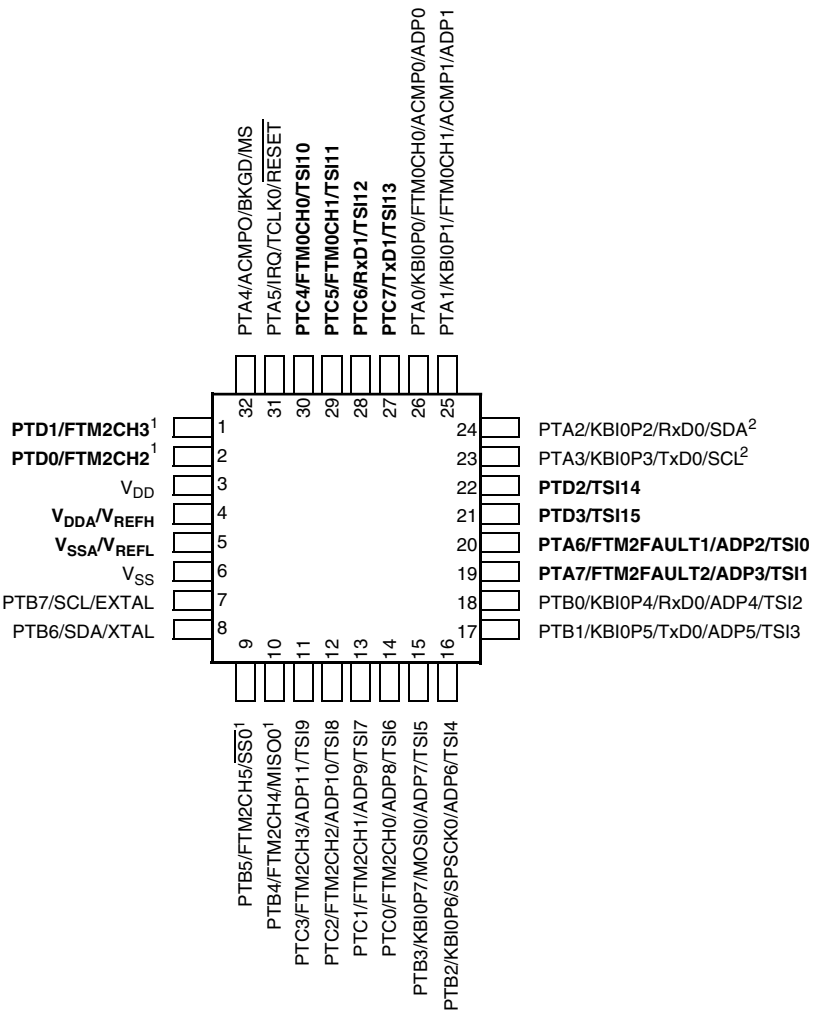
## 8.2 Device pin assignment




Pins in **bold** are not available on less pin-count packages.

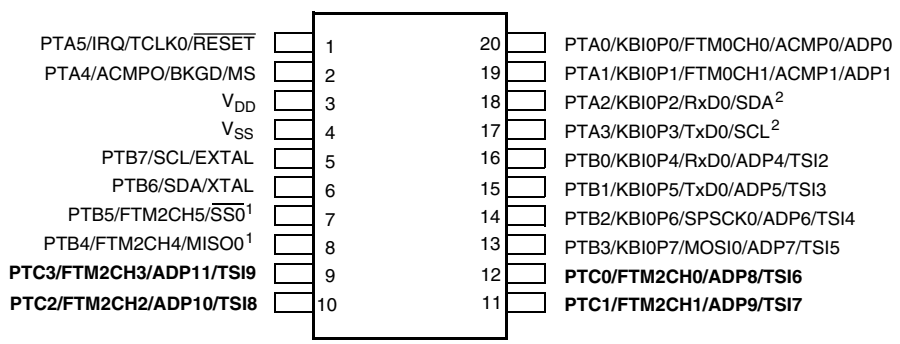
1. High source/sink current pins
2. True open drain pins

**Figure 17. MC9S08PT16 44-pin LQFP package**



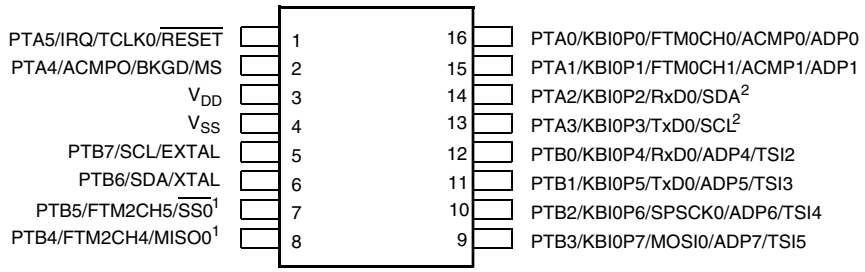

Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

## Figure 18. MC9S08PT16 32-pin LQFP package




Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

## Figure 19. MC9S08PT16 20-pin SOIC and TSSOP package




Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

**Figure 20. MC9S08PT16 16-pin TSSOP package**

# 9 Revision history

The following table provides a revision history for this document.

**Table 18. Revision history**

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| 1 | 7/2012 | Initial public release |

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