To our customers,

Old Company Name in Catalogs and Other Documents

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April 1st, 2010
Renesas Electronics Corporation

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7549 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0202-0202
Rev.2.02
Mar 31, 2009

DESCRIPTION

The 7549 Group is the 8-bit microcomputer based on the 740 family core technology.
The 7549 Group has an 8-bit timer, 16-bit timer, serial interface, A/D converter, power-on reset circuit and the low voltage detection circuit. Also, the Function set ROM is equipped.

FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time ..... 0.25 µs
  (at 8 MHz oscillation frequency, double-speed mode)
- Memory size
  - ROM ..... 2K, 4K, 6K bytes
  - RAM ..... 192/256 bytes
- Programmable I/O ports
  - I/O port 19
  - Output port 1
- Key-on wakeup 8
- LED direct drive port 8
- Interrupts ..... 12 sources, 12 vectors
- Timers ..... 8-bit × 2
  ..... 16-bit × 1
- Output compare ..... 3 channel
- Input capture ..... 1 channel
- Serial interface ..... 8-bit × 1
  (UART or clock synchronous)
- A/D converter ..... 10-bit resolution × 8-channel
- Clock generating circuit ..... Built-in type
  (connect to external ceramic resonator or quartz-crystal oscillator, 32 kHz quartz-crystal oscillation available)
- High-speed on-chip oscillator ..... Typ. : 4 MHz
- Low-speed on-chip oscillator ..... Typ. : 250 kHz
- Watchdog timer ..... 16-bit × 1
- Power-on reset circuit ..... Built-in type
- Low voltage detection circuit ..... Built-in type
- Power source voltage
  XIN oscillation frequency
  (at ceramic resonator, in double-speed mode)
  - At 8 MHz ..... 4.5 to 5.5 V
  - At 2 MHz ..... 2.4 to 5.5 V
  - At 1 MHz ..... 2.2 to 5.5 V

  XIN oscillation frequency
  (at ceramic resonator, in high-speed mode)
  - At 8 MHz ..... 4.0 to 5.5 V
  - At 4 MHz ..... 2.4 to 5.5 V
  - At 1 MHz ..... 1.8 to 5.5 V

  High-speed on-chip oscillator oscillation frequency
  - At 4 MHz ..... 4.0 to 5.5 V

  Low-speed on-chip oscillator oscillation frequency
  - At 250 kHz (typ. value at VCC = 5V) .... 1.8 to 5.5 V
- Power dissipation ..... 30 mW
- Operating temperature range ..... -20 to 85°C

APPLICATION

Office automation equipment, factory automation equipment, home electric appliances, consumer electronics, etc.

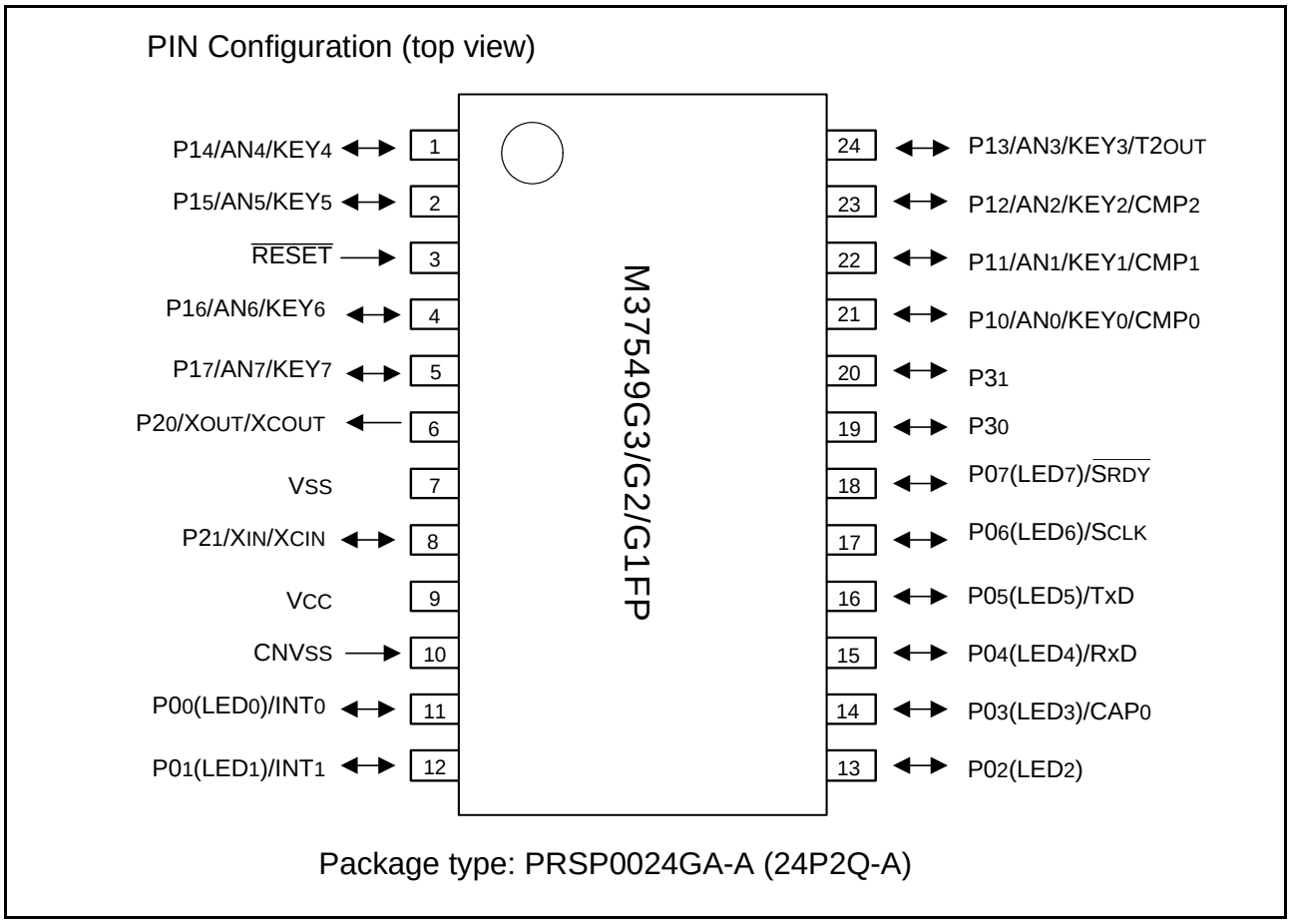


Fig 1. Pin configuration (PRSP0024GA-A type)

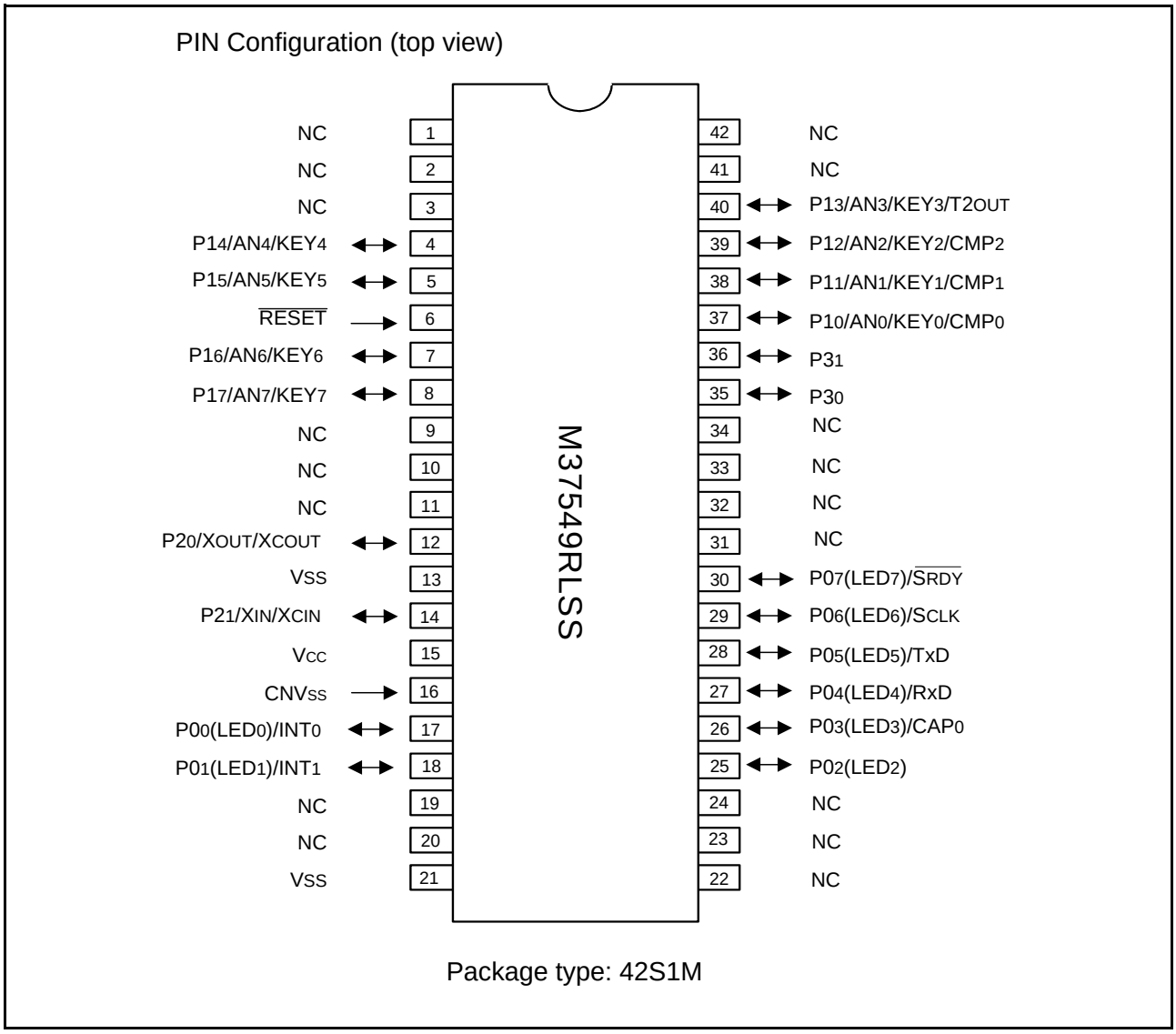


Fig 2. Pin configuration (42S1M type)

PERFORMANCE OVERVIEW

Table 1 Performance overview

Parameter			Function
Number of basic instructions			71
Instruction execution time			0.25 μs (Minimum instruction, oscillation frequency 8MHz, double-speed mode)
Oscillation frequency			8 MHz (Maximum)
Memory sizes	ROM	M37549G1	2K bytes × 8 bits
		M37549G2	4K bytes × 8 bits
		M37549G3	6K bytes × 8 bits
	RAM	M37549G1	192 bytes × 8 bits
		M37549G2	256 bytes × 8 bits
		M37549G3	256 bytes × 8 bits
I/O port	$P0_0$-$P0_7$	I/O	1-bit × 8, LED direct drive ports
	$P1_0$-$P1_7$	I/O	1-bit × 8
	$P2_0$	Output	1-bit × 1
	$P2_1$	I/O	1-bit × 1
	$P3_0$, $P3_1$	I/O	1-bit × 2
Interrupts	Source		12 sources, 12 vectors
Timer			8-bit × 2, 16-bit × 1
Output compare			3-channel
Input capture			1 channel
Serial interface			8-bit × 1 (UART or clock synchronous)
A/D converter			10-bit resolution × 8 channel
Watchdog timer			16-bit × 1
Power-on reset circuit			Built-in
Low voltage detection circuit			Built-in
Clock generating circuit			Built-in (external ceramic resonator or quartz-crystal oscillator, external 32-kHz quartz-crystal oscillator available) (built-in high/low-speed on-chip oscillator)
Function set ROM area	Function set ROM		Function set ROM is assigned to address $FFD8_{16}$ to $FFDA_{16}$. Valid/invalid of low voltage detection circuit can be selected. Oscillation mode can be selected. Enable/disable of watchdog timer and STP instruction can be selected.
	ROM code protect		ROM code protect is assigned to address $FFDB_{16}$. Read/write the built-in QzROM by serial programmer is disabled by setting “00” to ROM code protect.
Power source voltage (at ceramic resonator)	Double-speed mode	at 8 MHz oscillation	4.5 to 5.5 V
		at 2 MHz oscillation	2.4 to 5.5 V
		at 1 MHz oscillation	2.2 to 5.5 V
	High-speed mode	at 8 MHz oscillation	4.0 to 5.5 V
		at 4 MHz oscillation	2.4 to 5.5 V
		at 1 MHz oscillation	1.8 to 5.5 V
Power source voltage (at high-speed on-chip oscillator)	Double-speed mode	at 4 MHz oscillation	4.0 to 5.5 V
Power source voltage (at low-speed on-chip oscillator)	Double-speed mode	at 250 kHz oscillation	1.8 to 5.5 V
Power dissipation			30 mW (Typ.)
Operating temperature range			-20 to 85 °C
Device structure			CMOS silicon gate
Package			24-pin plastic molded SSOP (PRSP0024GA-A)

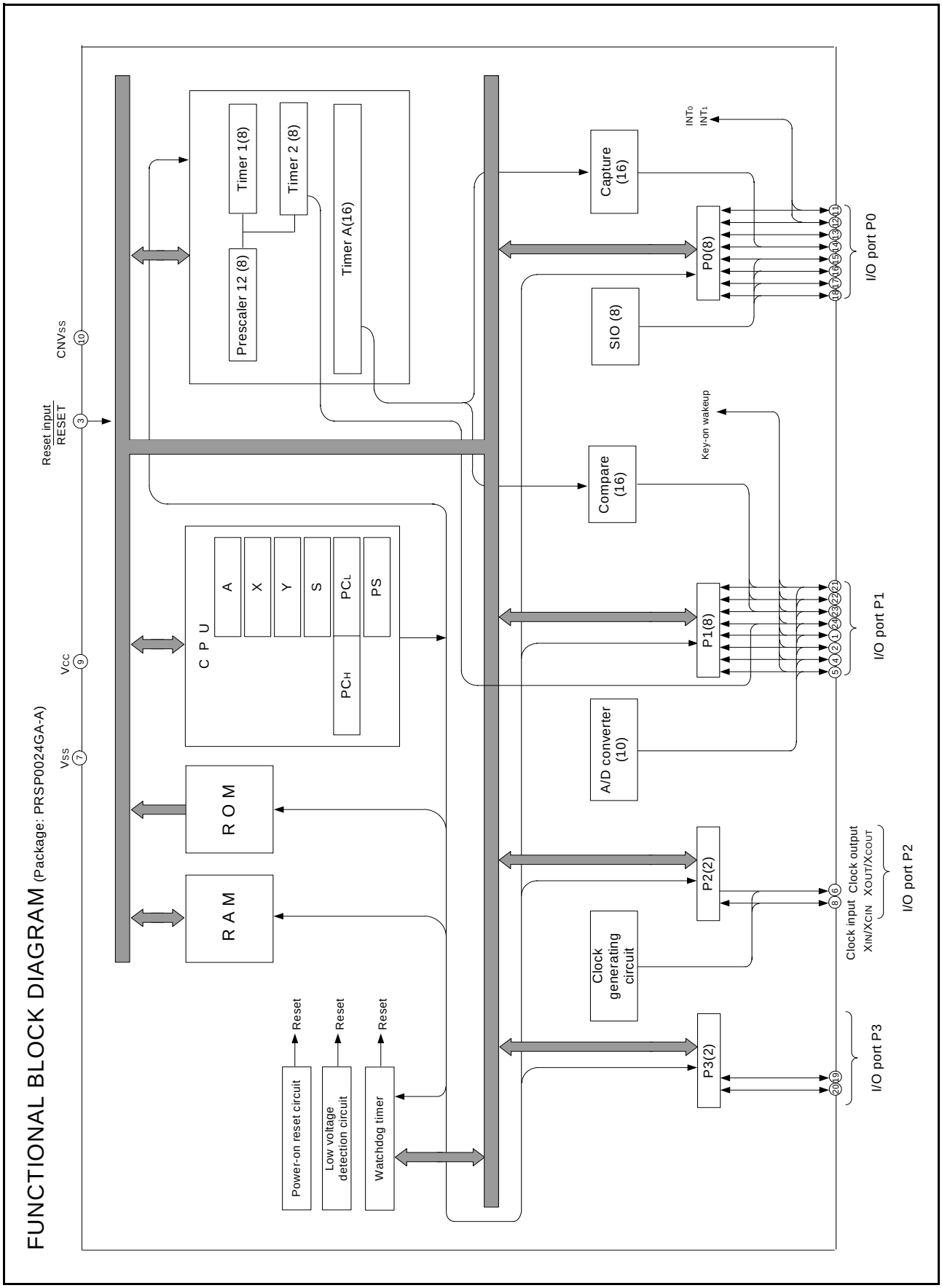


Fig 3. FUNCTIONAL BLOCK DIAGRAM

PIN DESCRIPTION

Table 2 Pin description

Pin	Name	Function	Function except a port function		
V_{CC},V_{SS}	Power source	Apply voltage of 1.8 to 5.5 V to Vcc, and 0 V to Vss.			
CNV_{SS}	CNV_{SS}	Controls the operation mode of the chip. Connected to V_{SS}.			
$\overline{RESET}$	Reset input	Reset input pin for active “L”			
$P0_0$(LED0)/INT_0 $P0_1$(LED1)/INT_1	I/O port P0	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •Whether a built-in pull-up resistor is to be used or not can be determined by program. •High drive capacity for LED drive port can be selected by program.	Interrupt input pin		
$P0_2$(LED2)					
$P0_3$(LED3)/CAP_0			Capture input pin		
$P0_4$(LED4)/R_XD $P0_5$(LED5)/T_XD $P0_6$(LED6)/S_{CLK} $P0_7$(LED7)/$\overline{S_{RDY}}$			Serial interface function pin		
$P1_0$/AN_0/KEY_0/CMP_0 $P1_1$/AN_1/KEY_1/CMP_1 $P1_2$/AN_2/KEY_2/CMP_2	I/O port P1	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •Whether a built-in pull-up resistor is to be used or not can be determined by program.	Input pins for A/D converter	Key-input (key-on wake up interrupt input) pin	Compare output pin
$P1_3$/AN_3/KEY_3/$T2_{OUT}$					Timer 2 output pin
$P1_4$/AN_4/KEY_4 $P1_5$/AN_5/KEY_5 $P1_6$/AN_6/KEY_6 $P1_7$/AN_7/KEY_7					
$P2_0$/X_{OUT}/X_{COUT} $P2_1$/X_{IN}/X_{CIN} (Note)	I/O port P2	•2-bit I/O port. ($P2_0$/X_{OUT}/X_{COUT} is only for output) •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •Function set ROM allows pins to be used as clock pins.	Pins X_{IN} and X_{OUT}, or pins X_{CIN} and X_{COUT}, can be used as clock pins by connecting a ceramic resonator, crystal oscillator, or 32 kHz crystal oscillator between them. Alternately, an external clock may be input to the $P2_0$/X_{OUT}/X_{COUT} pin. In this case, the $P2_1$/X_{IN}/X_{CIN} pin can be used as an I/O port.		
$P3_0$, $P3_1$	I/O port P3	•2-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure			

NOTE:
1. The oscillation circuit is built in the $P2_0$/X_{OUT}/X_{COUT} pin and the $P2_1$/X_{IN}/X_{CIN} pin. When the Vcc of the microcomputer is lower than the operation lower bound voltage even if these pins are used as I/O ports, the oscillation circuit is connected and undefined values may be output from these pins.

GROUP EXPANSION

Renesas plans to expand the 7549 group as follow:

Memory Type

Support for QzROM version and emulator MCU.

Memory Size

- ROM size ..... 2K to 6K bytes
- RAM size ..... 192 to 256 bytes

Packages

- PRSP0024GA-A .... 0.8 mm-pitch 24-pin plastic molded SSOP
- 42S1M ..... 42-pin shrink ceramic PIGGY BACK

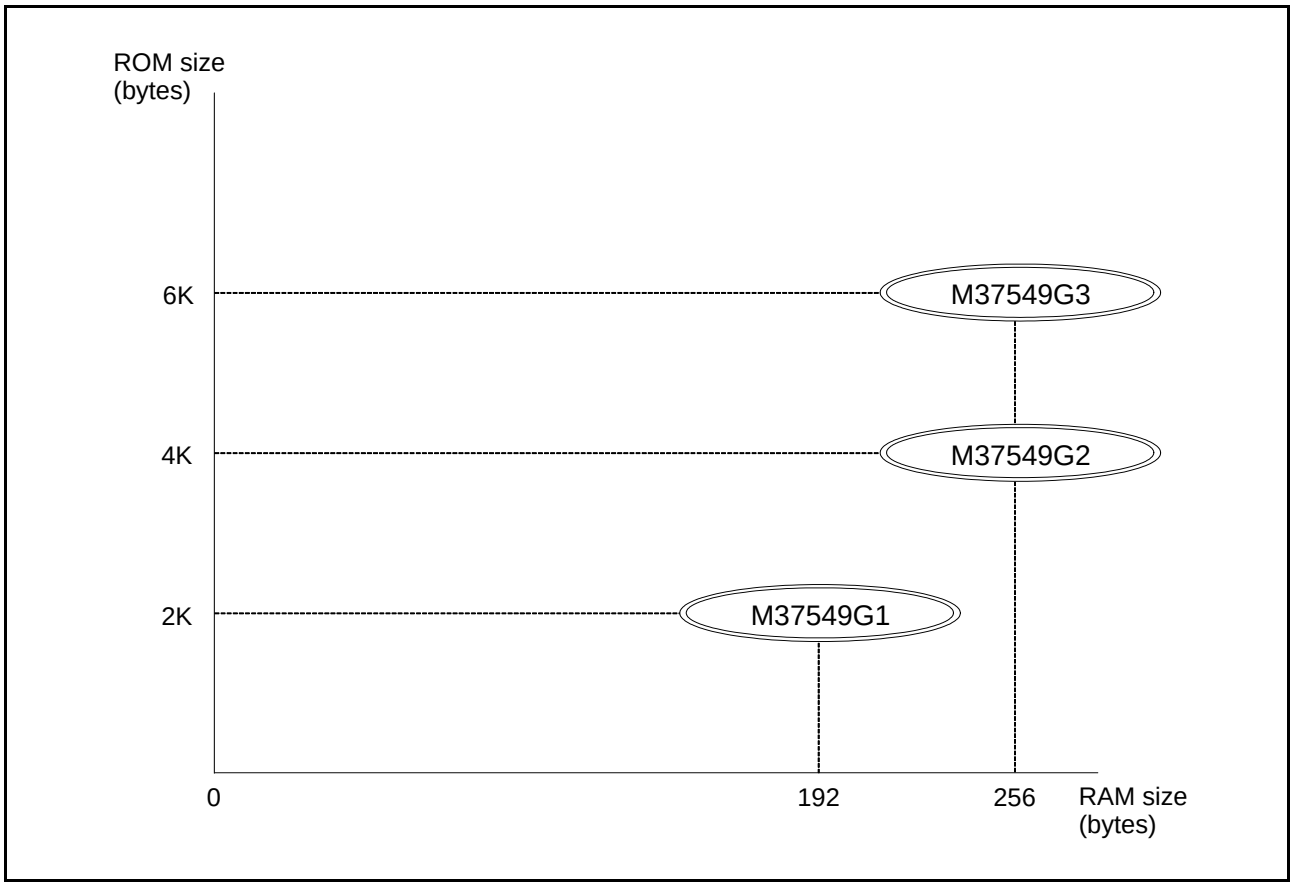


Fig 4. Memory expansion plan

Currently supported products are listed below.

As of Mar. 2009

Table 3 List of supported products

Part number	ROM size (bytes) ROM size for User ()	RAM size (bytes)	Package	Remarks
M37549G3-XXXFP	6144 (6014)	256	PRSP0024GA-A	QzROM version
M37549G3FP				QzROM version (blank)
M37549G2-XXXFP	4096 (3966)	256	PRSP0024GA-A	QzROM version
M37549G2FP				QzROM version (blank)
M37549G1-XXXFP	2048 (1918)	192	PRSP0024GA-A	QzROM version
M37549G1FP				QzROM version (blank)
M37549RLSS	–	256	42S1M	Emulator MCU

NOTE:
1. ROM size includes the function set ROM.

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The MCU uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine-language instructions or the SERIES 740 <SOFTWARE> USER'S MANUAL for details on each instruction set.
Machine-resident 740 family instructions are as follows:

1. The FST and SLW instructions cannot be used.
2. The MUL and DIV instructions can be used.
3. The WIT instruction can be used.
4. The STP instruction can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index register X (X), Index register Y (Y)]

Both index register X and index register Y are 8-bit registers. In the index addressing modes, the value of the OPERAND is added to the contents of register X or register Y and specifies the real address.
When the T flag in the processor status register is set to "1", the value contained in index register X becomes the address for the second OPERAND.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. The stack is used to store the current address data and processor status when branching to subroutines or interrupt routines.
The lower eight bits of the stack address are determined by the contents of the stack pointer. The upper eight bits of the stack address are determined by the Stack Page Selection Bit. If the Stack Page Selection Bit is "0", then the RAM in the zero page is used as the stack area. If the Stack Page Selection Bit is "1", then RAM in page 1 is used as the stack area.
The Stack Page Selection Bit is located in the SFR area in the zero page. Note that the initial value of the Stack Page Selection Bit varies with each microcomputer type. Also some microcomputer types have no Stack Page Selection Bit and the upper eight bits of the stack address are fixed. The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 6.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PCH and PCL. It is used to indicate the address of the next instruction to be executed.

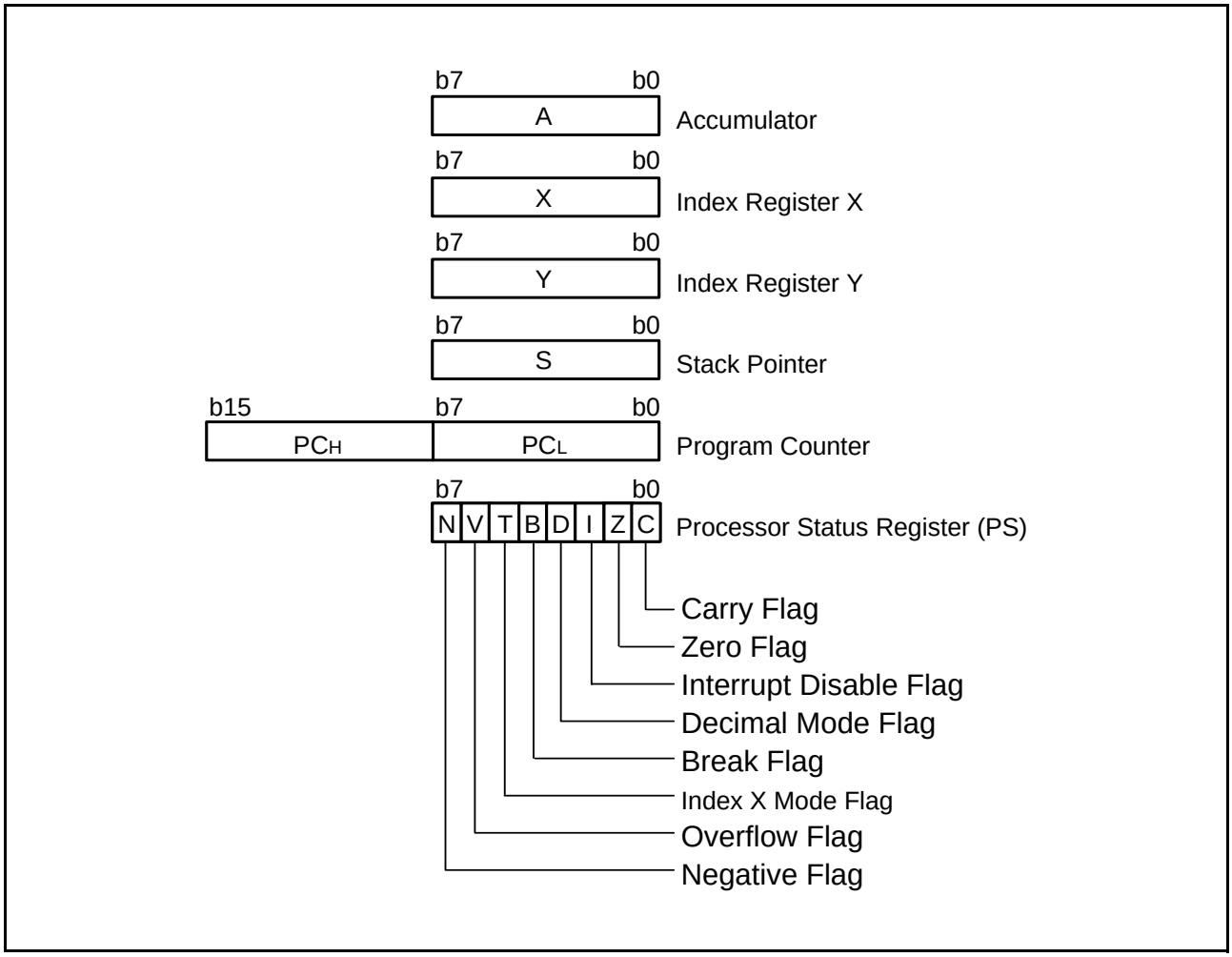


Fig 5. 740 Family CPU register structure

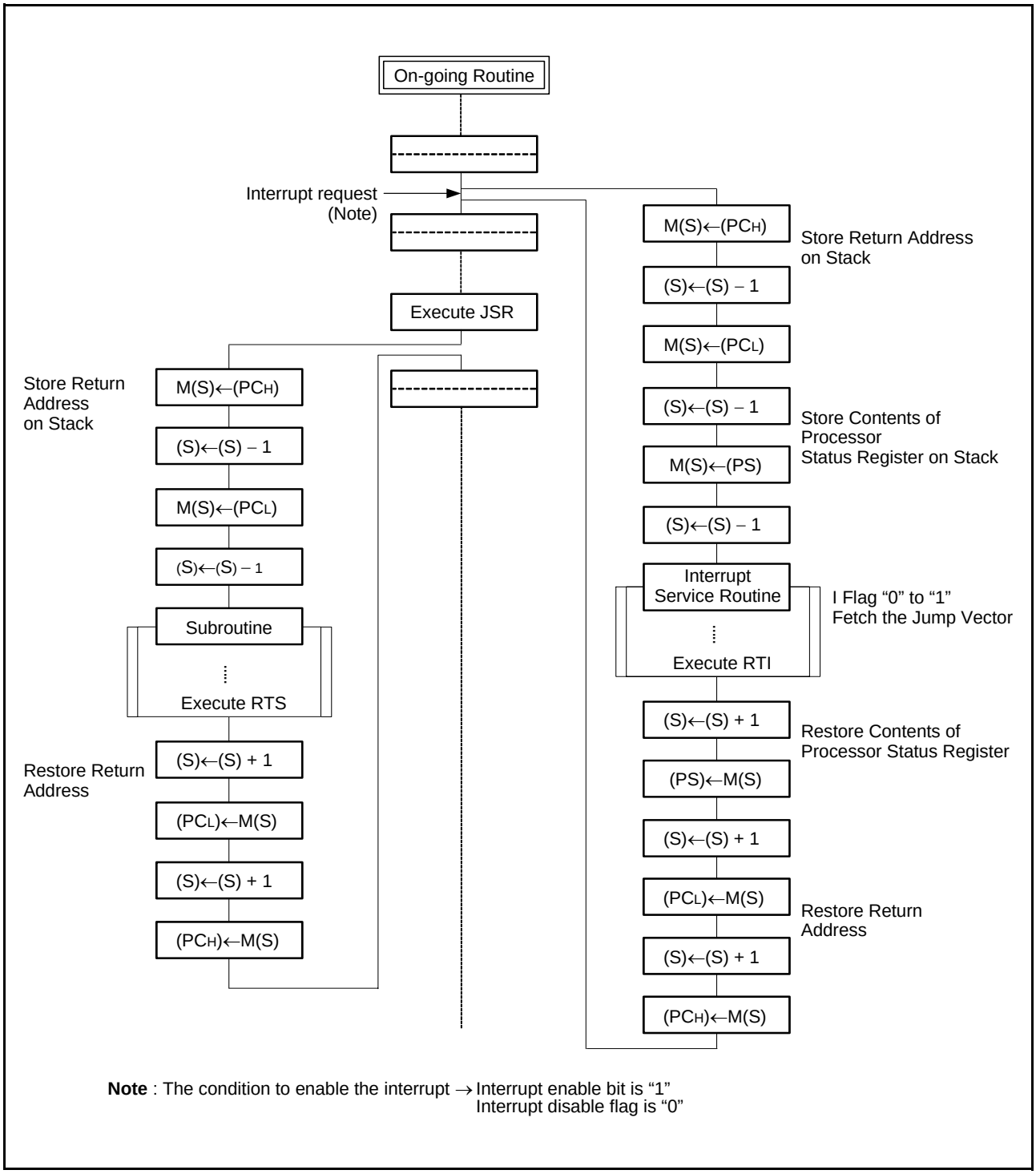


Fig 6. Register push and pop at interrupt generation and subroutine call

Table 4 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of flags which indicate the status of the processor after an arithmetic operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.
After reset, the Interrupt disable (I) flag is set to "1", but all other flags are undefined. Since the Index X mode (T) and Decimal mode (D) flags directly affect arithmetic operations, they should be initialized in the beginning of a program.

Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".

Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction. Interrupts are disabled when the I flag is "1".
When an interrupt occurs, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is serviced.

Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1".
Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1". The saved processor status is the only place where the break flag is ever set.

Bit 5: Index X mode flag (T)

When the T flag is "0", arithmetic operations are performed between accumulator and memory, e.g. the results of an operation between two memory locations is stored in the accumulator. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations, i.e. between memory and memory, memory and I/O, and I/O and I/O. In this case, the result of an arithmetic operation performed on data in memory location 1 and memory location 2 is stored in memory location 1. The address of memory location 1 is specified by index register X, and the address of memory location 2 is specified by normal addressing modes.

Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

Bit 7: Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 5 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU mode register] CPUM

The CPU mode register contains the stack page selection bit.
This register is allocated at address $003B_{16}$.

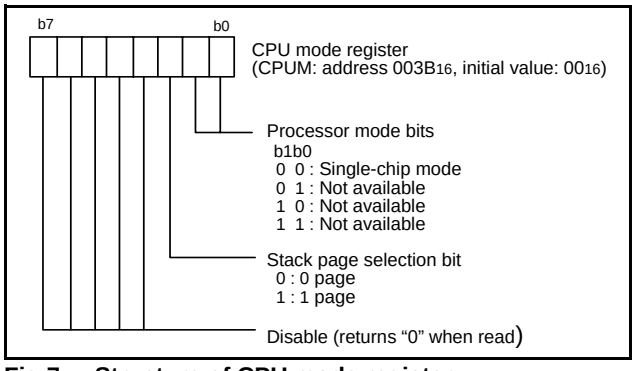


Fig 7. Structure of CPU mode register

The processor mode bits can be written only once after releasing reset. Always set them to "00_2". After written, rewriting any data to these bits is disabled because they are locked. (Emulator MCU is excluded.)
Also, the stack page selection bit (bit 2) is not locked.
In order to prevent error-writing to the processor mode bits (at program runaway), write the CPU mode register at the start of the program that runs after releasing reset.

Memory

• Special Function Register (SFR) Area

The SFR area in the zero page contains control registers such as I/O ports and timers.

• RAM

RAM is used for data storage and for a stack area of subroutine calls and interrupts.

• ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.
The user area includes the function set ROM area.

• Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

• Zero Page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

• Special Page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

• Function set ROM Area

[Renesas shipment test area]

Figure 8 shows the Assignment of Function set ROM area.
The random data are set to the Renesas shipment test areas (addresses $FFD4_{16}$ to address $FFD7_{16}$).
Do not rewrite the data of these areas.
When the checksum is included in the user program, avoid assigning it to these areas.

[Function set ROM data] FSROM0, FSROM1, FSROM2

Function set ROM data 0 to 2 (addresses $FFD8_{16}$ to $FFDA_{16}$) are used to set modes of peripheral functions.
By setting values to these areas, the operation mode of each peripheral function are set after releasing reset.
Refer to the descriptions of peripheral functions for the details of operation of peripheral functions.

- Clock generating circuit (page 46)
- Watchdog timer (page 42)
- Low voltage detection circuit (page 44)

[ROM code protect]

Address $FFDB_{16}$ of QzROM version is ROM code protect address and cannot be used for programming. "00_{16}" is written into this address when selecting the protect bit write by using a serial programmer and selecting protect enabled for writing shipment by Renesas Technology corp.. When "00_{16}" is set to the ROM code protect address, the protect function is enabled, so that reading or writing from/to the corresponding area is disabled by a serial programmer.
As for the QzROM product in blank, the ROM code is protected by selecting the protect bit write at ROM writing with a serial programmer.
As for the QzROM product shipped after writing, "00_{16}" (protect enabled) or "FF_{16}" (protect disabled) is written into the ROM code protect address when Renesas Technology corp. performs writing.
The writing of "00_{16}" or "FF_{16}" can be selected as ROM option setup ("MASK option" written in the mask file converter) when ordering.

<Notes>

(1) Because the contents of RAM are indefinite at reset, set initial values before using.
(2) Do not access to the reserved area.
(3) Random data is written into the Renesas shipment test area and the reserved ROM area. Do not rewrite the data in these areas. Data of these area may be changed without notice. Accordingly, do not include these areas into programs such as checksum of all ROM areas.
(4) The QzROM values in function set ROM data 0 to 2 set the operating modes of the various peripheral functions after an MCU reset is released. Do not fail to set the value for the selected function. Bits designated with a fixed value of 1 or 0 must be set to the designated value.

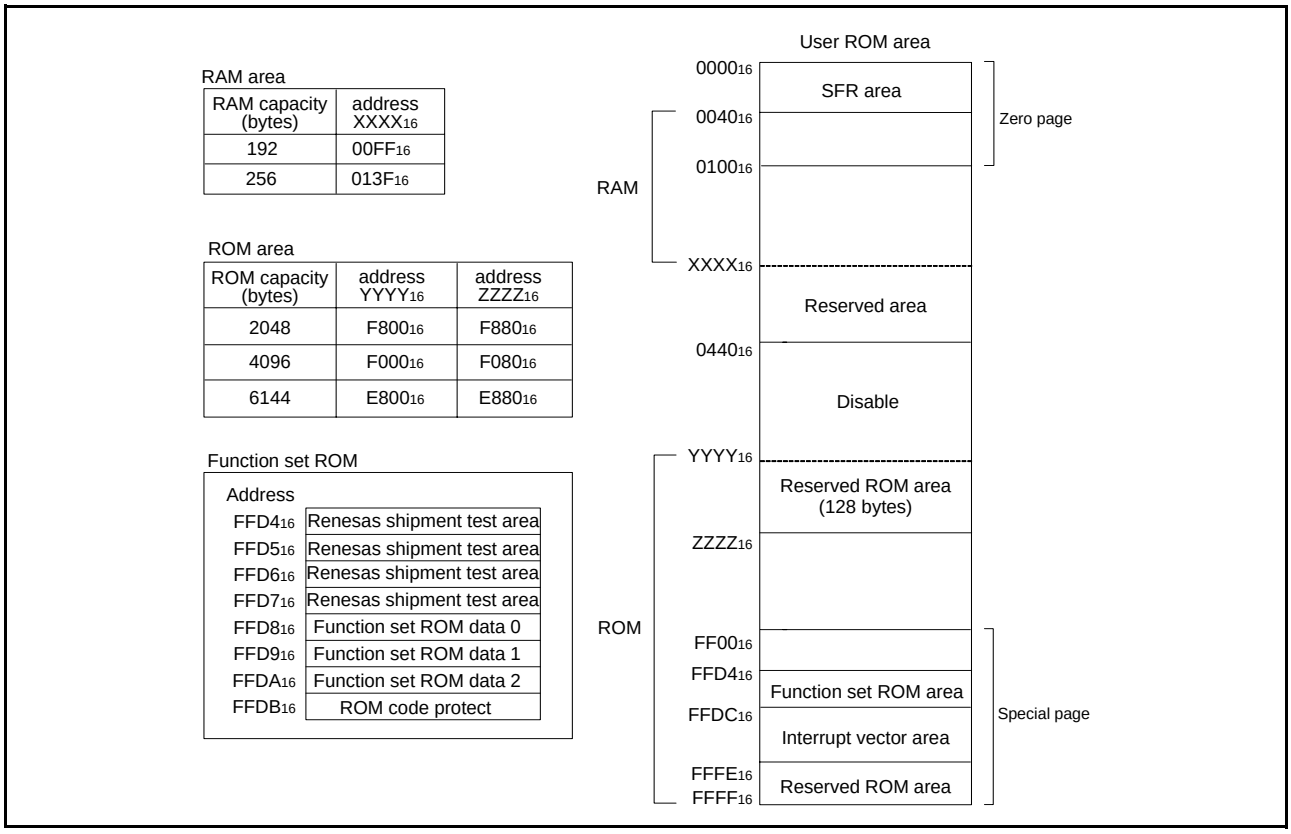


Fig 8. Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	Reserved
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Reserved
0002_{16}	Port P1 (P1)	0022_{16}	Reserved
0003_{16}	Port P1 direction register (P1D)	0023_{16}	Reserved
0004_{16}	Port P2 (P2)	0024_{16}	Reserved
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Reserved
0006_{16}	Port P3 (P3)	0026_{16}	Reserved
0007_{16}	Port P3 direction register (P3D)	0027_{16}	Reserved
0008_{16}	Reserved	0028_{16}	Prescaler 12 (PRE12)
0009_{16}	Reserved	0029_{16}	Timer 1 (T1)
$000A_{16}$	Reserved	$002A_{16}$	Timer 2 (T2)
$000B_{16}$	Reserved	$002B_{16}$	Timer mode register (TM)
$000C_{16}$	Port P0 drive capacity control register (DCCR)	$002C_{16}$	Timer count source set register (TCSS)
$000D_{16}$	Port P0 pull-up control register (PULL0)	$002D_{16}$	Compare register re-load register (CMPR)
$000E_{16}$	Port P1 pull-up control register (PULL1)	$002E_{16}$	Capture/Compare port register (CCPR)
$000F_{16}$	Key-on wakeup input selection register (KEYS)	$002F_{16}$	Capture/Compare status register (CCSR)
0010_{16}	Capture/Compare register (low-order) (CRAL)	0030_{16}	Compare interrupt source set register (CISR)
0011_{16}	Capture/Compare register (high-order) (CRAH)	0031_{16}	Capture software trigger register (CSTR)
0012_{16}	Capture/Compare register RW pointer (CCRP)	0032_{16}	Capture mode register (CAPM)
0013_{16}	Compare output mode register (CMOM)	0033_{16}	Reserved
0014_{16}	Timer A (low-order) (TAL)	0034_{16}	AD control register (ADCON)
0015_{16}	Timer A (high-order) (TAH)	0035_{16}	AD conversion register (low-order) (ADL)
0016_{16}	Reserved	0036_{16}	AD conversion register (high-order) (ADH)
0017_{16}	Reserved	0037_{16}	Clock mode register (CLKM)
0018_{16}	Transmit/Receive buffer register (TB/RB)	0038_{16}	Oscillation stop detection register (CLKSTP)
0019_{16}	Serial I/O status register (SIOSTS)	0039_{16}	Watchdog timer control register (WDTCON)
$001A_{16}$	Serial I/O control register (SIOCON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART control register (UARTCON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator (BRG)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$	Reserved	$003D_{16}$	Interrupt request register 2 (IREQ2)
$001E_{16}$	Reserved	$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$	Reserved	$003F_{16}$	Interrupt control register 2 (ICON2)

Note 1: Do not access to the reserved addresses.

Fig 9. Memory map of special function register (SFR)

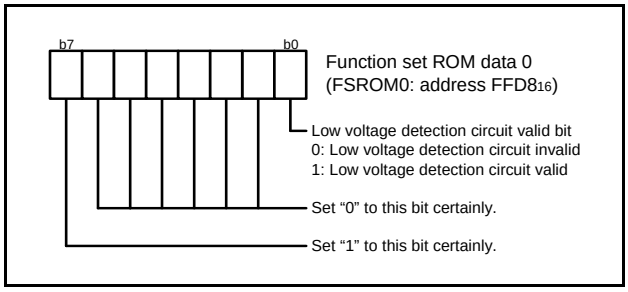
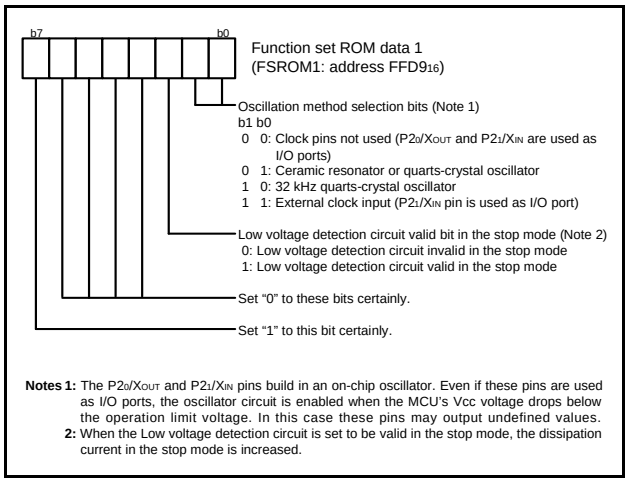
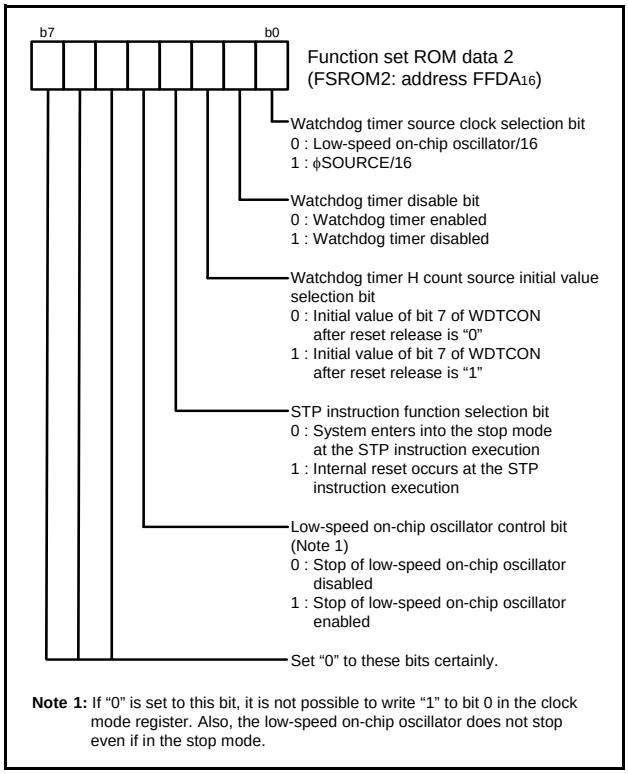


Fig 10. Structure of Function set ROM data 0



Notes 1: The P20/XOUT and P21/XIN pins build in an on-chip oscillator. Even if these pins are used as I/O ports, the oscillator circuit is enabled when the MCU's Vcc voltage drops below the operation limit voltage. In this case these pins may output undefined values.
2: When the Low voltage detection circuit is set to be valid in the stop mode, the dissipation current in the stop mode is increased.

Fig 11. Structure of Function set ROM data 1



Note 1: If “0” is set to this bit, it is not possible to write “1” to bit 0 in the clock mode register. Also, the low-speed on-chip oscillator does not stop even if in the stop mode.

Fig 12. Structure of Function set ROM data 2

I/O Ports

[Direction registers] PiD

The I/O ports have direction registers which determine the input/output direction of each pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input or output.

When "1" is set to the bit corresponding to a pin, this pin becomes an output port. When "0" is set to the bit, the pin becomes an input port.

When data is read from a pin set to output, not the value of the pin itself but the value of port latch is read. Pins set to input are floating, and permit reading pin values.

If a pin set to input is written to, only the port latch is written to and the pin remains floating.

If the port $P2_0$ is used as output port, write "1" to the port $P2_0$ direction register after reset.

[Port P0 drive capacity control register] DCCR

By setting the Port P0 drive capacity control register (address $000C_{16}$), the drive capacity of the N-channel output transistor for the port P0 can be selected.

[Pull-up control registers] PULL0, PULL1

By setting the pull-up control registers (address $000D_{16}$ and $000E_{16}$), ports P0 and P1 can exert pull-up control by program. However, this is valid only when the port direction registers are set to input.

When they are set to output, setting "pull-up on" does not pull up the ports.

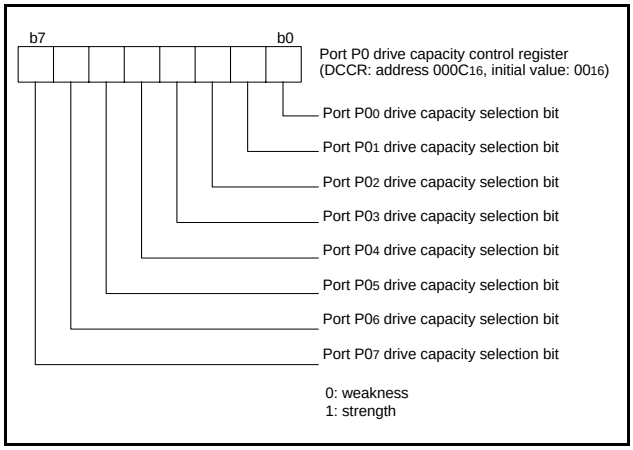


Fig 13. Structure of port P0 drive capacity control register

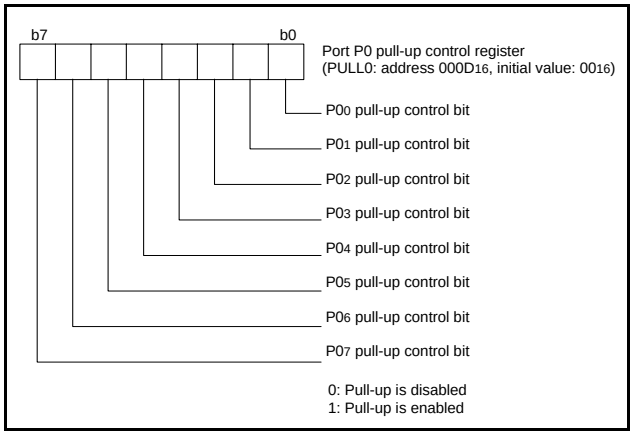


Fig 14. Structure of port P0 pull-up control register

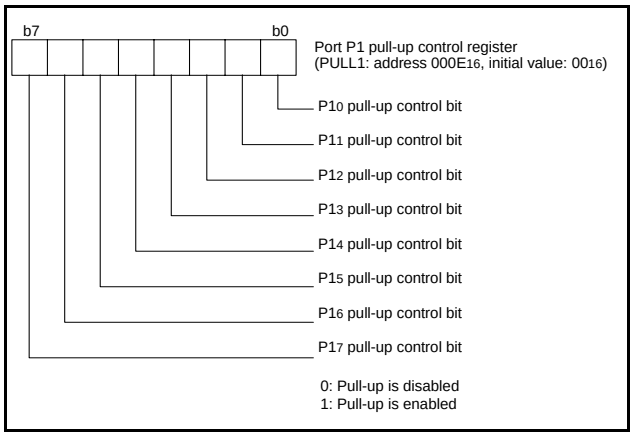


Fig 15. Structure of port P1 control register

Table 6 I/O port function table

Pin	Name	I/O format	Non-port function	SFRs related each pin
$P0_0$(LED_0)/INT_0 $P0_1$(LED_1)/INT_1	I/O port P0	CMOS compatible input level CMOS 3-state output	External interrupt input	Interrupt edge selection register Port P0 drive capacity control register Port P0 pull-up control register
$P0_2$(LED_2)				Port P0 drive capacity control register Port P0 pull-up control register
$P0_3$(LED_3)/CAP_0			Capture input	Capture/Compare port register Port P0 drive capacity control register Port P0 pull-up control register
$P0_4$(LED_4)/RxD			Serial interface input/ output	Serial I/O control register Port P0 drive capacity control register Port P0 pull-up control register
$P0_5$(LED_5)/TxD				Serial I/O control register UART control register Port P0 drive capacity control register Port P0 pull-up control register
$P0_6$(LED_6)/SCLK				Serial I/O control register Port P0 drive capacity control register Port P0 pull-up control register
$P0_7$(LED_7)/$\overline{SRDY}$				Serial I/O control register Port P0 drive capacity control register Port P0 pull-up control register
$P1_0$/AN_0/KEY_0/CMP_0 $P1_1$/AN_1/KEY_1/CMP_1 $P1_2$/AN_2/KEY_2/CMP_2	I/O port P1		Compare output Key input interrupt A/D conversion input	Capture/Compare port register Port P1 pull-up control register Key-on wakeup input selection register AD control register
$P1_3$/AN_3/KEY_3/T2OUT			Timer 2 output Key input interrupt A/D conversion input	Timer mode register Port P1 pull-up control register Key-on wakeup input selection register AD control register
$P1_4$/AN_4/KEY_4 $P1_5$/AN_5/KEY_5 $P1_6$/AN_6/KEY_6 $P1_7$/AN_7/KEY_7			Key input interrupt A/D conversion input	Port P1 pull-up control register Key-on wakeup input selection register AD control register
$P2_0$/XOUT/XCOUT	I/O port P2	CMOS 3-state output	Clock pin	Function set ROM data 1 (Note) Clock mode register
$P2_1$/XIN/XCIN		CMOS compatible input level CMOS 3-state output	Clock pin	Function set ROM data 1 (Note) Clock mode register
$P3_0$ $P3_1$	I/O port P3			

NOTE:
1. Function set ROM data 1 is included in the function set ROM area.

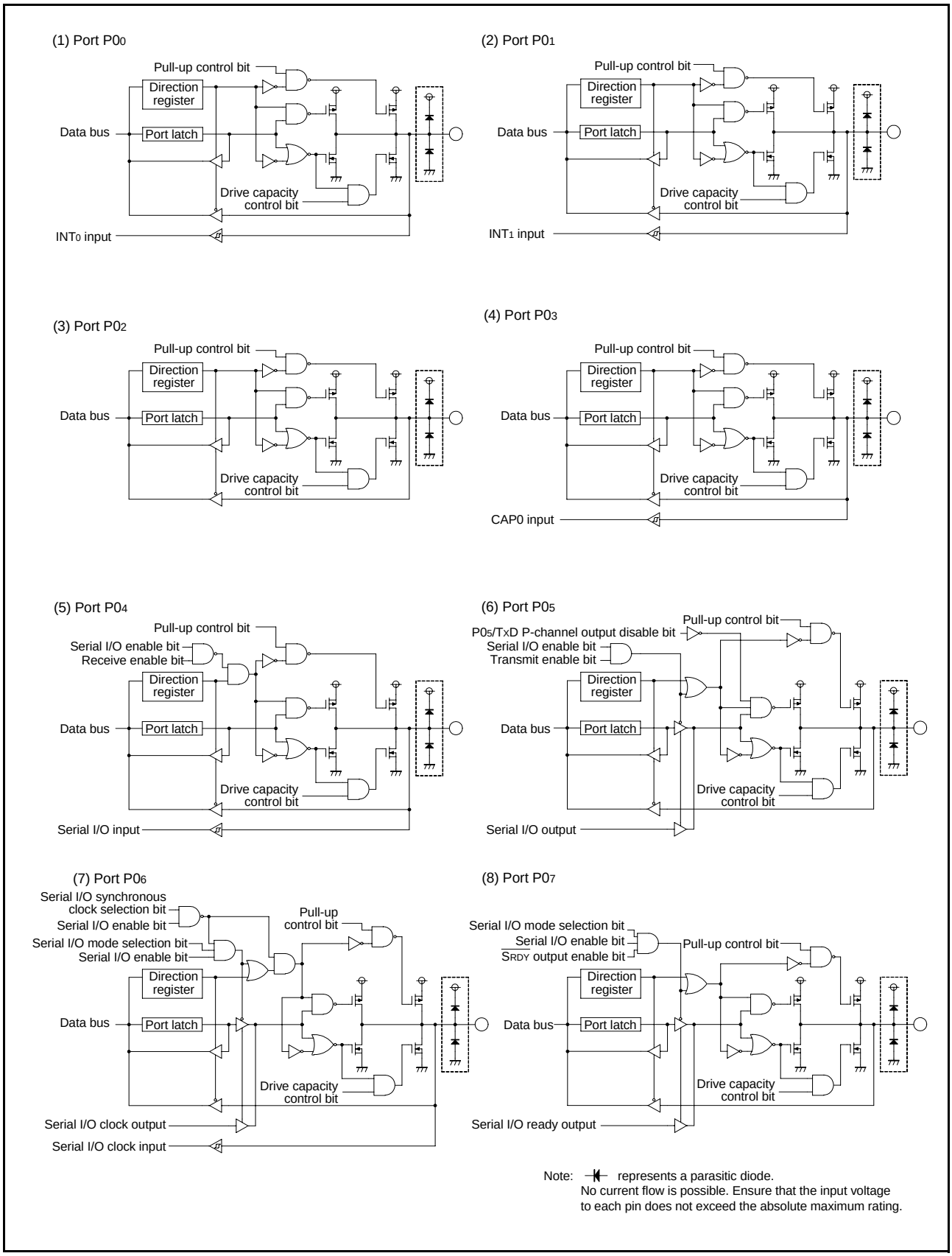


Fig 16. Block diagram of pins (1)

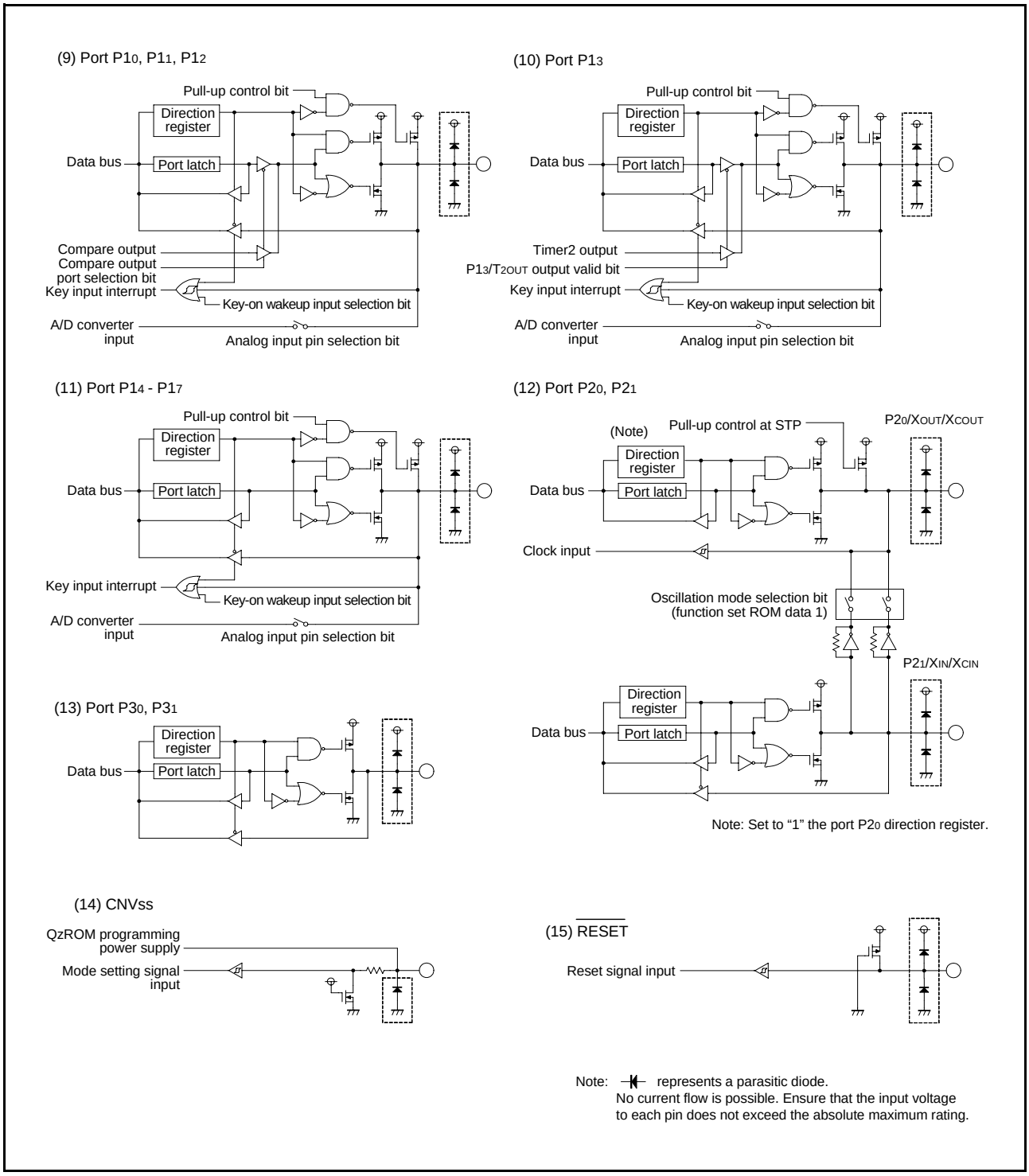


Fig 17. Block diagram of pins (2)

Termination of unused pins

- Termination of common pins

I/O ports: Select an input port or an output port and follow each processing method.

Output ports: Open.

Input ports: If the input level become unstable, through current flow to an input circuit, and the power supply current may increase.
Especially, when expecting low consumption current (at STP or WIT instruction execution etc.), pull-up or pull-down input ports to prevent through current (built-in resistor can be used).
We recommend processing unused pins through a resistor which can secure IOH (avg) or IOL (avg).
Because, when an I/O port or a pin which have an output function is selected as an input port, it may operate as an output port by incorrect operation etc.

Table 7 Termination of unused pins

Pin	Termination
$P0_0/INT_0$	Perform termination of I/O port.
$P0_1/INT_1$	
$P0_2$	
$P0_3$	
$P0_4/RxD$	
$P0_5/TxD$	
$P0_6/SCLK$	
$P0_7/\overline{SRDY}$	
$P1_0/AN_0/KEY_0/CMP_0$	
$P1_1/AN_1/KEY_1/CMP_1$	
$P1_2/AN_2/KEY_2/CMP_2$	
$P1_3/AN_3/KEY_3/T2OUT$	
$P1_4/AN_4/KEY_4$	
$P1_5/AN_5/KEY_5$	
$P1_6/AN_6/KEY_6$	
$P1_7/AN_7/KEY_7$	
$P2_0/XOUT/XCOUT$	Set the direction register to “1”, and perform termination of output port.
$P2_1/XIN/XCIN$	Perform termination of I/O port.
$P3_0$	
$P3_1$	
$\overline{RESET}$	To use the built-in power-on reset circuit, leave the $\overline{RESET}$ pin open.

Interrupts

The 7549 group interrupts are vector interrupts with a fixed priority scheme, and generated by 12 sources: 4 external, 7 internal, and 1 software.

The interrupt sources, vector addresses(1), and interrupt priority are shown in Table 8.

Each interrupt except the BRK instruction interrupt has the interrupt request bit and the interrupt enable bit. These bits and the interrupt disable flag (I flag) control the acceptance of interrupt requests. Figure 18 shows an interrupt control diagram.

An interrupt requests is accepted when all of the following conditions are satisfied:

- Interrupt disable flag.....“0”
- Interrupt request bit.....“1”
- Interrupt enable bit.....“1”

Though the interrupt priority is determined by hardware, priority processing can be performed by software using the above bits and flag.

Table 8 Interrupt vector address and priority

Interrupt source	Priority	Vector addresses (Note 1)		Interrupt request generating conditions	Remarks
		High-order	Low-order		
Reset (Note 2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset input	Non-maskable
Serial I/O receive	2	$FFFB_{16}$	$FFFA_{16}$	At completion of serial I/O data receive	Valid only when serial I/O is selected
Serial I/O transmit	3	$FFF9_{16}$	$FFF8_{16}$	At completion of serial I/O transmit shift or when transmit buffer is empty	Valid only when serial I/O is selected
INT_0	4	$FFF7_{16}$	$FFF6_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1	5	$FFF5_{16}$	$FFF4_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
Key-on wakeup	6	$FFF3_{16}$	$FFF2_{16}$	At falling of conjunction of input logical level for port P1 (at input)	External interrupt (valid at falling edge)
Capture	7	$FFF1_{16}$	$FFF0_{16}$	At detection of either rising or falling edge of Capture 0 input	External interrupt (active edge selectable)
Compare	8	$FFEF_{16}$	$FFEE_{16}$	At compare matched	Compare interrupt source is selected.
Timer A	9	$FFED_{16}$	$FFEC_{16}$	At timer A underflow	
Timer 2	10	$FFEB_{16}$	$FFEA_{16}$	At timer 2 underflow	
A/D conversion	11	$FFE9_{16}$	$FFE8_{16}$	At completion of A/D conversion	
Timer 1	12	$FFE7_{16}$	$FFE6_{16}$	At timer 1 underflow	STP release timer underflow
Not used	13	$FFE5_{16}$	$FFE4_{16}$		
	14	$FFE3_{16}$	$FFE2_{16}$		
	15	$FFE1_{16}$	$FFE0_{16}$		
	16	$FFDF_{16}$	$FFDE_{16}$		
BRK instruction	17	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

NOTES:
1. Vector addressed contain internal jump destination addresses.
2. Reset function in the same way as an interrupt with the highest priority.

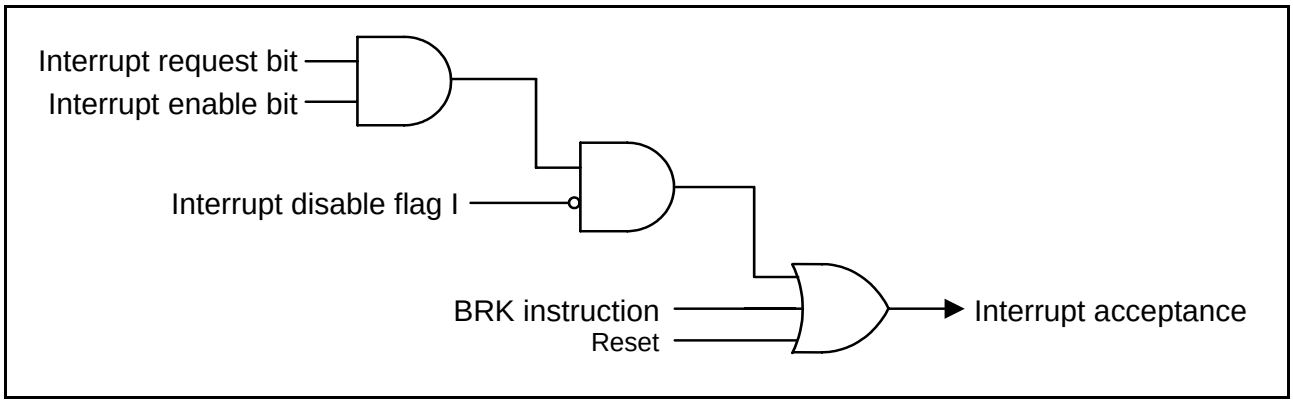


Fig 18. Interrupt control

• Interrupt Disable Flag

The interrupt disable flag is assigned to bit 2 of the processor status register. This flag controls the acceptance of all interrupt requests except for the BRK instruction. When this flag is set to "1", the acceptance of interrupt requests is disabled. When it is set to "0", acceptance of interrupt requests is enabled. This flag is set to "1" with the SET instruction and set to "0" with the CLI instruction.

When an interrupt request is accepted, the contents of the processor status register are pushed onto the stack while the interrupt disable flag remains set to "0". Subsequently, this flag is automatically set to "1" and multiple interrupts are disabled. To use multiple interrupts, set this flag to "0" with the CLI instruction within the interrupt processing routine.

The contents of the processor status register are popped off the stack with the RTI instruction.

• Interrupt Request Bits

Once an interrupt request is generated, the corresponding interrupt request bit is set to "1" and remains "1" until the request is accepted. When the request is accepted, this bit is automatically set to "0".

Each interrupt request bit can be set to "0", but cannot be set to "1", by software.

• Interrupt Enable Bits

The interrupt enable bits control the acceptance of the corresponding interrupt requests. When an interrupt enable bit is set to "0", the acceptance of the corresponding interrupt request is disabled. If an interrupt request occurs in this condition, the corresponding interrupt request bit is set to "1", but the interrupt request is not accepted. When an interrupt enable bit is set to "1", acceptance of the corresponding interrupt request is enabled. Each interrupt enable bit can be set to "0" or "1" by software.

The interrupt enable bit for an unused interrupt should be set to "0".

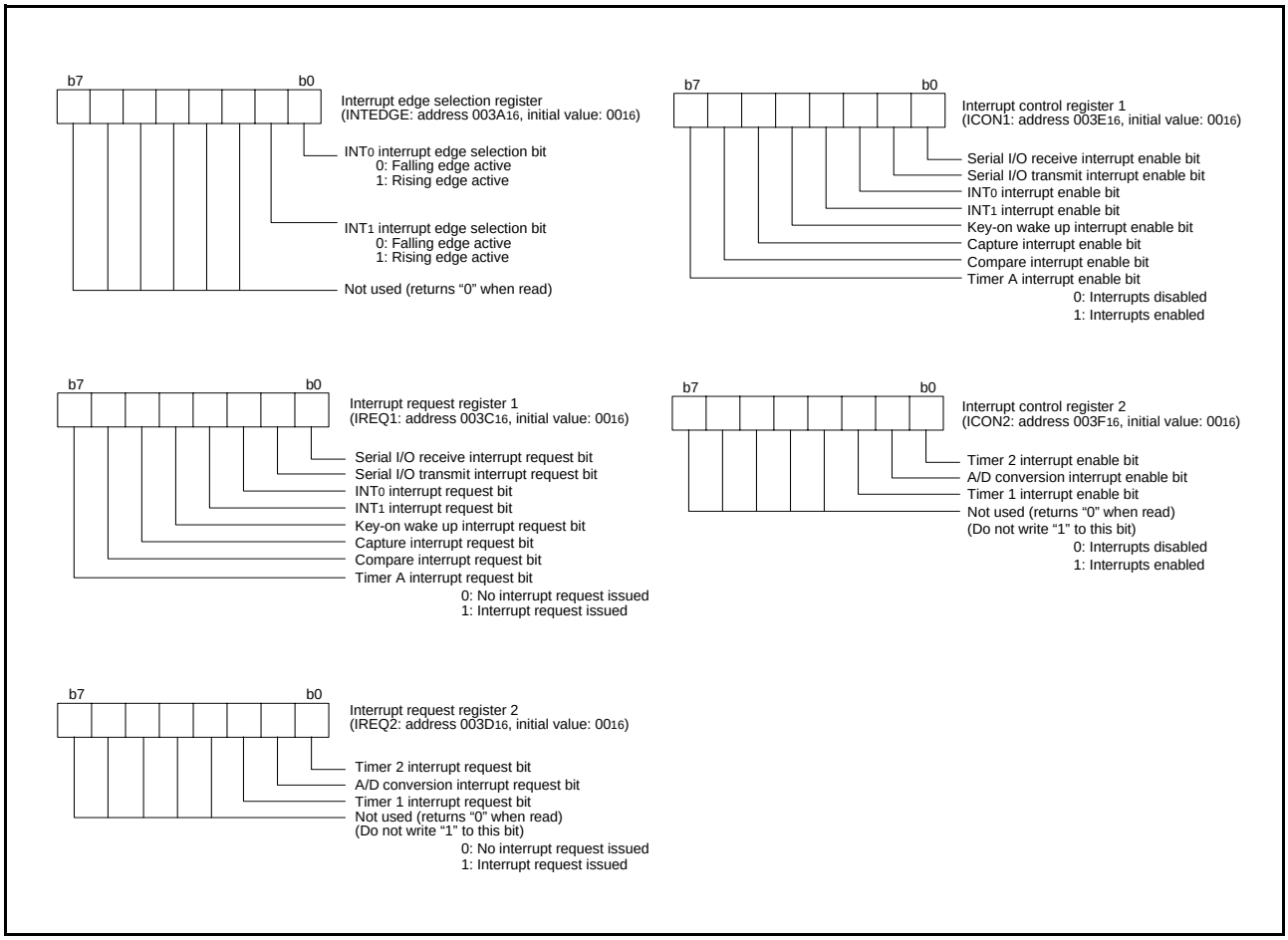


Fig 19. Structure of Interrupt-related registers

• Interrupt Request Generation, Acceptance, and Handling

Interrupts have the following three phases.

(i) Interrupt Request Generation
An interrupt request is generated by an interrupt source (external interrupt signal input, timer underflow, etc.) and the corresponding request bit is set to "1".

(ii) Interrupt Request Acceptance
Based on the interrupt acceptance timing in each instruction cycle, the interrupt control circuit determines acceptance conditions (interrupt request bit, interrupt enable bit, and interrupt disable flag) and interrupt priority levels for accepting interrupt requests. When two or more interrupt requests are generated simultaneously, the highest priority interrupt is accepted. The value of interrupt request bit for an unaccepted interrupt remains the same and acceptance is determined at the next interrupt acceptance timing point.

(iii) Handling of Accepted Interrupt Request
The accepted interrupt request is processed.

Figure 20 shows the time up to execution in the interrupt processing routine, and Figure 21 shows the interrupt sequence. Figure 22 shows the timing of interrupt request generation, interrupt request bit, and interrupt request acceptance.

• Interrupt Handling Execution

When interrupt handling is executed, the following operations are performed automatically.

(1) Once the currently executing instruction is completed, an interrupt request is accepted.

(2) The contents of the program counters and the processor status register at this point are pushed onto the stack area in order from 1 to 3.
1.High-order bits of program counter (PCH)
2.Low-order bits of program counter (PCL)
3.Processor status register (PS)

(3) Concurrently with the push operation, the jump address of the corresponding interrupt (the start address of the interrupt processing routine) is transferred from the interrupt vector to the program counter.

(4) The interrupt request bit for the corresponding interrupt is set to "0". Also, the interrupt disable flag is set to "1" and multiple interrupts are disabled.

(5) The interrupt routine is executed.

(6) When the RTI instruction is executed, the contents of the registers pushed onto the stack area are popped off in the order from 3 to 1. Then, the routine that was before running interrupt processing resumes.

As described above, it is necessary to set the stack pointer and the jump address in the vector area corresponding to each interrupt to execute the interrupt processing routine.

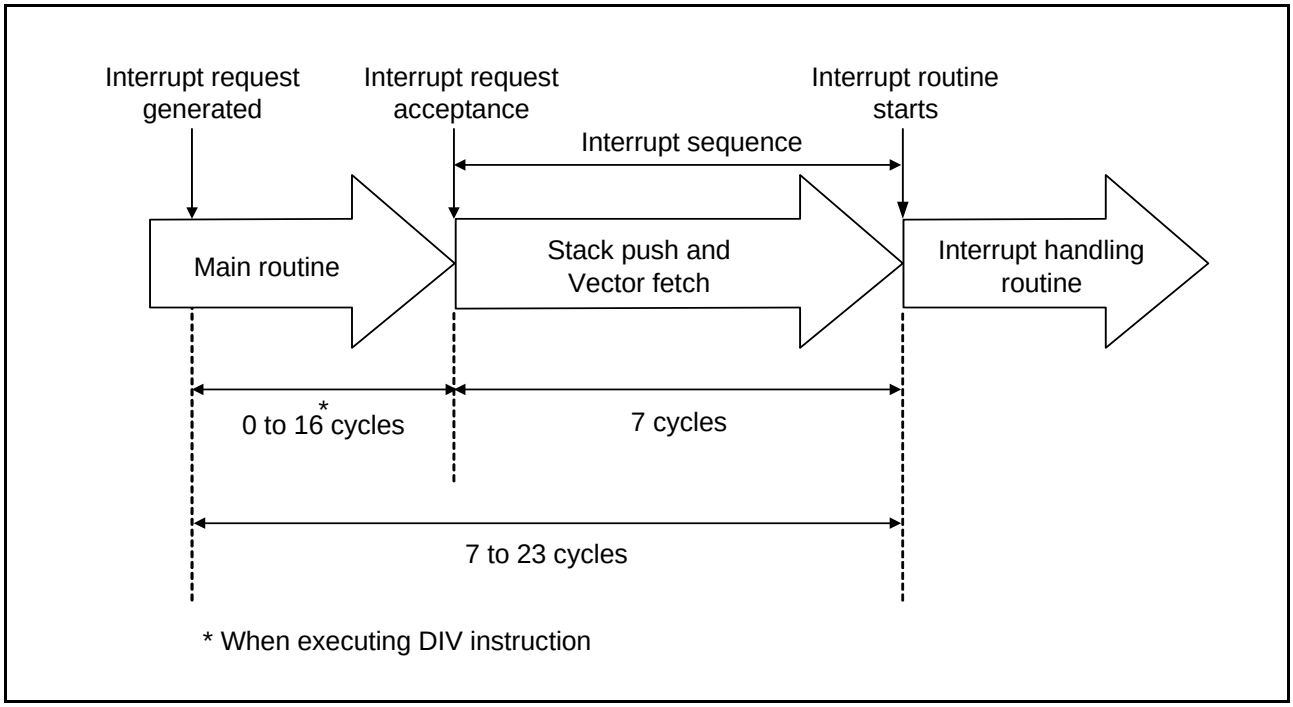
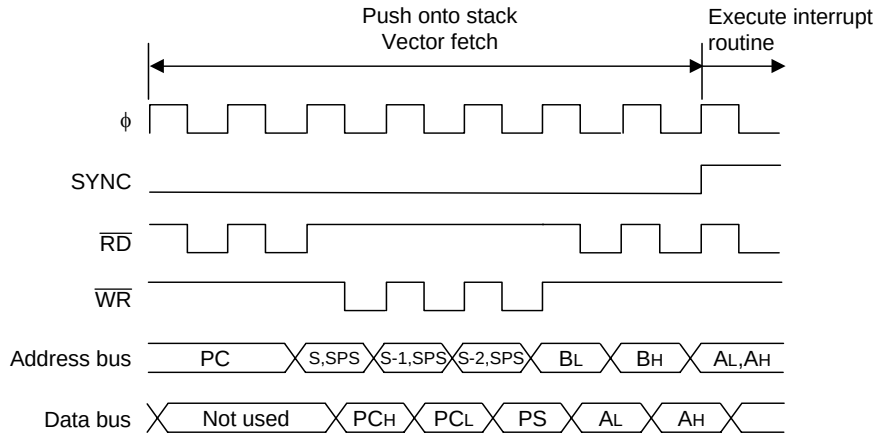
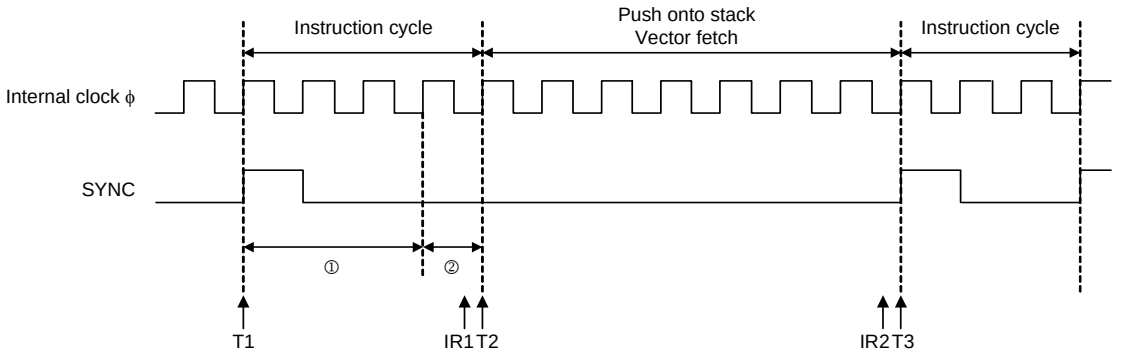


Fig 20. Time up to execution in interrupt routine



SYNC : CPU operation code fetch cycle
(This is an internal signal that cannot be observed from the external unit.)
BL, BH: Vector address of each interrupt
AL, AH: Jump destination address of each interrupt
SPS : "00$_{16}$" or "01$_{16}$"
([SPS] is a page selected by the stack page selection bit of CPU mode register.)

Fig 21. Interrupt sequence



T1 T2 T3 : Interrupt acceptance timing points
IR1 IR2 : Timings points at which the interrupt request bit is set to "1".

Note : Period 2 indicates the last ϕ cycle during one instruction cycle.

(1) The interrupt request bit for an interrupt request generated during period 1 is set to "1" at timing point IR1.
(2) The interrupt request bit for an interrupt request generated during period 2 is set to "1" at timing point IR1 or IR2. The timing point at which the bit is set to "1" varies depending on conditions. When two or more interrupt requests are generated during the period 2, each request bit may be set to "1" at timing point IR1 or IR2 separately.

Fig 22. Timing of interrupt request generation, interrupt request bit, and interrupt acceptance

<Notes>

The interrupt request bit may be set to "1" in the following cases.
<When switching external interrupt active edge>

- INT_0 interrupt edge selection bit
  (bit 0 of Interrupt edge selection register (address 003A$_{16}$))
- INT_1 interrupt edge selection bit
  (bit 1 of Interrupt edge selection register)

If it is not necessary to generate an interrupt synchronized with these settings, take the following sequence.

(1)Set the corresponding enable bit to "0" (disabled).
(2)Set the interrupt edge selection bit (the active edge switch bit) or the interrupt source bit.
(3)Set the corresponding interrupt request bit to "0" after one or more instructions have been executed.
(4)Set the corresponding interrupt enable bit to "1" (enabled).

Key Input Interrupt (Key-On Wakeup)

A key-on wakeup interrupt request is generated by applying "L" level to any pin of port P1 that has been set to input mode. In other words, it is generated when the AND of input level goes from "1" to "0". An example of using a key input interrupt is shown in Figure 23, where an interrupt request is generated by pressing one of the keys provided as an active-low key matrix which uses ports P10 to P13 as input ports.

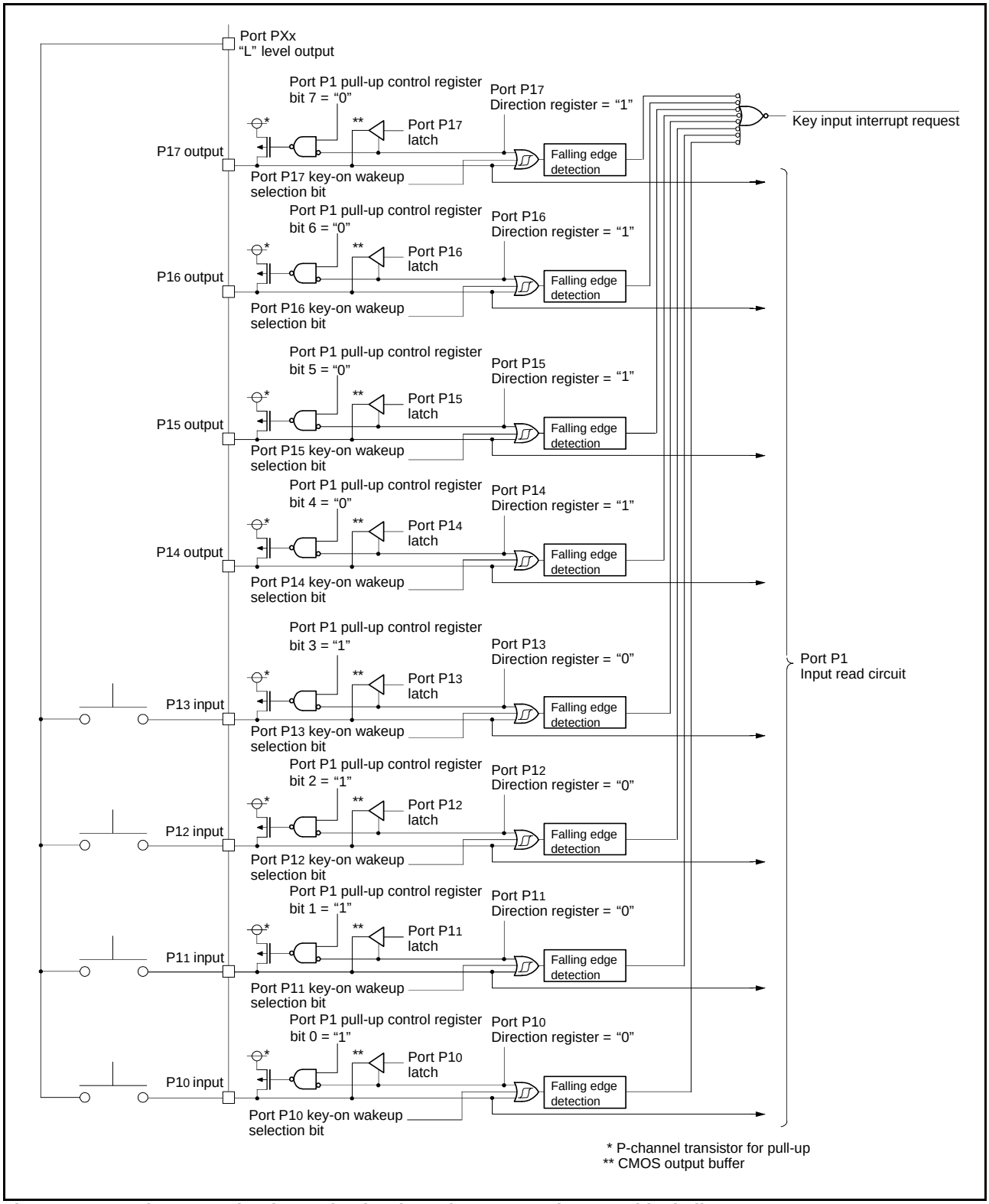


Fig 23. Connection example when using key input interrupt and port P1 block diagram

[Key-on wakeup input selection register] KEYS

Either of enable or disable of key-on wakeup for pins P10 to P15 can be selected by the key-on wakeup input selection bit, respectively.

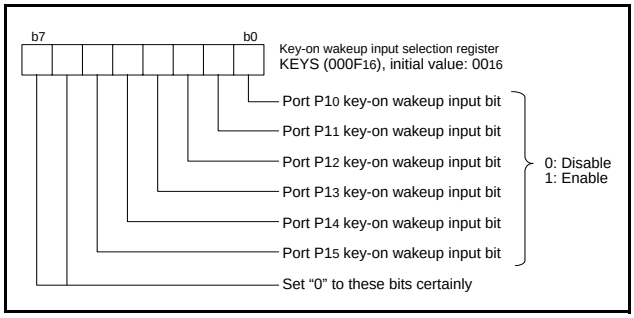


Fig 24. Structure of key input control register

Timers

The 7549 Group has two 8-bit timers (timer 1 and timer 2) and one 16-bit timer (timer A).
Timer 1 and timer 2 share the same 8-bit prescaler (prescaler 12). Each timer and prescaler has a separate timer latch and prescaler latch.
The division ratio of every timer and prescaler is 1/(n+1), where n is the value of the timer latch or prescaler latch.
The timers decrement at each count clock input. When the count value reaches "0", an underflow occurs at the next count pulse. The value of the corresponding timer latch is reloaded into the timer at underflow and counting is continued. When a timer underflow occurs, the interrupt request bit corresponding to each timer is set to "1".

• Prescaler 12 (PRE12)

Prescaler 12 is an 8-bit prescaler that counts the signal selected by the prescaler 12 count source selection bit. The count source can be selected from ϕSOURCE/16 and XCIN input clock.
Writing to prescaler 12 writes the value to both the prescaler latch and prescaler.
Reading from prescaler 12 reads the prescaler 12 count value. The initial value is set to "FF16" after reset.
The division ratio of prescaler 12 is 1/(n+1), where n is the setting value.
Prescaler 12 cannot stop counting by software.

• Timer 1 (T1)

Timer 1 is an 8-bit timer that counts the prescaler 12 output.
When Timer 1 underflows, the timer 1 interrupt request bit is set to "1".
Writing to timer 1 writes the value to both the timer 1 latch and timer 1.
Reading from timer 1 reads the timer 1 count value. The initial value is set to "0116" after reset.
The division ratio of timer 1 is 1/(m+1), where m is the setting value. This gives that the division ratio of prescaler 12 and timer 1 is 1/((n+1) × (m+1)), where n is the prescaler 12 setting value and m is the timer 1 setting value.
Timer 1 cannot stop counting by software.

• Timer 2 (T2)

Timer 2 is an 8-bit timer that counts the signal selected by the timer 2 count source selection bit.
The count source can be selected from among ϕSOURCE/16, /256, prescaler 12 output, and timer A output signal.
Timer 2 counts the selected count source and sets the timer 2 interrupt request bit to "1" at underflow.
When writing to timer 2, the value of the timer 2 write control bit can be used to select a write to both the timer 2 latch and timer 2 or a write to only the timer 2 latch.
Reading from timer 2 reads the timer 2 count value.
Timer 2 starts counting from "FF16" after reset.
The division ratio of timer 2 is 1/(n+1), where n is the timer 2 setting value. Timer 2 stops when the timer 2 count stop bit is set to "1".
When the P13/T2OUT output valid bit is set to "1", the polarity of the waveform output from the P13/T2OUT pin can be inverted at each timer 2 underflow. The output start level of the T2OUT pin can be selected using the T2OUT polarity switch bit. When this bit is set to 0, the output starts at "H" level. When this bit is set to "1", the output starts at "L" level.

• Notes

(1) Reading from and Writing to Timer 1 and 2 and Prescaler 12

If the timer/prescaler count source clock and ϕSOURCE are different clocks, the timers and prescaler cannot be read or written. Select the same clock to enable read and write operations.

Note that timer 2 can be read and written even using a different clock while its counting is stopped.

①Prescaler 12 and timer 1 cannot be read/written in the following conditions:

Prescaler 12 count source: XCIN input clock
ϕSOURCE: Clock other than XCIN input clock

②Timer 2 cannot be read/written during counting in the following conditions:

Timer 2 count source: Prescaler 12
Prescaler 12 count source: XCIN input clock
ϕSOURCE: Clock other than XCIN input clock
or
Timer 2 count source: Timer A underflow
Timer A count source: XCIN input clock
ϕSOURCE: Clock other than XCIN input clock
or
Timer 2 count source: Timer A underflow
Timer A count source: low-speed on-chip oscillator output
ϕSOURCE: Clock other than low-speed on-chip oscillator

(2) Count Source of Prescaler 12

The XCIN input clock can be selected as the prescaler count source only if the 32 kHz quartz crystal oscillator is selected by the oscillation method selection bit in FSROM1.

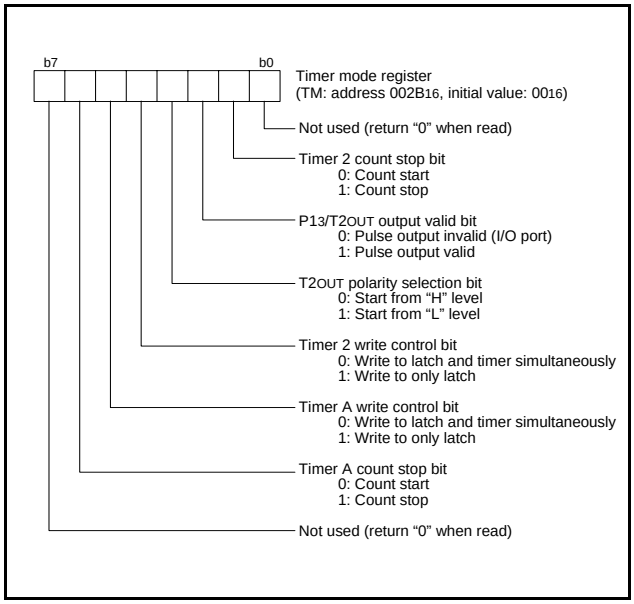


Fig 25. Structure of timer mode register

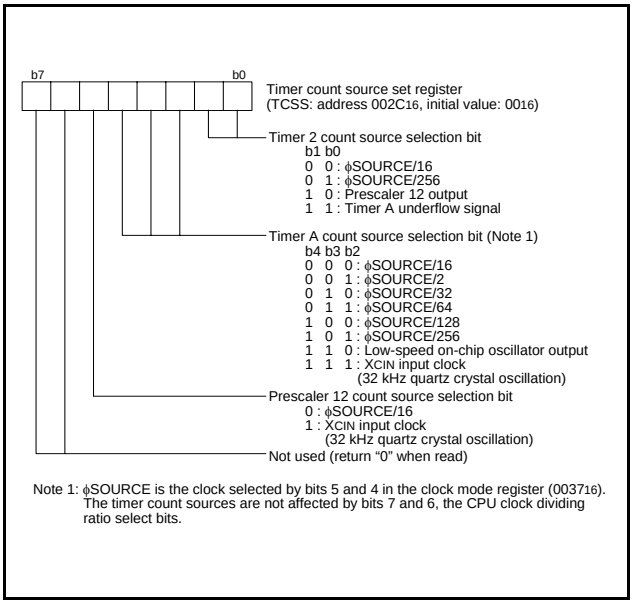


Fig 26. Structure of timer count source set register

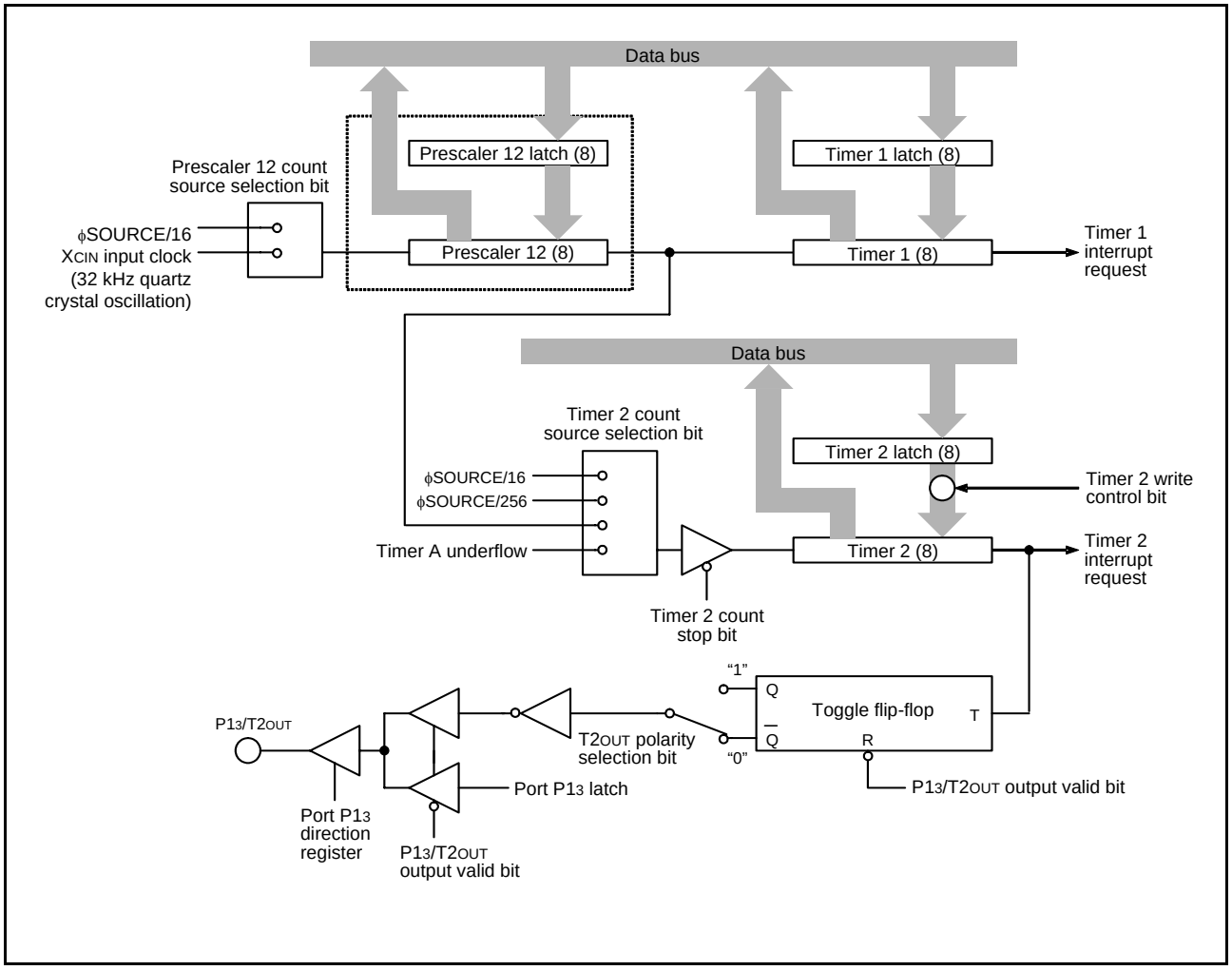


Fig 27. Block diagram of timer 1 and timer 2

Timer A (TA)

Timer A is a 16-bit timer and counts the signal selected by the timer A count source selection bit.
The count source of Timer A can be selected from among ϕSOURCE/2, /16, /32, /64, /128, /256, low-speed on-ship oscillator clock, and XCIN input clock.
Timer A counts the selected count source and sets the timer A interrupt request bit to "1".
When writing to timer A, the setting value of the timer A write control bit can be used to select a write to both the timer A latch and timer or a write to only the timer A latch.
Reading from timer A reads the timer A count value.
Be sure to write to and read from the low-order and the higher order of timer A in the following order:

- Read
  Read the high-order of Timer A (TAH) first, and the low-order of Timer A (TAL) next. Always read both of the registers.
- Write
  Write to the low-order of Timer A (TAL) first and the high-order of Timer A next. Always read both of the registers.

Counting starts from "FFFF16" after reset.
The division ratio of timer A is 1/(n+1), where n is the timer A setting value. Timer A stops when the timer A count stop bit is set to "1".
Timer A can be used as the timing timer for input capture and output compare functions.

• Notes

(1) Timer Value Setting

When the timer A write control bit is set to "write to only latch", written data is written to only to the latch even when the timer is stopped. To set the initial setting value when the timer is stopped, select "Write to timer and latch simultaneously" beforehand.

(2) Reading from and Writing to Timer A

If the timer A count source clock and ϕSOURCE are different clocks, timer A cannot be read or written during its counting. Select the same clock or set timer A to stop counting to enable read and write operations.

- Timer A cannot be read/written in the following conditions:
  Timer A count source: XCIN input clock
  ϕSOURCE: Clock other than XCIN input clock
  or
  Timer A count source: Low-speed on-chip oscillator output
  ϕSOURCE: Clock other than low-speed on-chip oscillator

(3) Count Source of Timer A

The XCIN input clock can be selected as the count source of timer A only if the 32 kHz quartz crystal oscillator is selected by the oscillation method selection bit in FSROM1.

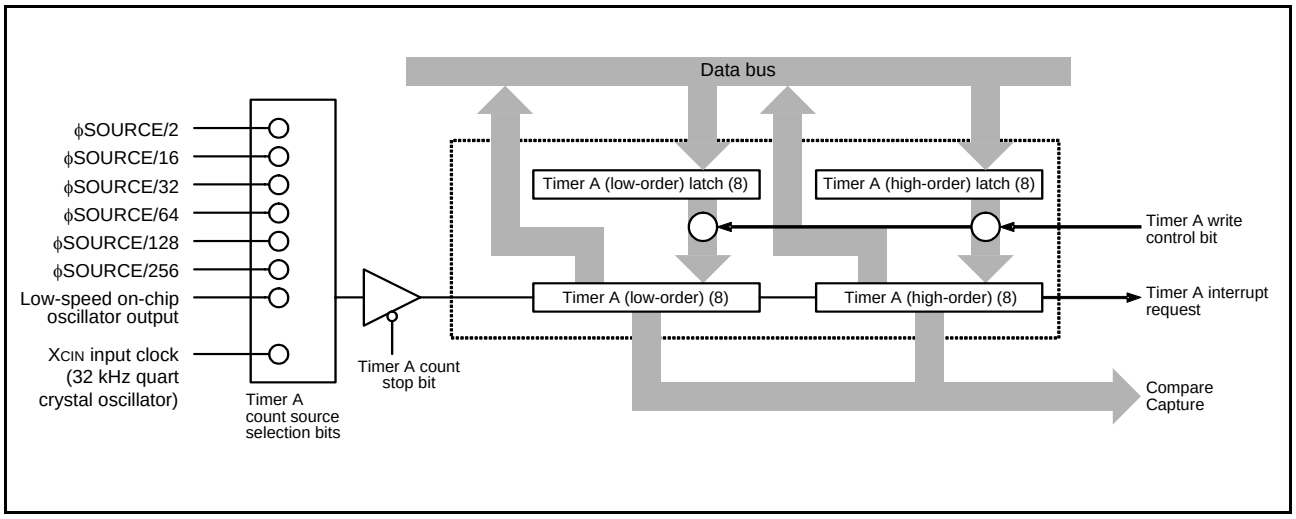


Fig 28. Block diagram of timer A

Output compare

7549 group has 3-output compare channels. Each channel (0 to 2) has the same function and can be used to output waveform by using count value of Timer A.
Three output compare channels share the registers with the input capture (one channel), but their individual circuits operate independently so that all the channels can be used at the same time.

To use each compare channel, set "1" to the compare x (x = 0, 1, 2) output port selection bit and set the port direction register corresponding to compare channel to output mode.
The compare value for each channel is set to the capture/compare register (low-order) and capture/compare register (high-order).
Writing to the register for each channel is controlled by setting value of capture/compare register RW pointer. Writing to each register is in the following order;

1. Set the corresponding compare latch to the capture/compare register RW pointer.
2. Write a value to the capture/compare register (low-order) and capture/compare register (high-order). (It doesn't care even if either low-order or high-order is written early.)
3. Set "1" to the compare latch y (y = 00, 01, 10, 11, 20, 21) re-load bit.

When "1" is set to the compare latch y re-load bit, the value set to the compare register is loaded to compare latch when the next timer underflow.
After loading, re-load bit is set to "0" automatically.

When the count value of timer A matches the compare latch setting value, a trigger to the compare output circuit is generated. The trigger can be enabled or disabled using the compare x trigger enable bit. When the compare x trigger enable bit is set to 1, the output waveform from the port is as follows.

- When the value of the compare x output level latch is "0"
  High level at compare latch x0 match
  Low level at compare latch x1 match
- When the value of the compare x output level latch is "1"
  Low level at compare latch x0 match
  High level at compare latch x1 match

The output waveform does not change if the compare x trigger enable bit is set to 0, so the port output remains fixed at high or low level.
The compare output level of each channel can be confirmed by reading the compare x output status bit.
Compare interrupt is available when match of each compare channel and timer count value. The interrupt request from each channel can be disabled or enabled by setting value of compare latch y interrupt source bit.

• Notes

(1) If timer A is stopped, when a value is written to the capture/compare register it is immediately transferred to the compare latch. In addition, if timer A is stopped and the compare x trigger enable bit is set to "1", the output latch is initialized.

(2) Do not write the same data to both of compare latch x0 and x1.

(3) When setting value of the compare latch is larger than timer setting value, compare match signal is not generated. Accordingly, the output waveform is fixed to "L" or "H" level.
However, when setting value of another compare latch is smaller than timer setting value, this compare match signal is generated. Accordingly, compare interrupt occurs.

(4) When the compare x trigger enable bit is cleared to "0" (disabled), the match trigger to the waveform output circuit is disabled, and the output waveform can be fixed to "L" or "H" level.
However, in this case, the compare match signal is generated.
Accordingly, compare interrupt occurs.

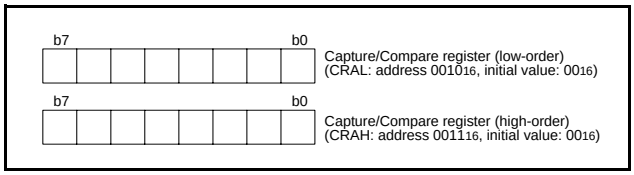


Fig 29. Structure of capture/compare register

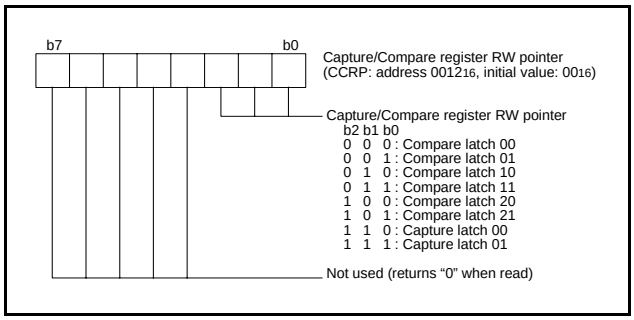


Fig 30. Structure of capture/compare register RW pointer

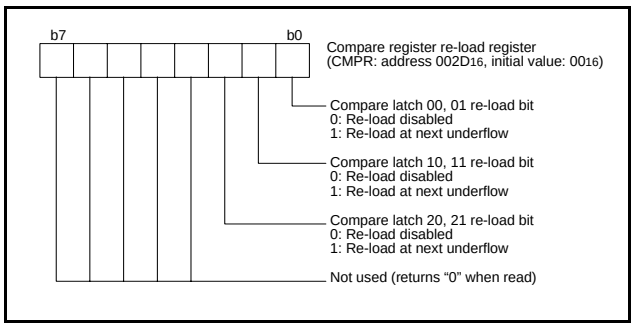


Fig 31. Structure of compare register re-load register

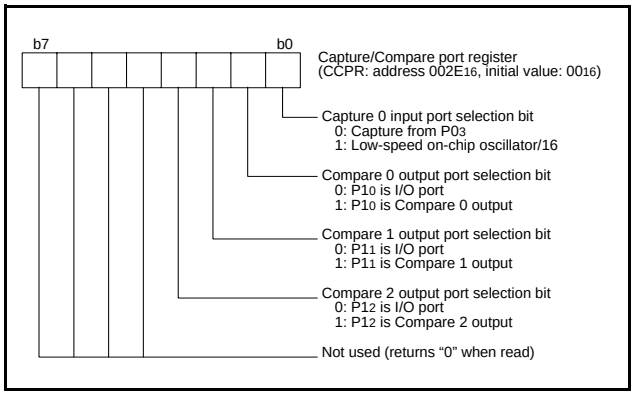


Fig 32. Structure of capture/compare port register

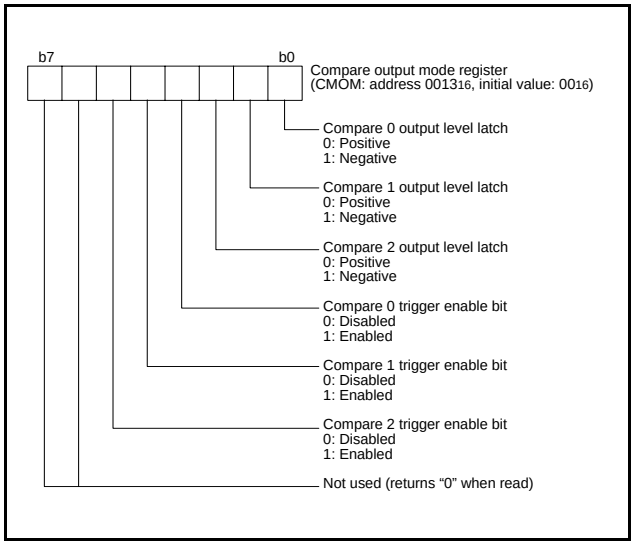


Fig 33. Structure of compare output mode register

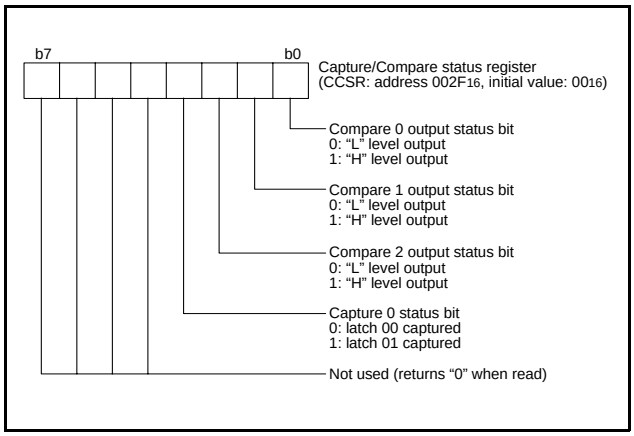


Fig 34. Structure of capture/compare status register

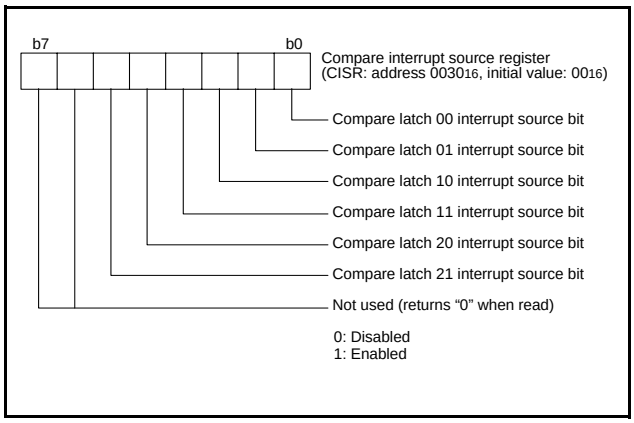


Fig 35. Structure of compare interrupt source register

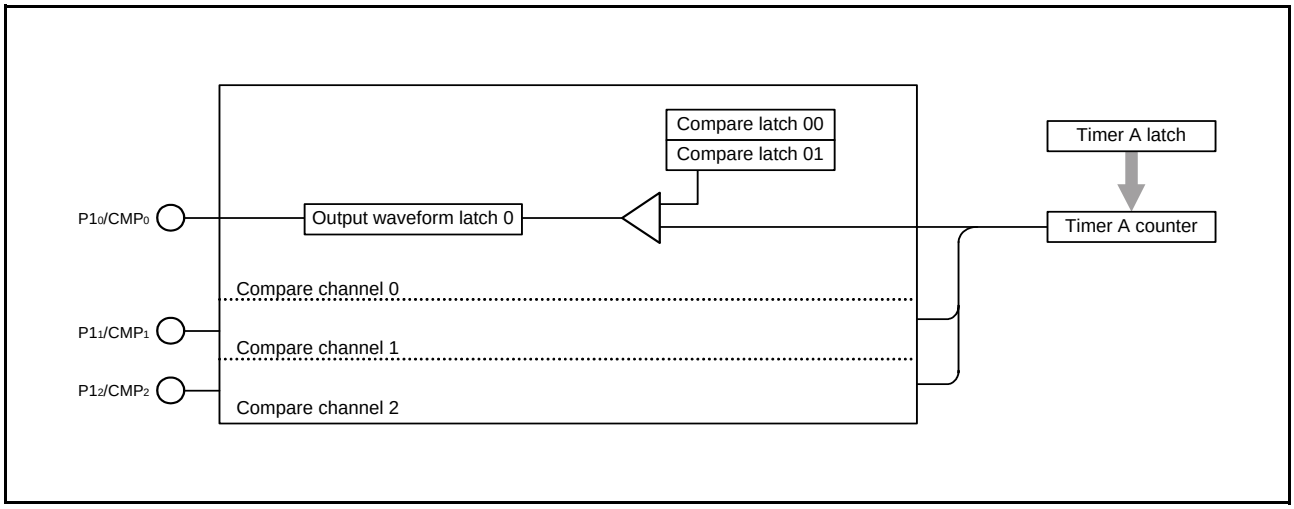


Fig 36. Block diagram of compare output circuit

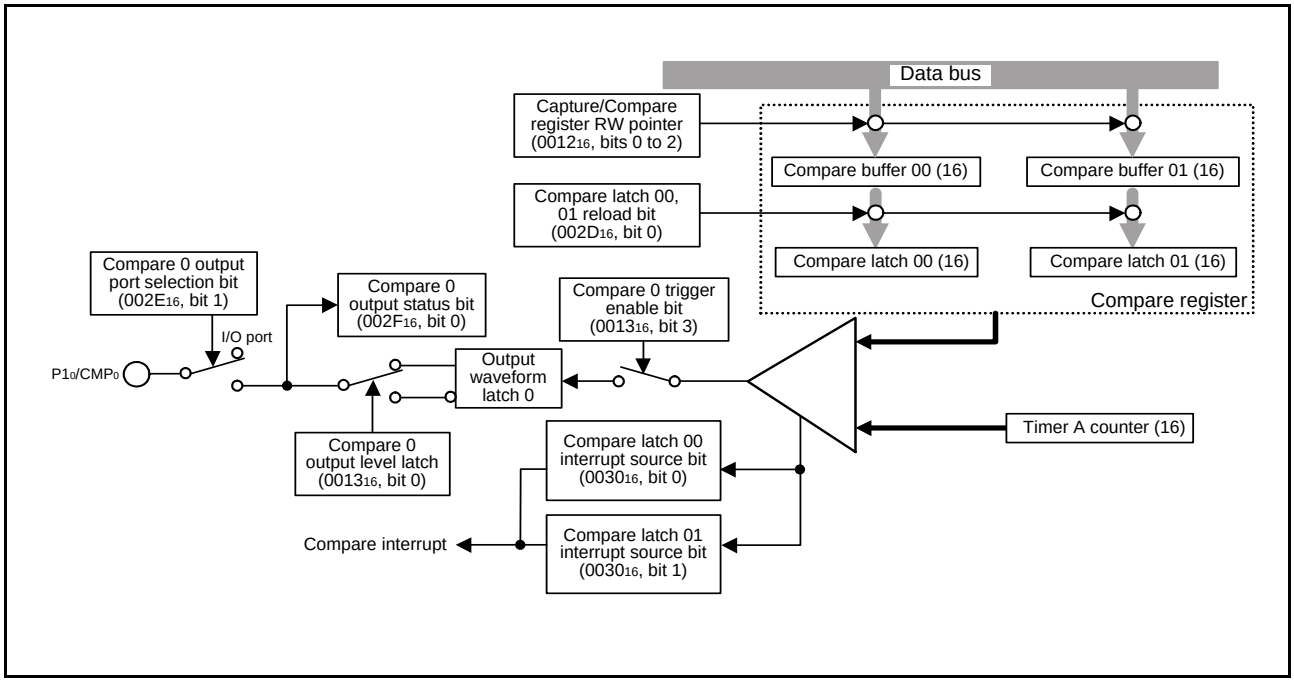
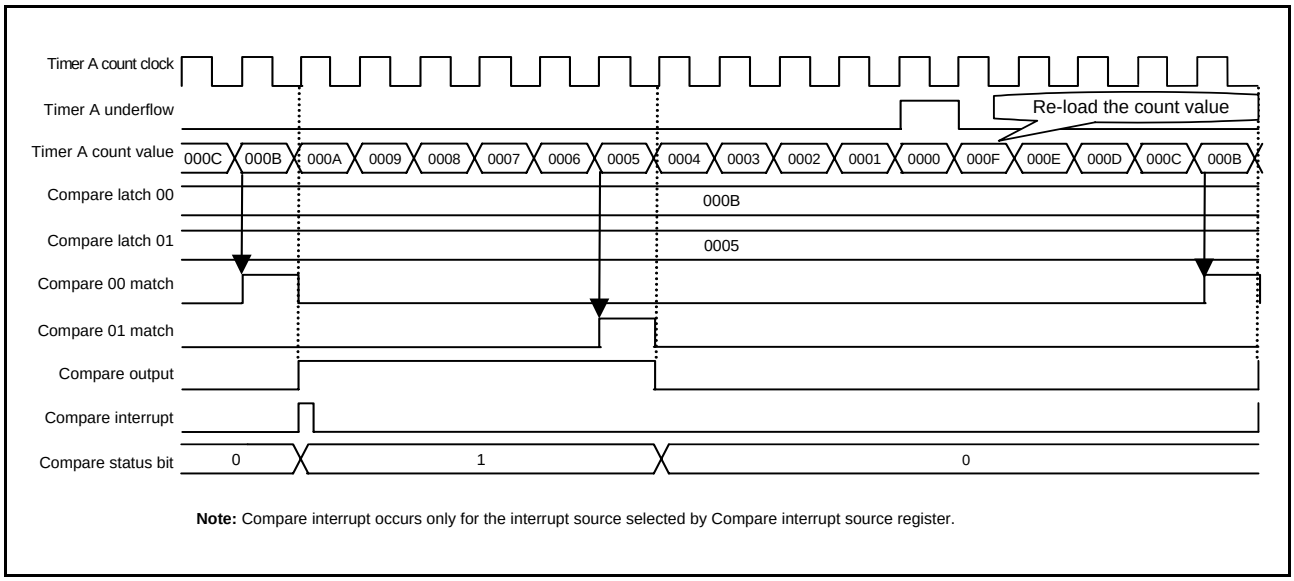


Fig 37. Block diagram of compare channel 0



Note: Compare interrupt occurs only for the interrupt source selected by Compare interrupt source register.

Fig 38. Output compare mode (general waveform)

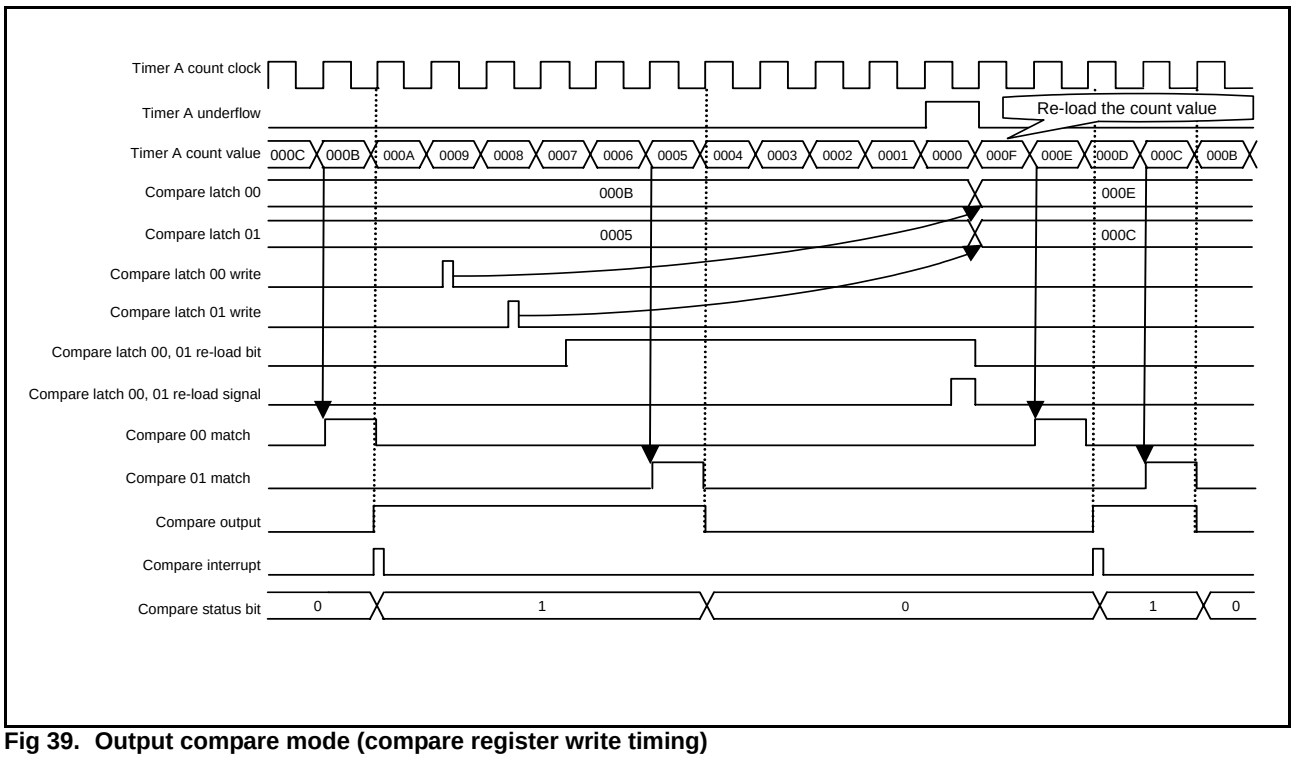


Fig 39. Output compare mode (compare register write timing)

Input capture

7549 group has 1-input capture channel and can be used to capture count value of Timer A.
Input capture shares the registers with three output compare channels, but their individual circuits operate independently so that all the channels can be used at the same time.
To use input capture, set the capture 0 input port selection bits. If P03 is selected, set the P03 direction register to 0. When an input capture trigger is input to the input capture circuit, the count value of timer A is saved to the capture latches. The timer count value at the rising edge of the external input trigger is saved to capture latch 00, and the timer count value at the falling edge of the external input trigger is saved to capture latch 01. Capture latch 00 and capture latch 01 can be read using the following procedure.

1. Set the capture/compare register RW pointer to the read target address.
2. Read the high-order bits of the capture/compare registers, then read the low-order bits of the capture/compare registers. (Read both the capture/compare registers in the sequence of high-order bits followed by low-order bits.)

The count value of timer can be retained by software by capture y (y = 00, 01, 10, 11) software trigger bit too. When "1" is set to this bit, count value of timer is retained to the corresponded capture latch.
When reading from the capture y software trigger bit is executed, "0" is read out.

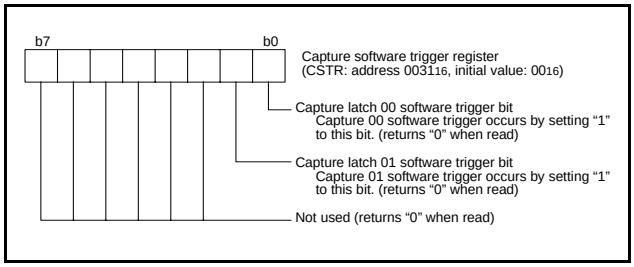


Fig 40. Structure of capture software trigger register

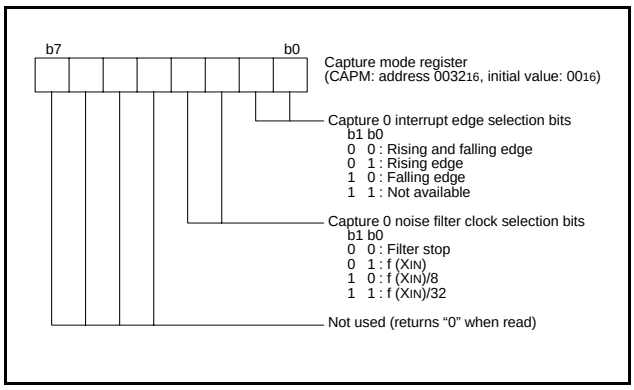


Fig 41. Structure of capture mode register

• Notes

- When the low-speed on-chip oscillator output or XCIN input clock is selected as the count source of timer A, input capture can be used only if the same clock source is selected as ϕSOURCE and as the count source of timer A.
- When writing "1" to capture y software trigger bit of capture latch 00 and 01 at the same time, or external trigger and software trigger occur simultaneously, if capture latches 00 and 01 are input simultaneously, the set value of capture 0 status bit is undefined.
- When setting the interrupt active edge selection bit and noise filter clock selection bit of capture 0 the interrupt request bit may be set to "1".

  When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.

(1) Set the capture interrupt enable bit to "0" (disabled).
(2) Set the interrupt edge selection bit or noise filter clock selection bit.
(3) Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
(4) Set the capture interrupt enable bit to "1" (enabled).

- When the capture interrupt is used as the interrupt for return from stop mode, set the capture 0 noise filter clock selection bits to "00 (Filter stop)".

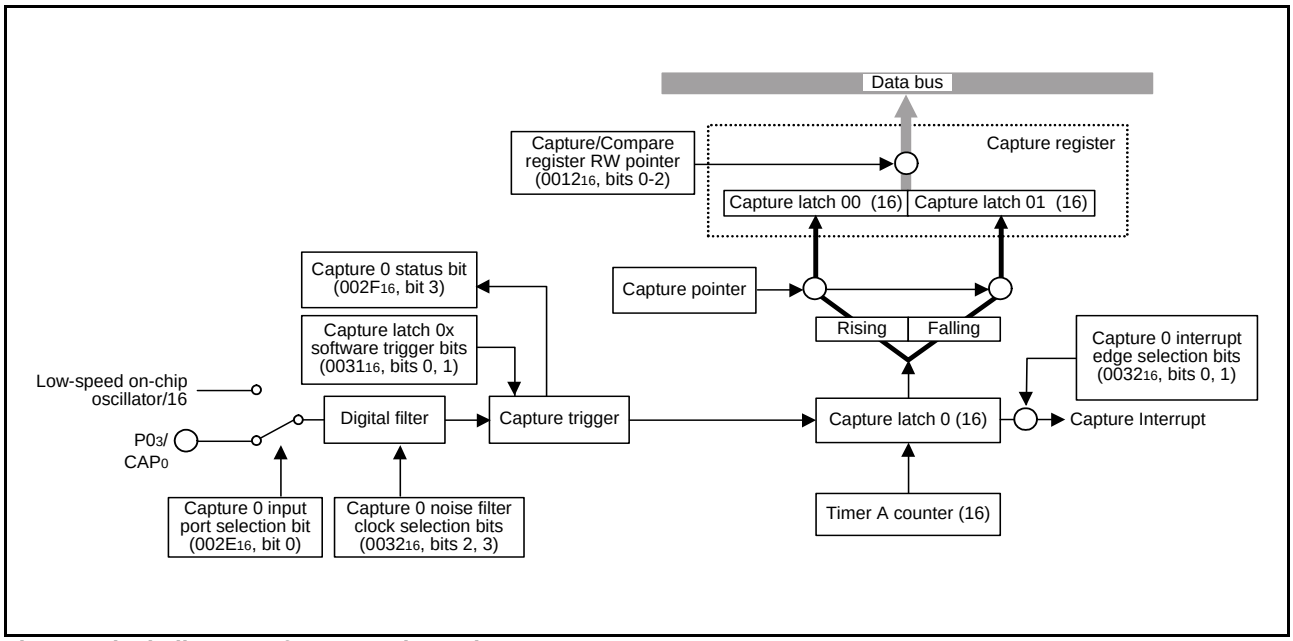


Fig 42. Block diagram of capture channel 0

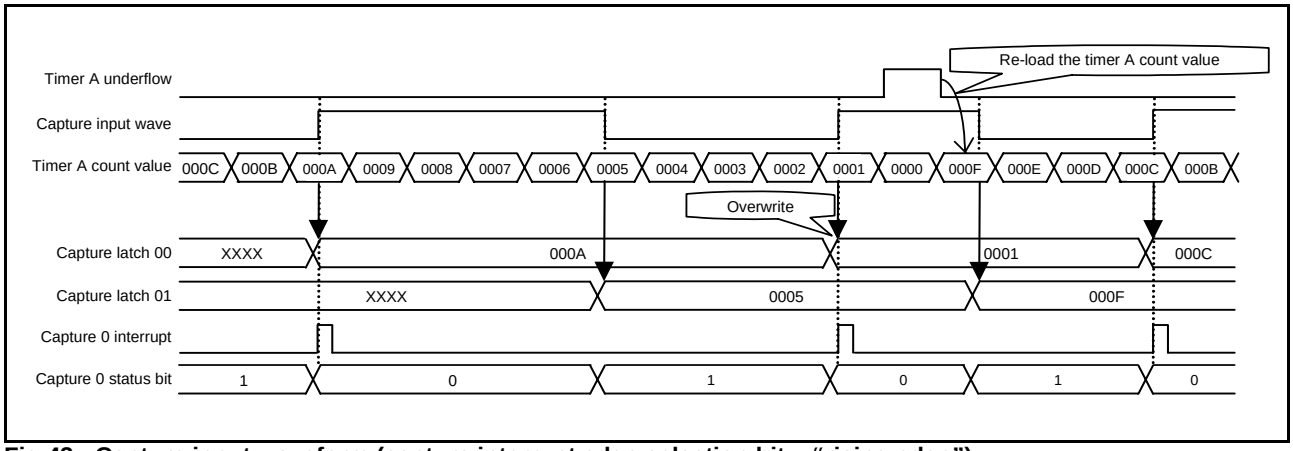


Fig 43. Capture input waveform (capture interrupt edge selection bit = “rising edge”)

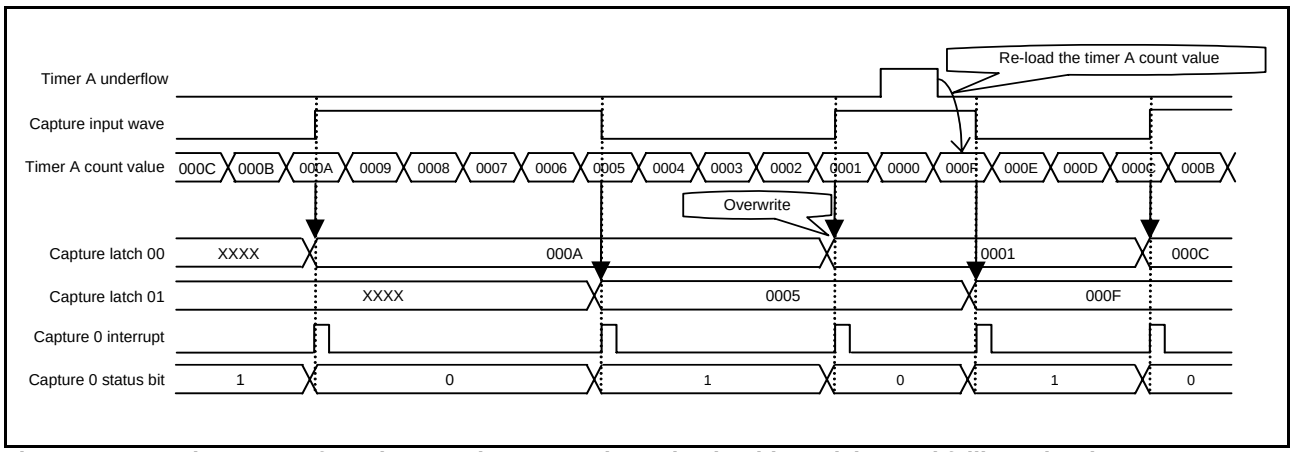


Fig 44. Capture input waveform (capture interrupt edge selection bit = “rising and falling edge”)

Serial Interface

• Serial I/O

Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the serial I/O mode selection bit of the serial I/O control register (bit 6) to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

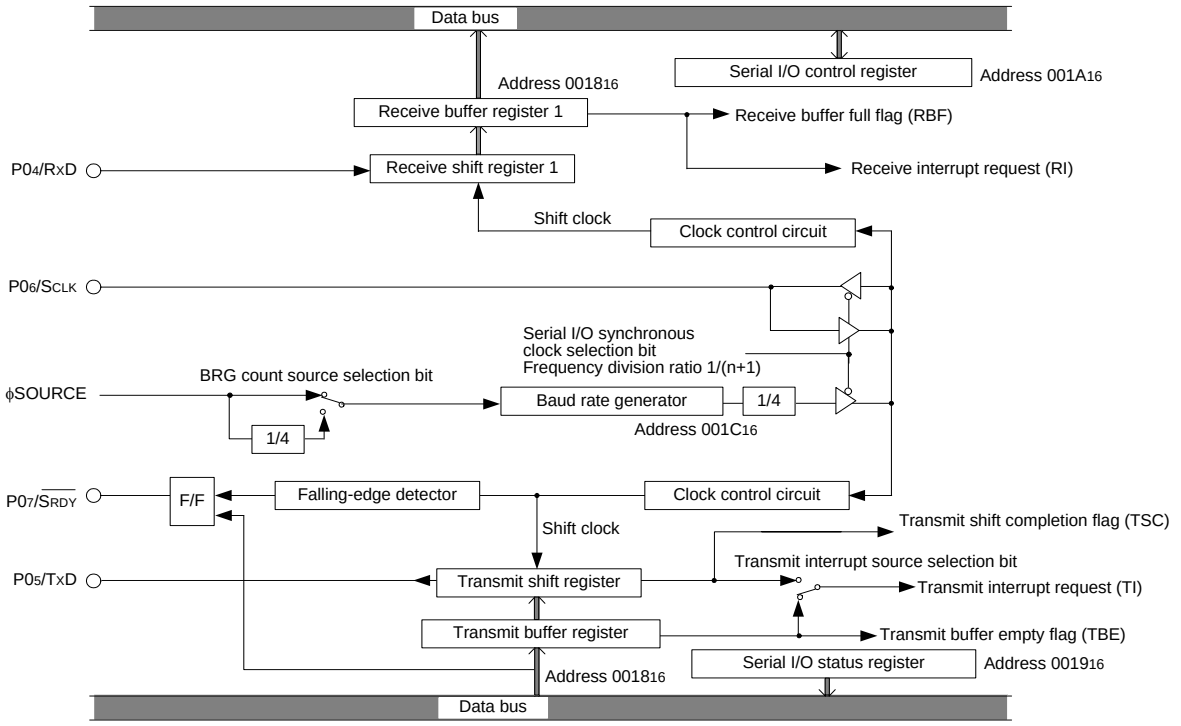
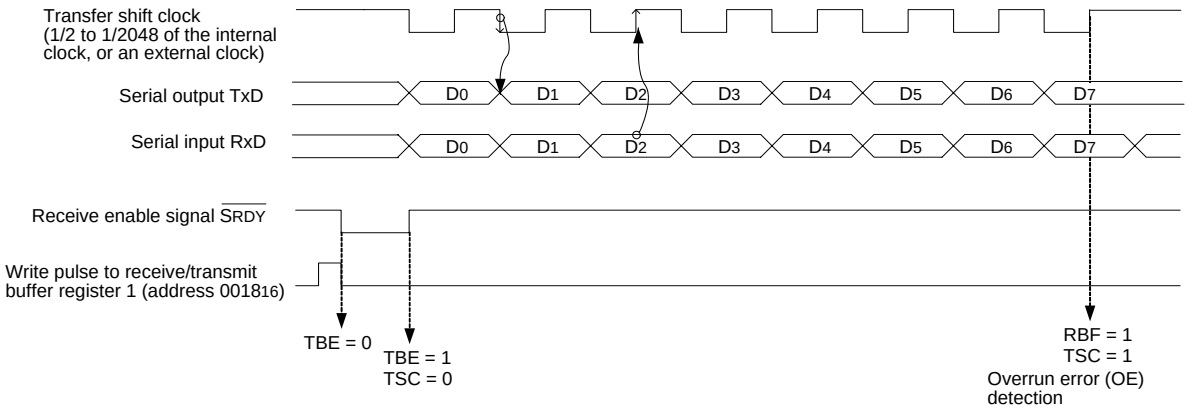


Fig 45. Block diagram of clock synchronous serial I/O



Notes 1: As the transmit interrupt (TI), which can be selected, either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O control register.

2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.

3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1" .

Fig 46. Operation of clock synchronous serial I/O function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to “0”.
Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.
The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

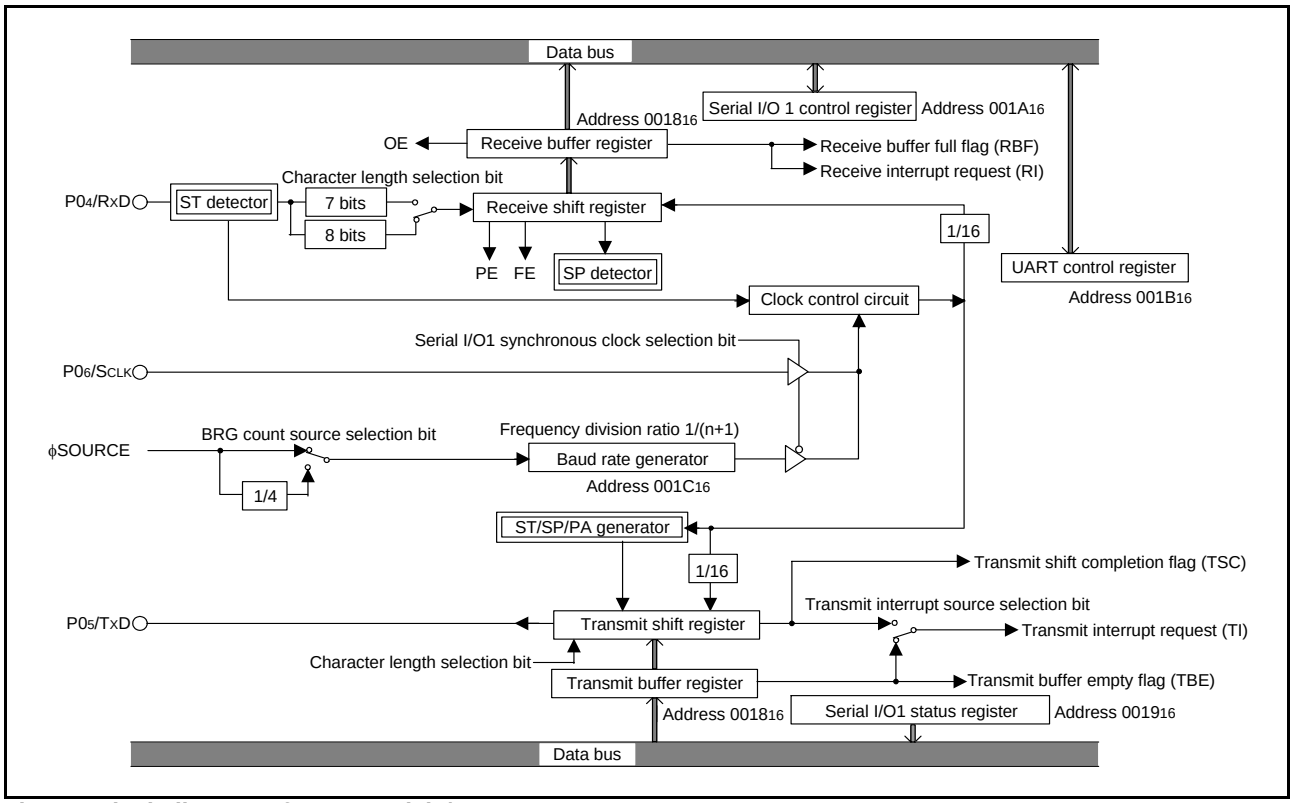
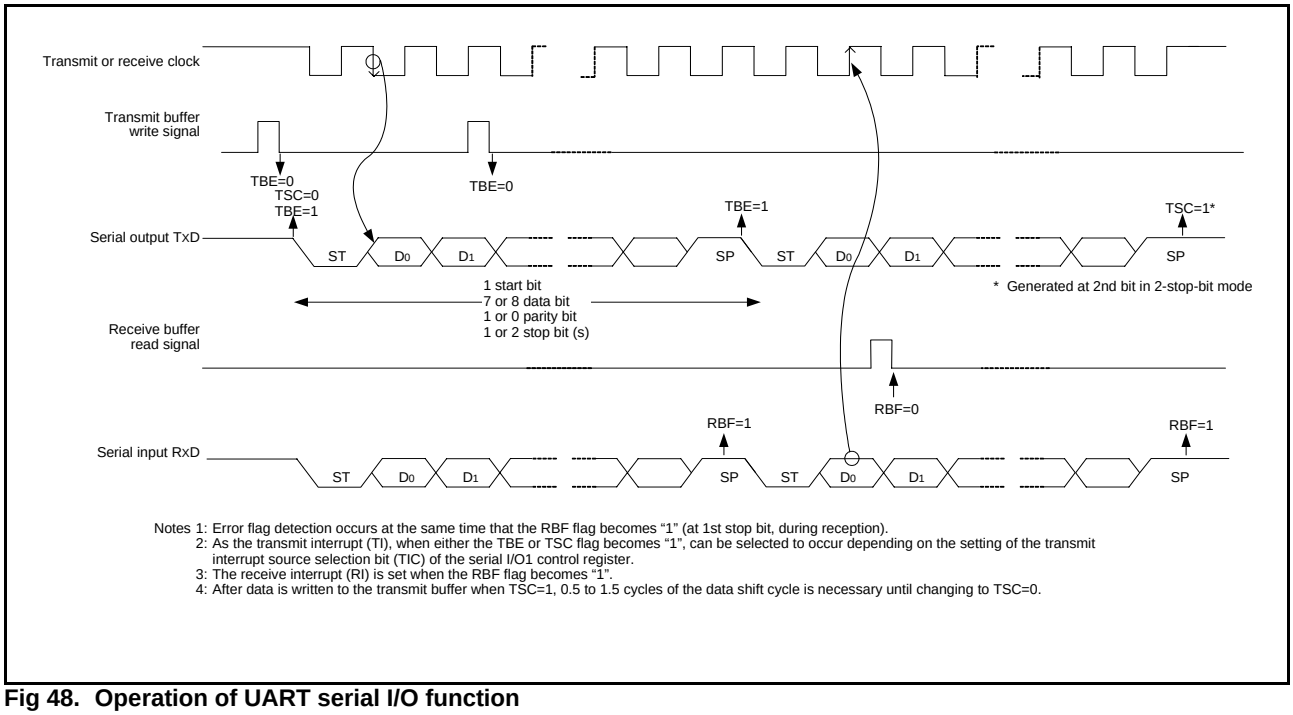


Fig 47. Block diagram of UART serial I/O



Notes 1: Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes “1”, can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
3: The receive interrupt (RI) is set when the RBF flag becomes “1”.
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig 48. Operation of UART serial I/O function

[Transmit buffer register/receive buffer register (TB/RB)] 0018$_{16}$

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O status register (SIOSTS)] 0019$_{16}$

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.
Three of the flags (bits 4 to 6) are valid only in UART mode.
The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.
If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O enable bit SIOE (bit 7 of the serial I/O control register) also clears all the status flags, including the error flags.
Bits 0 to 6 of the serial I/O status register are initialized to "0" at reset, but if the transmit enable bit of the serial I/O control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O control register (SIOCON)] 001A$_{16}$

The serial I/O control register consists of eight control bits for the serial I/O function.

[UART control register (UARTCON)] 001B$_{16}$

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the P0$_5$/TxD pin.

[Baud rate generator (BRG)] 001C$_{16}$

The baud rate generator determines the baud rate for serial transfer.
The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

•Notes

• Serial I/O interrupt

When setting the transmit enable bit to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

1. Set the serial I/O transmit interrupt enable bit to "0" (disabled).
2. Set the transmit enable bit to "1".
3. Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.
4. Set the serial I/O transmit interrupt enable bit to "1" (enabled).

• I/O pin function when serial I/O is enabled.

The functions of P0$_6$ and P0$_7$ are switched with the setting values of a serial I/O mode selection bit and a serial I/O synchronous clock selection bit as follows.

(1) Serial I/O mode selection bit → "1" :
Clock synchronous type serial I/O is selected.
Setup of a serial I/O synchronous clock selection bit
"0" : P0$_6$ pin turns into an output pin of a synchronous clock.
"1" : P0$_6$ pin turns into an input pin of a synchronous clock.
Setup of a $\overline{\text{SRDY}}$ output enable bit (SRDY)
"0" : P0$_7$ pin can be used as a normal I/O pin.
"1" : P0$_7$ pin turns into a $\overline{\text{SRDY}}$ output pin.

(2) Serial I/O mode selection bit → "0" :
Clock asynchronous (UART) type serial I/O is selected.
Setup of a serial I/O synchronous clock selection bit
"0" : P0$_6$ pin can be used as a normal I/O pin.
"1" : P0$_6$ pin turns into an input pin of an external clock.
When clock asynchronous (UART) type serial I/O is selected, it is P0$_7$ pin. It can be used as a normal I/O pin.

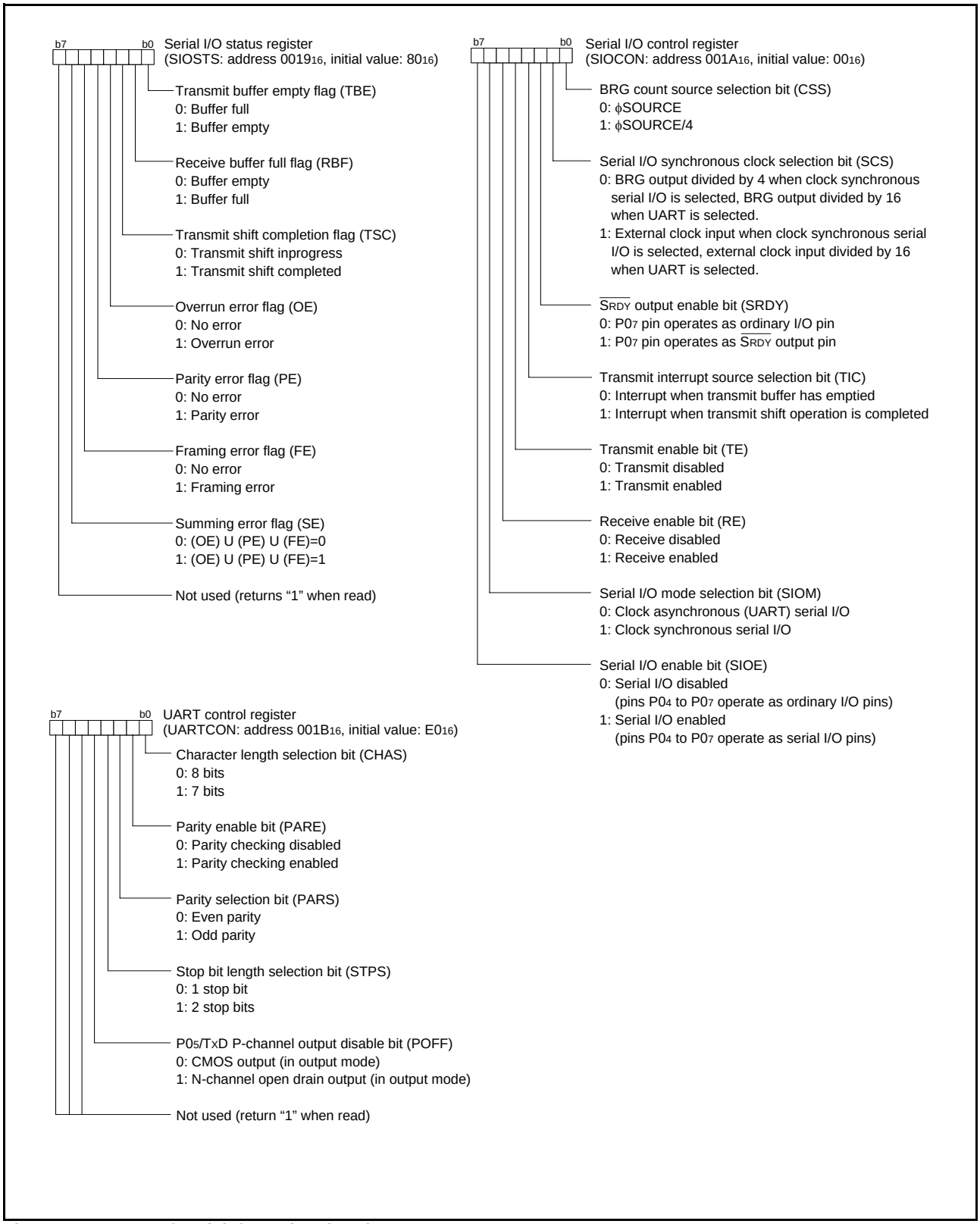


Fig 49. Structure of serial I/O1-related registers

A/D Converter

The functional blocks of the A/D converter are described below.

[AD conversion register] AD

The A/D conversion register is a read-only register that stores the result of A/D conversion. Do not read out this register during an A/D conversion.

[AD control register] ADCON

The AD control register controls the A/D converter.
Bit 2 to 0 are analog input pin selection bits.
Bit 3 is the AD conversion clock selection bit. When "0" is set to this bit, the A/D conversion clock is ϕSOURCE/2 and the A/D conversion time is 122 cycles of ϕSOURCE. When "1" is set to this bit, the A/D conversion clock is ϕSOURCE and the A/D conversion time is 61 cycles of ϕSOURCE.
Bit 4 is the AD conversion completion bit. The value of this bit remains at "0" during A/D conversion, and changes to "1" at completion of A/D conversion.
A/D conversion is started by setting this bit to "0".

[Comparison voltage generator]

The comparison voltage generator divides the voltage between V_{SS} and V_{CC} by 1024, and outputs the divided voltages.

[Channel selector]

The channel selector selects one of ports $P1_7/AN_7$ to $P1_0/AN_0$, and inputs the voltage to the comparator.

[Comparator and control circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores its result into the AD conversion register. When AD conversion is completed, the control circuit sets the AD conversion completion bit and the A/D conversion interrupt request bit to "1". Because the comparator is constructed linked to a capacitor, set ϕSOURCE in order that the A/D conversion clock is 250 kHz or over during A/D conversion.

• Notes

As for A/D translation accuracy, on the following operating conditions, accuracy may become low.

(1) When V_{CC} voltage is lower than [3.0 V], the accuracy at the low temperature may become extremely low compared with that at room temperature. When the system would be used at low temperature, the use at V_{CC} = 3.0 V or more is recommended.

(2) When X_{CIN} or the low-speed on-chip oscillator is selected as ϕSOURCE, the A/D converter cannot be used.

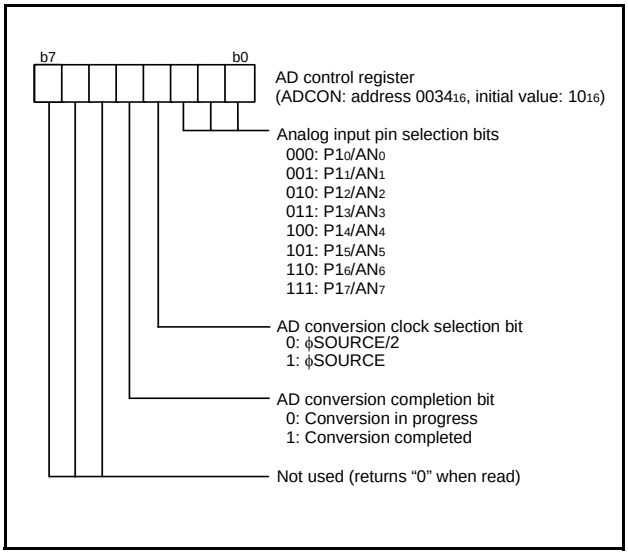


Fig 50. Structure of AD control register

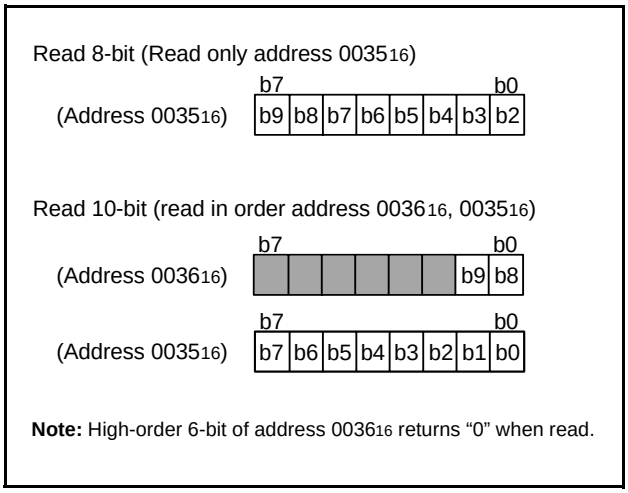


Fig 51. Structure of AD conversion register

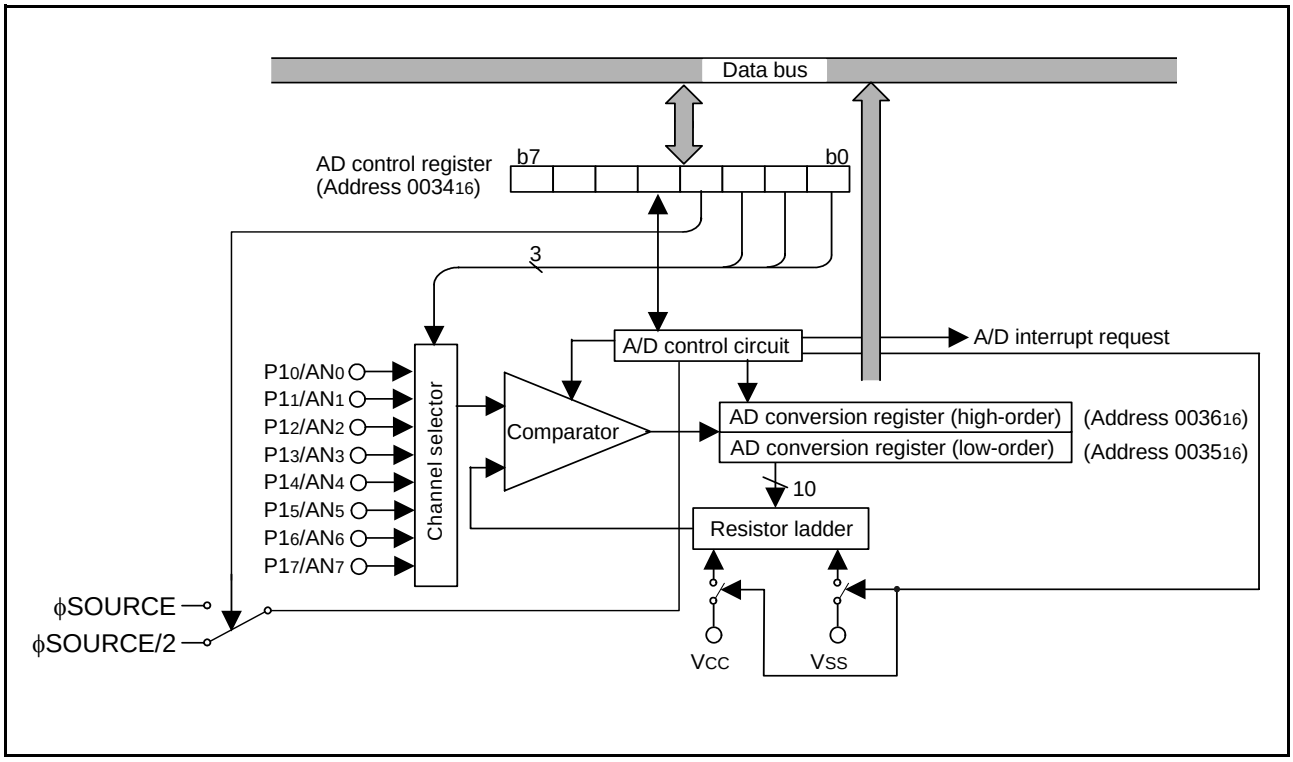


Fig 52. Block diagram of A/D converter

Watchdog Timer

The watchdog timer gives a means for returning to a reset status when the program fails to run on its normal loop due to a runaway. The watchdog timer consists of an 8-bit watchdog timer H and an 8-bit watchdog timer L, being a 16-bit counter. The operation of the watchdog timer is controlled by bits 2 to "0" in function set ROM data 2 and the watchdog timer control register.

• Watchdog timer disable bit

When the watchdog timer disable bit (bit 1 in function set ROM data 2(FSROM2)) is set to "0", the watchdog timer is enabled and starts counting after reset.
Setting this bit to "1" does not operate the watchdog timer.
This bit cannot be rewritten by executing the instruction.
To use the watchdog timer, always set this bit to "0".
After reset, the watchdog timer cannot start counting by a program.

• Watchdog timer source clock selection bit

The count source of the watchdog timer is selected by the watchdog timer source clock selection bit (bit 0 in FSROM2). This bit cannot be rewritten by executing the instruction.
When this bit is set to "0", the count source is always set to the low-speed on-chip oscillator output/16.
When this bit is set to "1", the count source is set to ϕSOURCE/16. ϕSOURCE is changed by setting the clock selection bits (bits 5 and 4 in the clock mode register (CLKM: address 0037_{16})).

• Watchdog timer H count source selection bit

The count source of watchdog timer H is selected by the watchdog timer control register (WDTCON: address 0039_{16}).
When the watchdog timer H count source selection bit (bit 7 in WDTCON) is set to "0", the count source is set to an underflow signal from watch dog timer L. When this bit is set to "1", the clock selected as the count source of watchdog timer L is input to watchdog timer H.
The initial value of this bit after releasing reset can be set by the bit 2 in FSROM2.

• Watchdog Timer Operation

Resetting or writing any data to WDTCON sets watchdog timer H to "FF_{16}" and watchdog timer L to "FF_{16}". When the watchdog timer starts, the selected clock is counted and internal reset occurs by the watchdog timer H underflow. Writing to WDTCON is usually programmed to be performed before underflow.
Reading WDTCON reads the values of the high-order 6 bits in the watchdog timer H counter and the watch dog timer count source selection bit.

The following shows the time to watchdog timer underflow after writing to the watchdog timer control register.
The example applies when the XIN input clock is selected as ϕSOURCE and f(XIN) = 8 MHz.

- Watchdog timer H count source selection bit = 0: 131.072 ms
- Watchdog timer H count source selection bit = 1: 512 μs

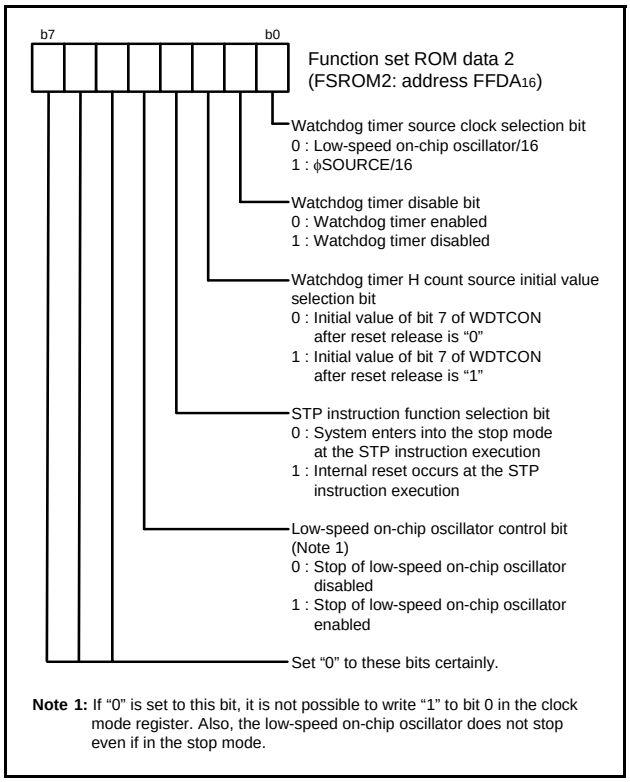


Fig 53. Structure of Function set ROM data 2

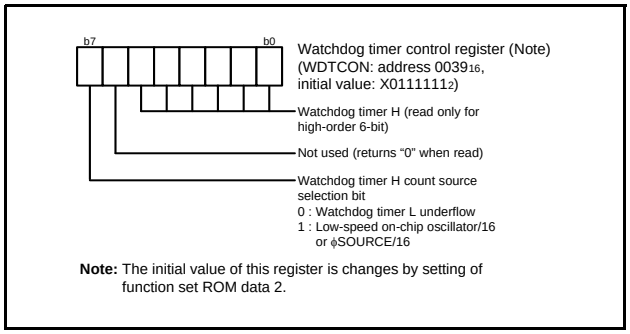


Fig 54. Structure of watchdog timer control register

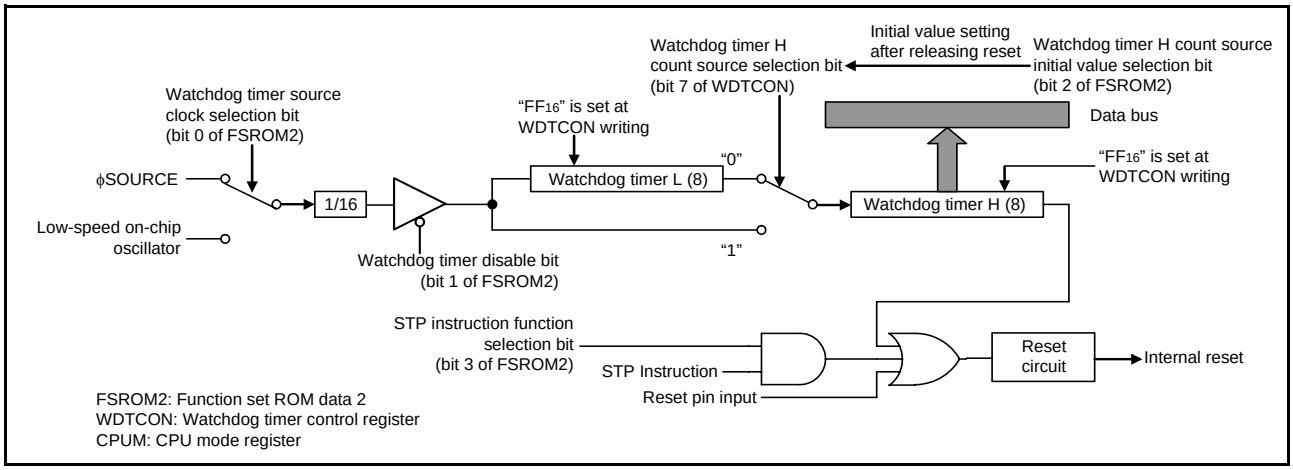


Fig 55. Block diagram of watchdog timer

• Notes

(1) The watchdog timer operates in wait mode. To prevent underflow, write to the watchdog timer control register.

The watchdog timer stops in stop mode, but starts counting at the same time as exiting stop mode. After exiting stop mode, it continues counting during oscillation stabilization time. To prevent underflow during the period, the watchdog timer H count source selection bit (bit 7) in the watchdog timer control register (address 0039_{16}) should be set to "0" before executing the STP instruction.

Note that the watchdog timer continues counting even if the STP instruction is executed in the following two conditions:

① Stopping the low-speed on-chip oscillator: Disabled (bit 4 in FSROM2)

Source clock of the watchdog timer: Low-speed on-chip oscillator/16 (bit 0 in FSROM2)

② Stopping the low-speed on-chip oscillator: Disabled (bit 4 in FSROM2)

Source clock of the watchdog timer: ϕSOURCE (bit 0 in FSROM2)

ϕSOURCE: Low-speed on-chip oscillator (bits 5 and 4 in CLKM)

(2) STP instruction function selection bit

The function of the STP instruction can be selected by the bit 2 in FSROM2. This bit cannot be used for rewriting by executing the STP instruction.

- When this bit is set to "0", stop mode is entered by executing the STP instruction.
- When this bit is set to "1", internal reset occurs by executing the STP instruction.

Power-on Reset Circuit

Reset can be automatically performed at power on (power-on reset) by the built-in power-on reset circuit.
To use the built-in power-on reset circuit, leave the $\overline{\text{RESET}}$ pin open (the pull-up resistor is built-in).

Low Voltage Detection Circuit

The built-in low voltage detection circuit is designed to detect a drop in voltage and to reset the microcomputer if the power source voltage drops below a set value (Typ.1.95 V).
The low voltage detection circuit is valid by setting "1" to bit 0 of the function set ROM data 0.
Also, when "1" is set to bit 2 of the function set ROM data 1, the low voltage detection circuit can be valid even in the stop mode.
The low voltage detection circuit is stopped in the stop mode by setting "0" to this bit, so that the power dissipation is reduced.

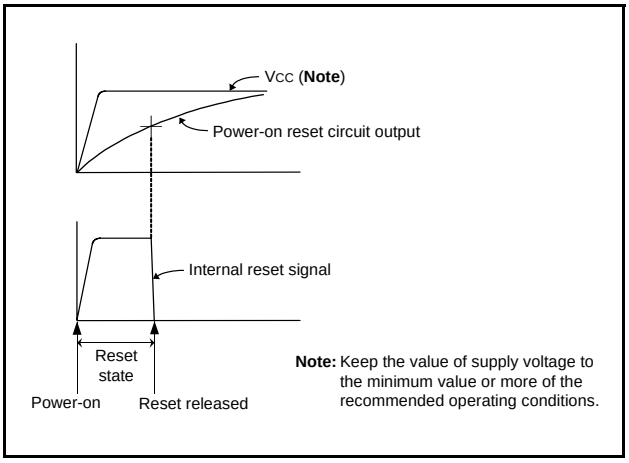


Fig 56. Operation waveform diagram of power-on reset circuit

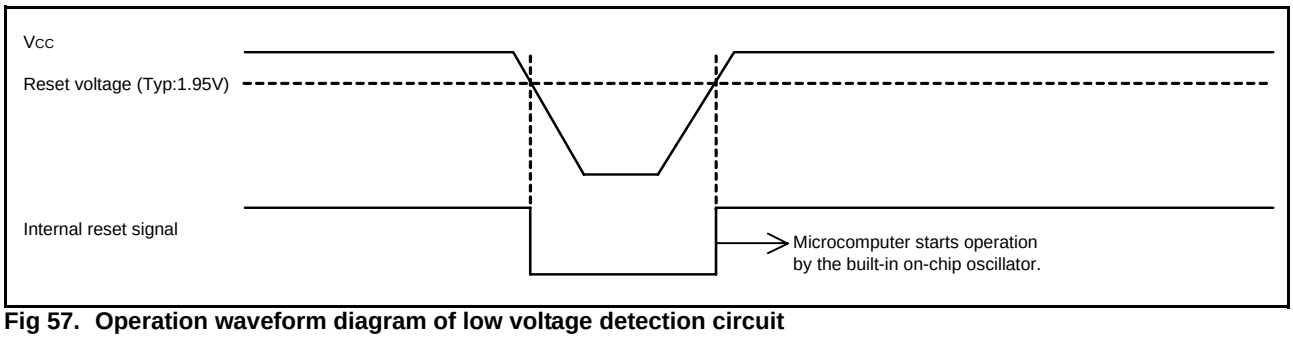


Fig 57. Operation waveform diagram of low voltage detection circuit

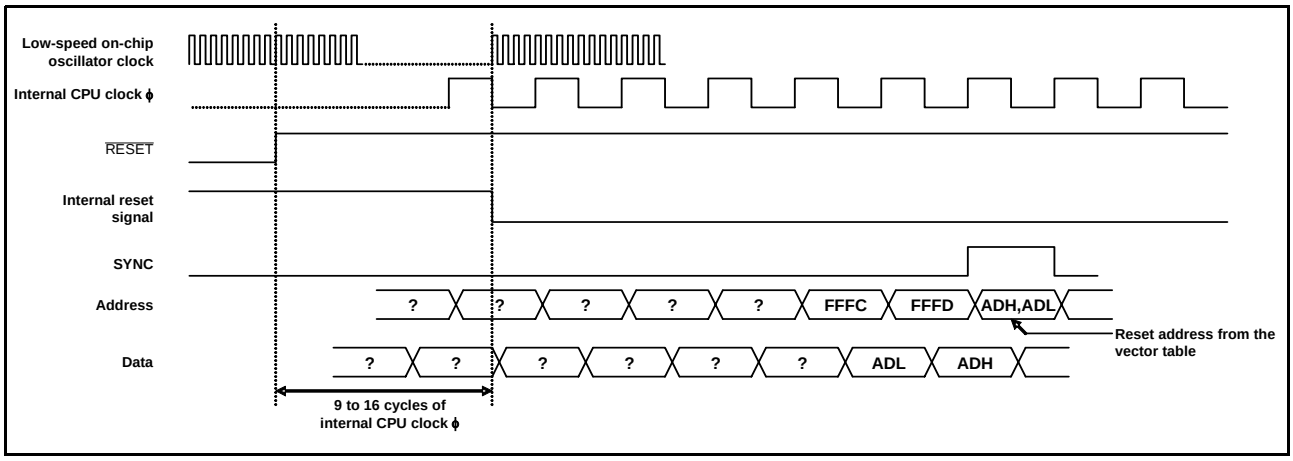


Fig 58. Timing diagram at reset

(1)	Port P0 direction register (P0D)	0001_{16}	00_{16}						
(2)	Port P1 direction register (P1D)	0003_{16}	00_{16}						
(3)	Port P2 direction register (P2D)	0005_{16}	00_{16}						
(4)	Port P3 direction register (P3D)	0007_{16}	00_{16}						
(5)	Port P0 drive capacity control register (DCCR)	$000C_{16}$	00_{16}						
(6)	Port P0 pull-up control register (PULL0)	$000D_{16}$	00_{16}						
(7)	Port P1 pull-up control register (PULL1)	$000E_{16}$	00_{16}						
(8)	Key-on wakeup input selection register (KEYS)	$000F_{16}$	00_{16}						
(9)	Capture/Compare register (low-order) (CRAL)	0010_{16}	00_{16}						
(10)	Capture/Compare register (high-order) (CRAH)	0011_{16}	00_{16}						
(11)	Capture/Compare register RW pointer (CCRP)	0012_{16}	00_{16}						
(12)	Compare output mode register (CMOM)	0013_{16}	00_{16}						
(13)	Timer A (low-order) (TAL)	0014_{16}	FF_{16}						
(14)	Timer A (high-order) (TAH)	0015_{16}	FF_{16}						
(15)	Serial I/O status register (SIOSTS)	0019_{16}	1	0	0	0	0	0	0	0
(16)	Serial I/O control register (SIOCON)	$001A_{16}$	00_{16}						
(17)	UART control register (UARTCON)	$001B_{16}$	1	1	1	0	0	0	0	0
(18)	Prescaler 12 (PRE12)	0028_{16}	FF_{16}						
(19)	Timer 1 (T1)	0029_{16}	0	0	0	0	0	0	0	1
(20)	Timer 2 (T2)	$002A_{16}$	FF_{16}						
(21)	Timer mode register (TM)	$002B_{16}$	00_{16}						
(22)	Timer count source set register (TCSS)	$002C_{16}$	00_{16}						
(23)	Compare register re-load register (CMPR)	$002D_{16}$	00_{16}						
(24)	Capture/Compare port register (CCPR)	$002E_{16}$	00_{16}						
(25)	Capture/Compare status register (CCSR)	$002F_{16}$	00_{16}						
(26)	Compare interrupt source set register (CISR)	0030_{16}	00_{16}						
(27)	Capture software trigger register (CSTR)	0031_{16}	00_{16}						
(28)	Capture mode register (CAPM)	0032_{16}	00_{16}						
(29)	AD control register (ADCON)	0034_{16}	0	0	0	1	0	0	0	0
(30)	Clock mode register (CLKM)	0037_{16}	0	0	0	0	0	0	1	0
(31)	Oscillation stop detection register (CLKSTP)	0038_{16}	00_{16}						
(32)	Watchdog timer control register (WDTCON)	0039_{16}	Note 4	0	1	1	1	1	1	1
(33)	Interrupt edge selection register (INTEDGE)	$003A_{16}$	00_{16}						
(34)	CPU mode register (CPUM)	$003B_{16}$	00_{16}						
(35)	Interrupt request register 1 (IREQ1)	$003C_{16}$	00_{16}						
(36)	Interrupt request register 2 (IREQ2)	$003D_{16}$	00_{16}						
(37)	Interrupt control register 1 (ICON1)	$003E_{16}$	00_{16}						
(38)	Interrupt control register 2 (ICON2)	$003F_{16}$	00_{16}						

Notes 1: X : Undefined
2: The content of other registers is undefined when the microcomputer is reset.
The initial values must be surely set before you use it.
3: Do not access to the SFR area including nothing.
4: When the setting by the function set ROM data 2 (FSROM2) is performed,
the initial values of this bit at reset are changed.

Fig 59. Timing diagram at reset

Clock Generating Circuit

The clock generating circuit includes the XIN clock (ceramic oscillator or crystal oscillator can be used), XCIN clock (32 kHz oscillator can be used), external clock input, high-speed on-chip oscillator, and low-speed on-chip oscillator.
Pins P20/XOUT/XCOUT and P21/XIN/XCIN can be shared for the ports, XIN oscillation, and XCIN oscillation.
Use the oscillation method selection bits (bits 1 and bit 0 in function set ROM data 1 (FSROM1)) to set the function of these pins.

• Ceramic Resonator or Crystal Oscillator

Set the oscillation method selection bits (bits 1 and bit 0 in FSROM1) to "01$_2$", and connect the ceramic resonator (or the oscillator) and external circuit with the shortest wiring length possible.
The constants of the oscillator circuit differ depending on the resonator. Use the values recommended by the resonator manufacturer. (An external feedback resistor may be necessary under some conditions.)
Setting the XIN/XCIN oscillation control bit to "0" starts oscillation. This bit is sets to "0" after reset.

• 32 kHz Crystal Oscillator

Set the oscillation method selection bits to "10$_2$", and connect the 32 kHz crystal oscillator and external circuit with the shortest wiring length possible.
The constants of the oscillator circuit differ depending on the resonator. Use the values recommended by the resonator manufacturer. (An external feedback resistor may be necessary under some conditions.)
Setting the XIN/XCIN oscillation control bit to "0" starts oscillation. This bit is sets to "0" after reset.

• External Clock Input

Set the oscillation method selection bits to "11$_2$", and connect the clock source to the P20/XOUT pin. In this case, the P21/XIN pin can be used as an I/O port.

• High-Speed On-Chip Oscillator

The high-speed on-chip oscillator is stopped after reset.
Setting the high-speed on-chip oscillator oscillation control bit (bit 1 in CLKM) to "0" starts oscillation. This bit is sets to "1" after reset.

• Low-Speed On-Chip Oscillator

The low-speed on-chip oscillator automatically starts oscillating after reset.
Setting the low-speed on-chip oscillator oscillation control bit (bit 0 in CLKM) to "1" stops oscillation. This bit is sets to "0" after reset. If the low-speed on-chip oscillator control bit (bit 4 in FSROM2) is set to "0" and stopping the low-speed on-chip oscillator is disabled, the low-speed on-chip oscillator oscillation control bit cannot be set to "1" and oscillation cannot be stopped. Also, the oscillator does not stop even when the STP instruction is executed.

• Using No Oscillator Pins (P20 as output port and P21 as I/O port)

To use only an internal on-chip oscillator, set the oscillation method selection bits to "00$_2$". The P20/XOUT pin can be used as an output port and the P21/XIN pin can be used as an I/O port.

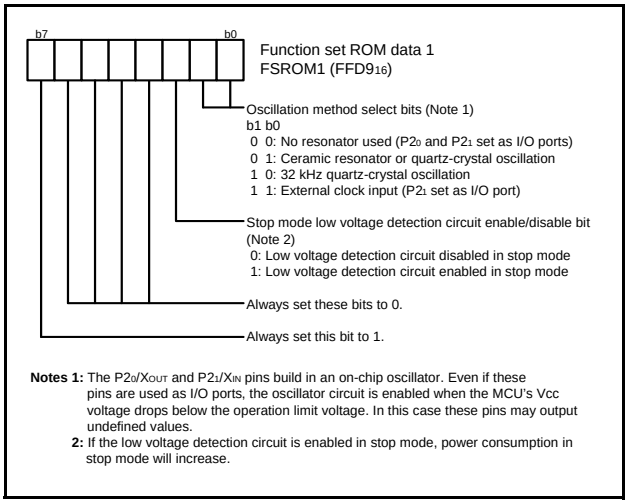


Fig 60. Structure of function set ROM data 1

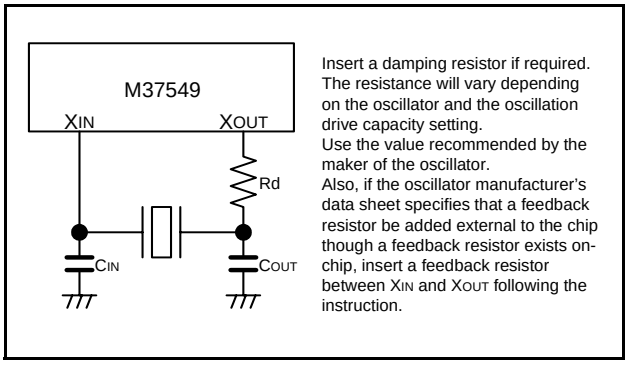


Fig 61. External circuit of ceramic resonator

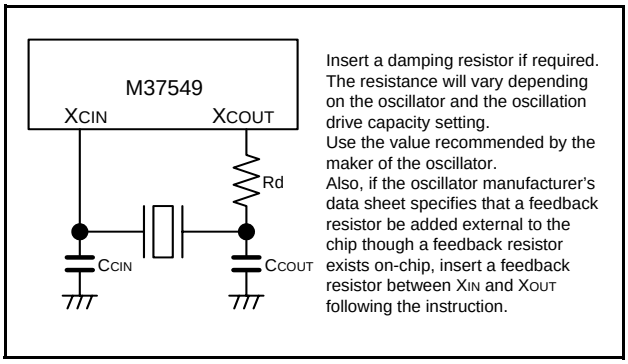


Fig 62. External circuit of 32 kHz quarts-crystal oscillator

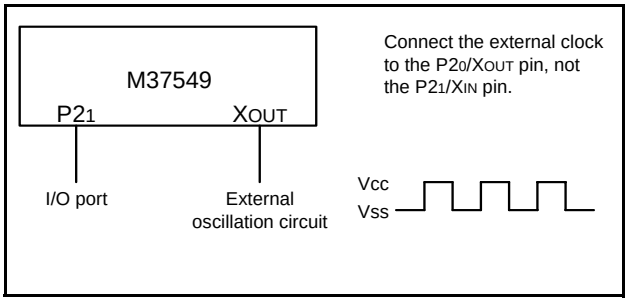
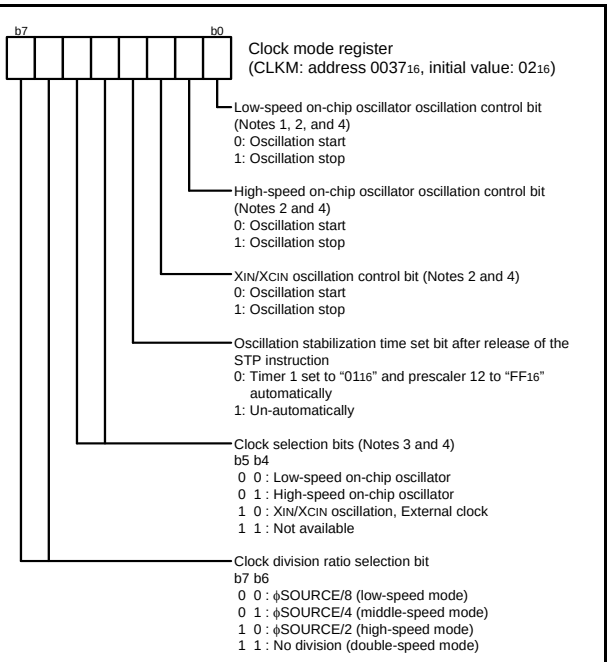


Fig 63. External clock input circuit



Notes 1: When stopping the low-speed on-chip oscillator is disabled by setting the low-speed on-chip oscillator control bit (bit 4 in FSROM2), "1" cannot be written to this bit. The low-speed on-chip oscillator does not stop even in stop mode.
2: "1" cannot be written to the oscillation control bits (bits 2 to 0) of the clock selected as ϕSOURCE by the clock selection bits.
3: When "oscillation pins not used" is set by the oscillation method selection bits (bits 1 and 0 in FSROM1), "10₂" cannot be written to these bits.
4: Do not change the values of the clock selection bits and the clock oscillation control bits at the same time using a single instruction. Always use different instructions to rewrite these values.

Fig 64. Structure of clock mode register

• Note

• Switching to XIN/XCIN Oscillator

After a reset is cleared, operation starts using the low-speed on-chip oscillator. When switching to XIN/XCIN oscillator, make sure to set a sufficient wait duration with the on-chip oscillator to allow the XIN/XCIN oscillator to stabilize.

Oscillation Control

• Clock mode register

Clock mode register contains the oscillation control bits of each oscillation circuits, clock selection bits and etc

• Clock selection bits

ϕSOURCE can be selected by the clock selection bits (bits 5 and 4 in clock mode register). ϕSOURCE can be selected from low-speed on-chip oscillator, high-speed on-chip oscillator, XIN/XCIN oscillaton or external clock input by the clock selection bits. ϕSOURCE is also used to the clock for peripheral functions.
When the oscillation method selection bits (bits 1 and 0 in FSROM1) is set to "00_2" (oscillation pins not used), setting the clock selection bits to "10_2" (XIN/XCIN oscillation, external clock input) is disabled.

• Clock division ratio selection bit

The internal clock ϕ is generated by dividing ϕSOURCE.
Select the division ratio using the clock division ration selection bits (bits 7 and 6 in CLKM).
The division ratio can be selected from among ϕSOURCE/8 (low-speed mode), /4 (middle-speed mode), /2 (high-speed mode), and no division (double-speed mode).
Table 9 shows the division ratio (mode) settings.

When releasing reset, the low-speed on-chip oscillator is selected as ϕSOURCE, and ϕSOURCE/8 is selected as the internal clock. The high-speed on-chip oscillator is stopped at this time. If an oscillation circuit is connected to the clock pin, oscillation starts. To switch ϕSOURCE to XIN/XCIN oscillation, generate wait time using the on-chip oscillator until the oscillation is stabilized.

Table 9 Setting the clock division (mode)

ϕSOURCE	bit / Mode	CLKM					FSROM1	FSROM2
		Clock division ratio selection bits	Clock selection bits	XIN/XCIN oscillation control bit	High-speed on-chip oscillator oscillation control bit	Low-speed on-chip oscillator oscillation control bit	Oscillation method selection bits	Low-speed on-chip oscillator control bit
		Bit 7, 6	Bit 5, 4	Bit 2	Bit 1	Bit 0	Bit 1, 0	Bit 4
XIN	Double-speed	11	10	0	–	–	01	–
	High-speed	10	10	0	–	–	01	–
	Middle-speed	01	10	0	–	–	01	–
	Low-speed	00	10	0	–	–	01	–
XCIN	Double-speed	11	10	0	–	–	10	–
	High-speed	10	10	0	–	–	10	–
	Middle-speed	01	10	0	–	–	10	–
	Low-speed	00	10	0	–	–	10	–
External clock	Double-speed	11	10	–	–	–	11	–
	High-speed	10	10	–	–	–	11	–
	Middle-speed	01	10	–	–	–	11	–
	Low-speed	00	10	–	–	–	11	–
High-speed on-chip oscillator	Double-speed	11	01	–	0	–	–	–
	High-speed	10	01	–	0	–	–	–
	Middle-speed	01	01	–	0	–	–	–
	Low-speed	00	01	–	0	–	–	–
Low-speed on-chip oscillator	Double-speed	11	00	–	–	0	–	1/0
	High-speed	10	00	–	–	0	–	1/0
	Middle-speed	01	00	–	–	0	–	1/0
	Low-speed	00	00	–	–	0	–	1/0

–: can be "0" or "1", no change in outcome

• Stop mode

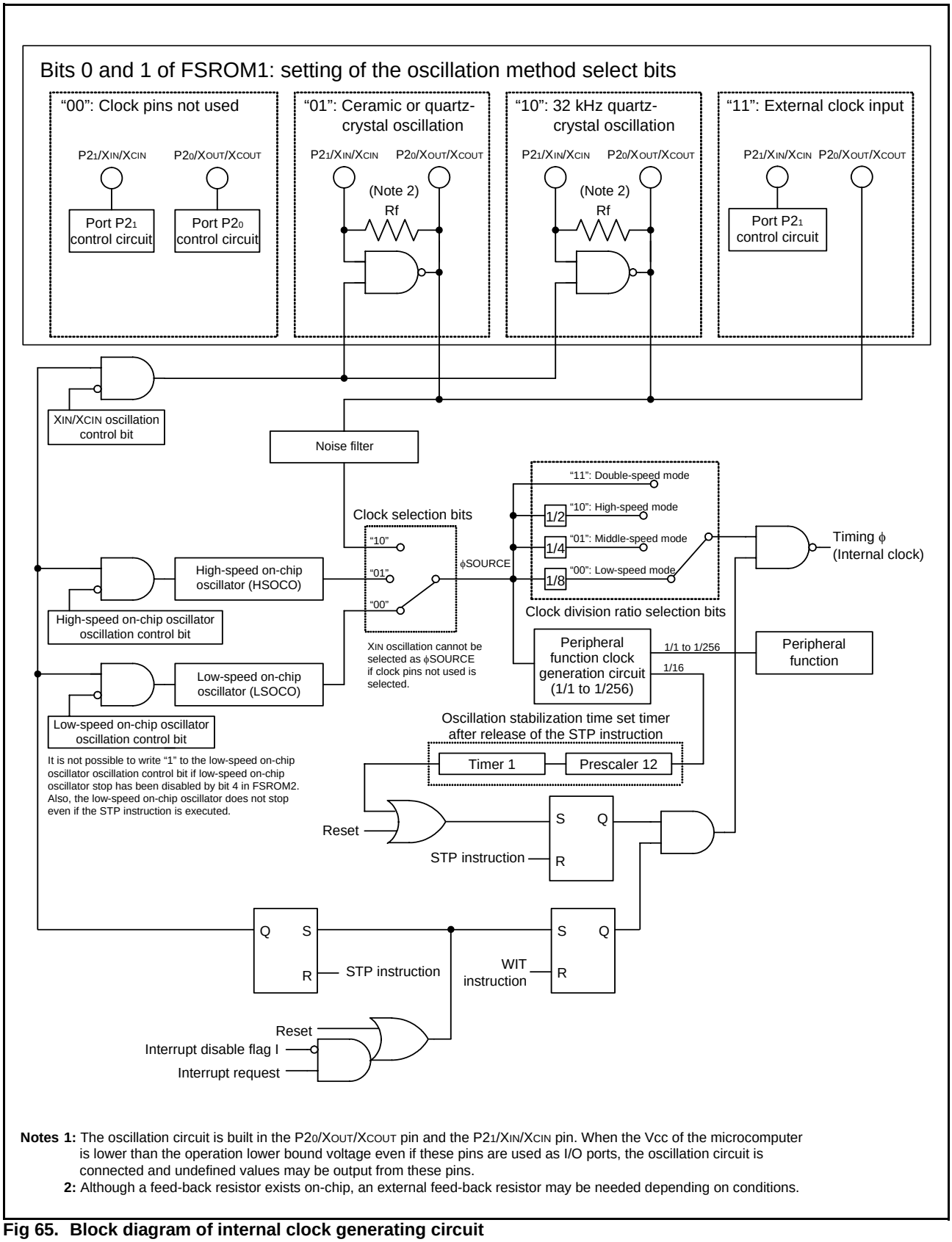
When the STP instruction is executed, the internal clock ϕ stops at an "H" level and the X_{IN}/X_{CIN} and on-chip oscillator stops. At this time, timer 1 is set to "01_{16}" and prescaler 12 is set to "FF_{16}" when the oscillation stabilization time set bit after release of the STP instruction is "0". On the other hand, timer 1 and prescaler 12 are not set when the above bit is "1". Accordingly, set the wait time fit for the oscillation stabilization time of the oscillator to be used. When an external interrupt is accepted, oscillation is restarted but the internal clock ϕ remains at "H" until timer 1 underflows. As soon as timer 1 underflows, the internal clock ϕ is supplied. This is because when a ceramic resonator is used, some time is required until a start of oscillation. In case oscillation is restarted by reset, no wait time is generated. So apply an "L" level to the $\overline{\text{RESET}}$ pin while oscillation becomes stable, or set the wait time by on-chip oscillator operation after system is released from reset until the oscillation is stabled.

• Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted. To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to "1" before the STP or WIT instruction is executed.

• Note

For use with the oscillation stabilization set bit after release of the STP instruction set to "1", set values in timer 1 and prescaler 12 after fully appreciating the oscillation stabilization time of the oscillator to be used.

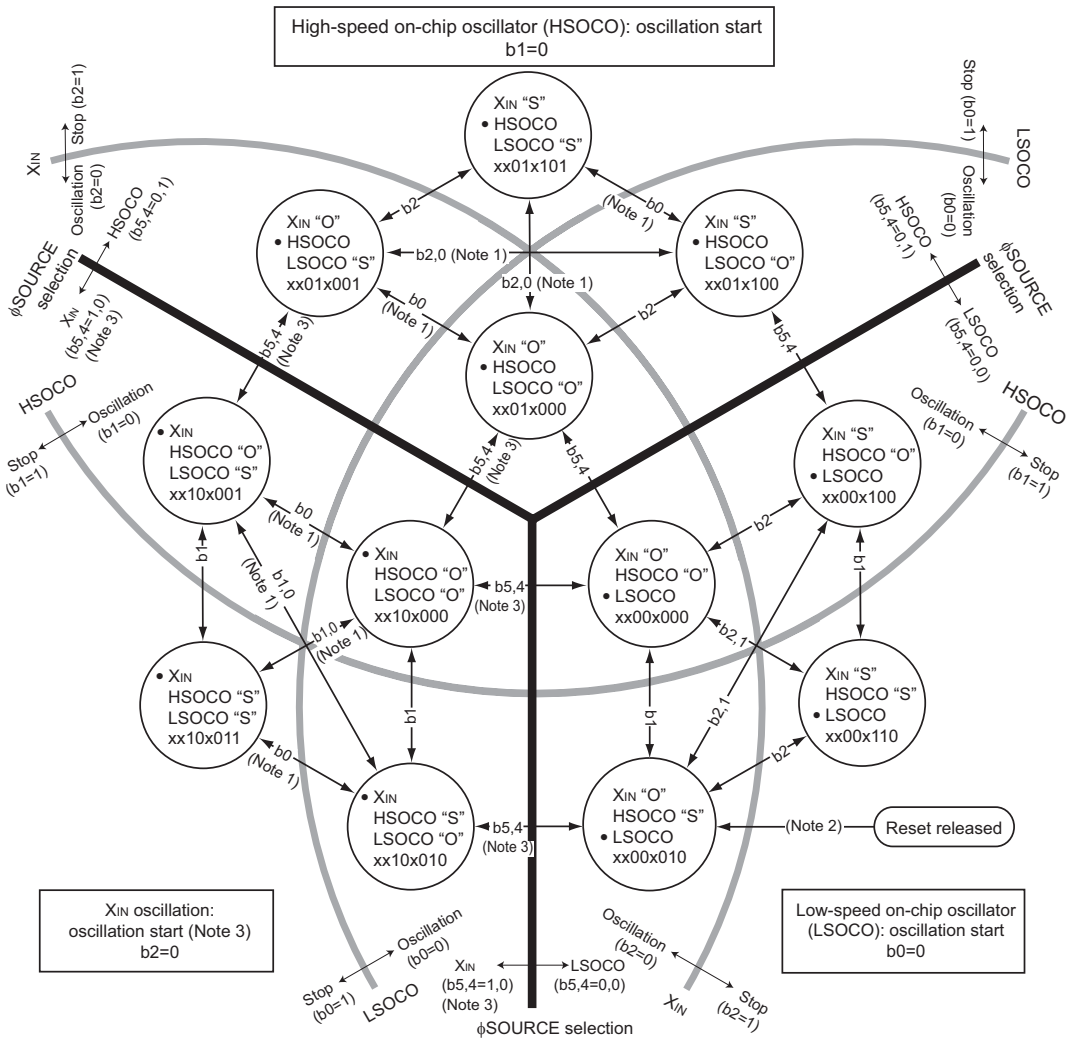


Notes 1: The oscillation circuit is built in the P20/XOUT/XCOUT pin and the P21/XIN/XCIN pin. When the Vcc of the microcomputer is lower than the operation lower bound voltage even if these pins are used as I/O ports, the oscillation circuit is connected and undefined values may be output from these pins.

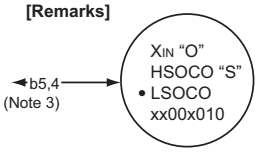
2: Although a feed-back resistor exists on-chip, an external feed-back resistor may be needed depending on conditions.

Fig 65. Block diagram of internal clock generating circuit

State transition of clock mode register CLKM (address: 0037$_{16}$) setting value and clock
(When X_{IN} oscillation is used. The same applies when X_{CIN} oscillation and external clock input are used.)



[Remarks]



X_{IN}, HSOCO, LSOCO, and respective oscillation and stop status in each mode are shown.
The symbol (•) indicates φSOURCE (oscillation) selected by the clock selection bits.
"O" indicates oscillation and "S" indicates stopping.
The values such as "xx00x010" indicate the values (binary) of the clock mode register in the mode.
The arrow (bx) indicates a bit in the clock mode register, showing a transition by changing the bit values.

Entering the mode should be performed according to the arrows. Wait mode and stop mode can be entered from all modes, and the original mode is returned after exiting.

Wait mode
- Low-speed on-chip oscillator: Status before executing WIT instruction is kept
- High-speed on-chip oscillator: Status before executing WIT instruction is kept
- X_{IN} oscillation: Status before executing the WIT instruction is kept

Stop mode
- Low-speed on-chip oscillator: Stopped (Note 1)
- High-speed on-chip oscillator: Stopped
- X_{IN} oscillation: Stopped

Notes 1: When stopping the low-speed on-chip oscillator is disabled by the low-speed on-chip oscillator control bit (bit 4 in FSROM2), "1" cannot be written to the bit 0 in CLKM. The low-speed on-chip oscillator does not stop even in stop mode.
2: After releasing reset, the low-speed on-chip oscillator is selected as φSOURCE and divided by 8 is selected as the CPU clock.
3: When the oscillation pins not used is set by the oscillation method selection bits (bits 1 and 0 in FSROM1), "10" cannot be written to bits 5 and 5 in CLKM. To use X_{IN} oscillation as φSOURCE, switch after X_{IN} oscillation is stabilized. Supply a stable clock when an external clock is used.
4: Do not change the values of the clock selection bits (bits 5 and 4) in CLKM and the individual clock oscillation control bits (bits 2 to 0) at the same time using a singe instruction. Always use different instructions to rewrite these values.
5: Wait until the oscillation used in the destination mode is stabilized before entering.

Fig 66. φSOURCE state transition

• Oscillation stop detection circuit

The oscillation stop detection circuit is used to detect an oscillation stop when a ceramic resonator or oscillation circuit stops due to disconnection. To use the oscillation stop detection circuit, set the low-speed on-chip oscillator to start operating.

The oscillation stop detection circuit is enabled by setting the XIN oscillation stop detection function active bit to 1. While this circuit is enabled, the operating status of the XIN oscillation circuit is monitored using the low-speed on-chip oscillator. If an oscillation stop is detected, the oscillation stop detection status bit is set to 1. If the oscillation stop detection reset enable bit is also set to 1, an internal reset is triggered at oscillation stop detection.

The XIN oscillation stop detection function active bit and the oscillation stop detection status bit are not initialized if an oscillation stop detection reset is triggered and these bits retain their value of 1. Since these bits are initialized to 0 by an external reset, an oscillation stop detection reset can be determined by checking the oscillation stop status bit.

The oscillation stop detection status bit is set to 0 by writing 0 to the XIN oscillation stop detection function enable bit.

To enable the oscillation detection circuit, first write 0 to the XIN oscillation stop detection function enable bit and set the oscillation stop detection status bit to 0. Then set the oscillation stop function to 1.

The XIN oscillation and external clock input are set as the clocks for oscillation stop detection. Refer to the electrical characteristics for the frequencies for oscillation stop detection.

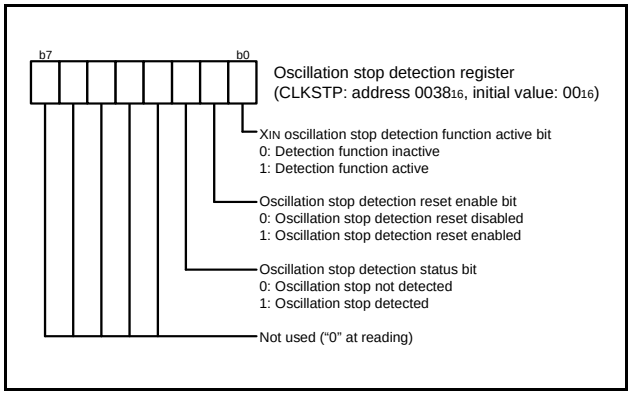


Fig 67. Structure of oscillation stop detection register

• Notes

(1) Do not execute the transition to “state 2’a” shown in Figure 68 State transition of oscillation stop detection circuit. In this state, no reset is triggered and the MCU is stopped even when the XIN oscillation stops.

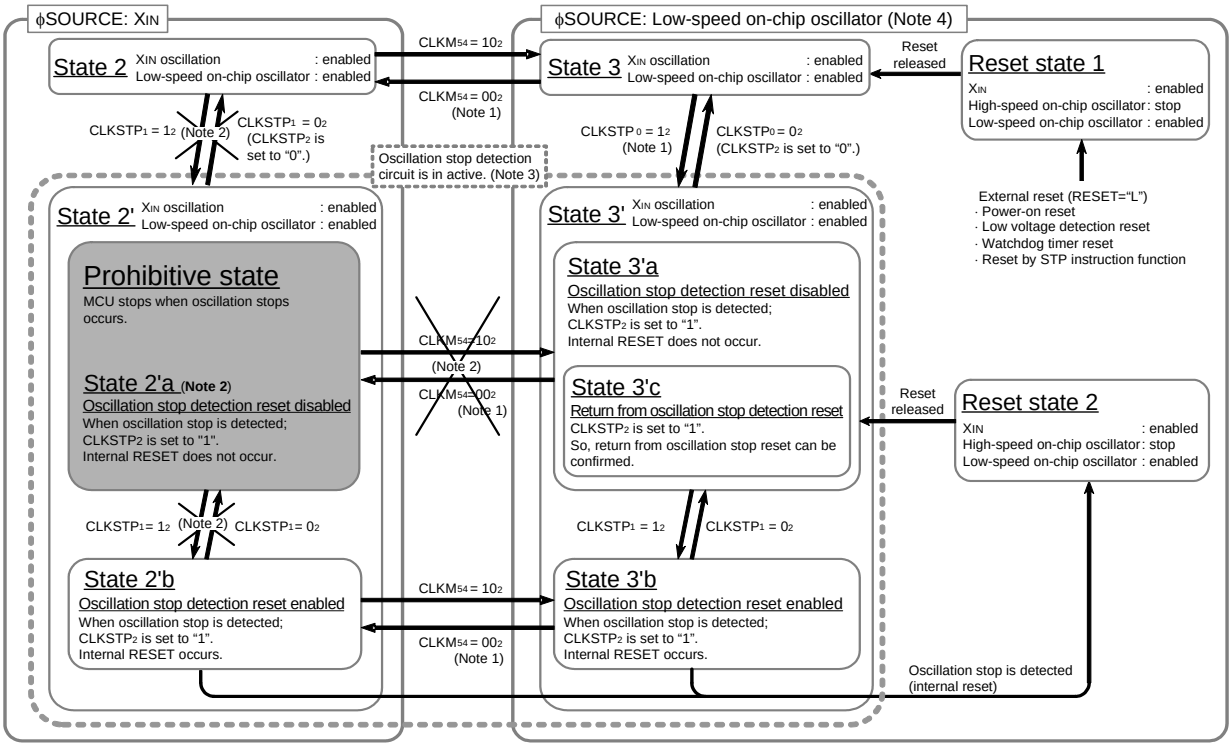
(2) After an oscillation stop detection reset, if this reset is enabled while bits XIN oscillation stop detection function active and oscillation stop detection status are retained, a reset is triggered again.

(3) The oscillation stop detection status bit is initialized under the following conditions:
- External reset, power-on reset, low-voltage detection reset, watchdog timer reset, and reset by the STP instruction function.
- Write 0 to the XIN oscillation stop detection function active bit

(4) While the oscillation stop detection function is in active, the oscillation stop detection status bit may set to 1 when the watchdog timer underflows or by a reset when the STP instruction is executed with the STP instruction function selection bit set to 1.

When an oscillation stop detection reset is triggered, reconfirm that oscillation is stopped.

(5) The oscillation stop detection circuit is not included in the emulator MCU “M37549RLSS”.



Notes on switch of clock

(1) Executing the state transition after stabilizing XIN oscillation.
(2) MCU cannot be returned by on-chip oscillator and its operation is stopped since internal reset does not occur at oscillation stop detected in state 2'a. Accordingly, do not execute the transition to state 2'a.
(3) STP instruction cannot be used when oscillation stop detection circuit is in active.
(4) The same applies when the high-speed on-chip oscillator is set as ϕSOURCE. Make sure that the low-speed on-chip oscillator should also oscillate. When a reset occurs, the high-speed on-chip oscillator stops.

Fig 68. State transition of oscillation stop detection circuit

QzROM Writing Mode

In the QzROM writing mode, the user ROM area can be written while the microcomputer is mounted on-board by using a serial programmer which is applicable for this microcomputer.
Table 10 lists the pin description (QzROM writing mode) and Figure 69 shows the pin connections.

Refer to Figure 70 and Figure 71 for examples of a connection with a serial programmer.
Contact the manufacturer of your serial programmer for serial programmer.
Refer to the user's manual of your serial programmer for details on how to use it.

Table 10 Pin description (QzROM writing mode)

Pin	Name	I/O	Function
V_{CC}, V_{SS}	Power source	Input	Apply 2.7 to 5.5 V to V_{CC}, and 0 V to V_{SS}.
RESET	Reset input	Input	Reset input pin.
$P2_1$ /X_{IN}	Clock input	Input	Set the same termination as the single-chip mode.
$P2_0$ /X_{OUT}	Clock output	Output	
$P0_0$ – $P0_5$ $P1_1$ – $P1_7$ $P3_0$, $P3_1$	I/O port	I/O	Input “H” or “L” level signal or leave the pin open.
CNV_{SS}	V_{PP} input	Input	QzROM programmable power source pin.
$P1_0$	ESDA I/O	I/O	Serial data I/O pin.
$P0_6$	ESCLK input	Input	Serial clock input pin.
$P0_7$	ESPGMB input	Input	Read/program pulse input pin.

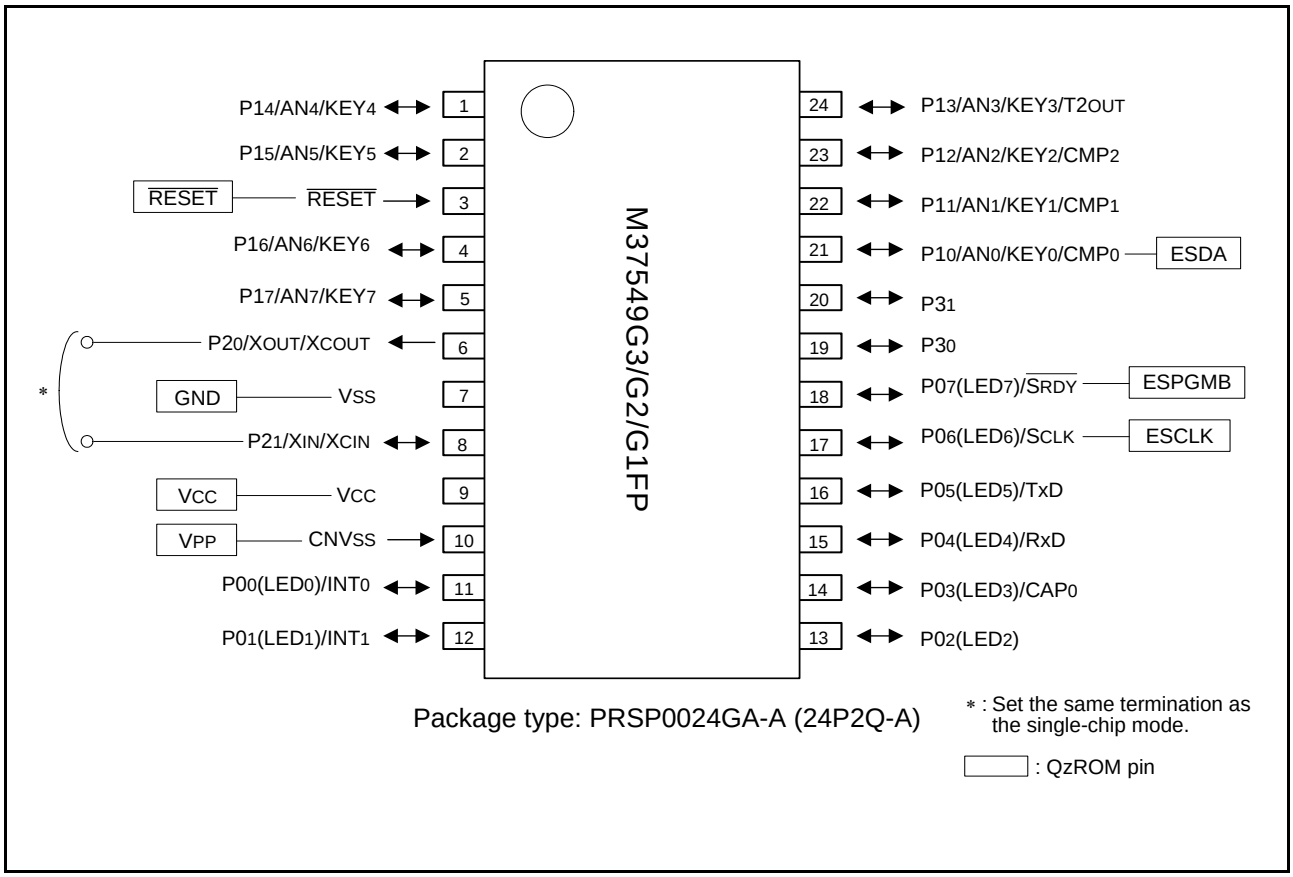
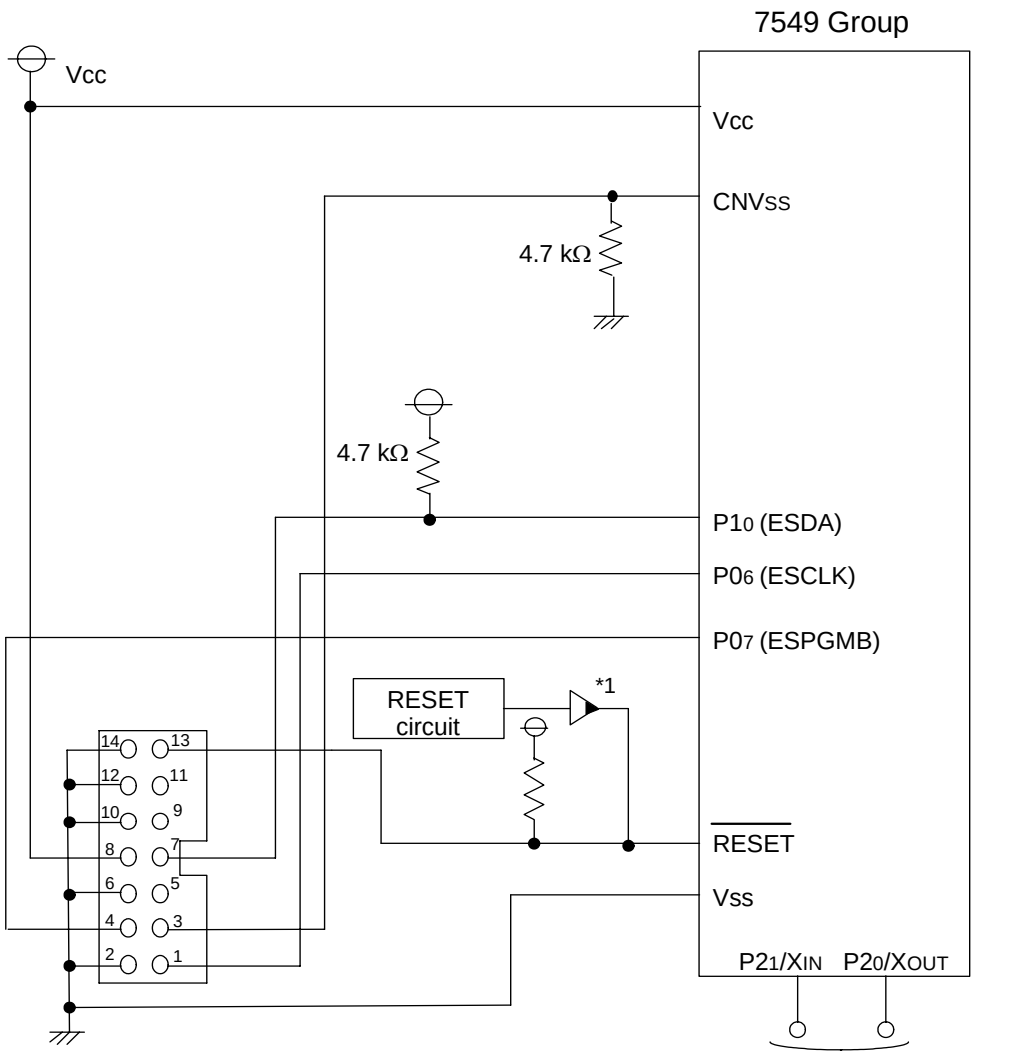


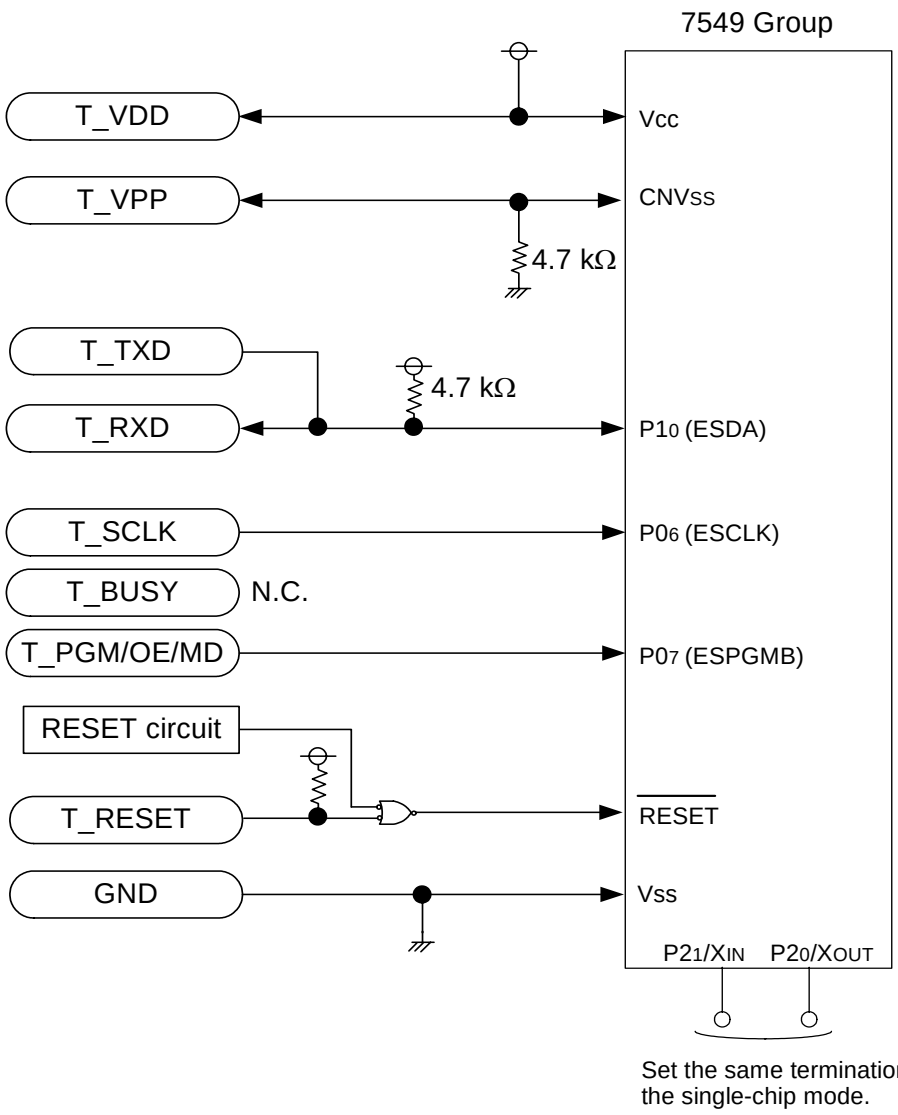
Fig 69. Pin connection diagram (M37549G3/G2/G1FP)



* 1: Open-collector buffer

Note : For the programming circuit, the wiring capacity of each signal pin must not exceed 47 pF

Fig 70. When using E8 programmer, connection example



Note: For the programming circuit, the wiring capacity of each signal pin must not exceed 47 pF.

Fig 71. When using programmer of Suisei Electronics System Co., LTD, connection example

NOTES ON PROGRAMMING

(1) Processor Status Register

The contents of the processor status register (PS) after reset are undefined except for the interrupt disable flag I which is "1". After reset, initialize flags which affect program execution. In particular, it is essential to initialize the T flag and the D flag because of their effect on calculations. Initialize these flags at the beginning of the program.

(2) Interrupts

The contents of the interrupt request bit do not change even if the BBC or BBS instruction is executed immediately after they are changed by program because this instruction is executed for the previous contents. For executing the instruction for the changed contents, execute one instruction before executing the BBC or BBS instruction.

(3) Decimal Calculations

- For calculations in decimal notation, set the decimal mode flag D to "1", then execute the ADC instruction or SBC instruction. In this case, execute SEC instruction, CLC instruction or CLD in-struction after executing one instruction before the ADC instruction or SBC instruction.
- In the decimal mode, the values of the N (negative), V (overflow) and Z (zero) flags are invalid.

(4) Ports

The values of the port direction registers cannot be read. That is, it is impossible to use the LDA instruction, memory operation instruction when the T flag is "1", addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS.
It is also impossible to use bit operation instructions such as CLB and SEB and read/modify/write instructions of direction registers for calculations such as ROR.
For setting direction registers, use the LDM instruction, STA in-struction, etc.

(5) A/D Conversion

Do not execute the STP instruction during A/D conversion.

(6) Instruction Execution Timing

The instruction execution time can be obtained by multiplying the frequency of the internal clock ϕ by the number of cycles mentioned in the machine-language instruction table.
The frequency of the internal clock ϕ is the same as that of the ϕSOURCE in double-speed mode, twice the ϕSOURCE cycle in high-speed mode, 4 times the ϕSOURCE cycle in middle-speed mode and 8 times the ϕSOURCE cycle in low-speed mode.

(7) CPU Mode Register

The processor mode bits can be written only once after releasing reset. Always set them to "00_2". After written, rewriting any data to these bits is disabled because they are locked. (Emulator MCU is excluded.)

(8) State transition

Do not stop the clock selected as the operation clock because of setting of bits 0 to 2.

NOTES ON HARDWARE

(1) Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (V_{CC} pin) and GND pin (V_{SS} pin). A ceramic capacitor of 0.01 μF to 0.1 μF is recommended.
Connect a capacitor across the power source pin and GND pin with the shortest possible wiring.

(2) Note on Power Source Voltage

When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.
In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the supply voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

NOTES ON USE

Countermeasures against noise

It is necessary not only design the system taking measures against the noise as follows but to evaluate before actual use.

1. Shortest wiring length

(1) Package

Select the smallest possible package to make the total wiring length short.

<Reason>

The wiring length depends on a microcomputer package. Use of a small package, for example QFP and not DIP, makes the total wiring length short to reduce influence of noise.

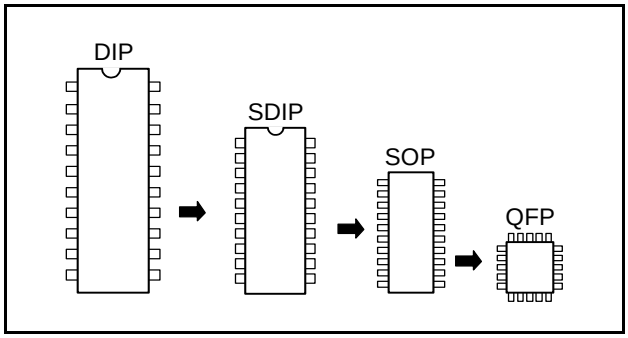


Fig 72. Selection of packages

(2) Wiring for $\overline{\text{RESET}}$ pin

Make the length of wiring which is connected to the $\overline{\text{RESET}}$ pin as short as possible. Especially, connect a capacitor across the $\overline{\text{RESET}}$ pin and the Vss pin with the shortest possible wiring (within 20 mm).

<Reason>

The width of a pulse input into the $\overline{\text{RESET}}$ pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the $\overline{\text{RESET}}$ pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

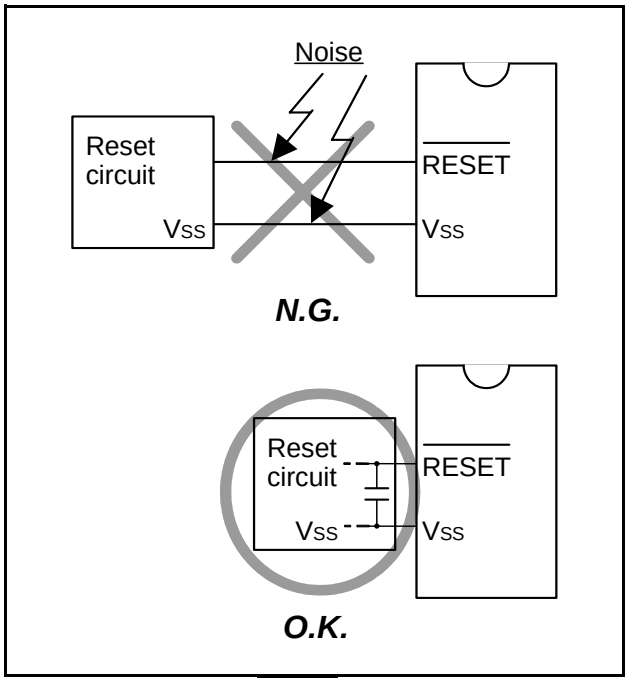


Fig 73. Wiring for the $\overline{\text{RESET}}$ pin

(3) Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20 mm) across the grounding lead of a capacitor which is connected to an oscillator and the Vss pin of a microcomputer as short as possible.
- Separate the Vss pattern only for oscillation from other Vss patterns.

<Reason>

If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the Vss level of a microcomputer and the Vss level of an oscillator, the correct clock will not be input in the microcomputer.

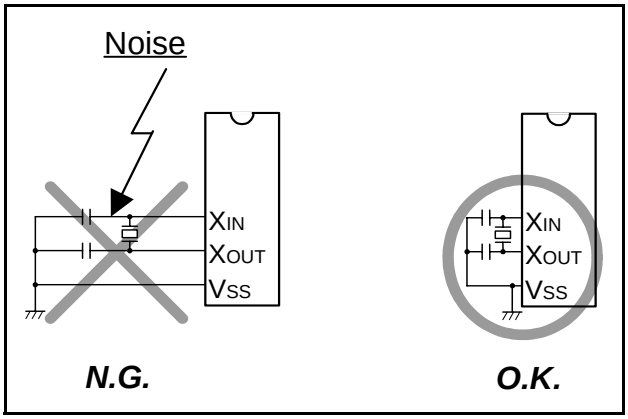


Fig 74. Wiring for clock I/O pins

(4) Wiring to CNVss pin

Connect CNVss pin to a GND pattern at the shortest distance. The GND pattern is required to be as close as possible to the GND supplied to Vss.

In order to improve the noise reduction, to connect a 5 kΩ resistor serially to the CNVss pin - GND line may be valid.

As well as the above-mentioned, in this case, connect to a GND pattern at the shortest distance. The GND pattern is required to be as close as possible to the GND supplied to Vss.

<Reason>

The CNVss pin of the QzROM is the power source input pin for the built-in QzROM. When programming in the built-in QzROM, the impedance of the CNVss pin is low to allow the electric current for writing flow into the QzROM. Because of this, noise can enter easily. If noise enters the CNVss pin, abnormal instruction codes or data are read from the built-in QzROM, which may cause a program runaway.

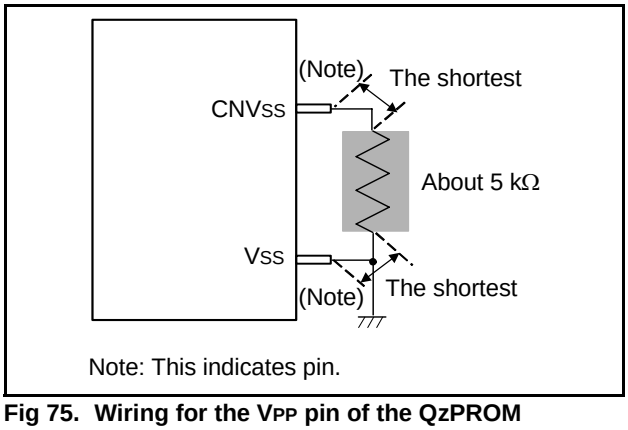


Fig 75. Wiring for the VPP pin of the QzPROM

2. Connection of bypass capacitor across Vss line and Vcc line

Connect an approximately 0.1 µF bypass capacitor across the VSS line and the VCC line as follows:

- Connect a bypass capacitor across the VSS pin and the VCC pin at equal length.
- Connect a bypass capacitor across the VSS pin and the VCC pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for VSS line and VCC line.
- Connect the power source wiring via a bypass capacitor to the VSS pin and the VCC pin.

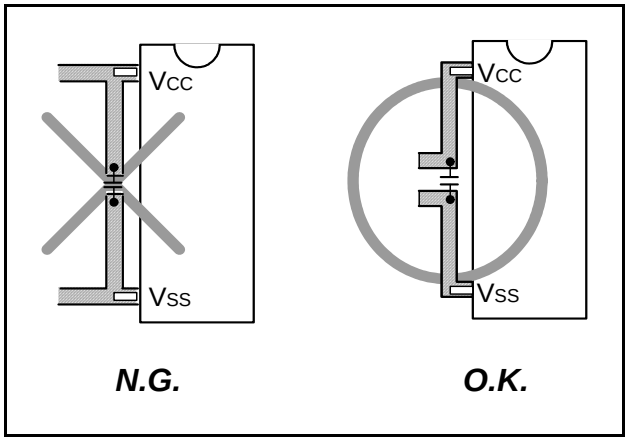


Fig 76. Bypass capacitor across the Vss line and the Vcc line

3. Wiring to analog input pins

The analog input pin is connected to the capacitor of a voltage comparator. Accordingly, sufficient accuracy may not be obtained by the charge/discharge current at the time of A/D conversion when the analog signal source of high-impedance is connected to an analog input pin. In order to obtain the A/D conversion result stabilized more, please lower the impedance of an analog signal source, or add the smoothing capacitor to an analog input pin.

4. Oscillator concerns

Take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

(1) Keeping oscillator away from large current signal lines

Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

<Reason>

In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

(2) Installing oscillator away from signal lines where potential levels change frequently

Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

<Reason>

Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

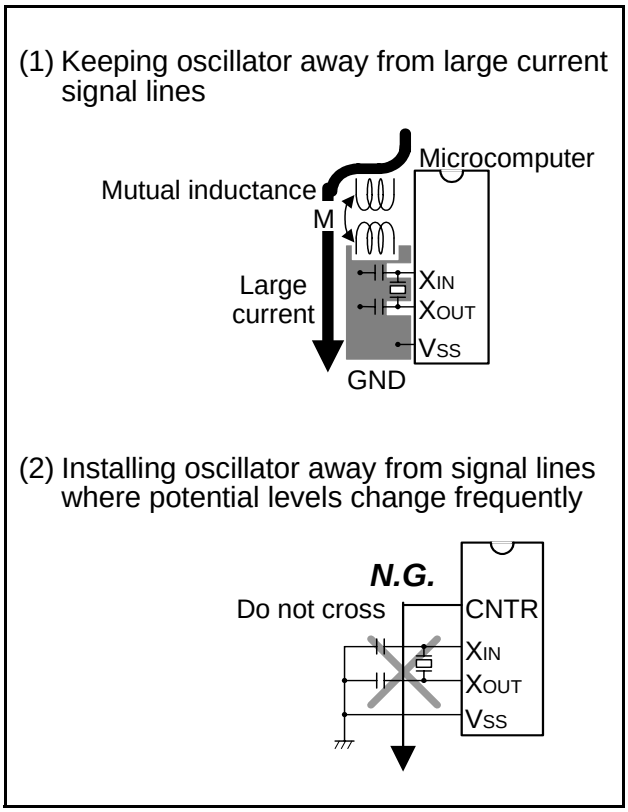


Fig 77. Wiring for a large current signal line/Writing of signal lines where potential levels change frequently

(3) Oscillator protection using VSS pattern

As for a two-sided printed circuit board, print a VSS pattern on the underside (soldering side) of the position (on the component side) where an oscillator is mounted.

Connect the VSS pattern to the microcomputer VSS pin with the shortest possible wiring. Besides, separate this VSS pattern from other VSS patterns.

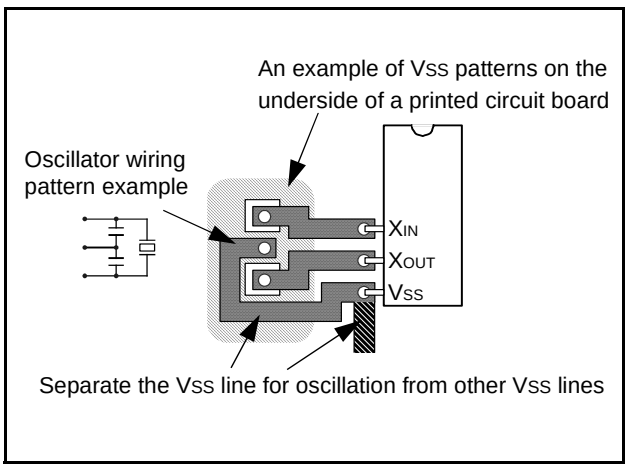


Fig 78. Vss pattern on the underside of an oscillator

5. Setup for I/O ports

Setup I/O ports using hardware and software as follows:

<Hardware>
- Connect a resistor of 100 Ω or more to an I/O port in series.

<Software>
- As for an input port, read data several times by a program for checking whether input levels are equal or not.
- As for an output port, since the output data may reverse because of noise, rewrite data to its port latch at fixed periods.
- Rewrite data to direction registers and pull-up control registers at fixed periods.

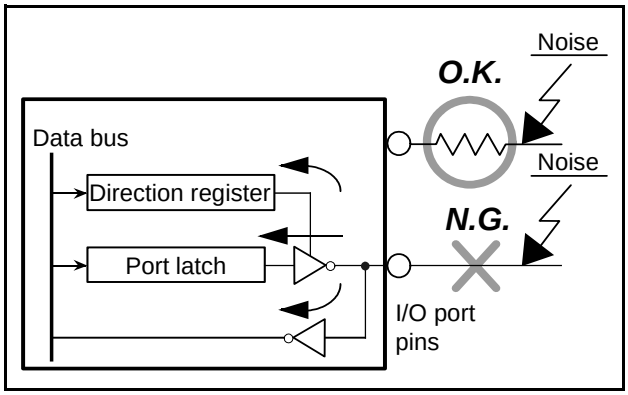


Fig 79. Setup for I/O ports

6. Providing of watchdog timer function by software

If a microcomputer runs away because of noise or others, it can be detected by a software watchdog timer and the microcomputer can be reset to normal operation. This is equal to or more effective than program runaway detection by a hardware watchdog timer. The following shows an example of a watchdog timer provided by software.
In the following example, to reset a microcomputer to normal operation, the main routine detects errors of the interrupt processing routine and the interrupt processing routine detects errors of the main routine.
This example assumes that interrupt processing is repeated multiple times in a single main routine processing.

<The main routine>
- Assigns a single byte of RAM to a software watchdog timer (SWDT) and writes the initial value N in the SWDT once at each execution of the main routine. The initial value N should satisfy the following condition:
  N + 1 ≥ (Counts of interrupt processing executed in each main routine)
  As the main routine execution cycle may change because of an interrupt processing or others, the initial value N should have a margin.
- Watches the operation of the interrupt processing routine by comparing the SWDT contents with counts of interrupt processing after the initial value N has been set.
- Detects that the interrupt processing routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:
  If the SWDT contents do not change after interrupt processing.

<The interrupt processing routine>
- Decrements the SWDT contents by 1 at each interrupt processing.
- Determines that the main routine operates normally when the SWDT contents are reset to the initial value N at almost fixed cycles (at the fixed interrupt processing count).
- Detects that the main routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:
  If the SWDT contents are not initialized to the initial value N but continued to decrement and if they reach 0 or less.

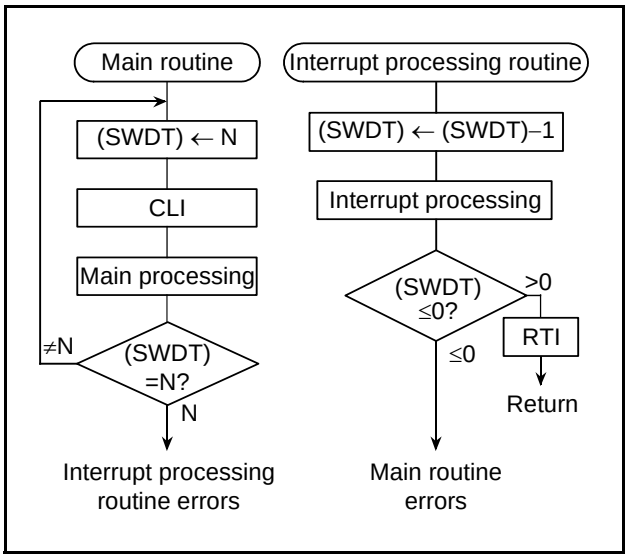


Fig 80. Watchdog timer by software

NOTES ON QzROM

Product shipped in blank

As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approx.0.1 % may occur.

Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

Overvoltage

Take care not to apply the voltage above the Vcc pin voltage to other pins. Make sure that the voltage of the CNVSS pin (VPP power input pin for QzROM) does not change as shown in the bold-lined periods (Figure 81) when powering on and off. If the voltage changes as shown, the QzROM contents may be rewritten.

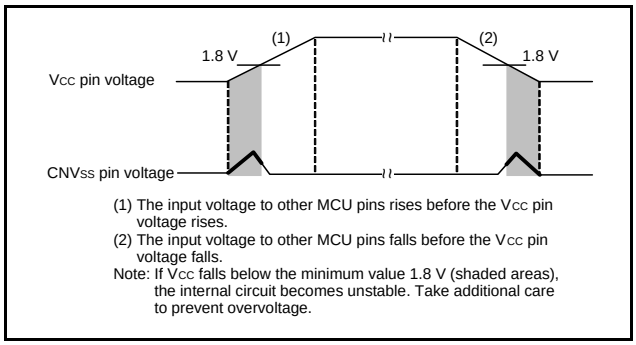


Fig 81. Timing Diagram (bold-lined periods are applicable)

Notes On QzROM Writing Orders

When ordering the QzROM product shipped after writing, submit the mask file (extension: .mask) which is made by the mask file converter MM.

- Be sure to set the ROM option data* setup when making the mask file by using the mask file converter MM.. The ROM code protect is specified according to the ROM option data* in the mask file which is submitted at ordering. Note that the mask file which has nothing at the ROM option data* or has the data other than "00$_{16}$" and "FF$_{16}$" can not be accepted.
- Set "FF$_{16}$" to the ROM code protect address in ROM data regardless of the presence or absence of a protect. When data other than "FF$_{16}$" is set, we may ask that the ROM data be submitted again.

* ROM option data: mask option noted in MM

<DATA REQUIRED FOR QzROM WRITING ORDERS

The following are necessary when ordering a QzROM product shipped after writing:

1. QzROM Writing Confirmation Form*
2. Mark Specification Form*
3. ROM data ..... Mask file

* For the QzROM writing confirmation form and the mark specification form, refer to the "Renesas Technology Corp." Homepage (http://www.renesas.com/homepage.jsp).

Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

ELECTRICAL CHARACTERISTICS of 7549 Group

(1) Absolute Maximum Ratings

Table 11 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. When an input voltage is measured, output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P3_0$, $P3_1$		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage $\overline{RESET}$		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage CNV_{SS}		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P3_0$, $P3_1$		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	T_a = 25 °C	300	mW
T_{opr}	Operating temperature	–	–20 to 85	°C
T_{stg}	Storage temperature	–	–40 to 125	°C

(2) Recommended Operating Conditions

Table 12 Recommended operating conditions (1)

(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter				Limits			Unit
					Min.	Typ.	Max.	
V_{CC}	Power source voltage	High-speed on-chip oscillator	Double-, high-, middle-, low-speed mode		4.0	5.0	5.5	V
		Low-speed on-chip oscillator	Double-, high-, middle-, low-speed mode		1.8	5.0	5.5	V
		X_{IN} oscillation, external clock input	Double-speed mode	$f(X_{IN}) \leq 8$MHz	4.5	5.0	5.5	V
				$f(X_{IN}) \leq 2$MHz	2.4	5.0	5.5	V
				$f(X_{IN}) \leq 1$MHz	2.2	5.0	5.5	V
			High-, middle-, low-speed mode	$f(X_{IN}) \leq 8$MHz	4.0	5.0	5.5	V
				$f(X_{IN}) \leq 4$MHz	2.4	5.0	5.5	V
				$f(X_{IN}) \leq 1$MHz	1.8	5.0	5.5	V
		X_{CIN} oscillation	Double-, high-, middle-, low-speed mode	$f(X_{CIN}) \leq 50$kHz	1.8	5.0	5.5	V
V_{SS}	Power source voltage					0		V
V_{IH}	"H" input voltage (Note 4) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_1$, $P3_0$, $P3_1$				0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage (Note 5) $\overline{RESET}$, X_{IN}, X_{CIN}				0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage (Note 4) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_1$, $P3_0$, $P3_1$				0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$, CNV_{SS}				0		0.2V_{CC}	V
V_{IL}	"L" input voltage (Note 5) X_{IN}, X_{CIN}				0		0.16V_{CC}	V
$\Sigma I_{OH(peak)}$	"H" total peak output current (Notes 1, 4) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P3_0$, $P3_1$						–60	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (Note 1) $P0_0$–$P0_7$						60	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (Notes 1, 4) $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P3_0$, $P3_1$						60	mA
$\Sigma I_{OH(avg)}$	"H" total average output current (Notes 1, 4) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P3_0$, $P3_1$						–30	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (Note 1) $P0_0$–$P0_7$						30	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (Notes 1, 4) $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P3_0$, $P3_1$						30	mA
$I_{OH(peak)}$	"H" peak output current (Notes 2, 4) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P3_0$, $P3_1$						–10	mA
$I_{OL(peak)}$	"L" peak output current (Notes 2, 4) $P0_0$–$P0_7$ (drive capacity: weakness), $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P3_0$, $P3_1$						10	mA
$I_{OL(peak)}$	"L" peak output current (Note 2) $P0_0$–$P0_7$ (drive capacity: strength)						30	mA
$I_{OH(avg)}$	"H" average output current (Notes 3, 4) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P3_0$, $P3_1$						–5	mA
$I_{OL(avg)}$	"L" average output current (Notes 3, 4) $P0_0$–$P0_7$ (drive capacity: weakness), $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P3_0$, $P3_1$						5	mA
$I_{OL(avg)}$	"L" average output current (Notes 3) $P0_0$–$P0_7$ (drive capacity: strength)						15	mA

NOTES:
1. The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2. The peak output current is the peak current flowing in each port.
3. The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100 ms.
4. $P2_0$ and $P2_1$ indicates these pins are used as I/O ports.
5. X_{IN} and X_{CIN} indicates these pins are used as clock pins.

Table 13 Recommended operating conditions (2)

(Vcc = 1.8 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter				Limits			Unit
					Min.	Typ.	Max.	
f(XIN)	XIN oscillation frequency (Note 1)	XIN oscillation External clock input	Double-speed mode	Vcc = 4.5–5.5 V			8	MHz
				Vcc = 2.4–4.5 V			$\frac{(Vcc - 2.4) \times 2}{0.7} + 2$	MHz
				Vcc = 2.2–2.4 V			$\frac{(Vcc - 2.2)}{0.2} + 1$	MHz
			High-, middle-, low-speed mode	Vcc = 4.0–5.5 V			8	MHz
				Vcc = 2.4–4.0 V			$\frac{(Vcc - 2.4)}{0.4} + 4$	MHz
				Vcc = 1.8–2.4 V			$\frac{(Vcc - 1.8)}{0.2} + 1$	MHz
	XCIN oscillation frequency (Note 1)	XCIN oscillation	Double-, high-, middle-, low-speed mode	Vcc = 1.8–5.5 V		32.768	50	kHz

NOTE:
1. When the oscillation frequency has a duty cycle of 50 %.

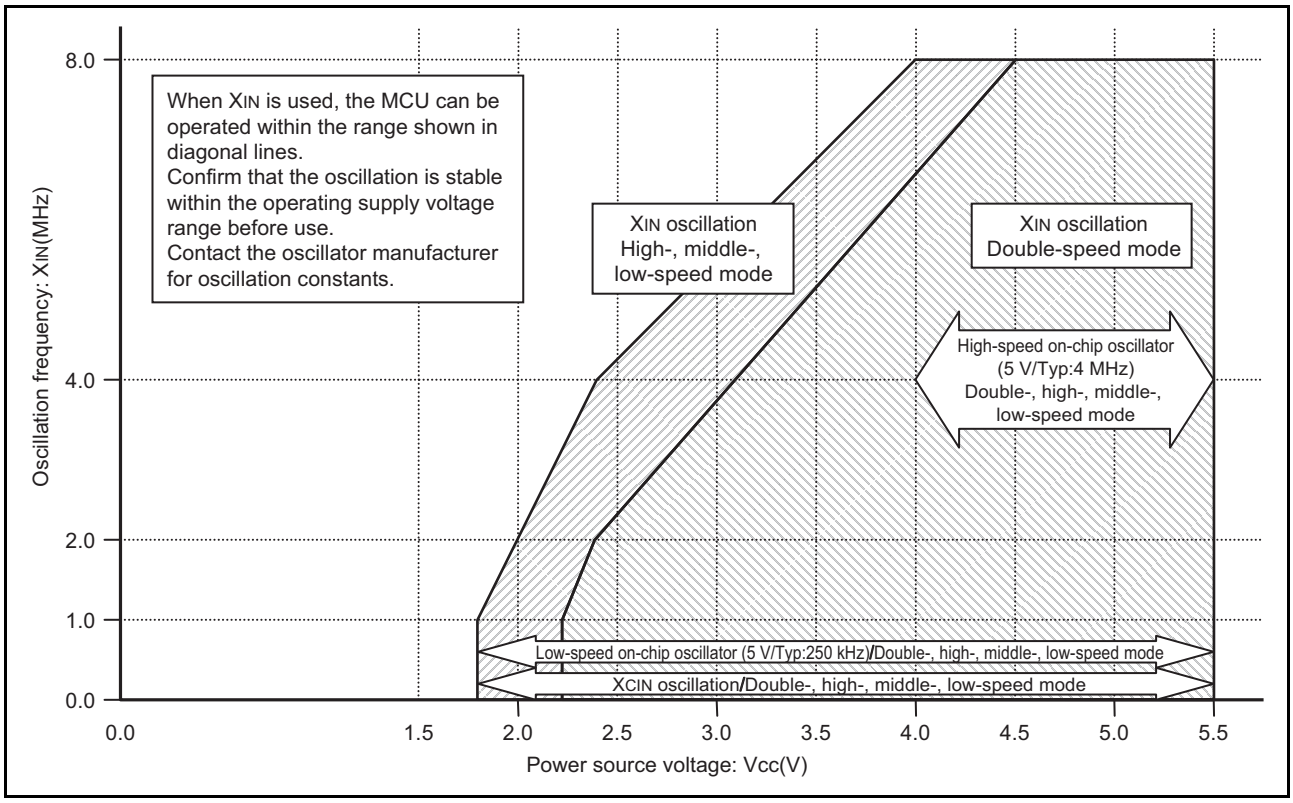


Fig 82. Power source voltage and oscillation frequency

(3) Electrical Characteristics

Table 14 Electrical characteristics (1)

(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage (Notes 1, 3) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_1$, $P3_0$, $P3_1$	I_{OH} = –5 mA, Vcc = 4.0–5.5 V	Vcc–1.5			V
		I_{OH} = –1.0 mA, Vcc = 1.8–5.5 V	Vcc–1.0			V
V_{OL}	"L" output voltage (Note 1) $P0_0$–$P0_7$ (drive capacity: weakness) $P1_0$–$P1_7$, $P2_1$, $P3_0$, $P3_1$	I_{OL} = 5 mA, Vcc = 4.0–5.5 V			1.5	V
		I_{OL} = 1.5 mA, Vcc = 4.0–5.5 V			0.3	V
		I_{OL} = 1.0 mA, Vcc = 1.8–5.5 V			1.0	V
V_{OL}	"L" output voltage $P0_0$–$P0_7$ (drive capacity: strength)	I_{OL} = 15 mA, Vcc = 4.0–5.5 V			2.0	V
		I_{OL} = 1.5 mA, Vcc = 4.0–5.5 V			0.3	V
		I_{OL} = 1.0 mA, Vcc = 1.8–5.5 V			1.0	V
$V_{T+} - V_{T-}$	Hysteresis INT_0, INT_1, CAP_0, $P1_0$–$P1_7$ (Note 4), RxD, SCLK, $\overline{RESET}$			0.5		V
I_{IH}	"H" input current (Note 1) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_1$, $P3_0$, $P3_1$	V_I = Vcc (Pin floating. Pull up transistors is disable)			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$	V_I = Vcc			5	µA
I_{IH}	"H" input current (Note 2) X_{IN}	V_I = Vcc		4.0		µA
I_{IH}	"H" input current (Note 2) X_{CIN}	V_I = Vcc		0.5		µA
I_{IL}	"L" input current (Note 1) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_1$, $P3_0$, $P3_1$	V_I = Vss (Pin floating. Pull up transistors is disable)			–5.0	µA
I_{IL}	"L" input current $\overline{RESET}$	V_I = Vss			–0.7	mA
I_{IL}	"L" input current (Note 2) X_{IN}	V_I = Vss		–4.0		µA
I_{IL}	"L" input current (Note 2) X_{CIN}	V_I = Vss		–0.3		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$	V_I = Vss (Pull up transistors is enable)		–0.2	–0.5	mA
R_{PH}	Pull-up resistor value $\overline{RESET}$	V_I = Vss		25		kΩ
V_{RAM}	RAM hold voltage	When clock stopped	1.6		5.5	V
R_{HSOCO}	High-speed on-chip oscillator oscillation frequency	Vcc = 4.0–5.5 V, Ta = 0–50 °C	3.8	4	4.2	MHz
		Vcc = 4.0–5.5 V, Ta = –20–85 °C	3.6	4	4.4	
R_{LSOCO}	Low-speed on-chip oscillator oscillation frequency	Vcc = 5.0 V, Ta = 25 °C	125	250	500	kHz
D_{OSC}	Oscillation stop detection circuit detection frequency	Vcc = 5.0 V, Ta = 25 °C	62.5	150	250	kHz

NOTES:
1. $P2_0$ and $P2_1$ indicates these pins are used as I/O ports.
2. X_{IN} and X_{CIN} indicates these pins are used as clock pins.
3. $P0_5$ is measured when the $P0_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
4. It is available only when operating key-on wake up.

Table 15 Electrical characteristics (2)

(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = −20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
Icc	Power source current	High-speed on-chip oscillator: oscillation · Vcc = 5.0 V · Low-speed on-chip oscillator: stop · XIN: stop · Output transistors “off” · Low voltage detection circuit: enable	Double-speed mode		2.5	5.2	mA
			Low-speed mode		0.6	1.7	mA
			Wait mode, functions except timer 1 disabled		0.35	1.0	mA
		Low-speed on-chip oscillator: oscillation · Vcc = 5.0 V · High-speed on-chip oscillator: stop · XIN: stop · Output transistors “off” · Low voltage detection circuit: enable	Double-speed mode		230	600	µA
			Low-speed mode		120	400	µA
			Wait mode, functions except timer 1 disabled		105	350	µA
		f(XIN)=8 MHz (ceramic resonator) · Vcc = 5.0 V · High-speed on-chip oscillator: stop · Low-speed on-chip oscillator: stop · Output transistors “off” · Low voltage detection circuit: enable	Double-speed mode		6.0	10	mA
			Low-speed mode		2.6	6.0	mA
			Wait mode, functions except timer 1 disabled		1.9	5.0	mA
		f(XCIN)=32.768 kHz · Vcc = 5.0 V · High-speed on-chip oscillator: stop · Low-speed on-chip oscillator: stop · Output transistors “off” · Low voltage detection circuit: enable	Double-speed mode		100	200	µA
			Low-speed mode		85	180	µA
			Wait mode, functions except timer 1 disabled		80	170	µA
		Low-speed on-chip oscillator: oscillation · Vcc = 2.0 V · High-speed on-chip oscillator: stop · XIN: stop · Output transistors “off” · Low voltage detection circuit: enable	Low-speed mode		25	70	µA
			Wait mode, functions except timer 1 disabled		23	60	µA
		f(XIN) = 2 MHz (ceramic resonator) · Vcc = 2.0 V · High-speed on-chip oscillator: stop · Low-speed on-chip oscillator: stop · Output transistors “off” · Low voltage detection circuit: enable	Low-speed mode		190	450	µA
			Wait mode, functions except timer 1 disabled		150	430	µA
		f(XCIN) = 32.768 kHz · Vcc = 2.0 V · High-speed on-chip oscillator: stop · Low-speed on-chip oscillator: stop · Output transistors “off” · Low voltage detection circuit: enable	Low-speed mode		24	65	µA
			Wait mode, functions except timer 1 disabled		23	55	µA
		Low voltage detection circuit self consumption current	Ta = 25 °C Vcc = 5.0 V		70		µA
			Ta = 25 °C Vcc = 2.0 V		20		µA
		Increment when A/D conversion is executed f(XIN) = 8 MHz, Vcc = 5.0 V			0.5		mA
		Stop mode · Output transistors “off” · Low-speed on-chip oscillator: stop · Low voltage detection circuit: stop	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	µA

(4) A/D Converter Characteristics

Table 16 A/D Converter characteristics

(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
———	Resolution				10	bits
———	Absolute accuracy (excluding quantization error)	Ta = –20–85 °C, 2.7 ≤ Vcc ≤ 5.5 V			3	LSB
t_{CONV}	Conversion time	A/D conversion clock = f(φSOURCE)/2			122	tc(φSOURCE)
		A/D conversion clock = f(φSOURCE)			61	tc(φSOURCE)
R_{LADDER}	Ladder resistor			55		kΩ
$I_{I(AD)}$	A/D port input current				5.0	μA

Table 17 A/D Converter Recommended Operating Conditions

(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage	Ta = –20–85 °C	2.7		5.5	V
$\phi_{(AD)}$	A/D conversion clock frequency (Note)	4.0 ≤ Vcc ≤ 5.5 V	0.016		8	MHz
		2.7 ≤ Vcc < 4.0 V	0.016		4	MHz

NOTE:
1. When X_{CIN} or the low-speed on-chip oscillator is selected as φSOURCE, the A/D converter cannot be used.

(5) Power-on reset circuit characteristics

Table 18 Power-on reset circuit characteristics

(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{POR}	Valid start voltage of power-on reset circuit (Note)				0	V
TW(V_{POR})	V_{POR} hold time		10			s
TW(V_{POR}-V_{DET})	Rising time of valid power source of power-on reset circuit	TW(V_{POR}) > 10s			20	ms

NOTE:
V_{POR} is the start voltage level of Vcc for the built-in power-on reset circuit to operate normally.
Keep V_{POR} to be lower than the Vcc voltage before rising of the Vcc power source to use the built-in power-on reset circuit.
Set the built-in low voltage detection circuit to be valid when the built-in power-on reset is used.

Table 19 Low voltage detection circuit characteristics

(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{LVD}	Valid start voltage of low voltage detection circuit (Note)		1.0			V
V_{DET}	Detection voltage of low voltage detection circuit	Ta = 0–50 °C	1.85	1.95	2.05	V
		Ta = –20–85 °C	1.80	1.95	2.10	V
T_{DET}	Detection time of low voltage detection circuit			20		µs

NOTE:
V_{LVD} is the start voltage level of Vcc for the built-in low voltage detection circuit to operate normally.
If the Vcc power source becomes lower than V_{LVD}, first set the Vcc voltage to be lower than V_{POR}. Next, according to the electrical characteristics of the power-on reset circuit, perform the rising of Vcc.

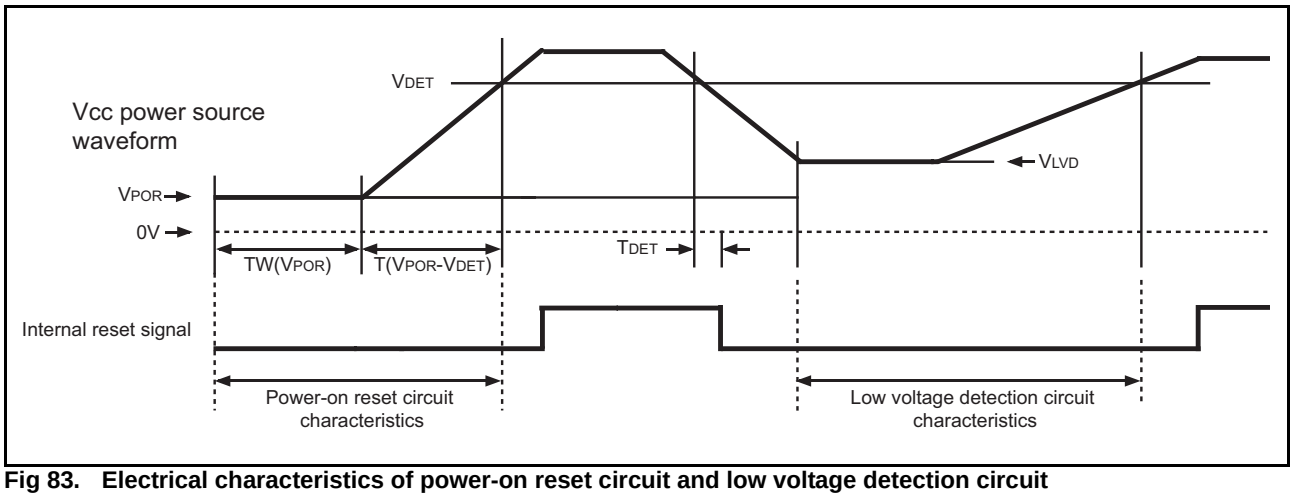


Fig 83. Electrical characteristics of power-on reset circuit and low voltage detection circuit

(6) Timing Requirements

Table 20 Timing requirements (1)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			μs
$t_{C(XIN)}$	External clock input cycle time	125			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	50			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	50			ns
$t_{WH(INT0)}$	INT_0, INT_1, CAP_0 input “H” pulse width (Note 1)	80			ns
$t_{WL(INT0)}$	INT_0, INT_1, CAP_0 input “L” pulse width (Note 1)	80			ns
$t_{C(SCLK)}$	Serial I/O clock input cycle time (Note 2)	800			ns
$t_{WH(SCLK)}$	Serial I/O clock input “H” pulse width (Note 2)	370			ns
$t_{WL(SCLK)}$	Serial I/O clock input “L” pulse width (Note 2)	370			ns
$t_{su(RXD-SCLK)}$	Serial I/O input set up time	220			ns
$t_{h(SCLK-RXD)}$	Serial I/O input hold time	100			ns

NOTES:
1. As for CAP_0, it is the value when noise filter is not used.
2. In this time, bit 6 of the serial I/O control register (address $001A_{16}$) is set to “1” (clock synchronous serial I/O is selected). When bit 6 of the serial I/O control register is “0” (clock asynchronous serial I/O is selected), the rating values are divided by 4.

Table 21 Timing requirements (2)

(V_{CC} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			μs
$t_{C(XIN)}$	External clock input cycle time	250			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	100			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	100			ns
$t_{WH(INT0)}$	INT_0, INT_1, CAP_0 input “H” pulse width (Note 1)	230			ns
$t_{WL(INT0)}$	INT_0, INT_1, CAP_0 input “L” pulse width (Note 1)	230			ns
$t_{C(SCLK)}$	Serial I/O clock input cycle time (Note 2)	2000			ns
$t_{WH(SCLK)}$	Serial I/O clock input “H” pulse width (Note 2)	950			ns
$t_{WL(SCLK)}$	Serial I/O clock input “L” pulse width (Note 2)	950			ns
$t_{su(RXD-SCLK)}$	Serial I/O input set up time	400			ns
$t_{h(SCLK-RXD)}$	Serial I/O input hold time	200			ns

NOTES:
1. As for CAP_0, it is the value when noise filter is not used.
2. In this time, bit 6 of the serial I/O control register (address $001A_{16}$) is set to “1” (clock synchronous serial I/O is selected). When bit 6 of the serial I/O control register is “0” (clock asynchronous serial I/O is selected), the rating values are divided by 4.

Table 22 Timing requirements (3)

(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = −20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			μs
$t_{C(XIN)}$	External clock input cycle time	500			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	200			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	200			ns
$t_{WH(INT0)}$	INT_0, INT_1, CAP_0 input “H” pulse width (Note 1)	460			ns
$t_{WL(INT0)}$	INT_0, INT_1, CAP_0 input “L” pulse width (Note 1)	460			ns
$t_{C(SCLK)}$	Serial I/O clock input cycle time (Note 2)	4000			ns
$t_{WH(SCLK)}$	Serial I/O clock input “H” pulse width (Note 2)	1900			ns
$t_{WL(SCLK)}$	Serial I/O clock input “L” pulse width (Note 2)	1900			ns
$t_{su(RXD-SCLK)}$	Serial I/O input set up time	800			ns
$t_{h(SCLK-RXD)}$	Serial I/O input hold time	400			ns

NOTES:
1. As for CAP_0, it is the value when noise filter is not used.
2. In this time, bit 6 of the serial I/O control register (address $001A_{16}$) is set to “1” (clock synchronous serial I/O is selected). When bit 6 of the serial I/O control register is “0” (clock asynchronous serial I/O is selected), the rating values are divided by 4.

(7) Switching Characteristics

Table 23 Switching characteristics (1)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WH}(SCLK)	Serial I/O clock output “H” pulse width	t_C(SCLK)/2–30			ns
t_{WL}(SCLK)	Serial I/O clock output “L” pulse width	t_C(SCLK)/2–30			ns
t_d(SCLK-TxD)	Serial I/O output delay time			140	ns
t_V(SCLK-TxD)	Serial I/O output valid time	–30			ns
t_r(SCLK)	Serial I/O clock output rising time			30	ns
t_f(SCLK)	Serial I/O clock output falling time			30	ns
t_r(CMOS)	CMOS output rising time (Note 1)		10	30	ns
t_f(CMOS)	CMOS output falling time (Note 1)		10	30	ns

NOTE:
1. Pin X_{OUT} is excluded.

Table 24 Switching characteristics (2)

(V_{CC} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WH}(SCLK)	Serial I/O clock output “H” pulse width	t_C(SCLK)/2–50			ns
t_{WL}(SCLK)	Serial I/O clock output “L” pulse width	t_C(SCLK)/2–50			ns
t_d(SCLK-TxD)	Serial I/O output delay time			350	ns
t_V(SCLK-TxD)	Serial I/O output valid time	–30			ns
t_r(SCLK)	Serial I/O clock output rising time			50	ns
t_f(SCLK)	Serial I/O clock output falling time			50	ns
t_r(CMOS)	CMOS output rising time (Note 1)		20	50	ns
t_f(CMOS)	CMOS output falling time (Note 1)		20	50	ns

NOTE:
1. Pin X_{OUT} is excluded.

Table 25 Switching characteristics (3)

(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WH}(SCLK)	Serial I/O clock output “H” pulse width	t_C(SCLK)/2–70			ns
t_{WL}(SCLK)	Serial I/O clock output “L” pulse width	t_C(SCLK)/2–70			ns
t_d(SCLK-TxD)	Serial I/O output delay time			450	ns
t_V(SCLK-TxD)	Serial I/O output valid time	–30			ns
t_r(SCLK)	Serial I/O clock output rising time			70	ns
t_f(SCLK)	Serial I/O clock output falling time			70	ns
t_r(CMOS)	CMOS output rising time (Note 1)		25	70	ns
t_f(CMOS)	CMOS output falling time (Note 1)		25	70	ns

NOTE:
1. Pin X_{OUT} is excluded.

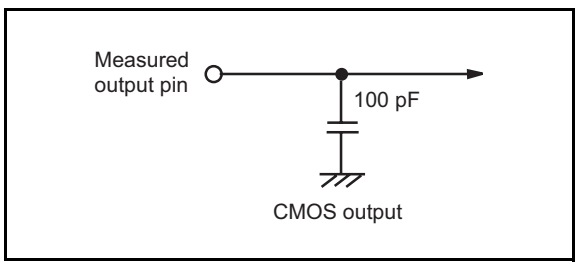


Fig 84. Switching characteristics measurement circuit diagram

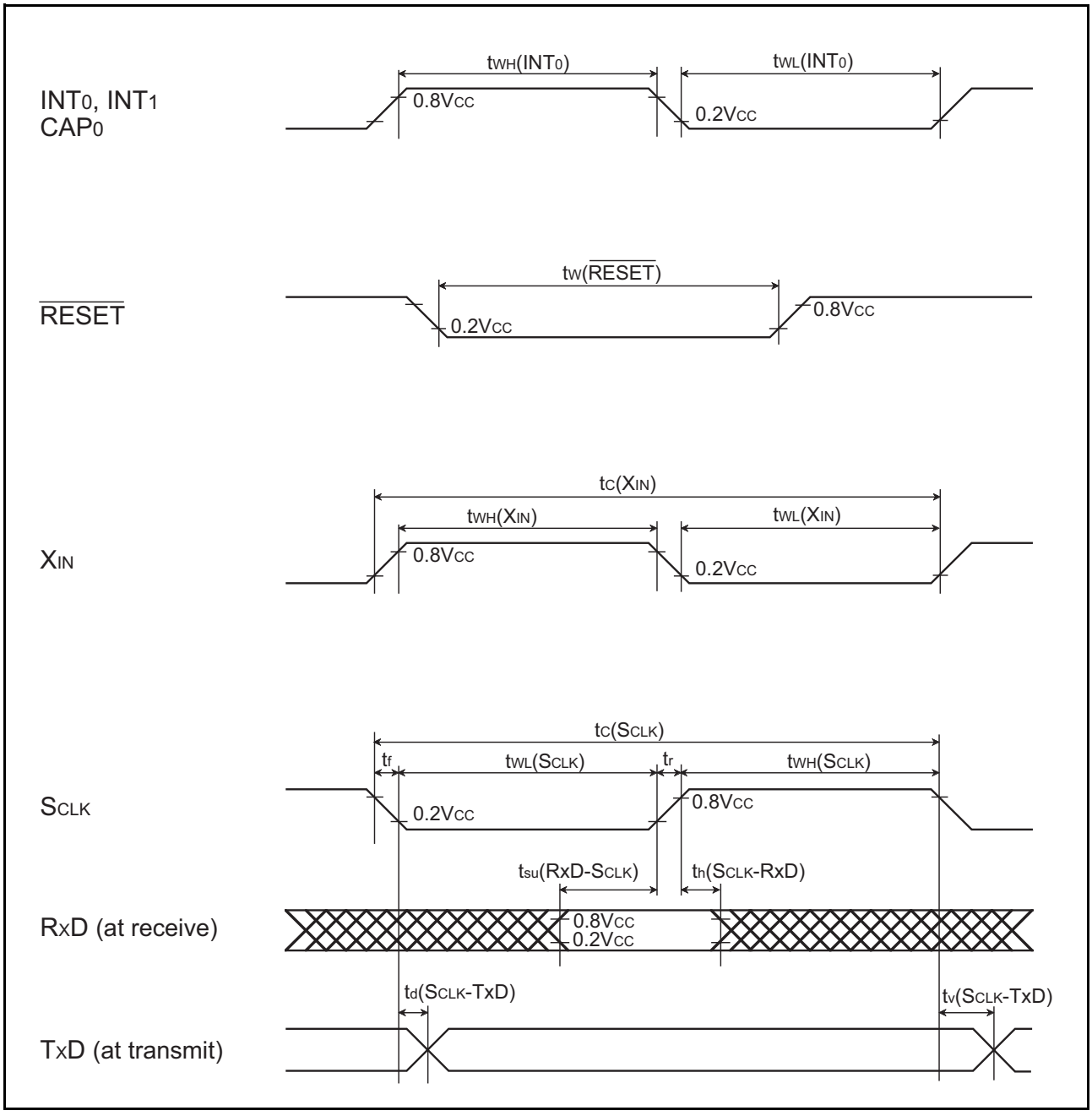
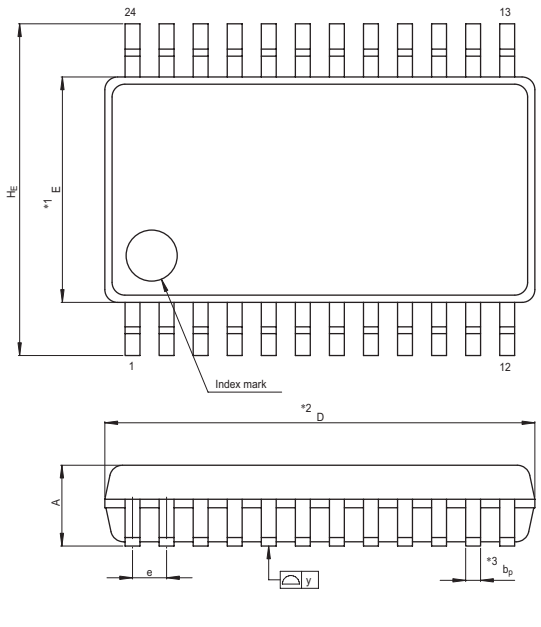


Fig 85. Timing chart

PACKAGE OUTLINE

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SSOP24-5.3x10.1-0.80	PRSP0024GA-A	24P2Q-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	10.0	10.1	10.2
E	5.2	5.3	5.4
A_2	—	1.8	—
A	—	—	2.1
A_1	0	0.1	0.2
b_p	0.3	0.35	0.45
c	0.18	0.2	0.25
θ	0°	—	8°
H_E	7.5	7.8	8.1
e	0.65	0.8	0.95
y	—	—	0.10
L	0.4	0.6	0.8

APPENDIX

Note on Programming

1. Processor Status Register

(1) Initialization of the processor status register

It is required to initialize the processor status register (PS) flags which affect program execution. It is particularly essential to initialize the T and D flags because of their effect on calculations. Initialize these flags at the beginning of the program.

<Reason>

At a reset, the contents of the processor status register (PS) are undefined except for the I flag which is "1".

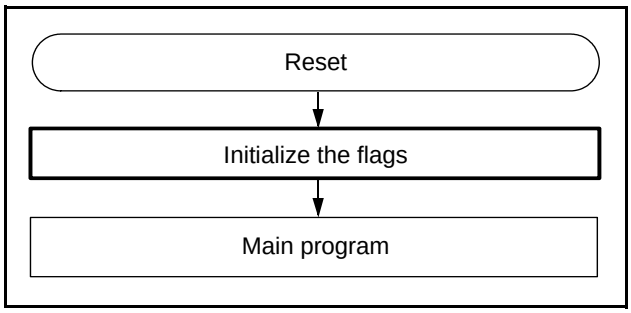


Fig. 86 Initialization of processor status register flags

(2) How to refer the processor status register

To refer the contents of the processor status register (PS), execute the PHP instruction once and then read the contents of (S+1). If necessary, execute the PLP instruction to return the stored PS to its original status.

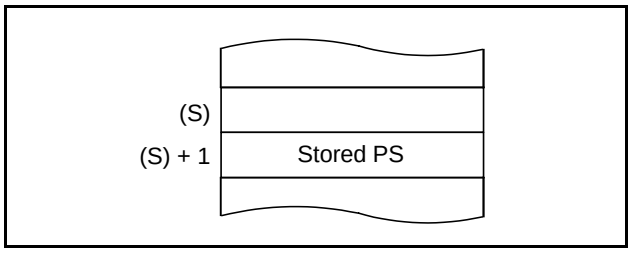


Fig 87. Stack memory contents after PHP instruction execution

2. Decimal Calculations

(1) Instructions for decimal calculations

To perform decimal calculations, set the decimal mode (D) flag to "1" with the SED instruction and execute the ADC or SBC instruction. In that case, after the ADC or SBC instruction, execute another instruction before the SEC, CLC, or CLD instruction.

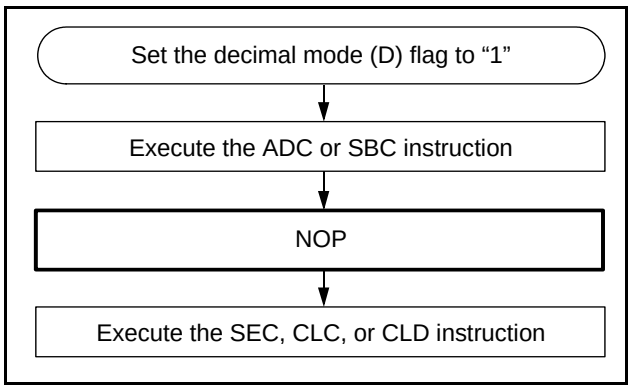


Fig 88. Instructions for decimal calculations

(2) Status flag at decimal calculations

When the ADC or SBC instruction is executed in decimal mode (D flag = "1"), three of the status flags (N, V, and Z) are disabled.

The carry (C) flag is set to "1" if a carry is generated and is cleared to "0" if a borrow is generated as a result of a calculation, so it can be used to determine whether the calculation has generated a carry or borrow.

Initialize the C flag before each calculation.

3. JMP Instruction

When using the JMP instruction (indirect addressing mode), do not specify the address where "FF_{16}" is allocated to the low-order 8 bits as the operand.

4. Multiplication and Division Instructions

(1) The MUL and DIV instructions are not affected by the T and D flags.

(2) Executing these instructions does not change the contents of the processor status register.

5. Read-Modify-Write Instruction

Do not execute any read-modify-write instruction to the read invalid (address) SFR.
The read-modify-write instruction reads 1-byte of data from memory, modifies the data, and writes 1-byte the data to the original memory.
In the 740 Family, the read-modify-write instructions are the following:

(1) Bit handling instructions:
CLB, SEB
(2) Shift and rotate instructions:
ASL, LSR, ROL, ROR, RRF
(3) Add and subtract instructions:
DEC, INC
(4) Logical operation instructions (1's complement):
COM

Although not the read-modify-write instructions, add and subtract/logical operation instructions (ADC, SBC, AND, EOR, and ORA) when T flag = "1" operate in the way as the read-modify-write instruction. Do not execute them to the read invalid SFR.
<Reason>
When the read-modify-write instruction is executed to the read invalid SFR, the following may result:
As reading is invalid, the read value is undefined. The instruction modifies this undefined value and writes it back, so the written value will be indeterminate.

Notes on Peripheral Functions

Notes on I/O Ports

1. Pull-up control register

When using each port which built in pull-up resistor as an output port, the pull-up control bit of corresponding port becomes invalid, and pull-up resistor is not connected.
<Reason>
Pull-up control is effective only when each direction register is set to the input mode.

2. Use in Stand-By State

When using the MCU in stand-by state*1 for low-power consumption, do not leave the input level of an I/O port undefined. Be especially careful to the I/O ports for the N-channel open-drain.
In this case, pull-up (connect to Vcc) or pull-down (connect to Vss) these ports through a resistor.
When determining a resistance value, note the following:

- External circuit
- Variation in the output level during ordinary operation

When using a built-in pull-up resistor, note variations in current values:

- When setting as an input port: Fix the input level
- When setting as an output port: Prevent current from flowing out externally.

<Reason>
Even if a port is set to output by the direction register, when the content of the port latch is "1", the transistor becomes the OFF state, which allows the port to be in the high-impedance state. This may cause the level to be undefined depending on external circuits.
As described above, if the input level of an I/O port is left undefined, the power source current may flow because the potential applied to the input buffer in the MCU will be unstable.

*1 Stand-by state: Stop mode by executing the STP instruction
Wait mode by executing the WIT instruction

3. Modifying Output Data with Bit Handling Instruction

When the port latch of an I/O port is modified with the bit handling instruction*1, the value of an unspecified bit may change.
<Reason>
I/O ports can be set to input mode or output mode in byte units.
When the port register is read or written, the following will be operated:

- Port as input mode
  Read: Read the pin level
  Write: Write to the port latch
- Port as output mode
  Read: Read the port latch or peripheral function output (specifications vary depending on the port)
  Write: Write to the port latch (output the content of the port latch from the pin)

Meanwhile, the bit handling instructions are the read-modify-write instructions*2. Executing the bit handling instruction to the port register allows reading and writing a bit unspecified with the instruction at the same time.
If an unspecified bit is set to input mode, the pin level is read and the value is written to the port latch. At this time, if the original content of the port latch and the pin level do not match, the content of the port latch changes.
If an unspecified bit is set to output mode, the port latch is normally read, but the peripheral function output is read in some ports and the value is written to the port latch. At this time, if the original content of the port latch and the peripheral function output do not match, the content of the port latch changes.

*1 Bit handling instructions: CLB, SEB
*2 Read-modify-write instruction: Reads 1-byte of data from memory, modifies the data, and writes 1-byte of the data to the original memory.

4. Direction Registers

The values of the port direction registers cannot be read. This means, it is impossible to use the LDA instruction, memory operation instruction when the T flag is “1”, addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS. It is also impossible to use bit operation instructions such as CLB and SEB, and read-modify-write instructions to direction registers, including calculations such as ROR. To set the direction registers, use instructions such as LDM or STA.

Termination of Unused Pins

1. Terminate unused pins

Perform the following wiring at the shortest possible distance (20 mm or less) from microcomputer pins.
(1) I/O ports
Set the I/O ports for the input mode and connect each pin to V_{CC} or V_{SS} through each resistor of 1 kΩ to 10 kΩ. The port which can select a built-in pull-up resistor can also use the built-in pull-up resistor.
When using the I/O ports as the output mode, open them at “L” or “H”.

- When opening them in the output mode, the input mode of the initial status remains until the mode of the ports is switched over to the output mode by the program after reset. Thus, the potential at these pins is undefined and the power source current may increase in the input mode. With regard to an effects on the system, thoroughly perform system evaluation on the user side.
- Since the direction register setup may be changed because of a program runaway or noise, set direction registers by program periodically to increase the reliability of program.

2. Termination remarks

(1) I/O ports setting as input mode
[1] Do not open in the input mode.
<Reason>

- The power source current may increase depending on the first stage circuit.
- An effect due to noise may be easily produced as compared with proper termination (1) shown on the above “1. Terminate unused pins”.

[2] Do not connect to V_{CC} or V_{SS} directly.
<Reason>
If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur.

[3] Do not connect multiple ports in a lump to V_{CC} or V_{SS} through a resistor.
<Reason>
If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between ports.

Notes on Interrupts

1. Change of relevant register settings

1. Change of relevant register settings
When not requiring for the interrupt occurrence synchronous with the following case, take the sequence shown in Figure 5.
- When switching external interrupt active edge
- When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated

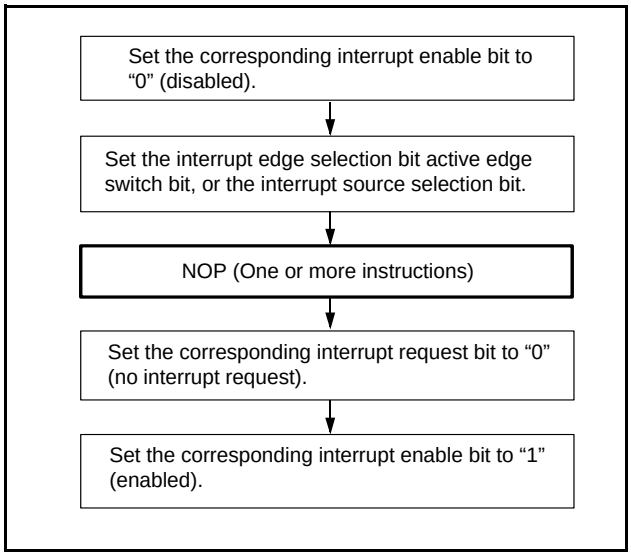


Fig 89. Sequence of changing relevant register

<Reason>
When setting the followings, the interrupt request bit of the corresponding interrupt may be set to "1".
- When switching external interrupt active edge
  INT_0 interrupt edge selection bit
  (bit 0 of Interrupt edge selection register (address $003A_{16}$))
  INT_1 interrupt edge selection bit
  (bit 1 of Interrupt edge selection register)
  Capture 0 interrupt edge selection bit
  (bits 1 and 0 of capture mode register (address 32_{16}))
  Capture 1 interrupt edge selection bit
  (bits 3 and 2 of capture mode register)

2. Check of interrupt request bit

When executing the BBC or BBS instruction to determine an interrupt request bit immediately after this bit is set to "0", take the following sequence.
<Reason>
If the BBC or BBS instruction is executed immediately after an interrupt request bit is cleared to "0", the value of the interrupt request bit before being cleared to "0" is read.

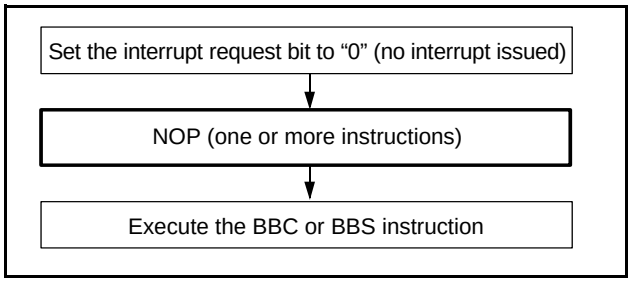


Fig 90. Sequence of check of interrupt request bit

Notes on Timers

1. Division Ratio of Timers 1, 2, and A

When n (0 to 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

2. Switching Count Source of Timers 1, 2, and A

When a count source of timer 1, timer 2 or timer A is switched, stop a count of the timer.

3. Reading from and Writing to Timers 1, 2, and Prescaler 12

If the timer/prescaler count source clock and ϕSOURCE are different clocks, the timers and prescaler cannot be read or written. Select the same clock to enable read and write operations.
Note that timer 2 can be read and written even using a different clock while its counting is stopped.
①Prescaler 12 and timer 1 cannot be read/written in the following conditions:
Prescaler 12 count source: X_{CIN} input clock
ϕSOURCE: Clock other than X_{CIN} input clock
②Timer 2 cannot be read/written during counting in the following conditions:
Timer 2 count source: Prescaler 12
Prescaler 12 count source: X_{CIN} input clock
ϕSOURCE: Clock other than X_{CIN} input clock
or
Timer 2 count source: Timer A underflow
Timer A count source: X_{CIN} input clock
ϕSOURCE: Clock other than X_{CIN} input clock
or
Timer 2 count source: Timer A underflow
Timer A count source: low-speed on-chip oscillator output
ϕSOURCE: Clock other than low-speed on-chip oscillator

4. Count Source of Prescaler 12

The X_{CIN} input clock can be selected as the prescaler count source only if the 32 kHz quartz crystal oscillator is selected by the oscillation method selection bit in FSROM1.

5. Timer Value Setting

When the timer A write control bit is set to "write to only latch", written data is written to only to the latch even when the timer is stopped. To set the initial setting value when the timer is stopped, select "Write to timer and latch simultaneously" beforehand.

6. Reading from and Writing to Timer A

If the timer A count source clock and ϕSOURCE are different clocks, timer A cannot be read or written during its counting. Select the same clock or set timer A to stop counting to enable read and write operations.

- Timer A cannot be read/written in the following conditions:
  Timer A count source: XCIN input clock
  ϕSOURCE: Clock other than XCIN input clock
  or
  Timer A count source: Low-speed on-chip oscillator output
  ϕSOURCE: Clock other than low-speed on-chip oscillator

7. Count Source of Timer A

The XCIN input clock can be selected as the count source of timer A only if the 32 kHz quartz crystal oscillator is selected by the oscillation method selection bit in FSROM1.

Notes on Output Compare

(1) If timer A is stopped, when a value is written to the capture/compare register it is immediately transferred to the compare latch. In addition, if timer A is stopped and the compare x trigger enable bit is set to “1”, the output latch is initialized.

(2) Do not write the same data to both of compare latch x0 and x1.

(3) When setting value of the compare latch is larger than timer setting value, compare match signal is not generated. Accordingly, the output waveform is fixed to “L” or “H” level.
However, when setting value of another compare latch is smaller than timer setting value, this compare match signal is generated. Accordingly, compare interrupt occurs.

(4) When the compare x trigger enable bit is cleared to “0” (disabled), the match trigger to the waveform output circuit is disabled, and the output waveform can be fixed to “L” or “H” level.
However, in this case, the compare match signal is generated.
Accordingly, compare interrupt occurs.

Notes on Input Capture

(1) When the low-speed on-chip oscillator output or XCIN input clock is selected as the count source of timer A, input capture can be used only if the same clock source is selected as ϕSOURCE and as the count source of timer A.

(2) When writing “1” to capture y software trigger bit of capture latch 00 and 01 at the same time, or external trigger and software trigger occur simultaneously, if capture latches 00 and 01 are input simultaneously, the set value of capture 0 status bit is undefined.

(3) When setting the interrupt active edge selection bit and noise filter clock selection bit of capture 0 the interrupt request bit may be set to “1”.
When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.
①Set the capture interrupt enable bit to “0” (disabled).
②Set the interrupt edge selection bit or noise filter clock selection bit.
③Set the corresponding interrupt request bit to “0” after 1 or more instructions have been executed.
④Set the capture interrupt enable bit to “1” (enabled).

(4) When the capture interrupt is used as the interrupt for return from stop mode, set the capture 0 noise filter clock selection bits to “00 (Filter stop)”.

Notes on Serial I/O

1. Serial I/O interrupt

When setting the transmit enable bit to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

1. Set the serial I/O transmit interrupt enable bit to "0" (disabled).
2. Set the transmit enable bit to "1".
3. Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.
4. Set the serial I/O transmit interrupt enable bit to "1" (enabled).

2. I/O pin function when serial I/O is enabled.

The functions of P06 and P07 are switched with the setting values of a serial I/O mode selection bit and a serial I/O synchronous clock selection bit as follows.

(1) Serial I/O mode selection bit → "1" :
Clock synchronous type serial I/O is selected.
- Setup of a serial I/O synchronous clock selection bit
"0" : P06 pin turns into an output pin of a synchronous clock.
- "1" : P06 pin turns into an input pin of a synchronous clock.
Setup of a $\overline{\text{SRDY}}$ output enable bit (SRDY)
"0" : P07 pin can be used as a normal I/O pin.
"1" : P07 pin turns into a $\overline{\text{SRDY}}$ output pin.

(2) Serial I/O mode selection bit → "0" :
Clock asynchronous (UART) type serial I/O is selected.
- Setup of a serial I/O synchronous clock selection bit
"0" : P06 pin can be used as a normal I/O pin.
"1" : P06 pin turns into an input pin of an external clock.
- When clock asynchronous (UART) type serial I/O is selected, it is P07 pin. It can be used as a normal I/O pin.

Notes on A/D conversion

1. Analog input pin

Make the signal source impedance for analog input low, or equip an analog input pin with an external capacitor of 0.01μF to 1μF. Further, be sure to verify the operation of application products on the user side.
<Reason>
An analog input pin includes the capacitor for analog voltage comparison.
Accordingly, when signals from signal source with high impedance are input to an analog input pin, charge and discharge noise generates. This may cause the A/D conversion/comparison precision to be worse.

2. Clock frequency during A/D conversion

The comparator consists of a capacity coupling, and a charge of the capacity will be lost if the clock frequency is too low. This may cause the A/D conversion precision to be worse. Accordingly, set f(XIN) in order that the A/D conversion clock is 250 kHz or over during A/D conversion.

3. Read A/D conversion register

- 8-bit read

Read only the A/D conversion low-order register (address 35_{16}).
- 10-bit read

Read the A/D conversion high-order register (address 36_{16}) first, and then, read the A/D conversion low-order register (address 35_{16}).
In this case, the high-order 6 bits of address 36_{16} returns "0" when read.

4. A/D translation accuracy

As for A/D translation accuracy, on the following operating conditions, accuracy may become low.

(1) When VCC voltage is lower than [3.0 V], the accuracy at the low temperature may become extremely low compared with that at room temperature. When the system would be used at low temperature, the use at VCC = 3.0 V or more is recommended.

(2) When XCIN or the low-speed on-chip oscillator is selected as φSOURCE, the A/D converter cannot be used.

Notes on Watchdog Timer

1. Watchdog Timer Underflow

The watchdog timer operates in wait mode. To prevent underflow, write to the watchdog timer control register.
The watchdog timer stops in stop mode, but starts counting at the same time as exiting stop mode. After exiting stop mode, it continues counting during oscillation stabilization time. To prevent underflow during the period, the watchdog timer H count source selection bit (bit 7) in the watchdog timer control register (address 003916) should be set to "0" before executing the STP instruction.
Note that the watchdog timer continues counting even if the STP instruction is executed in the following two conditions:

① Stopping the low-speed on-chip oscillator: Disabled (bit 4 in FSROM2)
Source clock of the watchdog timer: Low-speed on-chip oscillator/16 (bit 0 in FSROM2)

② Stopping the low-speed on-chip oscillator: Disabled (bit 4 in FSROM2)
Source clock of the watchdog timer: ϕSOURCE (bit 0 in FSROM2)
ϕSOURCE: Low-speed on-chip oscillator (bits 5 and 4 in CLKM)

2. STP instruction function selection bit

The function of the STP instruction can be selected by the bit 2 in FSROM2. This bit cannot be used for rewriting by executing the STP instruction.

- When this bit is set to "0", stop mode is entered by executing the STP instruction.
- When this bit is set to "1", internal reset occurs by executing the STP instruction.

Notes on RESET pin

1. Connecting capacitor

In case where the $\overline{\text{RESET}}$ signal rise time is long, connect a ceramic capacitor or others across the $\overline{\text{RESET}}$ pin and VSS pin.
And use a 1000 pF or more capacitor for high frequency use.
When connecting the capacitor, note the following:

- Make the length of the wiring which is connected to a capacitor as short as possible.
- Be sure to verify the operation of application products on the user side.

<Reason>
If the several nanosecond or several ten nanosecond impulse noise enters the $\overline{\text{RESET}}$ pin, it may cause a microcomputer failure.

Note on Generating Clock Circuit

1. Switching to XIN/XCIN Oscillator

After a reset is cleared, operation starts using the low-speed on-chip oscillator. When switching to XIN/XCIN oscillator, make sure to set a sufficient wait duration with the on-chip oscillator to allow the XIN/XCIN oscillator to stabilize.

Note on Oscillation Control

For use with the oscillation stabilization set bit after release of the STP instruction set to "1", set values in timer 1 and prescaler 12 after fully appreciating the oscillation stabilization time of the oscillator to be used.

Notes on Oscillation Stop Detection Circuit

(1) Do not execute the transition to "state 2'a" shown in Figure 68 State transition of oscillation stop detection circuit. In this state, no reset is triggered and the MCU is stopped even when the XIN oscillation stops.

(2) After an oscillation stop detection reset, if this reset is enabled while bits XIN oscillation stop detection function active and oscillation stop detection status are retained, a reset is triggered again.

(3) The oscillation stop detection status bit is initialized under the following conditions:
- External reset, power-on reset, low-voltage detection reset, watchdog timer reset, and reset by the STP instruction function.
- Write 0 to the XIN oscillation stop detection function active bit

(4) While the oscillation stop detection function is in active, the oscillation stop detection status bit may set to 1 when the watchdog timer underflows or by a reset when the STP instruction is executed with the STP instruction function selection bit set to 1.
When an oscillation stop detection reset is triggered, reconfirm that oscillation is stopped.

(5) The oscillation stop detection circuit is not included in the emulator MCU "M37549RLSS".

Note on Power Source Voltage

When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.
In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the supply voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

Note on Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (VCC pin) and GND pin (VSS pin). A ceramic capacitor of 0.01 μF to 0.1 μF is recommended.
Connect a capacitor across the power source pin and GND pin with the shortest possible wiring.

Note on Memory

(1) Because the contents of RAM are indefinite at reset, set initial values before using.
(2) Do not access to the reserved area.
(3) Random data is written into the Renesas shipment test area and the reserved ROM area. Do not rewrite the data in these areas. Data of these area may be changed without notice. Accordingly, do not include these areas into programs such as checksum of all ROM areas.
(4) The QzROM values in function set ROM data 0 to 2 set the operating modes of the various peripheral functions after an MCU reset is released. Do not fail to set the value for the selected function. Bits designated with a fixed value of 1 or 0 must be set to the designated value.

Notes on QzROM

1. Note on Product shipped in blank

As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approx.0.1 % may occur.
Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

2. Overvoltage

Take care not to apply the voltage above the Vcc pin voltage to other pins. Make sure that the voltage of the CNVss pin (VPP power input pin for QzROM) does not change as shown in the bold-lined periods (Figure 91) when powering on and off. If the voltage changes as shown, the QzROM contents may be rewritten.

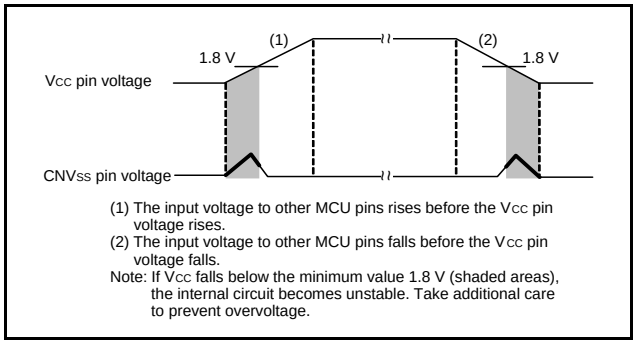


Fig 91. Timing Diagram (bold-lined periods are applicable)

3. QzROM Writing Orders

When ordering the QzROM product shipped after writing, submit the mask file (extension: .mask) which is made by the mask file converter MM.

- Be sure to set the ROM option data* setup when making the mask file by using the mask file converter MM.. The ROM code protect is specified according to the ROM option data* in the mask file which is submitted at ordering. Note that the mask file which has nothing at the ROM option data* or has the data other than "00$_{16}$" and "FF$_{16}$" can not be accepted.
- Set "FF$_{16}$" to the ROM code protect address in ROM data regardless of the presence or absence of a protect. When data other than "FF$_{16}$" is set, we may ask that the ROM data be submitted again.

* ROM option data: mask option noted in MM

4. Data Required for QzROM Writing Orders

The following are necessary when ordering a QzROM product shipped after writing:
1. QzROM Writing Confirmation Form*
2. Mark Specification Form*
3. ROM data.....Mask file

* For the QzROM writing confirmation form and the mark specification form, refer to the "Renesas Technology Corp." Homepage (http://www.renesas.com/homepage.jsp).
Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

REVISION HISTORY	7549 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Dec 15, 2006	-	First edition issued
2.00	Feb 19, 2007	1	FEATURES: "• LED output port" → "• LED direct drive port" "• Built-in high-speed on-chip oscillator" → "High-speed on-chip oscillator" "• Built-in low-speed on-chip oscillator" → "Low-speed on-chip oscillator" •Power dissipation: "TBD" → "30 mW"
		4	Table 1: I/O port $P0_0$-$P0_7$; "LED direct drive ports" is added A/D converter; "8 channel" → "× 8 channel"
		6	Table 2: $P0_3$ "Capture function pin" → "Capture input pin" $P1_0$-$P1_2$ "Compare function pin" → "Compare output pin" $P1_3$ "Timer 2 function pin" → "Timer 2 output pin" $P2_0$, $P2_1$ "external oscillator pin" → "clock pins"
		10	[CPU mode register]: Description is revised and moved from the page 12.
		11	Function set ROM Area: Description is revised and moved from the page 47. <Notes>: (2) is added, (3) is revised
		12	Fig 8 Note is deleted
		14	Fig 10, Fig 11, Fig 12 is moved from the page 47. Fig 12 is revised
		15	[Pull-up control registers]: Description revised Fig 13, Fig 14, Fig 15 is revised
		16	Table 6 is revised
		17, 18	Fig 16, Fig 17; Title is revised
		19	Contents of Table 7 is added
		21	Table 8: Key-on wakeup "P0" → "P1"
		24	Timers, • Notes on Timers 1 and 2: Description is revised
		26	Timer A (TA), • Notes on Timer A: Description is revised
		27	Output compare: Contents of description added Fig 29 "oscillator/512" → "oscillator/16"
		31	Input capture: Contents of description added
		32	Fig 39 "oscillator/512" → "oscillator/16"
		37, 38	register name: "A/D" → "AD"
		38	• Notes on A/D converter: (2) is added
		39	Watchdog Timer is revised Fig 50, Fig 53 is revised
		40	• Notes on Watchdog Timer is revised
		42	Fig 56 is revised
		43	Clock Circuit is revised
		44	Oscillation Control is added Table 9 is added Fig 61 is revised
		47	Fig 62 is revised
		48	Fig 63 is revised
		49	"oscillation stop" → "oscillation stop detection" Fig 64 is revised Fig 65 is revised, Note 4 is added • Notes on Function Set ROM Data 2 is deleted
		50	Table 10: $P1_0$ "ESDA input" → "ESDA I/O", "Output" → "I/O"

REVISION HISTORY	7549 Group Datasheet

Rev.	Date	Description	
		Page	Summary
2.00	Feb 19, 2007	53	(7) CPU Mode Register is revised
		58	Overvoltage: Description revised, Fig 79 is added
		59	ELECTRICAL CHARACTERISTICS is added
2.01	Oct 15, 2007	1	Interrupts. “13 sources, 13 vectors”→“12 sources, 12 vectors”
		4	Interrupts. “13 sources, 13 vectors”→“12 sources, 12 vectors” Power dissipation “TBD”→“30 mW”
		10	“Stack page bit”→“Stack page selection bit”
		14	Fig 12 is revised.
		17	Fig 16 (6) and (8) are revised.
		19	Table 7 RESET is added.
		20-24	Interrupts is revised. Fig 20-22 are added.
		26	Fig 24 is revised.
		30	Fig 32 is revised.
		42	Fig 53 is revised.
		43	Fig 55 is revised.
		52	Oscillation stop detection circuit is revised.
		54	V_{CC}, V_{SS} “Apply 1.8 to 5.5 V to V_{CC}”→“Apply 2.7 to 5.5 V to V_{CC}”
		57	(7) CPU Mode Register is revised.
		59	3. Writing to analog input pins is revised.
		65	Table 14 “R_{HSOSC}”→“R_{HSOSO}” Min.: “TBD”→“3.8”, “3.6”, Max.: “TBD”→“4.2”, “4.4” “R_{LSOSC}”→“R_{LSOSO}”
		67	Table 16 Absolute accuracy Max.: “TBD”→“3” Table 17 A/D Conversion clock frequency Min.: “TBD”→“0.016”
		74	APPENDIX is added.
		All pages	“PRELIMINARY” deleted.
2.02	Mar 31, 2009	4	Table 1 Power dissipation: 30 mW → 30 mW (Typ.)
		57, 74	“Processor Status Register” revised.
		63	Table 12 V_{CC}: X_{IN} oscillation, X_{CIN} oscillation, ... → X_{CIN} oscillation deleted.
		65	Table 14 NOTE 3 $P0_5/T_XD1$ → $P0_5/T_XD$
		68	- Power-on reset circuit characteristics: TW(V_{POR}) Limits Max. and Min. values changed. - Low voltage detection circuit characteristics: TW(V_{LVD}) and TW (V_{LVD} -V_{DET}) eliminated. V_{DET-} → V_{DET}, V(V_{DET+}- V_{DET-}) deleted. - Fig. 83 revised.
		61, 81	“Notes On QzROM Writing Orders” revised.

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