

Medium Integrated Power Solution Using a Dual DC/DC Converter and an LDO

Ambreesh Tripathi

PMP - DC/DC Low-Power Converters

ABSTRACT

This reference design is intended for users designing with the TMS320C6742, TMS320C6746, TMS320C6748, or OMAP-L138 processor. Using sequenced power supplies, this reference design describes a system having a 3.3-V input voltage and a high-efficiency dc/dc converter with integrated FETs for a small, simple design.

Sequenced power supply architectures are becoming commonplace in high-performance microprocessor and digital signal processor (DSP) systems. To save power and increase processing speeds, processor cores have smaller geometry cells and require lower supply voltages than the system bus voltages. Power management in these systems requires special attention. This application report addresses these topics and suggests solutions for output voltage sequencing.

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1 Introduction

In dual voltage architectures, coordinated management of power supplies is necessary to avoid potential problems and ensure reliable performance. Power supply designers must consider the timing and voltage differences between core and input/output (I/O) voltage supplies during power-up and power-down operations.

Sequencing refers to the order, timing, and differential in which the two voltage rails are powered up and down. A system designed without proper sequencing may be at risk for two types of failures. The first of these represents a threat to the long-term reliability of the dual voltage device, whereas the second is more immediate, with the possibility of damaging interface circuits in the processor or system devices such as memory, logic or data converter integrated circuits (IC).

Another potential problem with improper supply sequencing is bus contention. Bus contention is a condition when the processor and another device both attempt to control a bidirectional bus during power up. Bus contention may also affect I/O reliability. Power supply designers must check the requirements regarding bus contention for individual devices.

The power-on sequencing for the OMAP-L138, TMS320C6742, TMS320C6746, and TMS320C6748 are shown in [Table 1](#). No specific voltage ramp rate is required for any of the supplies as long as the 3.3-V rail never exceeds the 1.8-V rail by more than 2 V.

2 Power Requirements

The power requirements are as specified in [Table 1](#).

Table 1. Power Requirements

	PIN NAME	VOLTAGE ⁽¹⁾ ⁽²⁾ (V)	I _{max} (mA)	TOLERANCE	SEQUENCING ORDER	TIMING DELAY
I/O	RTC_CVDD	1.2	1	–25%, +10%	1 ⁽³⁾	
Core	CVDD ⁽⁴⁾	1 / 1.1 / 1.2	600	–9.75%, +10%	2	
I/O	RVDD, PLL0_VDDA, PLL1_VDDA, SATA_VDD, USB_CVDD, USB0_VDDA12	1.2	200	–5%, +10%	3	
I/O	USB0_VDDA18, USB1_VDDA18, DDR_DVDD18, SATA_VDDR, DVDD18	1.8	180	±5%	4	
I/O	USB0_VDDA33, USB1_VDDA33	3.3	24	±5%	5	
I/O	DVDD3318_A, DVDD3318_B, DVDD3318_C	1.8 / 3.3	50 / 90 ⁽⁵⁾	±5%	4 / 5	

⁽¹⁾ If 1.8-V LVCMOS is used, power rails up with the 1.8-V rails. If 3.3-V LVCMOS is used, power it up with the ANALOG33 rails (VDDA33_USB0/1).

⁽²⁾ No specific voltage ramp rate is required for any of the supplies LVCMOS33 (USB0_VDDA33, USB1_VDDA33) if STATIC18 (USB0_VDDA18, USB1_VDDA18, DDR_DVDD18, SATA_VDDR, DVDD18) never exceeds more than 2 volts.

⁽³⁾ If RTC is not used/maintained on a separate supply, it can be included in the STATIC12 (fixed 1.2 V) group.

⁽⁴⁾ If using CVDD at fixed 1.2 V, all 1.2-V rails may be combined.

⁽⁵⁾ If DVDD3318_A, B, and C are powered independently, maximum power for each rail is 1/3 the above maximum power.

3 Features

The design uses the following high-efficiency dc/dc converter with integrated FETs.

INPUT VOLTAGE	~3.3 V
	INTEGRATION AND HIGH EFFICIENCY (Without DVFS)
COMBINE RTC AND STATIC 1.2	
Core 1.2 V at 600 mA	TPS62420 (DCDC1)
Static 1.2 V + VRTC at 251 mA	
Static 1.8 V at 230 mA	TPS62420 (DCDC2)
Static 3.3 V at 115 mA	TPS71733 (DRV)

In the preceding table, VRTC is included in the STATIC12 (fixed 1.2 V) group.

TPS62420

- High efficiency – up to 95%
- VIN range From 2.5 V to 6 V
- Output current 600 mA and 1000 mA
- EasyScale™ optional 1-pin serial interface for dynamic output voltage adjustment
- Power-Save mode at light-load currents
- Available in a 10-pin QFN (3×3mm)

TPS71733

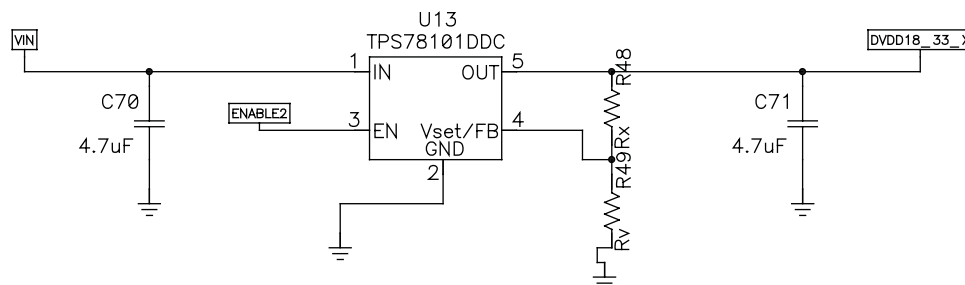
- 150-mA low-dropout (LDO) regulator with enable
- Low noise: 30 μ V typical (100 Hz to 100 kHz)
- Excellent load/line transient response
- Small SC70-5, 2 mm × 2 mm SON-6, and 1,5 mm × 1,5 mm SON-6 packages

More information on the devices can be found in the data sheets.

- TPS62420, [SLVS676](#)
- TPS71733, [SBVS068](#)



Proper sequencing is ensured in the design with the use of a NPN transistor and a N-channel MOSFET. As required, Core 1.2 V at 600 mA comes first, which in turn pulls up the gate of a N-channel MOSFET to 3.3 V with the use of a NPN transistor. Then 1.2 V + VRTC at 251 mA comes up. This 1.2 V further enables the DCDC1 and sequentially 1.8 V comes up, which again enables an LDO to give 3.3 V at 115 mA.



- (1) Use three such LDOs to power up DVDDA, DVddb, and DVDDC. (It can be either 1.8 V or 3.3 V.)
- (2) $R_x = 0.499 \text{ M}\Omega$, $R_y = 1 \text{ M}\Omega$ for $V_{out} = 1.8 \text{ V}$
- (3) $R_x = 1.8 \text{ M}\Omega$, $R_y = 1 \text{ M}\Omega$ for $V_{out} = 3.3 \text{ V}$
- (4) For proper sequencing of output, enable of the LDOs are fed either from a 1.2-V output from TPS62420 DCDC2 if DVDDX is 1.8 V or from a 1.8-V output from TPS62420 DCDC1 if DVDDX is 3.3 V.

Figure 2. Optional Circuit for DVDD_A, DVDD_B and DVDD_C

4 Bill of Materials

Table 2. PMP4978 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR	Area
1	C1	0.1 μ F	Capacitor, Ceramic, 50V, C0G, 5%	0603	Std	Std	5650
1	C2	33pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	Std	Std	5650
6	C3	10 μ F	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	C2012X5R0J106M	TDK	10560
	C4	10 μ F	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	C2012X5R0J106M	TDK	10560
	C5	10 μ F	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	C2012X5R0J106M	TDK	10560
	C6	10 μ F	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	C2012X5R0J106M	TDK	10560
	C7	10 μ F	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	C2012X5R0J106M	TDK	10560
	C8	10 μ F	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	C2012X5R0J106M	TDK	10560
1	C9	2.2 μ F	Capacitor, Ceramic, 16V, X5R, 10%	0603	C1608X5R1C225K	TDK	5650
1	C10	1.0 μ F	Capacitor, Ceramic, 25V, X5R, 10%	0603	C1608X5R1E105K	TDK	5650
1	C11	0.01 μ F	Capacitor, Ceramic, 50V, X7R, 10%	0603	C1608X7R1H103K	TDK	5650
1	J1	PEC36SAAN	Header, Male 5-pin, 100mil spacing, (36-pin strip)	0.100 inch $\times$ 5	PEC36SAAN	Sullins	60000
2	L1	2.2 μ H	Inductor, SMT, 1.2A, 100m Ω	0.102 $\times$ 0.110 inch	VLF3014AT-2R2M1R2	TDK	24,7
	L2	2.2 μ H	Inductor, SMT, 1.2A, 100m Ω	0.102 $\times$ 0.110 inch	VLF3014AT-2R2M1R2	TDK	24,7
2	Q1	2N3904	Transistor, NPN, 40V, 200mA, 625mW	TO-92	2N3904	Fairchild	37800
	Q2	2N3904	Transistor, NPN, 40V, 200mA, 625mW	TO-92	2N3904	Fairchild	37800
1	Q3	Si1012R/X	MOSFET, N-ch, 20V, 600mA, 0.7ohms	SC89-3	Si1012R/X	Vishay	12125
2	R1	10k	Resistor, Chip, 1/16W, 1%	0603	CRCW0603-xxxx-F	Vishay	9100
	R2	10k	Resistor, Chip, 1/16W, 1%	0603	CRCW0603-xxxx-F	Vishay	9100
1	R3	100k	Resistor, Chip, 1/16W, 1%	0603	CRCW0603-xxxx-F	Vishay	9100
1	R4	20k	Resistor, Chip, 1/16W, 1%	0603	CRCW0603-xxxx-F	Vishay	9100
3	R5	365K	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
	R6	365K	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
1	R7	10K	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
1	R8	12.5K	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
	R9	365K	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
1	R10	182K	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
1	U1	TPS62420DRC	IC, 2.25 MHz Dual Step Down Converter	QFN10	TPS62420DRC	TI	40500
1	U2	TPS71733DCK	IC, 150mA, Low Iq, Wide Bandwidth, LDO Linear Regulators	SC70	TPS71728DCK	TI	18.6

- Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Failure to use clean flux is unacceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Reference designators marked with an asterisk (***) cannot be substituted. All other components can be substituted with equivalent MFG's components.

4.1 Test Result

The start-up waveform (Figure 3) specifies the sequencing order that is required.

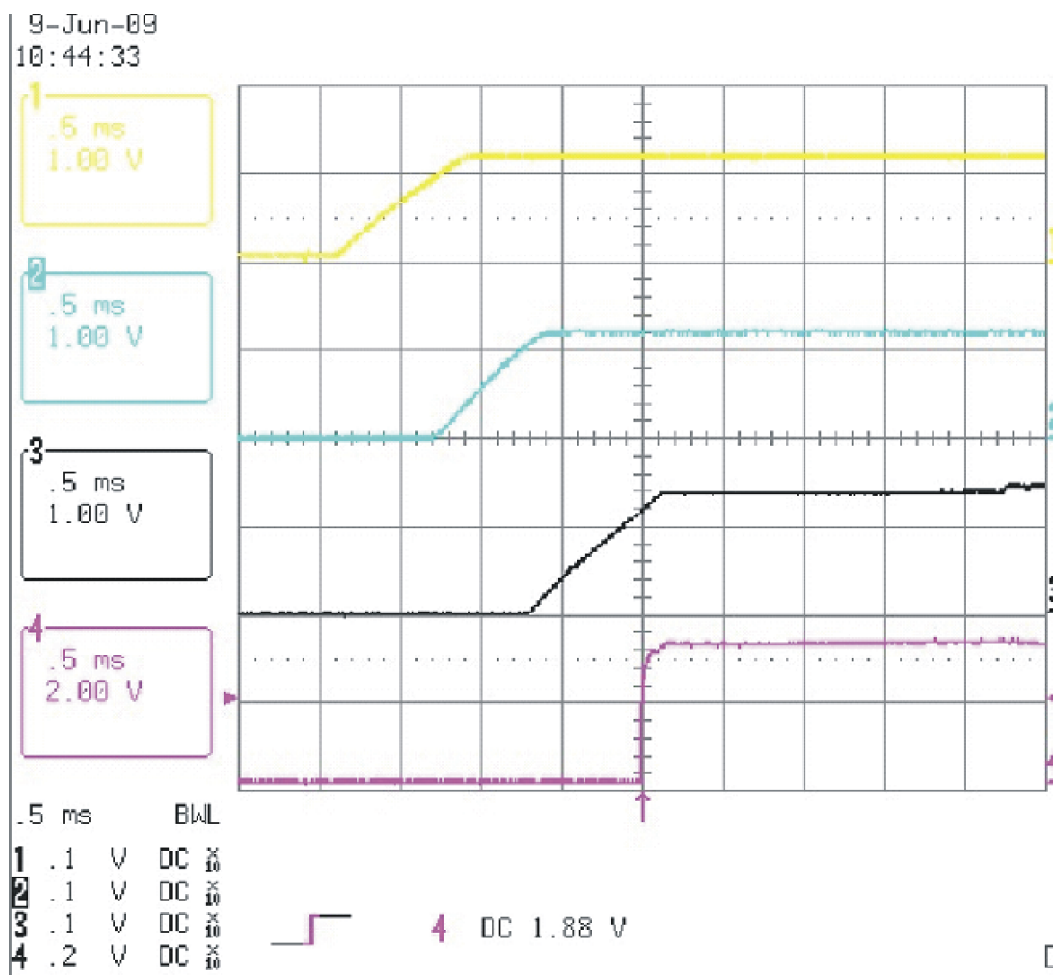


Figure 3. Sequencing in Start-up Waveform

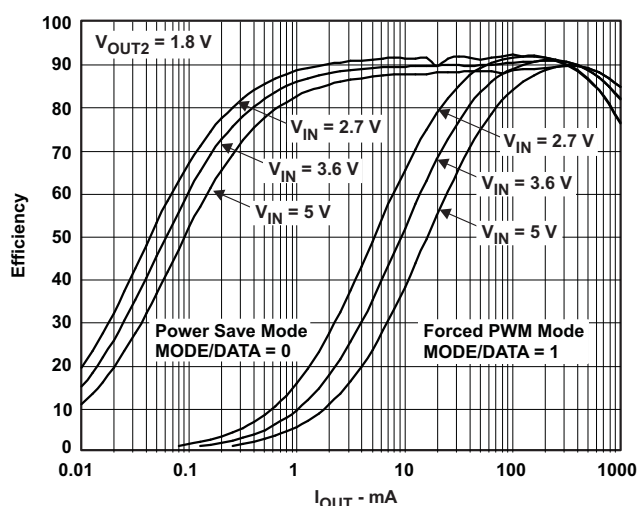


Figure 4. Efficiency $V_{OUT2} = 1.8 \text{ V}$

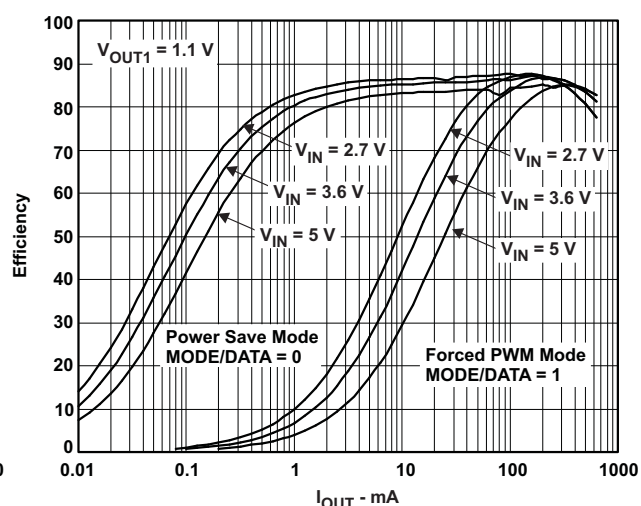


Figure 5. Efficiency $V_{OUT1} = 1.1 \text{ V}$

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