

TRIACs, 12A

Snubberless, Logic Level and Standard

FEATURES

- Medium current triac
- Low thermal resistance with clip bonding
- Low thermal resistance insulation ceramic for insulated TO-220AB package
- High commutation (4Q) or very high commutation (3Q) capability
- 12T series are **UL** certified (File ref: E320098)
- Packages are RoHS compliant

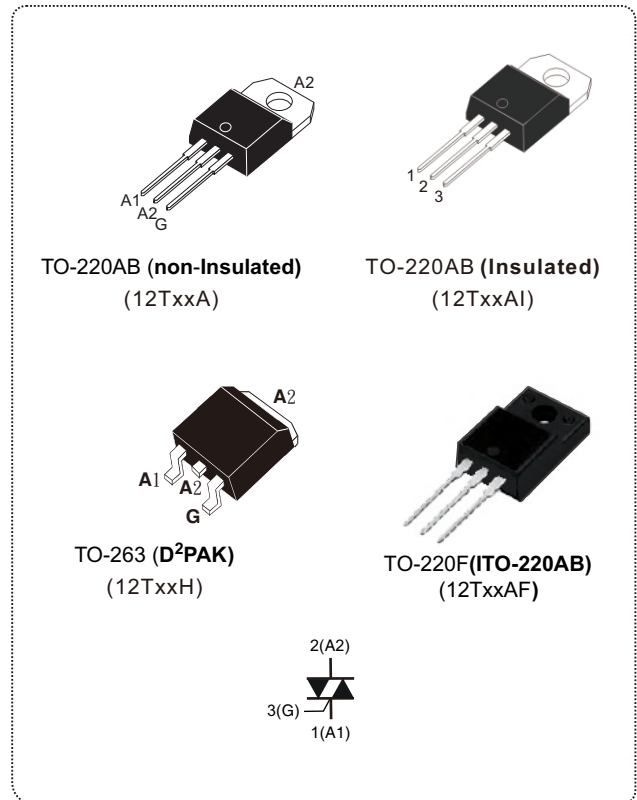
APPLICATIONS

ON/OFF or phase angle function in applications such as static relays, light dimmers and appliance motors speed controllers.

The snubberless versions (with suffix W) are especially recommended for use on inductive loads, because of their high commutation performances. The 12T series provides an insulated tab (rated at 2500V_{RMS}).

MAIN FEATURES

SYMBOL	VALUE	UNIT
$I_{T(RMS)}$	12	A
V_{DRM}/V_{RRM}	600 to 1000	V
$I_{GT(Q1)}$	5 to 50	mA



ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUE	UNIT
RMS on-state current (full sine wave)	$I_{T(RMS)}$	TO-263/TO-220AB	$T_c = 105^\circ\text{C}$	12	A
		TO-220AB insulated/TO-220F (ITO-220AB)	$T_c = 90^\circ\text{C}$		
Non repetitive surge peak on-state current (full cycle, T_j initial = 25°C)	I_{TSM}	F = 50 Hz	t = 20 ms	120	A
		F = 60 Hz	t = 16.7 ms	126	
I^2t Value for fusing	I^2t	$t_p = 10$ ms		72	A^2s
Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$, $t_r \leq 100\text{ns}$	di/dt	F = 100 Hz	$T_j = 125^\circ\text{C}$	50	$\text{A}/\mu\text{s}$
Peak gate current	I_{GM}	$T_p = 20$ μs	$T_j = 125^\circ\text{C}$	4	A
Average gate power dissipation	$P_{G(AV)}$	$T_j = 125^\circ\text{C}$		1	W
Storage temperature range	T_{stg}			- 40 to + 150	$^\circ\text{C}$
Operating junction temperature range	T_j			- 40 to + 125	

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SNUBBERLESS and Logic level (3 quadrants)								
SYMBOL	TEST CONDITIONS	QUADRANT		12Txxxx				Unit
				TW	SW	CW	BW	
I _{GT} ⁽¹⁾	V _D = 12 V, R _L = 30Ω	I - II - III	MAX.	05	10	35	50	mA
V _{GT}		I - II - III	MAX.	1.3				V
V _{GD}	V _D = V _{DRM} , R _L = 3.3KΩ T _j = 125°C	I - II - III	MIN.	0.2				V
I _H ⁽²⁾	I _T = 100 mA		MAX.	10	15	40	60	mA
I _L	I _G = 1.2 I _{GT}	I - III	MAX.	10	20	50	70	mA
		II		15	35	60	80	
dV/dt ⁽²⁾	V _D = 67% V _{DRM} , gate open, T _j = 125°C		MIN.	20	40	500	1000	V/μs
(dI/dt) _c ⁽²⁾	(dV/dt) _c = 0.1 V/μs	T _j = 125°C	MIN.	3.5	6.5	-	-	A/ms
	(dV/dt) _c = 10 V/μs	T _j = 125°C		1	2.9	-	-	
	Without snubber	T _j = 125°C		-	-	6.5	12	

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Standard (4 quadrants)							
SYMBOL	TEST CONDITIONS	QUADRANT		12Txxxx			UNIT
				A	C	B	
I _{GT} ⁽¹⁾	V _D = 12 V, R _L = 30Ω	I - II - III	MAX.	10	25	50	mA
V _{GT}		IV		25	50	100	
V _{GD}	V _D = V _{DRM} , R _L = 3.3KΩ, T _j = 125°C	ALL		1.3			V
V _{GD}	V _D = V _{DRM} , R _L = 3.3KΩ, T _j = 125°C	ALL		0.2			V
I _H ⁽²⁾	I _T = 500 mA		MAX.	25	25	50	mA
I _L	I _G = 1.2 I _{GT}	I - III - IV	MAX.	30	40	50	mA
		II		40	80	80	
dV/dt ⁽²⁾	V _D = 67% V _{DRM} , gate open, T _j = 125°C		MIN.	100	200	400	V/μs
(dV/dt) _c ⁽²⁾	(dI/dt) _c = 5.3 A/ms, T _j = 125°C		MIN.	3	5	10	V/μs

STATIC CHARACTERISTICS					
SYMBOL	TEST CONDITIONS			VALUE	UNIT
V _{TM} ⁽²⁾	I _{TM} = 17 A, t _P = 380 μs	T _j = 25°C	MAX.	1.55	V
V _{I0} ⁽²⁾	Threshold voltage	T _j = 125°C	MAX.	0.85	V
R _d ⁽²⁾	Dynamic resistance	T _j = 125°C	MAX.	35	mΩ
I _{DRM} I _{RRM}	V _D = V _{DRM} V _R = V _{RRM}	T _j = 25°C	MAX.	5	μA
		T _j = 125°C		1	mA

Note 1: Minimum I_{GT} is guaranteed at 5% of I_{GT} max.

Note 2: For both polarities of A2 referenced to A1.

THERMAL RESISTANCE				
SYMBOL			VALUE	UNIT
$R_{th(j-c)}$	Junction to case (AC)	TO-220AB, TO-263	1.4	°C/W
		TO-220AB Insulated/TO-220F	2.3	
$R_{th(j-a)}$	Junction to ambient	$S = 1 \text{ cm}^2$ TO-263	45	°C/W
		TO-220AB Insulated, TO-220AB, TO-220F	60	

S = Copper surface under tab.

PRODUCT SELECTOR						
PART NUMBER	VOLTAGE (xx)			SENSITIVITY	TYPE	PACKAGE
	600 V	800 V	1000 V			
12TxxA-B/12TxxAI-B	V	V	V	50 mA	Standard	TO-220AB
12TxxA-BW/12TxxAI-BW	V	V	V	50 mA	Snubberless	
12TxxA-C/12TxxAI-C	V	V	V	25 mA	Standard	
12TxxA-CW/12TxxAI-CW	V	V	V	35 mA	Snubberless	
12TxxA-SW/12TxxAI-SW	V	V	V	10 mA	Logic level	
12TxxA-TW/12TxxAI-TW	V	V	V	5 mA	Logic level	
12TxxH-B	V	V	V	50 mA	Standard	D ² PAK
12TxxH-C	V	V	V	25 mA	Standard	
12TxxH-SW	V	V	V	10 mA	Logic level	
12TxxH-CW	V	V	V	35 mA	Snubberless	
12TxxH-BW	V	V	V	50 mA	Snubberless	
12TxxH-TW	V	V	V	5 mA	Logic level	
12TxxAF-B	V	V	V	50 mA	Standard	TO-220F (ITO-220AB)
12TxxAF-C	V	V	V	25 mA	Standard	
12TxxAF-BW	V	V	V	50 mA	Snubberless	
12TxxAF-CW	V	V	V	35 mA	Snubberless	
12TxxAF-SW	V	V	V	10 mA	Logic level	
12TxxAF-TW	V	V	V	10 mA	Logic level	

AI: Insulated TO-220AB package

ORDERING INFORMATION					
ORDERING TYPE	MARKING	PACKAGE	WEIGHT	BASE Q'TY	DELIVERY MODE
12TxxA-yy	12TxxA-yy	TO-220AB	2.0g	50	Tube
12TxxAI-yy	12TxxAI-yy	TO-220AB (insulated)	2.3g	50	Tube
12TxxAF-yy	12TxxAF-yy	TO-220F(ITO-220AB)	2.5g	50	Tube
12TxxH-yy	12TxxH-yy	TO-236(D ² PAK)	2.0g	50	Tube

Note: xx = voltage, yy = sensitivity

ORDERING INFORMATION SCHEME

	12	T	06	A - BW
Current				
12 = 12A				
Triac series				
Voltage				
06 = 600V				
08 = 800V				
10 = 1000V				
Package type				
A = TO-220AB (non-insulated)				
AI = TO-220AB (insulated)				
AF = TO-220F (ITO-220AB, insulated)				
H = TO-263 (D ² PAK)				
IGT Sensitivity				
B = 50mA Standard			BW = 50mA Snubberless	
C = 25mA Standard			CW = 35mA Snubberless	
SW = 10mA Logic Level			TW = 5mA Logic Level	

Fig.1 Maximum power dissipation versus RMS on-state current (full cycle)

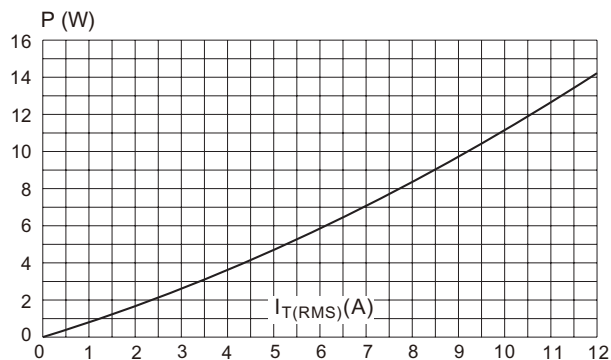


Fig.2 RMS on-state current versus case temperature (full cycle)

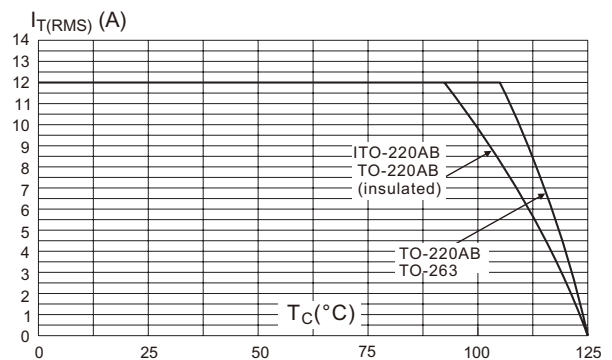


Fig.3 RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35μm)(full cycle)

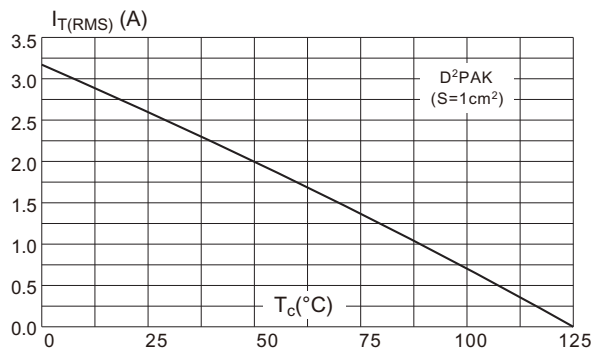


Fig.4 Relative variation of thermal impedance versus pulse duration.

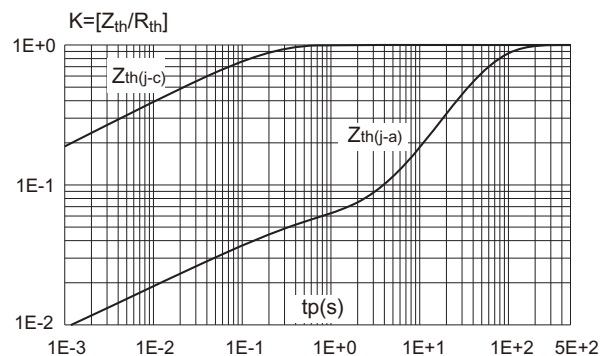


Fig.5 On-state characteristics (maximum values).

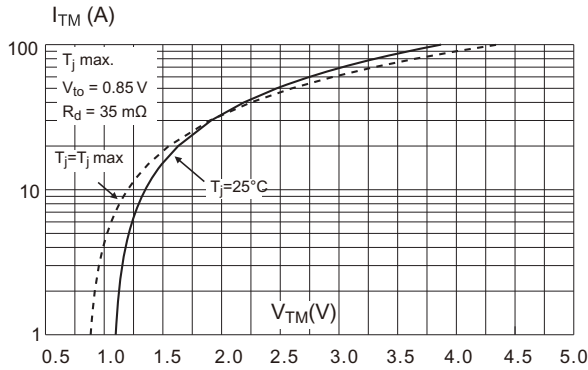


Fig.6 Surge peak on-state current versus number of cycles.

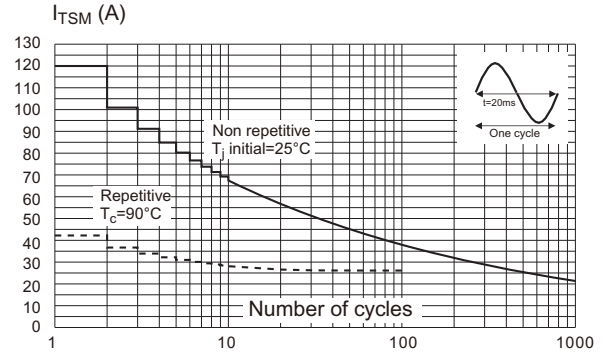


Fig.7 Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10\text{ms}$, and corresponding value of I^2t .

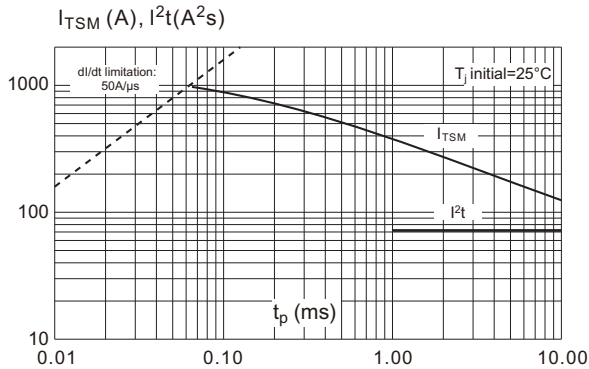


Fig.8 Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values).

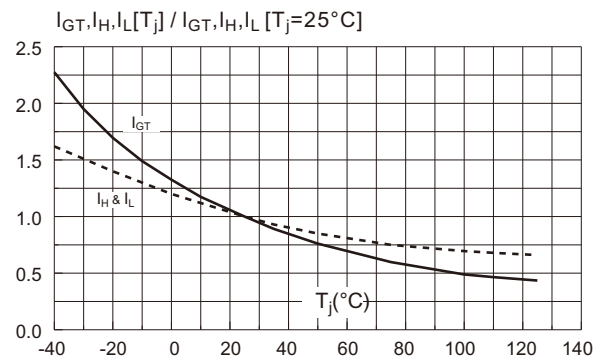


Fig.9 Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$ (typical values).

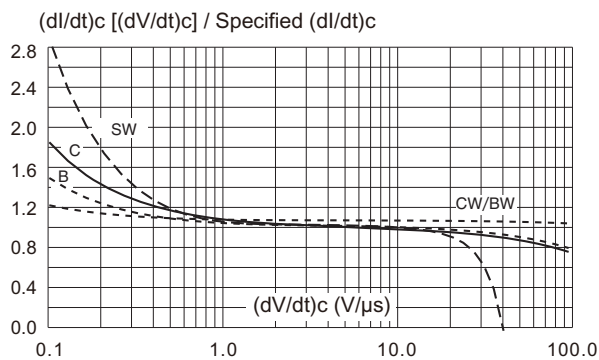


Fig.10 Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$ (typical values).

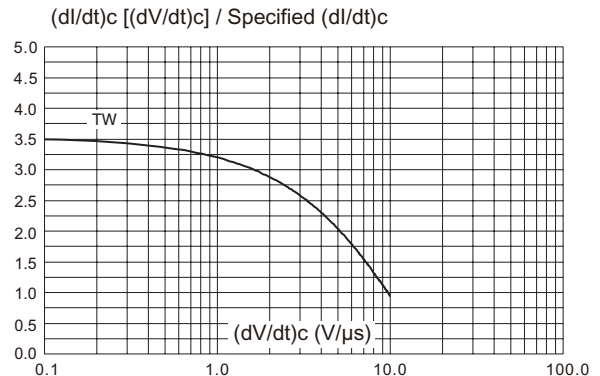


Fig.11 Relative variation of critical rate of decrease of main current versus junction temperature

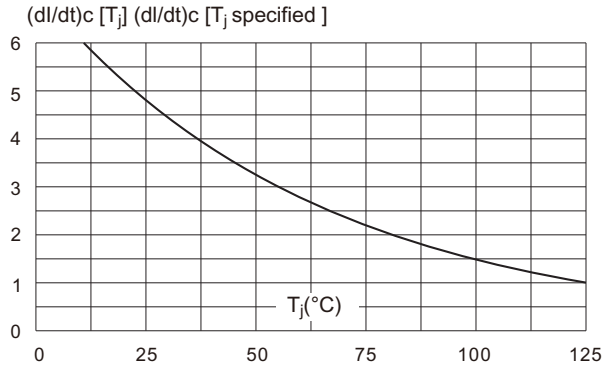
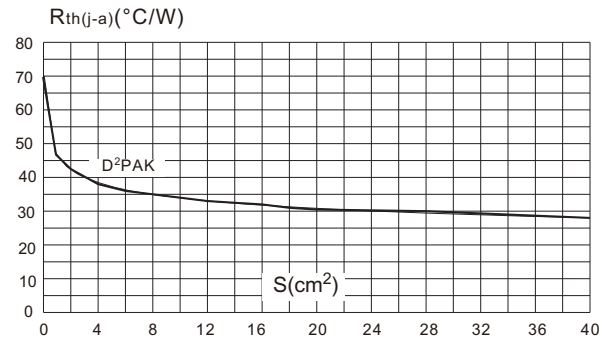
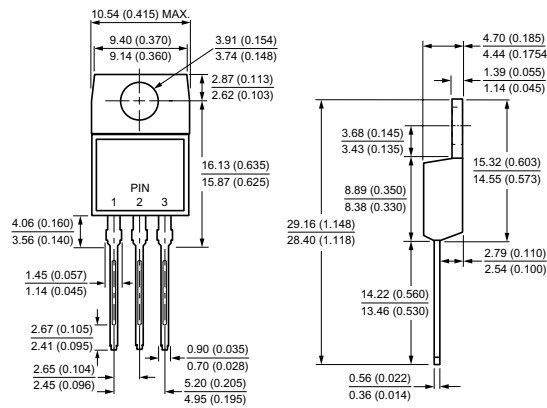


Fig.12 D²PAK thermal resistance junction to ambient versus copper surface under tab (printed circuit board FR4, copper thickness: 35μm)

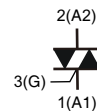
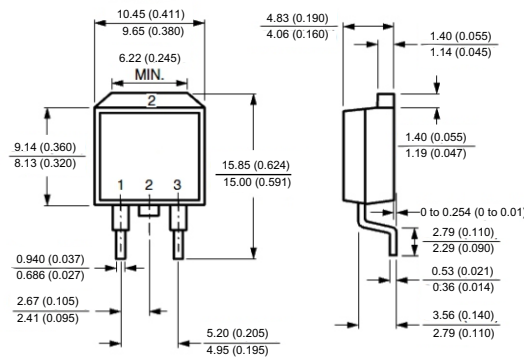


Case Style

TO-220AB



TO-263(D²PAK)



All dimensions in millimeters(inches)

Case Style

ITO-220AB

