UCC28064 Natural Interleaving™ Transition-Mode PFC Controller with Improved Light-Load Efficiency

1 Features

- Input Filter and Output Capacitor Ripple-Current Cancellation
  - Reduced Current Ripple for Higher System Reliability and Smaller Bulk Capacitor
  - Reduced EMI Filter Size
- Sensorless Current-Shaping Simplifies Board Layout and Improves Efficiency
- Non-Linear Error-Amplifier Gain for Fast Dynamic Response
- Soft Recovery on Overvoltage
- Integrated Brownout and Dropout Handling
- Inrush-Safe Current Limiting:
  - Prevents MOSFET Conduction During Inrush
  - Eliminates Reverse Recovery Events in Output Rectifiers
- Improved Light-Load Efficiency:
  - User Adjustable Phase Management
  - Burst Mode Operation with Adjustable Burst Threshold
- Soft start and Soft Stop of Burst Packets
- Reduced ICC Current During Burst Mode
- 1-A Source, 1.8-A Sink Gate Drivers
- –40°C to +125°C Operating Temperature Range in a 16-Lead SOIC Package
- Create a Custom Design Using the UCC28064 With the WEBENCH® Power Designer

2 Applications

- 100-W to 800-W Power Supplies
- Gaming
- All in One PC
- Adapters
- HD, U-HD, and LED TVs
- Home Audio Systems

3 Description

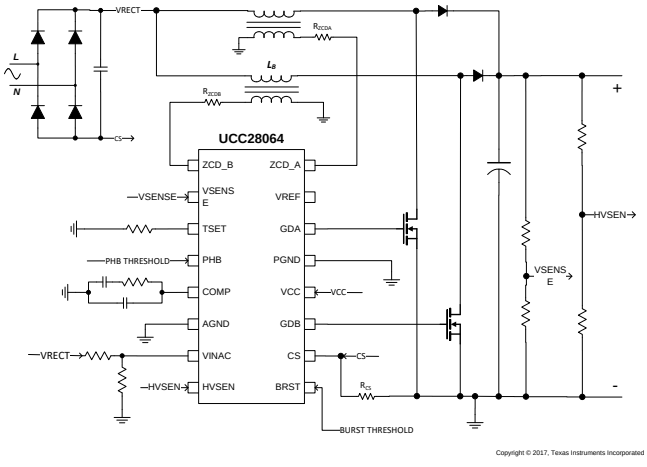
This solution extends the advantages of transition mode – high efficiency with low-cost components – to higher power ratings than previously possible. By utilizing a Natural Interleaving™ technique, both channels operate as masters (that is, there is no slave channel) synchronized to the same frequency. This approach delivers inherently strong matching, faster responses and ensures that each channel operates in transition Mode. UCC28064 improves line transients response of UCC28063 because has implemented line feed forward compensation. Improved light load efficiency is obtained thanks to burst mode operation. Burst mode and phase management operation can be set and fine tuned, according to application needs, thanks to flexibility in configuration of these features.

Device Information(1)

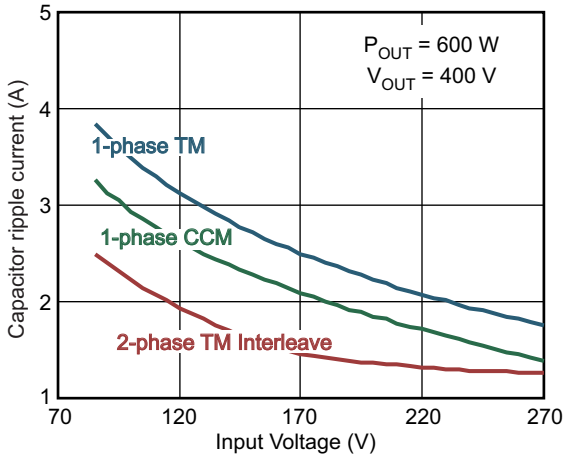
PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC28064	SOIC (16)	9.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



Input Ripple Current Reduction with Interleaving



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

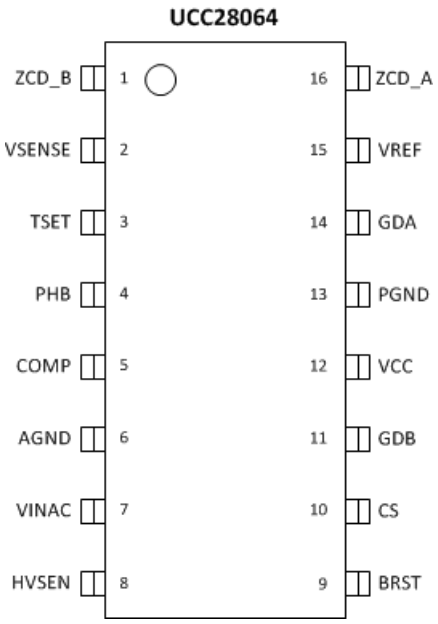
DATE	REVISION	NOTES
December 2017	*	Advance Information release.

5 Description (Continued)

Expanded system level protections feature input brownout and dropout recovery, output over-voltage, open-loop, overload, soft-start, phase-fail detection, and thermal shutdown. The additional failsafe overvoltage protection (OVP) feature protects against shorts to an intermediate voltage that, if undetected, could lead to catastrophic device failure. Advanced non-linear gain results in rapid, yet smoother response to line and load transient events. Special line-dropout handling avoid significant current disruption. Strong reduction of bias current when not switching during burst mode operation, improves stand-by performance.

6 Pin Configuration and Functions

D Package
16-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	6	-	Analog ground
BRST	9	I	Burst mode threshold input
COMP	5	O	Error amplifier output
CS	10	I	Current sense input
GDA	14	O	Phase A gate driver output
GDB	11	O	Phase B gate driver output
HVSEN	8	I	High voltage output sense
PGND	13	-	Power ground
PHB	4	I	Phase B enable disable threshold input
TSET	3	I	Timing set
VCC	12	-	Bias supply input
VINAC	7	I	Input AC voltage sense
VSENSE	2	I	Error amplifier input
VREF	15	O	Voltage reference output
ZCDA	16	I	Phase A zero current detection input
ZCDB	1	I	Phase B zero current detection input

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7 Specifications

7.1 Absolute Maximum Ratings

All voltages are with respect to GND, −40°C < T_J = T_A < 125°C, currents are positive into and negative out of the specified terminal, unless otherwise noted.

			MIN	MAX	UNIT
	Continuous input voltage	VCC	−0.5	21	V
		COMP, PHB, HVSEN, VINAC, VSENSE, TSET, BRST	–0.5	7	
		ZCDA, ZCDB	–0.5	4	
		CS	–0.5	3	
		GDA, GDB	–0.5	VCC + 0.3	
	Continuous input current	VCC		20	mA
		ZCDA, ZCDB		±5	
		GDA, GDB	–25	25	
		VREF	–2		
	Peak input current	CS	–30		mA
T_J	Operating junction temperature		–40	125	°C
T_{stg}	Storage temperature		–65	150	°C

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	±500	

7.3 Recommended Operating Conditions

All voltages are with respect to GND, −40°C < T_J = T_A < 125°C, currents are positive into and negative out of the specified terminal, unless otherwise noted.

	MIN	MAX	UNIT
VCC input voltage from a low-impedance source	14	21	V
VCC input current from a high-impedance source	8	18	mA
VINAC input voltage	0	6	V
VREF load current	0	–2	mA
ZCDA, ZCDB series resistor	20	80	kΩ
TSET resistor to program PWM on-time	66.5	400	kΩ
HVSEN input voltage	0.8	4.5	V

7.4 Thermal Information

THERMAL METRIC		UCC28064 SOIC (D) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.4	°C/W

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7.5 Electrical Characteristics

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 0V, BRST = 0V, R_{TSET} = 133 kΩ, CS = 0.2V, all voltages are with respect to GND, all outputs unloaded, −40°C < T_J = T_A < 125°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC BIAS SUPPLY						
VCC_{SHUNT}	VCC shunt voltage	I_{VCC} = 10 mA	22	24	26	V
$I_{VCC(UVLO)}$	VCC current, UVLO	VCC = 9.3 V prior to turn on		95	200	µA
$I_{VCC(stby)}$	VCC current, disabled	VSENSE = 0 V		100	200	µA
$I_{VCC(on)}$	VCC current, enabled	VSENSE = 2 V		5	8	mA
$I_{VCC(BURST)}$	VCC current burst mode no switching	V_{COMP} < V_{BURST}			500	µA
UNDERVOLTAGE LOCKOUT (UVLO)						
VCC_{ON}	VCC turnon threshold	VCC rising	9.45	10.35	11.1	V
VCC_{OFF}	VCC turnoff threshold	VCC falling	8.8	9.6	10.7	V
ΔVCC_{UVLO}	UVLO Hysteresis	VCC_{ON} - VCC_{OFF}	0.62	0.75	0.88	V
REFERENCE						
V_{REF}	VREF output voltage, no load	I_{VREF} = 0 mA	5.82	6.00	6.18	V
ΔV_{REF_LOAD}	VREF change with load	0 mA ≤ I_{VREF} ≤ −2 mA		−1	−6	mV
ΔV_{REF_VCC}	VREF change with VCC	12 V ≤ VCC ≤ 20 V		2	10	mV
ERROR AMPLIFIER						
VSENSEreg25	VSENSE input regulation voltage	T_A = 25°C	5.85	6	6.15	V
VSENSEreg	VSENSE input regulation voltage		5.82	6	6.18	V
I_{VSENSE}	VSENSE input bias current	In regulation	50	100	150	nA
V_{ENAB}	VSENSE enable threshold, rising		1.15	1.25	1.35	V
	VSENSE enable hysteresis		0.02	0.07	0.15	V
V_{COMP_CLMP}	COMP high voltage, clamped	VSENSE = VSENSEreg – 0.3 V	4.70	4.95	5.10	V
V_{COMP_SAT}	COMP low voltage, saturated	VSENSE = VSENSEreg + 0.3 V		0.03	0.125	V
g_{M1}	VSENSE to COMP transconductance, small signal	0.99(VSENSEreg) < VSENSE < 1.01(VSENSEreg), COMP = 3 V	40	55	70	µS
$V_{SENSE\_gM2\_SINK}$	VSENSE high-going threshold to enable COMP large signal gain, percent	Relative to VSENSEreg, COMP = 3 V	3.25%	5%	6.75%	
$V_{SENSE\_gM2\_SOURCE}$	VSENSE low-going threshold to enable COMP large signal gain, percent	Relative to VSENSEreg, COMP = 3 V	–3.25%	−5%	−6.75%	
g_{M2_SOURCE}	VSENSE to COMP transconductance, large signal	VSENSE = VSENSEreg – 0.4 V , COMP = 3 V	210	290	370	µS
g_{M2_SINK}	VSENSE to COMP transconductance, large signal	VSENSE = VSENSEreg + 0.4 V, COMP = 3 V	210	290	370	µS
$I_{COMP\_SOURCE\_MAX}$	COMP maximum source current	VSENSE = 5 V, COMP = 3 V	−80	−125	−170	µA
$R_{COMPDCHG}$	COMP discharge resistance	HVSEN = 5.2 V, COMP = 3 V	1.6	2	2.4	kΩ
I_{DODCHG}	COMP discharge current during Dropout	VSENSE = 5 V, VINAC = 0.3 V, COMP = 1V	3.2	4	4.8	µA
V_{LOW_OV}	VSENSE overvoltage threshold, rising	Relative to VSENSEreg	7%	8%	10%	
$\Delta V_{LOW\_OV\_HYST}$	VSENSE overvoltage hysteresis	Relative to V_{LOW_OV}	−1.5%	−2%	−3%	
V_{HIGH_OV}	VSENSE 2nd overvoltage threshold, rising	Relative to VSENSEreg	10.5%	11.3%	14%	

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Electrical Characteristics (continued)

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 0V, BRST = 0V, R_{TSET} = 133 kΩ, CS = 0.2V, all voltages are with respect to GND, all outputs unloaded, −40°C < T_J = T_A < 125°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT START						
V_{SSTHR}	COMP Soft-Start threshold, falling	VSENSE = 1.5 V	15	23	30	mV
$I_{SS,FAST}$	COMP Soft-Start current, fast	SS-state, V_{ENAB} < VSENSE < VREF/2	−80	−125	−170	µA
$I_{SS,SLOW}$	COMP Soft-Start current, slow	SS-state, VREF/2 < VSENSE < 0.88VREF	−11.5	−16	−20	µA
K_{EOSS}	VSENSE End-of-Soft-Start threshold factor	Percent of VSENSEreg	96.5%	98.3%	99.8%	
OUTPUT MONITORING						
$V_{HV\_OV\_FLT}$	HVSEN threshold to overvoltage fault	HVSEN rising	4.64	4.87	5.1	V
$V_{HV\_OV\_CLR}$	HVSEN threshold to overvoltage clear	HVSEN falling	4.45	4.67	4.8	V
GATE DRIVE						
V_{GDx_H}	GDA, GDB output voltage, high	I_{GDA}, I_{GDB} = −100 mA	11.5	12.4	15	V
R_{GDx_H}	GDA, GDB on-resistance, high	I_{GDA}, I_{GDB} = −100 mA		8.8	14	Ω
V_{GDx_L}	GDA, GDB output voltage, low	I_{GDA}, I_{GDB} = 100 mA		0.18	0.32	V
R_{GDx_L}	GDA, GDB on-resistance, low	I_{GDA}, I_{GDB} = 100 mA		2	3.2	Ω
$V_{GDx\_H\_VCCH}$	GDA, GDB output voltage high, clamped	VCC = 20 V, I_{GDA}, I_{GDB} = −5 mA	12	13.5	15	V
$V_{GDx\_H\_VCCL}$	GDA, GDB output voltage high, low VCC	VCC = 12 V, I_{GDA}, I_{GDB} = −5 mA	10	10.5	11.5	V
$V_{GDx\_L\_UVLO}$	GDA, GDB output voltage, UVLO	VCC = 3.0 V, I_{GDA}, I_{GDB} = 2.5 mA		100	200	mV
t_{GDx_RISE}	Rise time	1 V to 9 V, C_{LOAD} = 1 nF		18	30	ns
t_{GDx_FALL}	Fall time	9 V to 1 V, C_{LOAD} = 1 nF		12	25	ns
ZERO CURRENT DETECTOR						
V_{ZCDx_TRIG}	ZCDA, ZCDB voltage threshold, falling		0.8	1	1.2	V
V_{ZCDx_ARM}	ZCDA, ZCDB voltage threshold, rising		1.5	1.7	1.9	V
$V_{ZCDx\_CLMP\_H}$	ZCDA, ZCDB clamp, high	I_{ZCDA} = +2 mA, I_{ZCDB} = +2 mA	2.6	3	3.4	V
$V_{ZCDx\_CLMP\_L}$	ZCDA, ZCDB clamp, low	I_{ZCDA} = −2 mA, I_{ZCDB} = −2 mA	0	−0.2	−0.4	V
I_{ZCDx}	ZCDA, ZCDB input bias current	ZCDA = 1.4 V, ZCDB = 1.4 V	-0.5	0	0.5	µA
t_{ZCDx_DEL}	ZCDA, ZCDB delay to GDA, GDB outputs	From ZCDx input falling to 1 V to respective gate drive output rising 10%		50	100	ns
t_{ZCDx_BLNK}	ZCDA, ZCDB blanking time	From GDx rising to GDx falling		100		ns

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Electrical Characteristics (continued)

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 0V, BRST = 0V, R_{TSET} = 133 kΩ, CS = 0.2V, all voltages are with respect to GND, all outputs unloaded, −40°C < T_J = T_A < 125°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE						
I_{CS}	CS input bias current, dual-phase	At rising threshold	−120	−166	−200	µA
V_{CS_DPh}	CS current-limit rising threshold, dual-phase		−0.18	−0.2	−0.22	V
V_{CS_SPh}	CS current-limit rising threshold, single-phase	PHB = 6 V	−0.149	−0.166	−0.183	V
V_{CS_RST}	CS current-limit reset falling threshold		−0.003	–0.015	–0.025	V
t_{CS_DEL}	CS current-limit response time	From CS exceeding threshold−0.05 V to GDx dropping 10%		60	100	ns
t_{CS_BLNK}	CS blanking time	From GDx rising and falling edges		100		ns
VINAC INPUT						
I_{VINAC}	VINAC input bias current, above brownout	VINAC = 2 V	-0.5	0	0.5	µA
V_{BODET}	VINAC brownout detection threshold	VINAC falling	1.38	1.45	1.5	V
t_{BODLY}	VINAC brownout filter time	VINAC below the brownout detection threshold for the brownout filter time	500	640	800	ms
V_{BOHYS}	VINAC brownout threshold hysteresis	VINAC rising	30	62	75	mV
I_{BOHYS}	VINAC brownout hysteresis current	VINAC = 1 V for > t_{BODLY}	1.6	2	2.5	µA
V_{DODET}	VINAC dropout detection threshold	VINAC falling	0.315	0.35	0.38	V
t_{DODLY}	VINAC dropout filter time	VINAC below the dropout detection threshold for the dropout filter time	3.5	5	7	ms
V_{DOCLR}	VINAC dropout clear threshold	VINAC rising	0.67	0.71	0.75	V

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Electrical Characteristics (continued)

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 0V, BRST = 0V, R_{TSET} = 133 kΩ, CS = 0.2V, all voltages are with respect to GND, all outputs unloaded, −40°C < T_J = T_A < 125°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PULSE-WIDTH MODULATOR						
K_{TL}	On-time factor, two phases operating, low VINAC_PK	VINAC=1.6V, VCOMP=4V	3.2	4.43	5.6	µs/V
K_{TH}	On-time factor, two phases operating, high VINAC_PK	VINAC= 5V, VCOMP = 4V	0.36	0.43	0.5	µs/V
K_{TSL}	On-time factor, single-phase operating, low VINAC_PK	VINAC=1.6V, VCOMP = 1.5V, PHB = 2V	6.7	9.1	11.5	µs/V
K_{TSH}	On-time factor, single-phase operating, high VINAC_PK	VINAC= 5V, VCOMP = 1.5V, PHB=2V	0.73	0.87	1.01	µs/V
t_{ZCC}	Zero-crossing distortion correction additional on time	COMP = 0.5 V, VINAC = 1 V	1.55	2.4	3.33	µs
		COMP = 0.5 V, VINAC = 0.1 V	18	28.5	39	µs
t_{MIN}	Minimum Switching period	R_{TSET} = 133 kΩ, VCOMP = 0.3, VINAC = 3 V	1.7	2.2	3	µs
t_{START}	PWM restart time	ZCDA = ZCDB = 2 V	165	210	265	µs
t_{ONMAX_L}	Maximum FET on time at low VINAC	VSENSE = 5.8 V, VINAC=1.6V	15.5	21	27	µs
t_{ONMAX_H}	Maximum FET on time at HighVINAC	VSENSE = 5.8 V, VINAC= 5V	1.73	2	2.43	µs
t_{ONMAX_SL}	Maximum FET on time at low VINAC, Single Phase operation.	VSENSE = 5.8V, VINAC=1.6V, PHB = 6V	12.5	17	21.5	µs
t_{ONMAX_SH}	Maximum FET on time at low VINAC, single phase operation	VSENSE = 5.8V, VINAC=5 V, PHB = 6V	1.37	1.66	1.95	µs
$\Delta t_{ONMAX\_AB\_L}$	Phase B to phase A on-time matching error	VSENSE = 5.8 V, VINAC=1.6V	–%6		6%	
$\Delta t_{ONMAX\_AB\_H}$	Phase B to phase A on-time matching error	VSENSE = 5.8 V, VINAC= 5V	–6%		6%	
ΔV_{BRST_HYST}	BRST Hysteresis, COMP voltage rising	BRST = 1V, VINAC = 1.5 V	40	50	60	mV
ΔV_{PHB_HYST}	PHB Hysteresis COMP voltage rising	PHB = 3V, VINAC = 2.5 V	40	50	60	mV
I_{PHB_RANGE}	PHB pin sourced current when high input voltage	VINAC = 3.75V, PHB = 2V	2	3	4.1	µA
I_{BRST_RANGE}	BRST pin sourced current when high input voltage	VINAC = 3.75V, BRST = 2V	2	3	4.1	µA
$V_{VINAC\_RANGE\_THR}$	VINAC range rising threshold	PHB = 2V, BRST = 2V		3.57		V
$V_{VINAC\_RANGE\_THF}$	VINAC range falling threshold	PHB = 2V, BRST = 2V		3.22		V
THERMAL SHUTDOWN						
T_J	Thermal shutdown temperature	Temperature rising		160		°C
T_J	Thermal restart temperature	Temperature falling		140		°C

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8 Detailed Description

8.1 Overview

Transition Mode Control is the most popular choice for the Boost Power Factor Correction topology at lower power levels because of its lower complexity in achieving high power factor while at the same time not placing demanding requirements on the power component specifications. A lower cost boost diode with higher reverse recovery current specification may be used, for instance, in the Transition Mode Boost. Interleaved Transition Mode Control retains this benefit and generally extends the applicability up to much higher power levels while simultaneously conferring the interleaving benefits of reduced input and output ripple and system thermal optimization.

In UCC28064, in order to achieve higher efficiency in medium to light load and very light load condition, burst mode operation was introduced. Also an accurate voltage feed forward compensation was added. Phase management feature was slightly modified respect UCC28063. Now it is possible to set the load value with good precision so that below that value converter operates in single phase mode and above that value converter operates in dual phase mode. This setting is realized with low external component counts.

Line voltage feed forward compensation provides several benefits: it maintains constant bandwidth of the control loop versus line voltage variation, avoids high current in Fets, inductors and line filter when line transitions from low to high happens, improves device Phase management control so the phase shut-off load level can be selected according to load value and its changes with line voltage can be also programmed by user for efficiency optimization. Burst Mode enables high efficiency at light load and soft-start and soft stop in burst mode reduce risk of audible noise. The load levels below which converter operates in burst mode can be different according if converter is working with US main ([90; 132] V_{RMS}) or European main ([190; 265] V_{RMS}). Both load values can be programmed by the user.

Crossover Notch Reduction block implements a non-linear current shaping characteristic on the instantaneous voltage sense (VINAC) in order to reduce distortion and increase Power Factor

The UCC28064 enables a very cost effective solution with a particular focus on ruggedness, fault management, fault recovery, efficiency and higher end performance.

Interleaving control and phase management facilitates high efficiency 80+ and Energy Star designs with reduced input and output ripple. The Natural Interleaving method allows TM operation and achieves 180 degrees between the phases by On-time management and does not rely on tight tolerance requirements on the inductors. The Crossover Notch Reduction block implements a non-linear current shaping characteristic on the instantaneous voltage sense (VINAC) to reduce distortion and increase Power Factor. Negative current sensing is implemented on the total input current instead of just the MOSFET current which prevents MOSFET switching during inrush surges or in any mode where the inductor current may become substantially continuous (CCM). This prevents reverse recovery conduction events between the MOSFET and output rectifier.

Independent output voltage sense chains with their separate fault management behaviors provide a high degree of redundancy against PFC stage over-voltage. Brownout, HVSENSE OV, UVLO, and device over-temperature will all cause a complete Soft-Start cycle. Other faults such as short duration AC Drop-Out, minor over-voltage or cycle-by-cycle over-current cause a live recovery process to initiate by pulling down on the COMP pin or by terminating the pulses early.

The Error amplifier transconductance is designed to allow smaller compensation components and optimum transient response for larger deviations. The Soft-Start process is carefully optimized. A complete Soft Start is implemented on recovery from every fault, for consistency. The Soft Start speed is dependent on the output voltage sense to speed up start-up from low AC line and to minimize the effect of excessive capacitor on COMP pin during start-up into no-load. This complete discharge of COMP aids with preventing excessive currents on recovery from an AC Brown-Out event.

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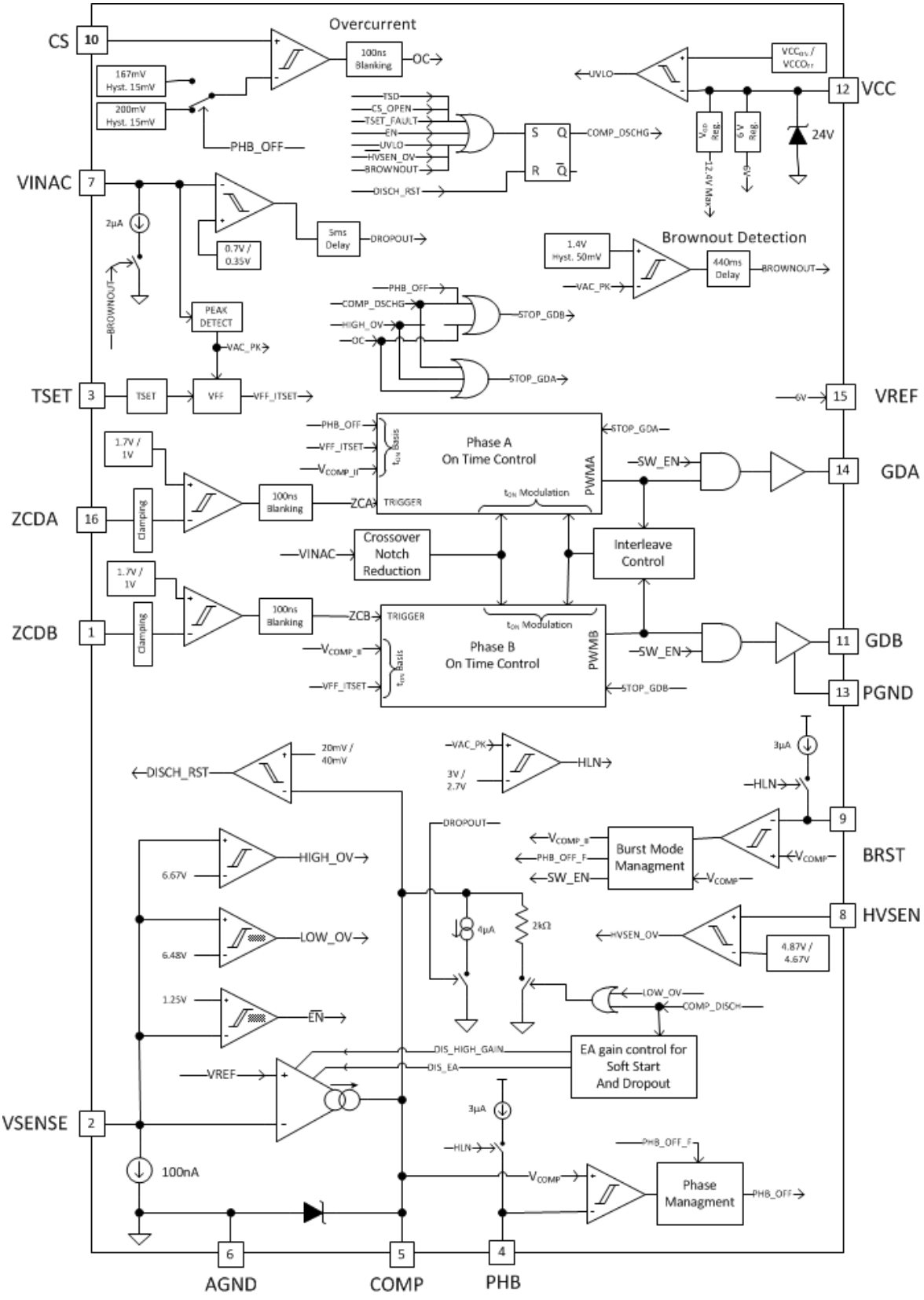
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Principles of Operation

The UCC28064 contains the control circuits for two parallel-connected boost pulse-width modulated (PWM) power converters. The boost PWM power converters ramp current in the boost inductors for a time period proportional to the voltage on the error amplifier output. Each power converter then turns off the power MOSFET until current in the boost inductor decays to zero, as sensed on the zero current detection inputs (ZCDA and ZCDB). Once the inductor is demagnetized, the power converter starts another cycle. This on/off cycling produces a triangular waveform of current, with peak current set by the on-time and the instantaneous power mains input voltage, $V_{IN}(t)$ value, as shown in equation (1) Equation 1.

$$I_{PEAK}(t) = \frac{V_{IN}(t) \times T_{ON}}{L} \quad (1)$$

The average line current is exactly equal to half of the peak line current, as shown in Equation 2.

$$I_{AVG}(t) = \frac{V_{IN}(t) \times T_{ON}}{2 \times L} \quad (2)$$

With t_{ON} and L being essentially constant during an AC-line period, the resulting triangular current waveform during each switching cycle will have an average value proportional to the instantaneous value of the rectified AC-line voltage. This architecture results in a resistive input impedance characteristic at the line frequency and a near-unity power factor.

8.3.2 Natural Interleaving

Under normal operating conditions, the UCC28064 regulates the relative phasing of the channel A and channel B inductor currents to be very close to 180°. This greatly reduces the switching-frequency ripple currents seen at the line-filter and output capacitors, compared to the ripple current of each individual converter. This design allows a reduction in the size and cost of input and output filtering. The phase-control function differentially modulates the on-times of the A and B channels based on their phase and frequency relationship. The Natural Interleaving method allows the converter to achieve 180° phase-shift and transition-mode operation for both phases without tight requirements on boost inductor tolerance.

Ideally, the best current-sharing is achieved when both inductors are exactly the same value. Typically the inductances are not the same, so the current-sharing of the A and B channels is proportional to the inductor tolerance. Also, switching delays and resonances of each channel typically differ slightly, and the controller allows some necessary phase-error deviation from 180° to maintain equal switching frequencies. Optimal phase balance occurs if the individual power stages and the on-times are well matched. Mismatches in inductor values do not affect the phase relationship.

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Feature Description (continued)

8.3.3 On-Time Control, Maximum Frequency Limiting, Restart Timer and Input Voltage Feed-Forward compensation

CAUTION

APPLICABLE TO PRE-PRODUCTION UNITS:

Pre-production units have a silicon issue which causes some small steps variation of the MOSFETs on time. It occurs simultaneously in both MOSFETs around every 18ms. This does not affect normal operation of the system. Another issue causes slow system reaction when fast AC input voltage variation from high AC input voltage to low AC input voltage occurs. When a fast AC input voltage variation from low to high occurs device response is as expected. Both issues will be fixed for production units.

Gate-drive on-time varies proportionately with the error-amplifier output voltage (V_{COMP}) and inversely proportional to the squared value of the peak of the rectified input voltage sensed through VINAC pin as stated by equation (3). In equation (3) is also shown that the on-time is inversely proportionally to the value of resistor (R_{TSET}) connected between pin TSET and pin AGND. In order to calculate on-time formula (4) can be used. Parameter K_T is function of the rectified peak input voltage sensed by pin VINAC as reported in graph of Figure (5). In this graph 3 curves are reported for three different values of R_{TSET}. Two values of parameter K_T are reported in electrical specs table for two values of VINAC: K_{TL} and K_{TH} corresponding at the VINAC = 1.6V and VINAC = 5V and R_{TSET} = 133kΩ. Because voltage on VINAC is proportional to the line rectified voltage, for t_{ON} calculation purpose we refers to the peak value of this voltage that is obtained through an internal peak detect. K_T is inversely proportional to the squared value of VINAC peak value so it is the t_{ON} time realizing the so called voltage feed-forward compensation. The Voltage Feed forward function modify the Mosfet On time according to line voltage so, ideally output power delivery do not change if line voltage change. When operating in single phase mode K_T is called K_{TS} and its value is doubled. Values of K_T and K_{TS} are reported in the electrical specs table for VINAC = 1.6V and VINAC = 5V.

$$t_{ON} = \propto \frac{(V_{COMP} - 125mV)}{V_{INAC\_PK}{}^2 \cdot R_{TSET}} \tag{3}$$

The COMP pin voltage value is clamped at 4.95V so the maximum on time can be calculated by: .

$$t_{ON} = (V_{COMP} - 125mV) \cdot K_T(V_{INAC}) \tag{4}$$

Figure 1 shows the values of K_T versus the peak voltage value on VINAC pin.

The maximum switching frequency of each phase is limited by minimum-period timers. If inductor current decays to zero before the minimum-period timer elapses, the next turn on will be delayed, resulting in discontinuous phase current.

A restart timer ensures starting under all circumstances by restarting both phases if the ZCD input of either phase has not transitioned from high-to-low within approximately 200 µs.

The minimum switching period, $T_{(MIN)}$, is inversely proportional to the time-setting resistor R_{TSET} (the resistor from the TSET pin to ground).

ADVANCE INFORMATION

Feature Description (continued)

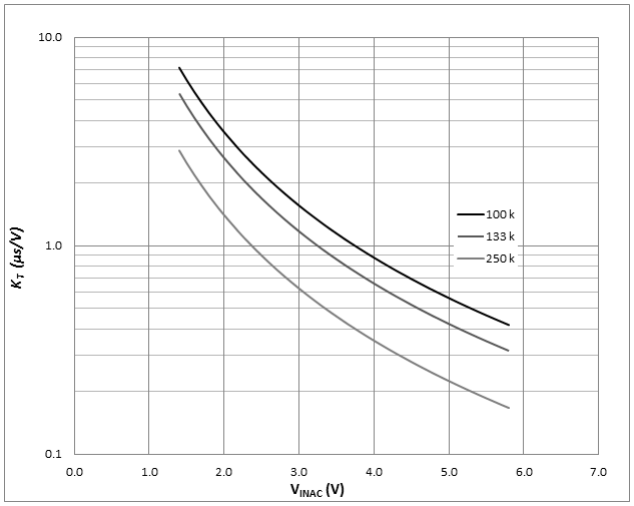


Figure 1. K_T vs Peak Voltage

ADVANCE INFORMATION

Feature Description (continued)

8.3.4 Distortion Reduction

Due to the parasitic resonance between the drain-source capacitance of the switching MOSFET and the boost inductor, conventional transition-mode PFC circuits may not be able to absorb power from the input line when the input voltage is near zero. This limitation increases total harmonic distortion as a result of ac-line current waveform distortion in the form of flat spots. To help reduce line-current distortion, the UCC28064 increases switching MOSFET on-time when the input voltage is near 0 V to improve the power absorption capability and compensate for this effect.

in the section shows the increase in on-time with respect to VINAC voltage. Excessive filtering of the VINAC signal will nullify this function.

8.3.5 Zero-Current Detection and Valley Switching

In transition-mode PFC circuits, the MOSFET turns on when the boost inductor current reaches zero. Because of the resonance between the boost inductor and the parasitic capacitance at the MOSFET drain node, part of the energy stored in the MOSFET junction capacitor can be recovered, reducing switching losses. Furthermore, when the rectified input voltage is less than half of the output voltage, all the energy stored in the MOSFET junction capacitor can be recovered and zero-voltage switching (ZVS) can be realized. By adding an appropriate delay, the MOSFET can be turned on at the valley of its resonating drain voltage (valley-switching). In this way, the energy recovery can be maximized and switching loss is minimized.

The optimal time delay is generally derived empirically, but a good starting point is a value equal to 25% of the resonant period of the drain circuit. The delay can be realized by a simple RC filter, as shown in Figure 2, but the delay time increases slightly as the input voltage nears the output voltage. Because the ZCD pin is internally clamped, a more accurate delay can also be realized by using the circuit shown in Figure 3.

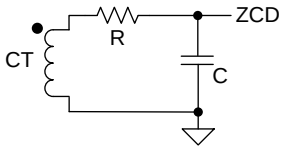


Figure 2. Simple RC Delay Circuit

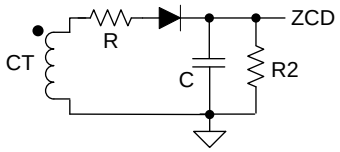


Figure 3. More Accurate Time Delay Circuit

ADVANCE INFORMATION

Feature Description (continued)

8.3.6 Phase Management and Light-Load Operation

CAUTION

APPLICABLE TO PRE-PRODUCTION UNITS:

Pre-production units have a silicon issue. If COMP pin Voltage is very close to Voltage on PHB pin it is possible that Phase B turns on and off continuously. This issue can occurs even if COMP pin Voltage is pretty constant, PHB voltage is pretty constant and RMS value of the input voltage is constant. This issue will be fixed for production units.

Under light-load conditions, switching losses may dominate over conduction losses and efficiency may be improved if one phase (channel) is turned off. At a certain power level, the reduction of switching losses is greater than the increase in conduction losses. Turning off one phase at light load is especially valuable for meeting light-load efficiency standards. This is one of the major benefits of interleaved PFC and it is especially valuable for meeting 80+ design requirements.

The PHB input can be used to set the load value when UCC28064 has to operate in single-phase mode. UCC28064 internally compares the voltage feed to PHB pin with COMP pin voltage and if Voltage of COMP pin is below PHB voltage converter is forced to operate in single phase mode: channel B will stop switching and channel A on-time will automatically double to compensate the missing power from channel B. When operating in single phase mode in order to avoid risk of inductor saturation an internal clamp ensure the ton time never can exceed the maximum on time you will have when operating in dual phase mode (PHB Voltage < COMP voltage). The device will resume dual-phase mode when Comp Voltage exceeds PHB voltage plus PHB histeresys that typically is 100mV. In order to avoid that a Voltage ripple on comp pin causes repetitive in and out from single phase mode beside the voltage hysteresis a filter was also added. In order to change from normal operation to single phase mode COMP voltage should stay below PHB pin voltage for typically 3 line half cycles. The filter does not apply for the opposite transition. when COMP voltage exceeds PHB pin voltage + the hysteresis system immediately switches to double phase mode.

ADVANCE INFORMATION

Feature Description (continued)

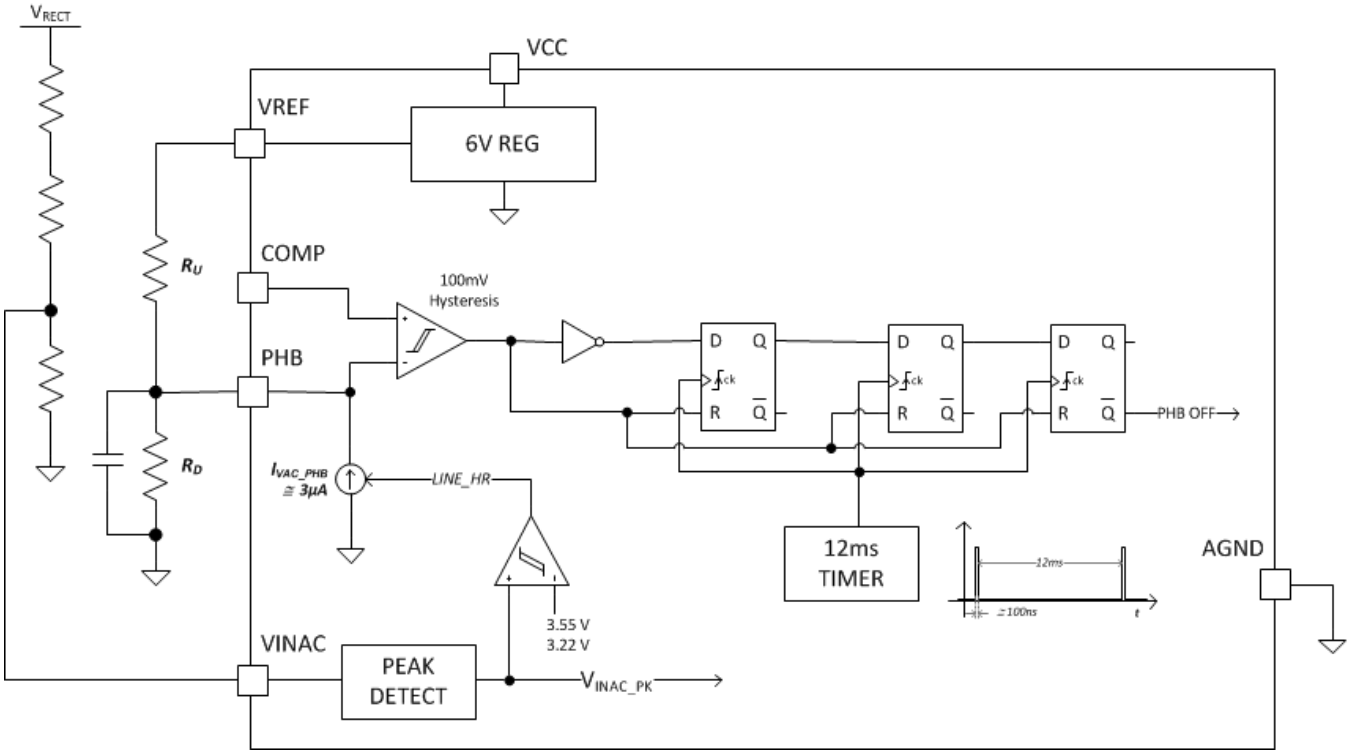


Figure 4. Phase Management Block Diagram

ADVANCE INFORMATION

Feature Description (continued)

The Voltage on PHB pin can be set using a simple resistor divider connected to V_{REF} pin. Another important feature, that allows optimization of phase management feature is that it is possible to set different thresholds according if PFC input voltage is in the range [90;132] V_{RMS} (US main) or in the range [180; 265] V_{RMS} (European main). if the peak voltage sensed by V_{INAC} pin exceeds 3.55V the converter assumes that input voltage is in the [180; 265] V_{RMS} and starts sourcing from PHB a small current (3 µA typically) that increases the voltage on PHB pin if this voltage was set by a resistor divider.

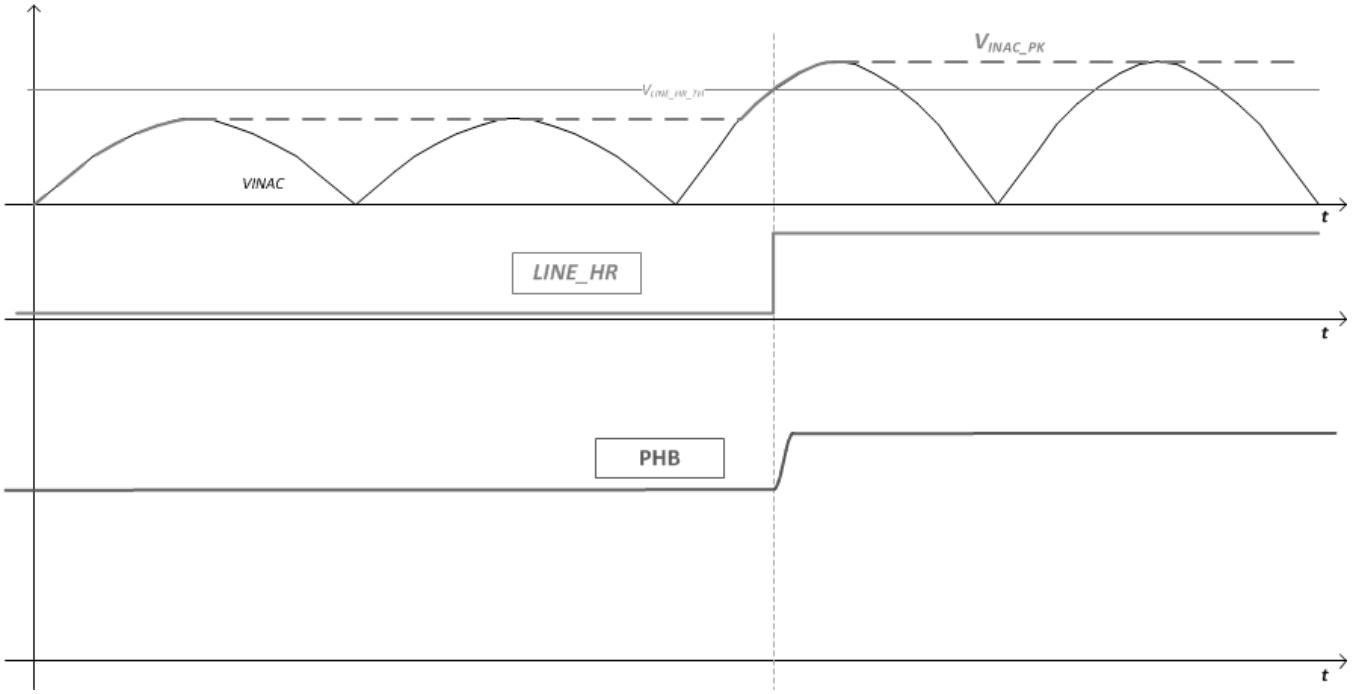


Figure 5. Change Phase Management Thresholds

Formulas that allows to calculate PHB thresholds in the two cases are the following:

$$V_{PHB\_LR} = \frac{R_D}{R_U + R_D} \cdot V_{REF} \quad (5)$$

$$V_{PHB\_HR} = \frac{R_D}{R_U + R_D} \cdot V_{REF} + \frac{R_D \cdot R_U}{R_U + R_D} \cdot I_{PHB\_RANGE} \quad (6)$$

The load value at which the system moves between single phase and dual phase modes of operation is part of the system specification. Generally we want to calculate resistor divider resistance values that allows to get the wanted thresholds. The formulas to do so are reported here below.

$$R_U = \frac{\Delta V_{PHB} \cdot V_{REF}}{V_{PHB\_LR} \cdot I_{PHB\_RANGE}} \quad (7)$$

$$R_D = \frac{\Delta V_{PHB} \cdot V_{REF}}{(V_{REF} - V_{PHB\_LR}) \cdot I_{PHB\_RANGE}} \quad (8)$$

Where $R_D$is the lower resistor of the resistor divider that provides voltage to PHB pin that is sourced by V_{REF}

$R_U$is the upper resistor of the before said resistor divider.

ADVANCE INFORMATION

Feature Description (continued)

$$\Delta V_{PHB} = V_{PHB\_HR} - V_{PHB\_LR} \tag{9}$$

PHB thresholds are selected by user according to the load value where they want to turn off Phase B. So assuming we want turn off Phase B when load goes belowP_{OUT_PHB} we can calculate the threshold using formula (11). We can use the same formula in order to calculate the two thresholds V_{PHB_HR} and V_{PHB_LR} once provided the two different load values, fro US range and EU range where Phase B has to be turned off. Of course main EU range PHB_OFF load value has to be greater than main US range PHB_OFF load value. Reasonable range of load values is [20%; 30%] of maximum load

$$V_{PHB} = \frac{(4.825V)}{V_{REF}} \cdot \frac{P_{OUT\_PHB}}{P_{OUT\_MAX}} + 125mV \tag{10}$$

ADVANCE INFORMATION

Feature Description (continued)

8.3.7 Burst Mode Operation

To further improve light load efficiency a burst mode operation can be set. Also in this case the Burst mode threshold is fed to BRST pin by external source that could be a simple resistor divider connected to V_{REF} pin. If COMP pin voltage goes below BRST pin voltage converter stops switching. When COMP voltage exceed BRST pin voltage plus hysteresis, that typically is 50mV, converter restarts switching.

In order to have smooth transition between switching to not switching and vice-versa the Burst soft start and Burst soft stop features were added. So when the COMP voltage goes below BRST voltage switching is not stopped immediately, but there will be 8 additional switching cycles where FET on time is decreased gradually. In similar way when COMP voltage exceeds BRST voltage a soft start occurs where the on time is increase gradually to value that corresponds to the present COMP voltage in eight switching cycles.

When load decreases the device is intended to operates in single phase mode starting from 35% to 15% of rated load and goes to burst mode at lower load value when single phase operation is activated. In case PHB thresholds is lower respect Burst mode threshold single phase operation is forced by burst mode operation during soft star and soft stop.

Similar to the PHB feature the burst mode threshold have two different levels according if PFC input voltage is in the range [90;132] V_{RMS} (US main) or in the range [180; 265] V_{RMS} (European main). If the peak voltage on VINAC pin exceeds 3.55V (typ.) a small current (3µA typically) is provided from BRST pin. This current rises the voltage on BRST pin if this voltage was set by a resistor divider.

Formula used to calculate the Burst mode threshold according to the resistor divider resistance are equal to the formula used to calculate the PHB thresholds.

8.3.8 External Disable

The UCC28064 can be externally disabled by Pulling the VSENSE pin to ground with an open-drain or open-collector driver. When disabled, the device supply current drops significantly and COMP is actively pulled low. This disable method forces the device into standby mode and minimizes its power consumption. This is particularly useful when standby power is a key design aspect. When VSENSE is released, the device enters soft-start mode.

ADVANCE INFORMATION

Feature Description (continued)

8.3.9 Improved Error Amplifier

The voltage-error amplifier is a transconductance amplifier. Voltage-loop compensation is connected from the error amplifier output, COMP, to analog ground, AGND. The recommended Type-II compensation network is shown in Figure 6. For loop-stability purposes, the compensation network values are calculated based on small-signal perturbations of the output voltage using the nominal transconductance (gain) of 55 μS.

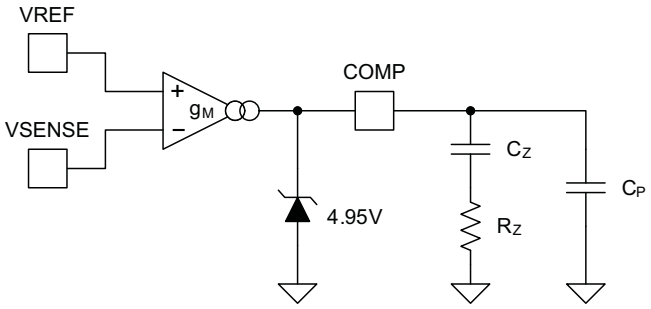
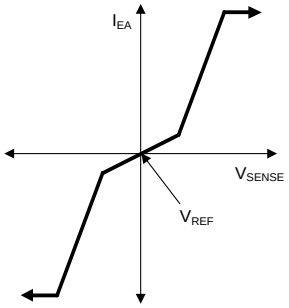


Figure 6. Transconductance Error Amplifier With Typical Compensation Network

To improve the transient response to large perturbations, the error amplifier gain increases by a factor of ~5X when the error amp input deviates more than ±5% from the nominal regulation voltage, VSENSEreg. This increase allows faster charging and discharging of the compensation components following sudden load-current increases or decreases (also refer to in the).



Basic voltage-error amplifier transconductance curve showing small-signal and large-signal gain sections, with maximum current limitations.

Figure 7. Basic Voltage-Error Amplifier Transconductance Curve

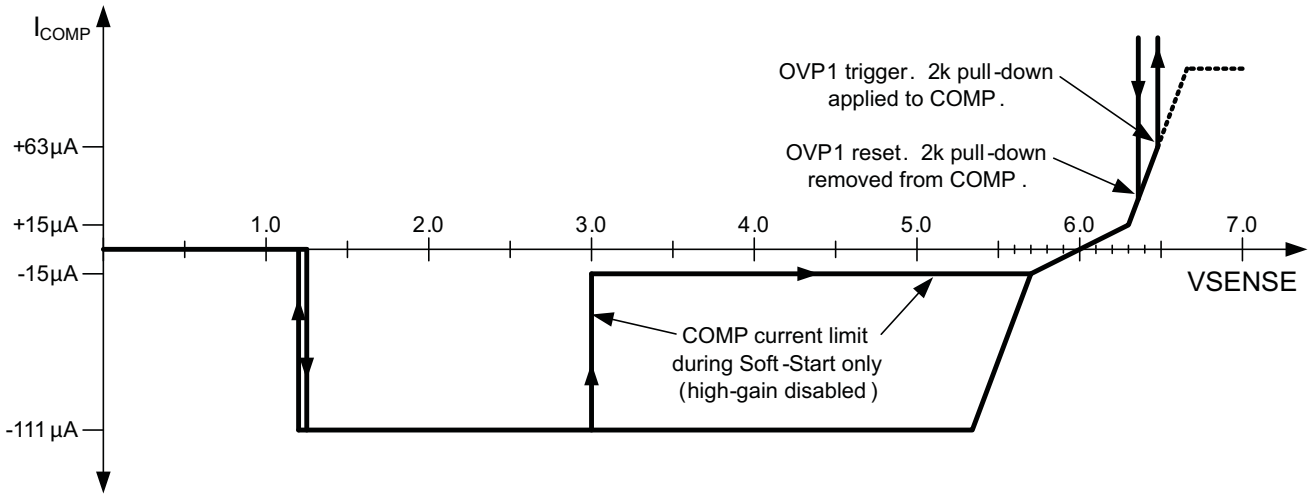
ADVANCE INFORMATION

Feature Description (continued)

8.3.10 Soft Start

Soft-start is a process for boosting the output voltage of the PFC converter from the peak of the ac-line input voltage to the desired regulation voltage under controlled conditions. Instead of a dedicated soft-start pin, the UCC28064 uses the voltage error amplifier as a controlled current source to increase the PWM duty-cycle by way of increasing the COMP voltage. To avoid excessive start-up time-delay when the ac-line voltage is low, a higher current is applied until VSENSE exceeds 3 V at which point the current is reduced to minimize the tendency for excess COMP voltage at no-load start-up.

The PWM gradually ramps from zero on-time to normal on-time as the compensation capacitor from COMP to AGND charges from zero to near its final value. This process implements a soft-start, with timing set by the output current of the error amplifier and the value of the compensation capacitors. In the event of a HVSEN FailSafe OVP, brownout, external-disable, UVLO fault, or other protection faults, COMP is actively discharged and the UCC28064 will soft-start after the triggering event is cleared. Even if a fault event happens very briefly, the fault is latched into the soft-start state and soft-start is delayed until COMP is fully discharged to 20 mV and the fault is cleared. See Figure 8 for details on the COMP current. See Figure 9 which illustrates an example of typical system behavior during soft-start.



Expanded COMP output current curve including voltage-error amplifier transconductance and modifications applicable to soft-start and overvoltage conditions.

Figure 8. Expanded Comp Output Current Curve

ADVANCE INFORMATION

Feature Description (continued)

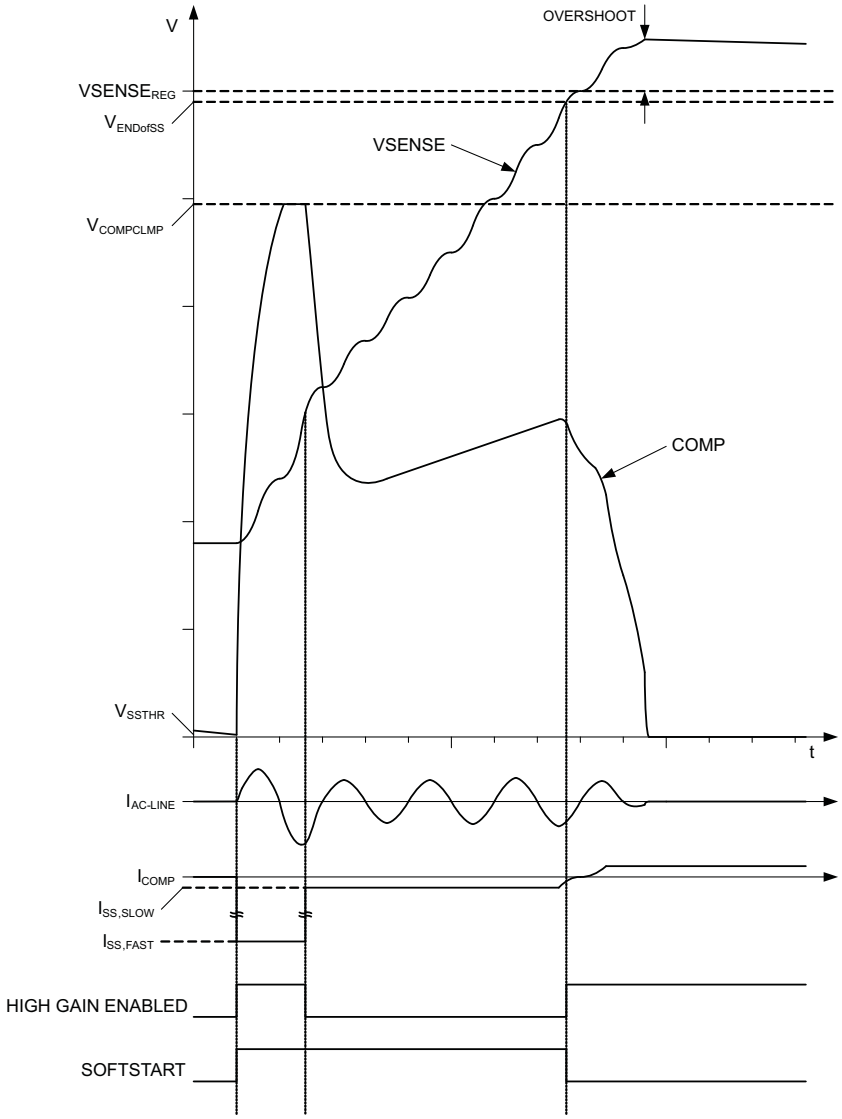


Figure 9. Soft-Start Timing With Illustrative System Behavior

ADVANCE INFORMATION

Feature Description (continued)

8.3.11 Brownout Protection

CAUTION

APPLICABLE TO PRE-PRODUCTION UNITS:

Pre-production units have a silicon issue which can occur at low line when operating in burst mode. Brown out protection has two thresholds, one higher and one lower, sets by resistor divider that senses input voltage and is connected on VINAC pin. If, and only if, device is operating in Burst mode and line voltage goes below the higher thresholds (not the lower as expected) Brown out protection is triggered and device turns off. This issue will be fixed for production units.

As the power line RMS voltage decreases, RMS input current must increase to maintain a constant output voltage for a specific load. Brownout protection helps prevent excess system thermal stress (due to the higher RMS input current) from exceeding a safe operating level. Power-line voltage is sensed at VINAC. When the VINAC fails to exceed the brownout threshold for the brownout filter time, a brownout condition is detected and both gate drive outputs are turned off. During brownout, COMP is actively pulled low and a soft-start condition is initiated. Hysteresis is built into the brownout detection circuit to avoid chatter around the threshold. When VINAC rises above the brownout threshold, the power stage soft-starts as COMP rises with controlled current.

The brownout detection threshold and its hysteresis are set by the voltage-divider ratio and resistor values. Brownout protection is based on VINAC peak voltage; the threshold and hysteresis are also based on the line peak voltage. Major hysteresis is provided by a 2-μA current-sink (I_{BOHYS}) enabled whenever VINAC falls below the brownout detection threshold. Minor hysteresis is also present in the form of a 50-mV offset (V_{BOHYS}) between the VINAC detection and clear thresholds. The peak VINAC voltage can be easily translated into an RMS value. Example resistor values for the voltage divider are 8.61 MΩ ±1% from the rectified input voltage to VINAC and 133 kΩ ±1% from VINAC to ground. These resistors set the typical thresholds for RMS line voltages, as shown in Table 1.

Table 1. Brownout Thresholds (For Conditions Stated in the Text)

THRESHOLD	AC-LINE VOLTAGE (RMS)
Falling	66 V
Rising	78 V

Equation 11 and Equation 12 can be used to calculate the VINAC divider-resistor values based on desired brownout detection and brownout clear voltage levels. V_{AC_OK} is the desired RMS turnon voltage, V_{AC_BO} is the desired RMS turnoff brownout voltage, and V_{LOSS} is total series voltage drop due to wiring, EMI-filter, and bridge-rectifier impedances at V_{AC_BO}. V_{BODET}, V_{BOHYS} and I_{BOHYS} are found in the data-tables of this datasheet.

$$R_A = \left(\frac{\sqrt{2}(V_{AC\_OK} - V_{AC\_BO}) - V_{BOHYS}}{I_{BOHYS}} \right) \left(1 + \frac{V_{BOHYS}}{V_{BODET}} \right) \tag{11}$$

$$R_B = \frac{R_A}{\left(\frac{\sqrt{2}V_{AC\_BO} - V_{LOSS}}{V_{BODET}} - 1 \right)} \tag{12}$$

When standard values for the VINAC divider-resistors R_A and R_B are selected, the actual turnon and brownout threshold RMS voltages for the ac-line can be back-calculated with Equation 13 and Equation 14:

$$V_{AC\_BO} = \left(1 + \frac{R_A}{R_B} \right) \frac{V_{BODET}}{\sqrt{2}} + \frac{V_{LOSS}}{\sqrt{2}} \tag{13}$$

ADVANCE INFORMATION

$$V_{AC\_OK} = V_{AC\_BO} + \frac{R_A I_{BOHYS}}{\sqrt{2}\left(1+\frac{V_{BOHYS}}{V_{BODET}}\right)} + \frac{V_{BOHYS}}{\sqrt{2}} \quad (14)$$

An example of the timing for the brownout function is illustrated in Figure 10.

For a quick estimation of the turnon and brownout voltages, simplify the foregoing equations by setting the V_{LOSS} and V_{BOHYS} terms to zero.

8.3.12 Dropout Detection

It is often the case that the ac-line voltage momentarily drops to zero or nearly zero, due to transient abnormal events affecting the local ac power distribution network. Referred to as ac-line dropouts (or sometimes as line-dips) the duration of such events usually extends to only 1 or 2 line cycles. During a dropout, the down-stream power conversion stages depend on sufficient energy storage in the PFC output capacitance, which is sized to provide the ride-through energy for a specified hold-up time. Typically while the PFC output voltage is falling, the voltage-loop error amplifier output rises in an attempt to maintain regulation. As a consequence, excess duty-cycle is commanded when the ac-line voltage returns and high peak current surges may saturate the boost inductors with possible overstress and audible noise.

The UCC28064 incorporates a dropout detection feature which suspends the action of the error amplifier for the duration of the dropout. If the VINAC voltage falls below 0.35 V for longer than 5 ms, a dropout condition is detected and the error amplifier output is turned off. In addition, a 4-μA pulldown current is applied to COMP to gently discharge the compensation network capacitors. In this way, when the ac-line voltage returns, the COMP voltage (and corresponding duty-cycle setting) remains very near or even slightly below the level it was before the dropout occurred. Current surges due to excess duty-cycle, and their undesired attendant effects, are avoided. The dropout condition is cancelled and the error amplifier resumes normal operation when VINAC rises above 0.71 V.

Based on the VINAC divider-resistor values calculated for brownout in the previous section, the input RMS voltage thresholds for dropout detection V_{AC_DO} and dropout clearing V_{DO_CLR} can be determined using Equation 15 and Equation 16, below.

$$V_{AC\_DO} = \frac{V_{DODET}\left(\frac{R_A}{R_B}+1\right) + V_{LOSS}}{\sqrt{2}} \quad (15)$$

$$V_{DO\_CLR} = \frac{V_{DOCLR}\left(\frac{R_A}{R_B}+1\right) + V_{LOSS}}{\sqrt{2}} \quad (16)$$

ADVANCE INFORMATION

Avoid excessive filtering of the VINAC signal, or dropout detection may be delayed or defeated. An RC time-constant of ≤ 100-µs should provide good performance. An example of the timing for the dropout function is illustrated in Figure 11.

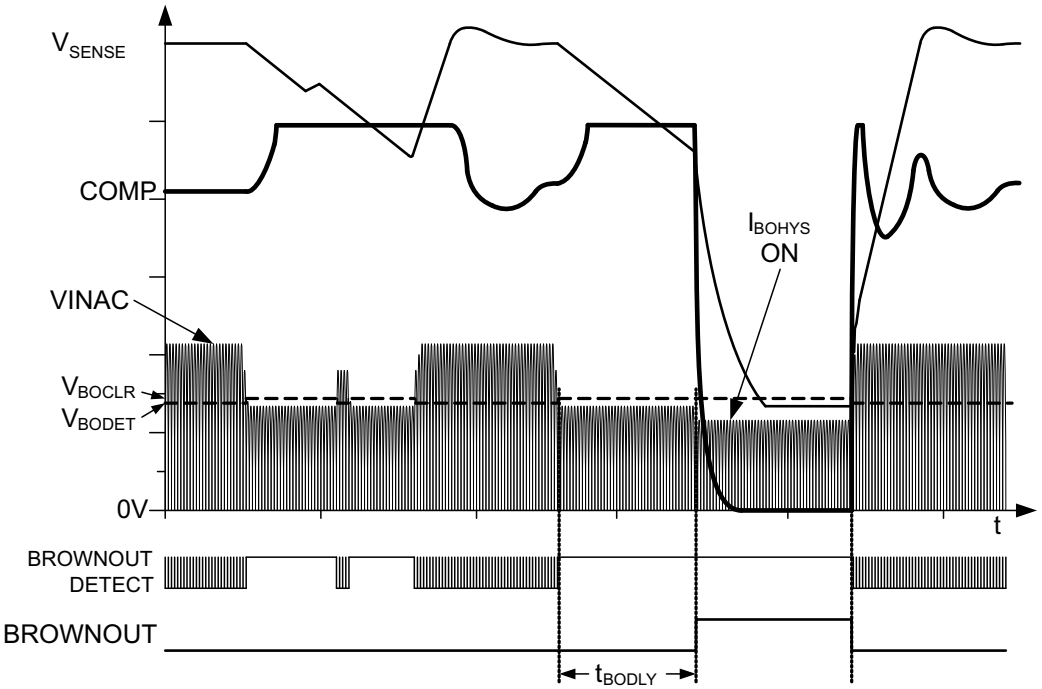


Figure 10. AC-Line Brownout Timing With Illustrative System Behavior

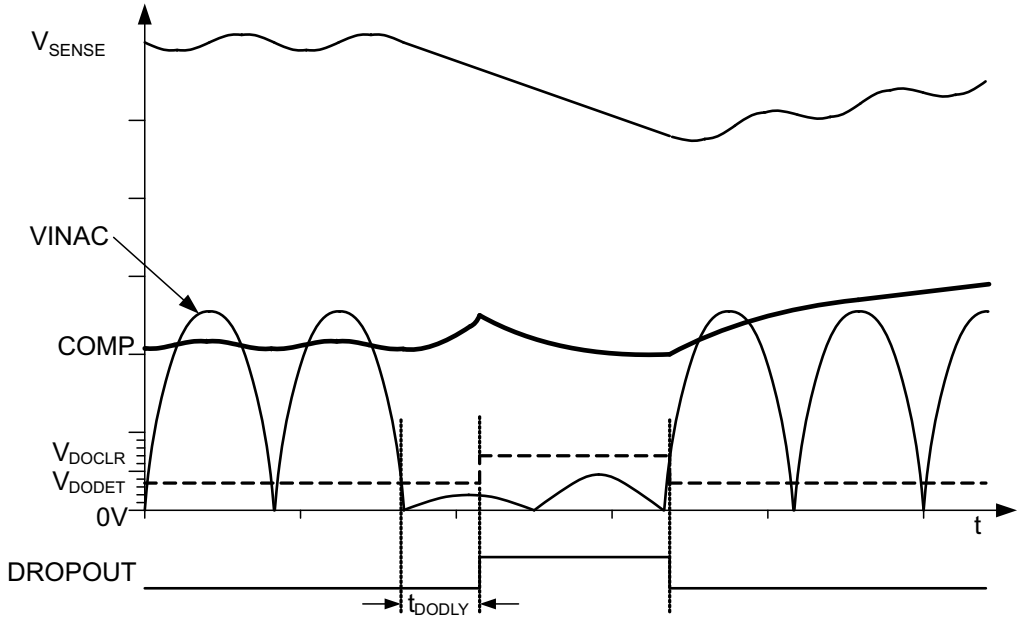


Figure 11. AC-Line Dropout Timing With Illustrative System Behavior

ADVANCE INFORMATION

8.3.13 VREF

VREF is an output which supplies a well-regulated reference voltage to circuits within the device as well as serving as a limited source for external circuits. This output must be bypassed to GND with a low-impedance 0.1-μF or larger capacitor placed as close to the VREF and GND pins as possible. Current draw by external circuits should not exceed a few milli-amperes and should not be pulsing.

The VREF output is disabled under the following conditions: when VCC is in UVLO, or when VSENSE is below the Enable threshold. This output can only source current and is unable to accept current into the pin.

8.3.14 VCC

VCC is usually connected to a bias supply of between 13 V and 21 V. To minimize switching ripple voltage on VCC, it should be by-passed with a low-impedance capacitor as close to the VCC and GND pins as possible. The capacitance should be sized to adequately decouple the peak currents due to gate-drive switching at the highest operating frequency. When powered from a poorly-regulated low-impedance supply, an external zener diode is recommended to prevent excessive current into VCC.

The undervoltage-lockout (UVLO) condition is when VCC voltage has not yet reached the turnon threshold or has fallen below the turnoff threshold, having already been turned on. While in UVLO, the VREF output and most circuits within the device are disabled and VCC current falls significantly below the normal operating level. The same situation applies when VSENSE is below its Enable threshold. This helps minimize power loss during pre-powerup and standby conditions.

8.3.15 System Level Protections

8.3.15.1 Failsafe OVP - Output Overvoltage Protection

FailSafe OVP prevents any single failure from allowing the output to boost above safe levels. Redundant paths for output voltage sensing provide additional protection against output overvoltage. Over-voltage protection is implemented through two independent paths: VSENSE and HVSEN. The converter shuts down if either input senses a severe overvoltage condition. The output voltage can still remain below a safe limit if either sense path fails. The device is re-enabled when both sense inputs fall back into their normal ranges. At that time, the gate drive outputs will resume switching under PWM control. A low-level overvoltage on VSENSE does not trigger soft-start, but the COMP pin is discharged by an internal 2-kΩ resistance until the output voltage falls below the 2% hysteresis OV-clear threshold. A higher-level overvoltage on VSENSE additionally shuts off the gate-drive outputs until the OV clears, but still does not trigger a soft-start. However, an overvoltage detected on HVSEN does trigger a full soft-start and the COMP pin is fully discharged to 20 mV before the soft-start can begin.

8.3.15.2 Overcurrent Protection

CAUTION

APPLICABLE TO PRE-PRODUCTION UNITS:

Pre-production units have a silicon issue. If OC current protection is triggered device stops switching and switching is disabled until the sensed current goes down to low current as expected. When switching restarts it restarts operating the same soft start as it was restart switching in burst mode. This is not wanted behavior. The wanted behavior should be that the device restart switching soon with the expected on time fixed by line RMS voltage and COMP pin voltage. This issue will be fixed for production units.

Under certain conditions (such as inrush, brownout-recovery, and output over-load) the PFC power stage sees large currents. It is critical that the power devices be protected from switching during these conditions.

The conventional current-sensing method uses a shunt resistor in series with each MOSFET source leg to sense the converter currents, resulting in multiple ground points and high power dissipation. Furthermore, since no current information is available when the MOSFETs are off, the source-resistor current-sensing method results in repeated turnon of the MOSFETs during overcurrent (OC) conditions. Consequently, the converter may temporarily operate in continuous conduction mode (CCM) and may experience failures induced by excessive reverse-recovery currents in the boost diodes or other abnormal stresses.

The UCC28064 uses a single resistor to continuously sense the combined total inductor (input) current. This way, turnon of the MOSFETs is completely avoided when the inductor currents are excessive. The gate drive to the MOSFETs is inhibited until total inductor current drops to near zero, precluding reverse-recovery-induced failures (these failures are most likely to occur when the ac-line recovers from a brownout condition).

The nominal OC threshold voltage during two-phase operation is -200 mV, which helps minimize losses. This threshold is automatically reduced to -166 mV during single-phase operation, either by detection of a phase failure or because PHB is driven below 0.8 V. Note that the single-phase threshold is not simply 1/2 of the dual-phase threshold, because the ratio of the single-phase peak current to the interleaved peak current is higher than 1/2.

An OC condition immediately turns off both gate-drive outputs, but does not trigger a soft-start and does not modify the error amplifier operation. The overcurrent condition is cleared when the total inductor current-sense voltage falls below the OC-clear threshold (–15 mV).

Following an overcurrent condition, both MOSFETs are turned on simultaneously once the input current drops to near zero. Because the two phase currents are temporarily operating in-phase, the current-sense resistance should be chosen so that OC protection is not triggered with twice the maximum current peak value of either phase to allow quick return to normal operation after an overcurrent event. Automatic phase-shift control will re-establish interleaving within a few switching cycles.

8.3.15.3 Open-Loop Protection

If the feedback loop is disconnected from the device, a 100-nA current source internal to the UCC28064 pulls the VSENSE pin voltage towards ground. When VSENSE falls below 1.20 V, the device becomes disabled. When disabled, the bias supply current decreases, both gate-drive outputs and COMP are actively pulled low, and a soft-start condition is initiated. The device is re-enabled when VSENSE rises above 1.25 V. At that time, the gate drive outputs will begin switching under soft-start PWM control.

If the feedback loop is disconnected from ground, the VSENSE voltage will be pulled high. When VSENSE rises above the 2nd-level overvoltage protection threshold, both gate drive outputs are shut off and COMP is actively pulled low. The device is re-enabled when VSENSE falls below the OV-clear threshold. The VSENSE input can tolerate a limited amount of current into the device under abnormally high input voltage conditions. Refer to the Absolute Maximum Ratings table near the beginning of this datasheet for details.

ADVANCE INFORMATION

8.3.15.4 VCC Undervoltage Lock-Out (UVLO) Protection

VCC must rise above the turnon threshold for the PWM to begin functioning. If VCC drops below the UVLO threshold during operation, both gate-drive outputs are actively pulled low, COMP is actively pulled low, and a soft-start condition is triggered. VCC must again rise above the turnon threshold for the PWM function to restart in soft-start mode.

8.3.15.5 Phase-Fail Protection

The UCC28064 detects failure of either of the phases by monitoring the sequence of ZCD pulses. During normal two-phase operation, if one ZCD input remains idle for longer than approximately 400µs while the other ZCD input switches normally, the overcurrent threshold is reduced. During normal single-phase operation (PHB < 0.8 V), phase failure is not monitored. Phase failure is not monitored also when COMP is below approximately 250 mV.

8.3.15.6 Thermal Shutdown Protection

Overloading of the gate-drive outputs, VREF, or both can dissipate excess power within the device which may raise the internal temperature of the circuits beyond a safe level. Even normal power dissipation can generate excess heat if the thermal impedance is too high or the ambient temperature is too high. When the UCC28064 detects an internal over-temperature condition it will shutdown the outputs and trigger a full soft-start condition. When the internal device junction temperature has cooled below the thermal hysteresis temperature, operation will resume under soft-start control.

8.3.15.7 AC-Line Brownout and Dropout Protections

See specific discussions for each topic in previous sections of this data sheet.

8.3.15.8 Fault Logic Diagram

Figure 12 depicts the fault-handling logic involving VSENSE, COMP, and several internal states.

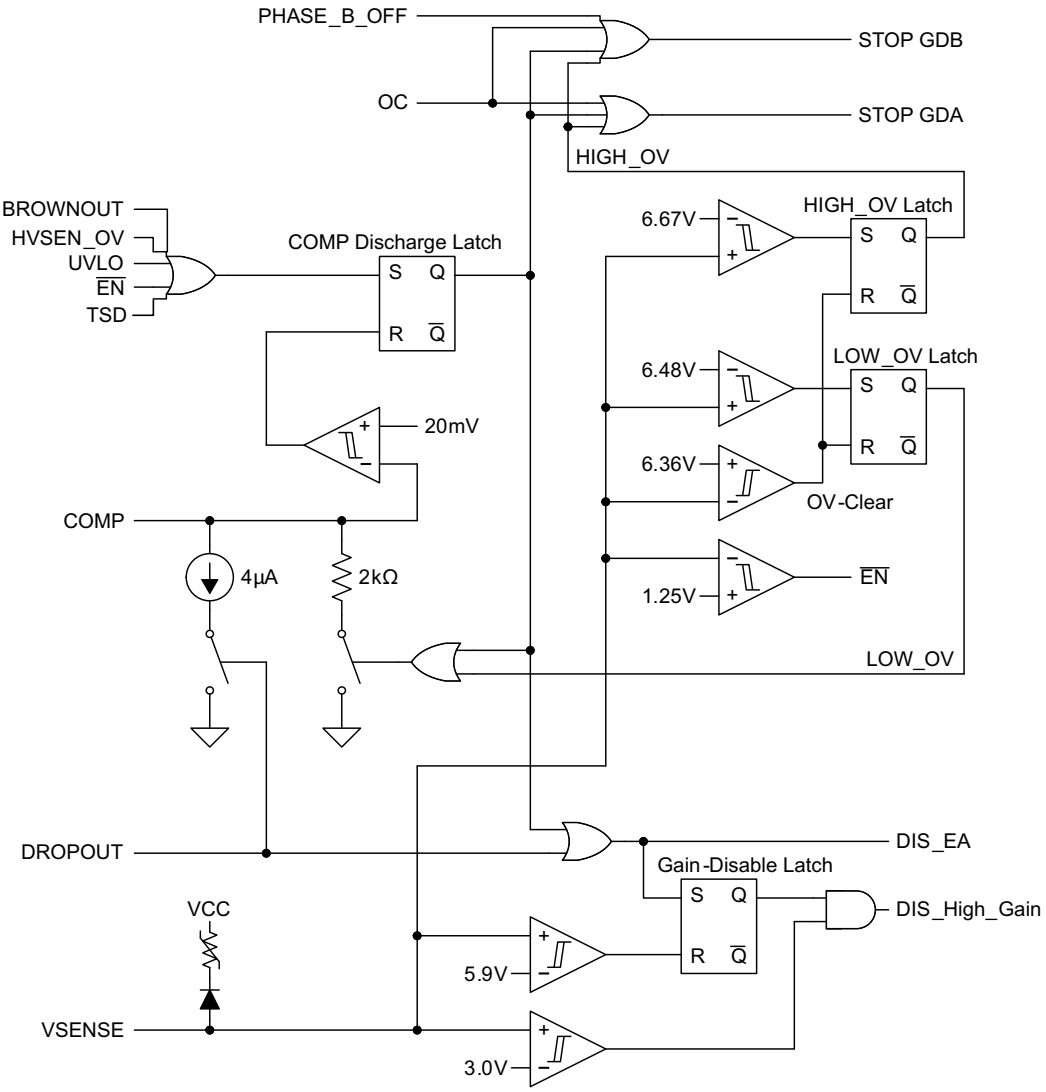


Figure 12. Fault Logic With VSENSE Detections and Error Amplifier Control

ADVANCE INFORMATION

8.4 Device Functional Modes

The controller is primarily intended for set up as a dual phase interleaved PFC which utilizes inductor demagnetization information based on inductor sense winding voltages which are routed to ZCDA and ZCDB to trigger the start of a switching cycle.

The functionality may be extended in a couple of ways:

Phase-B Enable and Disable: Phase-B can be *shed* by explicit user control or it may be set up as an automatic light load efficiency management feature. When the voltage applied on pin COMP is below the voltage on the PHB pin , Phase B and the Phase Fail Detector will be disabled. The On-time for Phase-A will be doubled to minimize the output voltage transient which would otherwise occur. When the voltage on pin COMP is greater than the PHB pin voltage, two phase mode is enabled. Connect PHB to a resistor divider sourced by VREF to set a threshold for COMP pin and obtain a automatic light load efficiency managment feature. Alternatively PHB may be driven by external command from 5V to 0 to external force phase shedding. When PHB voltage is higher then COMP voltage, the ton time is doubled, so in order to avoid risk of inductor saturation an internal clamp ensure the ton time never can exceed the maximum on time you will have when operating in dual phase mode (PHB Voltage < COMP voltage).

PFC Stage Enable and Disable Control: Controller operation is enabled when VSENSE voltage exceeds the 1.25-V enable threshold. The primary disable method should be by pulling VSENSE low by an open drain or open collector logic output. This will disable the outputs and significantly reduce VCC current. Releasing VSENSE will initiate a soft-start. Avoid any PCB traces which would couple any noise into this node.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This control device is generally applicable to the control of AC-DC power supplies which require Active Power Factor Correction off Universal AC line. Applications using this device generally meet the Class-D equipment input current harmonics standards per EN61000-3-2. This standard applies to equipment with rated Powers higher than 75W. The device brings two phase interleaved control capability to the Transition Mode Boost and hence will be generally a very good choice for cost optimized applications in the 150W to 800W space, or to even lower powers that wish to exploit the interleaving benefits of reduced filtering component size, lower profile solutions and distributed thermal management.

9.2 Typical Application

Figure 13 shows an example of the UCC28064 PFC controller in a two-phase interleaved, transition-mode PFC preregulator.

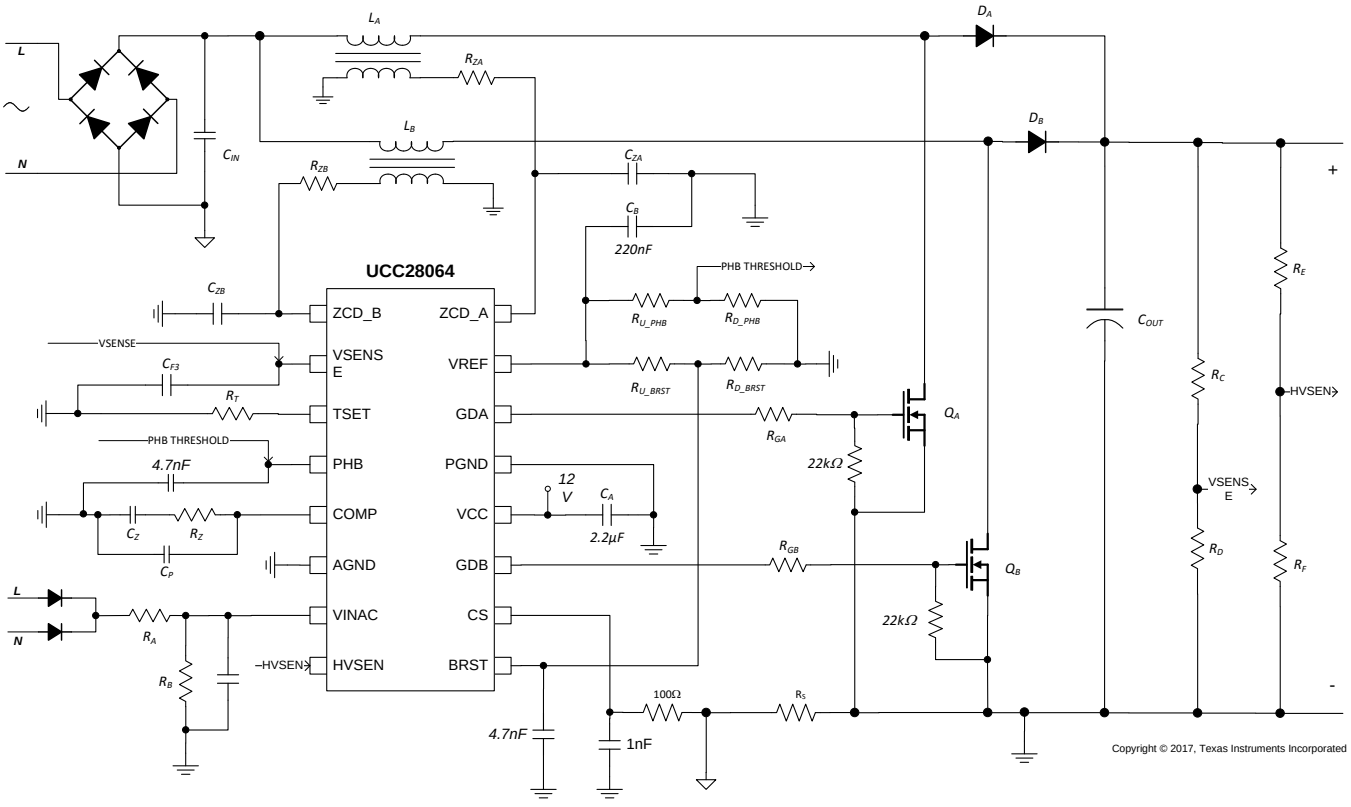


Figure 13. Typical Interleaved Transition-Mode PFC Preregulator

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Typical Application (continued)

9.2.1 Design Requirements

The specifications for this design were chosen based on the power requirements of a typical 300-W LCD TV. Table 2 lists these specifications.

Table 2. Design Specifications

DESIGN PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	RMS input voltage	85 (VIN_MIN)		265 (VIN_MAX)	VRMS
V_{OUT}	Output voltage		390		V
f_{LINE}	AC-line frequency	47		63	Hz
PF	Power factor at maximum load	0.90			
P_{OUT}				300	W
η	Full-load efficiency	92%			
f_{MIN}	Minimum switching frequency	45			kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCC28064 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

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9.2.2.2 Inductor Selection

The boost inductor is selected based on the inductor ripple current requirements at the peak of low line. Selecting the inductor requires calculating the boost converter duty cycle at the peak of low line ($D_{PEAK\_LOW\_LINE}$), as shown in Equation 17.

$$D_{PEAK\_LOW\_LINE} = \frac{V_{OUT} - V_{IN\_MIN}\sqrt{2}}{V_{OUT}} = \frac{390\,V - 85\,V\sqrt{2}}{390\,V} \approx 0.69 \quad (17)$$

The minimum switching frequency of the converter (f_{MIN}) under low line conditions occurs at the peak of low line and is set between 25 kHz and 50 kHz to avoid audible noise. For this design example, f_{MIN} is set to 45 kHz. For a 2-phase interleaved design, L1 and L2 are determined as shown in Equation 18.

$$L1 = L2 = \frac{\eta \times V_{IN\_MIN}^{2} \times D_{PEAK\_LOW\_LINE}}{P_{OUT} \times f_{MIN}} = \frac{0.92(85\,V)^{2}0.69}{300\,W \times 45\,kHz} \approx 340\,\mu H \quad (18)$$

The inductor for this design would have a peak current (I_{LPEAK}) of 5.4 A, as shown in Equation 19, and an RMS current (I_{LRMS}) of 2.2 A, as shown in Equation 20.

$$I_{LPEAK} = \frac{P_{OUT}\sqrt{2}}{V_{IN\_MIN} \times \eta} = \frac{300\,W\sqrt{2}}{85\,V \times 0.92} \approx 5.4\,Apk \quad (19)$$

$$I_{LRMS} = \frac{I_{LPEAK}}{\sqrt{6}} = \frac{5.4\,A}{\sqrt{6}} \approx 2.2\,Arms \quad (20)$$

This converter uses constant on time (T_{ON}) and zero-current detection (ZCD) to set up the converter timing. Auxiliary windings on L1 and L2 detect when the inductor currents are zero. Selecting the turns ratio using Equation 21 ensures that there will be at least 2 V at the peak of high line to reset the ZCD comparator after every switching cycle.

The turns-ratio of each auxiliary winding is:

$$\frac{N_P}{N_s} = \frac{V_{OUT} - V_{IN\_MAX}\sqrt{2}}{2\,V} = \frac{390\,V - 265\,V\sqrt{2}}{2\,V} \approx 8 \quad (21)$$

9.2.2.3 ZCD Resistor Selection (R_{ZA}, R_{ZB})

The minimum value of the ZCD resistors is selected based on the internal clamps maximum current ratings of 3 mA, as shown in Equation 22.

$$R_{ZA} = R_{ZB} \geq \frac{V_{OUT}N_S}{N_P \times 3\,mA} = \frac{390\,V}{8 \times 3\,mA} \approx 16.3\,k\Omega \quad (22)$$

In this design the ZCD resistors are set to 20 kΩ, as shown in Equation 23.

$$R_{ZA} = R_{ZB} = 20\,k\Omega \quad (23)$$

9.2.2.4 HVSEN

According to R_E and R_F resistor values, the FailSafe OVP threshold will be set according to Equation 24

$$V_{OV\_FAILSAFE} = \frac{4.87\,V\left(R_E + R_F\right)}{R_F} = \frac{4.87\,V\left(8.22M\Omega + 82.5k\Omega\right)}{82.5k\Omega} \approx 490\,V \quad (24)$$

ADVANCE INFORMATION

9.2.2.5 Output Capacitor Selection

The output capacitor (C_{OUT}) is selected based on holdup requirements, as shown in Equation 25.

$$C_{OUT} \geq \frac{2\frac{P_{OUT}}{\eta}\frac{1}{f_{LINE}}}{V_{OUT}^{2} - (V_{OUT\_MIN})^{2}} = \frac{2\frac{300\,W}{0.92}\frac{1}{47\,Hz}}{390\,V^{2} - (252\,V)^{2}} \approx 156\,\mu F \tag{25}$$

Two 100-µF capacitors were used in parallel for the output capacitor.

$$C_{OUT} = 200\,\mu F \tag{26}$$

For this size capacitor, the low-frequency peak-to-peak output voltage ripple (V_{RIPPLE}) is approximately 14 V, as shown in Equation 27:

$$V_{RIPPLE} = \frac{2 \times P_{OUT}}{\eta}\frac{1}{V_{OUT} \times 4\pi \times f_{LINE} \times C_{OUT}} = \frac{2 \times 300\,W}{0.92 \times 390\,V \times 4\pi \times 47\,Hz \times 200\,\mu F} \approx 14\,Vppk \tag{27}$$

In addition to holdup requirements, a capacitor must be selected so that it can withstand the low-frequency RMS current (I_{COUT_100Hz}) and the high-frequency RMS current (I_{COUT_HF}); see Equation 28 to Equation 30. High-voltage electrolytic capacitors generally have both a low- and a high-frequency RMS current ratings on the product data sheets.

$$I_{COUT\_100Hz} = \frac{P_{OUT}}{V_{OUT} \times \eta \times \sqrt{2}} = \frac{300\,W}{390\,V \times 0.92 \times \sqrt{2}} = 0.591\,Arms \tag{28}$$

$$I_{COUT\_HF} = \sqrt{\left(\frac{P_{OUT}\,2\sqrt{2}}{2 \times \eta \times V_{IN\_MIN}}\sqrt{\frac{4\sqrt{2}V_{IN\_MIN}}{9\pi V_{OUT}}}\right)^{2} - \left(I_{COUT\_100Hz}\right)^{2}} \tag{29}$$

$$I_{COUT\_HF} = \sqrt{\left(\frac{300\,W \times 2\sqrt{2}}{2 \times 0.92 \times 85\,V}\sqrt{\frac{4\sqrt{2} \times 85\,V}{9\pi \times 390\,V}}\right)^{2} - (0.591A)^{2}} \approx 0.966\,Arms \tag{30}$$

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9.2.2.6 Selecting (R_S) For Peak Current Limiting

The UCC28064 peak limit comparator senses the total input current and is used to protect the MOSFETs during inrush and over-load conditions. For reliability, the peak current limit (I_{PEAK}) threshold in this design is set for 120% of the nominal maximum current that will be observed during power up, as shown in Equation 31.

$$I_{PEAK} = \frac{2P_{OUT}\sqrt{2}(1.2)}{\eta \times V_{IN\_MIN}} = \frac{2 \times 300\,W\sqrt{2} \times 1.2}{0.92 \times 85\,V} \approx 13\,A \tag{31}$$

A standard 15-mΩ metal-film current-sense resistor will be used for current sensing, as shown in Equation 32. The estimated power loss of the current-sense resistor (P_{RS}) is less than 0.25 W during normal operation, as shown in Equation 33.

$$R_S = \frac{200\,mV}{I_{PEAK}} = \frac{200\,mV}{13\,A} \approx 15\,m\Omega \tag{32}$$

$$P_{RS} = \left(\frac{P_{OUT}}{V_{IN\_MIN} \times \eta}\right)^2 R_S = \left(\frac{300\,W}{85\,V \times 0.92}\right)^2 \times 15\,m\Omega \approx 0.22\ W \tag{33}$$

The most critical parameter in selecting a current-sense resistor is the surge rating. The resistor needs to withstand a short-circuit current larger than the current required to open the fuse (F1). I^2t (ampere-squared-seconds) is a measure of thermal energy resulting from current flow required to melt the fuse, where I^2t is equal to RMS current squared times the duration of the current flow in seconds. A 4-A fuse with an I^2t of 14 A^2s was chosen to protect the design from a short-circuit condition. To ensure the current-sense resistor has high-enough surge protection, a 15-mΩ, 500-mW, metal-strip resistor was chosen for the design. The resistor has a 2.5-W surge rating for 5 seconds. This result translates into 833 A^2s and has a high-enough I^2t rating to survive a short-circuit before the fuse opens, as described in Equation 34.

$$I^2t = \frac{2.5\,W}{0.015\,\Omega} \times 5s = 833\,A^2s \tag{34}$$

9.2.2.7 Power Semiconductor Selection (Q1, Q2, D1, D2)

The selection of Q1, Q2, D1, and D2 are based on the power requirements of the design. For an explanation of how to select power semiconductor components for transition-mode PFC preregulators, refer to *UCC38050 100-W Critical Conduction Power Factor Corrected (PFC) Pre-regulator*.

The MOSFET (Q1, Q2) pulsed-drain maximum current is shown in Equation 35:

$$I_{DM} \geq I_{PEAK} = 13\,A \tag{35}$$

The MOSFET (Q1, Q2) RMS current calculation is shown in Equation 36:

$$I_{DS} = \frac{I_{PEAK}}{2}\sqrt{\frac{1}{6} - \frac{4\sqrt{2}\,V_{IN\_MIN}}{9\pi \times V_{OUT}}} = \frac{13\,A}{2}\sqrt{\frac{1}{6} - \frac{4\sqrt{2} \times 85\,V}{9\pi \times 390\,V}} \approx 2.3\,A \tag{36}$$

To meet the power requirements of the design, IRFB11N50A 500-V MOSFETs were chosen for Q1 and Q2.

The boost diode (D1, D2) RMS current is shown in Equation 37:

$$I_D = \frac{I_{PEAK}}{2}\sqrt{\frac{4\sqrt{2} \times V_{IN\_MIN}}{9\pi \times V_{OUT}}} = \frac{13\,A}{2}\sqrt{\frac{4\sqrt{2} \times 85\,V}{9\pi \times 390\,V}} \approx 1.4\,A \tag{37}$$

To meet the power requirements of the design, MURS360T3, 600-V diodes were chosen for D1 and D2.

ADVANCE INFORMATION

9.2.2.8 Brownout Protection

Resistor R_A and R_B are selected to activate brownout protection at ~75% of the specified minimum-operating input voltage. Resistor R_A programs the brownout hysteresis comparator, which is selected to provide 17 V (~12 V_{RMS}) of hysteresis. Calculations for R_A and R_B are shown in Equation 38 through Equation 41.

$$R_A = \frac{\text{Hysteresis}}{2\mu A} = \frac{17\,V}{2\mu A} = 8.5M\Omega \tag{38}$$

To meet voltage requirements, three 2.87-MΩ resistors were used in series for R_A.

$$R_A = 3 \times 2.87M\Omega = 8.61M\Omega \tag{39}$$

$$R_B = \frac{1.4\,V \times R_A}{V_{IN\_MIN} \times 0.75\sqrt{2} - 1.4\,V} = \frac{1.4\,V \times 8.61M\Omega}{85\,V \times 0.75\sqrt{2} - 1.4\,V} = 135.8k\Omega \tag{40}$$

Select a standard value for R_B.

$$R_B = 133k\Omega \tag{41}$$

In this design example, brownout becomes active (shuts down PFC) when the input drops below 66 V_{RMS} for longer than 440 ms and deactivates (restarts with a full soft start) when the input reaches 78 V_{RMS}.

9.2.2.9 Converter Timing

The MOSFET on-time T_{ON} depends on value of the selected inductance on load value, represented by COMP pin voltage and by the converter AC input voltage Equation 42. To ensure proper operation, the timing must be set based on the highest boost inductance ($L1_{MAX}$) and output power (P_{OUT}) at minimum operating AC input Voltage. Becasue the input voltage is sensed by VINAC pin the on time setting needs to take into account of the selected resistor divider that provide voltage at VINAC pin. In this design example, the boost inductor could be as high as 390 µH.

Let's call K_{BO} the ratio:Equation 46.

$$K_{BO} = \frac{R_A + R_B}{R_B} = \frac{8.61M\Omega + 133k\Omega}{133k\Omega} = 65.74 \tag{42}$$

the Maximum on time at full load (P_{OUT} = 300W) and minimum input voltage (85V_{AC}) is given by formula;

$$t_{ON\_MAX} = \frac{P_{OUT} \cdot L1_{MAX}}{\eta \cdot PF \cdot (V_{IN\_MIN})^2} = \frac{(300W) \cdot (390\mu H)}{0.92 \cdot 0.9 \cdot (85)^2} = 19.56\mu s \tag{43}$$

The value of the resistor (R_T) connected to TSET pin to set the on time timers is the minimum of R_{TH} and R_{TL} provided by formulas (46) and (47)

$$R_T = min(R_{TL}, R_{TH}) \tag{44}$$

$$R_{TH} = \frac{K_{TH\_min} \cdot (5V)^2 \cdot (133k\Omega) \cdot (4.825V)}{\left(\frac{\sqrt{2} \cdot V_{IN\_MIN}}{K_{BO}}\right)^2 \cdot t_{ON\_MAX}} \tag{45}$$

$$R_{TL} = \frac{K_{TL\_min} \cdot (1.6V)^2 \cdot (133k\Omega) \cdot (4.825V)}{\left(\frac{\sqrt{2} \cdot V_{IN\_MIN}}{K_{BO}}\right)^2 \cdot t_{ON\_MAX}} \tag{46}$$

Where the values of K_{TL_min} and K_{TH_min} are the minimum values of K_{TL} and K_{TH} parameters reported on the electrical characteristic table at page 7 of this datasheet.

The selected value for R_T is 91 kΩ.

ADVANCE INFORMATION

9.2.2.10 Programming V_{OUT}

Resistor R_C is selected to minimize loading on the power line when the PFC is disabled. Construct resistor R_C from two or more resistors in series to meet high-voltage requirements. Resistor R_D is then calculated based on R_C, the reference voltage, V_{REF}, and the required output voltage, V_{OUT}. Based on the values shown in Equation 47 to Equation 50, the primary output overvoltage protection threshold should be as shown in Equation 51:

$$R_C = 2.74\,M\Omega + 2.74\,M\Omega + 3.01\,M\Omega = 8.49\,M\Omega \quad (47)$$

$$V_{REF} = 6\ V \quad (48)$$

$$R_D = \frac{V_{REF} \times R_C}{V_{OUT} - V_{REF}} = \frac{6\,V \times 8.49\,M\Omega}{390\,V - 6\,V} = 132.7\,k\Omega \quad (49)$$

Select a standard value for R_D.

$$R_D = 133\,k\Omega \quad (50)$$

$$V_{OVP} = 6.48\,V \frac{R_C + R_D}{R_D} = 6.48\,V \frac{8.49\,M\Omega + 133\,k\Omega}{133\,k\Omega} = 420.1V \quad (51)$$

9.2.2.11 Voltage Loop Compensation

Resistor R_Z is sized to attenuate low-frequency ripple to less than 2% of the voltage amplifier output range. This value ensures good power factor and low harmonic distortion on the input current.

The transconductance amplifier small-signal gain is shown in Equation 52:

$$g_m = 50\,\mu S \quad (52)$$

The voltage-divider feedback gain is shown in Equation 53:

$$H = \frac{V_{REF}}{V_{OUT}} = \frac{6\,V}{390\,V} \approx 0.015 \quad (53)$$

The value of R_Z is calculated as shown in Equation 54:

$$R_Z = \frac{100\,mV}{V_{RIPPLE} \times H \times g_m} = \frac{100\,mV}{14\,V \times 0.015 \times 50\,\mu S} = 9.52\ k\Omega \quad (54)$$

C_Z is then set to add 45° phase margin at 1/5th of the line frequency, as shown in Equation 55:

$$C_Z = \frac{1}{2\pi \times \frac{f_{LINE}}{5} \times R_Z} = \frac{1}{2\pi \times \frac{47\,Hz}{5} \times 9.52\,k\Omega} = 1.78\,\mu F \quad (55)$$

C_P is sized to attenuate high-frequency switching noise, as shown in Equation 56:

$$C_p = \frac{1}{2\pi \times \frac{f_{MIN}}{2} \times R_Z} = \frac{1}{2\pi \times \frac{45\,kHz}{2} \times 9.52\,k\Omega} = 770\,pF \quad (56)$$

Standard values should be chosen for R_Z, C_Z and C_P, as shown in Equation 57 to Equation 59.

$$R_Z = 9.53\,k\Omega \quad (57)$$

$$C_Z = 2.2\,\mu F \quad (58)$$

$$C_P = 820\,pF \quad (59)$$

ADVANCE INFORMATION

9.2.3 Application Curves

9.2.3.1 Input Ripple Current Cancellation with Natural Interleaving

Figure 14 through Figure 16 show the input current (M1= IL1 + IL2), Inductor Ripple Currents (IL1, IL2) versus rectified line voltage. From these graphs, it can be observed that natural interleaving reduces the overall magnitude of input (and output) ripple current caused by the individual inductor current ripples.

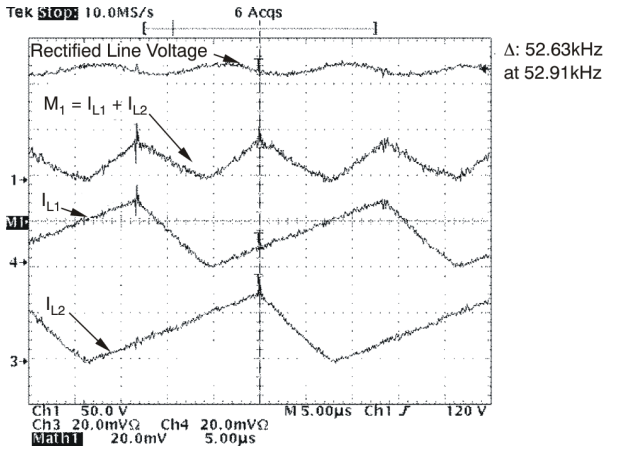


Figure 14. Inductor and Input Ripple Current at 85 V_{RMS} at Peak of Line Voltage

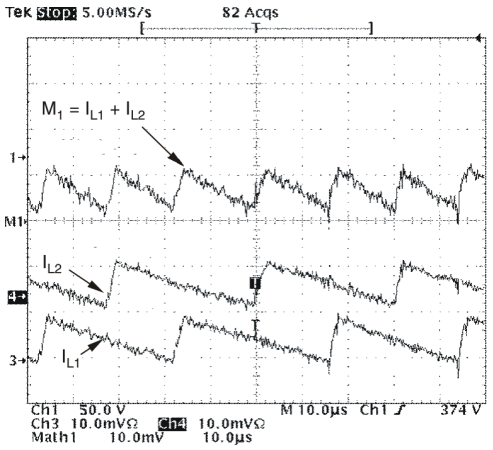


Figure 15. Inductor and Input Ripple Current at 265 V_{RMS} Input at Peak Line Voltage

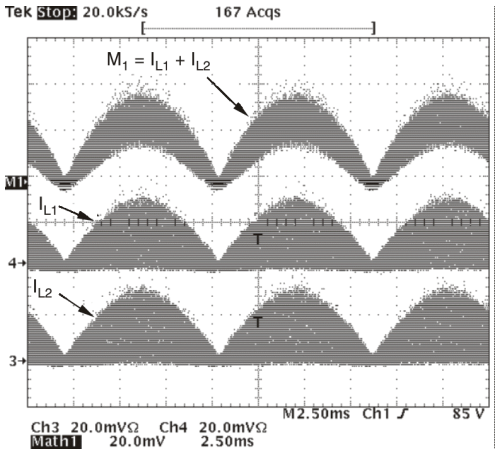


Figure 16. Inductor and Input Ripple Current at V_{IN} = 85 V_{RMS}, P_{OUT} = 300 W

ADVANCE INFORMATION

9.2.3.2 Brownout Protection

The UCC28064 has a brownout protection that shuts down both gate drives (GDA and GDB) when the VINAC pin detects that the RMS input voltage is too low. Figure 17.

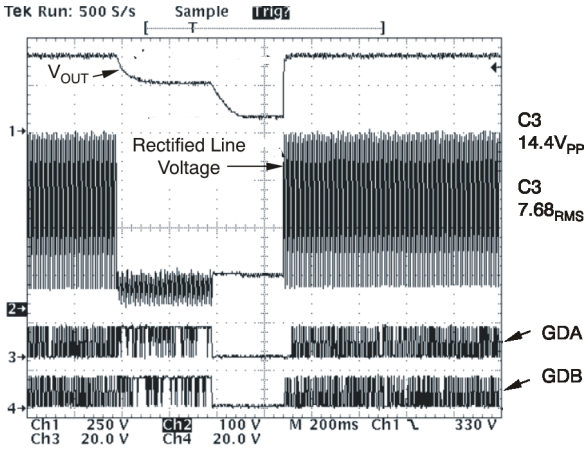


Figure 17. UCC28064 Response to a Line Brownout Event at 265 V_{RMS}

10 Power Supply Recommendations

The device receives all of its power through the VCC pin. This voltage should be as well regulated as possible through all of the operating conditions of the PFC stage. Consider creating the steady state bias for this stage from a downstream DC:DC stage which will in general be able to provide a bias winding with very well regulated voltage. This strategy will enhance the overall efficiency of the bias generation. A lower efficiency alternative will be to consider a series-connected fixed positive-voltage regulator such as the UA78L15A.

For all normal and abnormal operating conditions it is critically important that VCC remains within the recommended operating range for both Voltage and Input Current. VCC overvoltage may cause excessive power dissipation in the internal voltage clamp and undervoltage may cause inadequate drive levels for power MOSFETs, UVLO events (causing interrupted PFC operation) or inadequate headroom for the various on-chip linear regulators and references.

Note also that the high RMS and peak currents required for the MOSFET gate drives are provided through the device 13.5-V linear regulator, which does not have provision for the addition of external decoupling capacitance. For higher Powers, very high Q_G power MOSFETs or high switching frequencies, consider using external driver transistors, local to the power MOSFETs. These will reduce the device operating temperature and ensure that the VCC maximum input current rating is not exceeded.

Use decoupling capacitances between VREF and AGND and between VCC and PGND which are as local as possible to the device. These should have some ceramic capacitance which will provide very low ESR. PGND and AGND should ideally be star connected at the control device so that there is negligible DC or high frequency AC voltage difference between PGND and AGND. Use values for decoupling capacitors similar to or a little larger than those used in the EVM.

Pay close attention to start-up and shutdown VCC bias bootstrap arrangements so that these provide adequate regulated bias power as early as possible during power application and as late as possible during power removal. Ensure that these start-up bias bootstrap circuits do not cause unnecessary steady-state power drain.

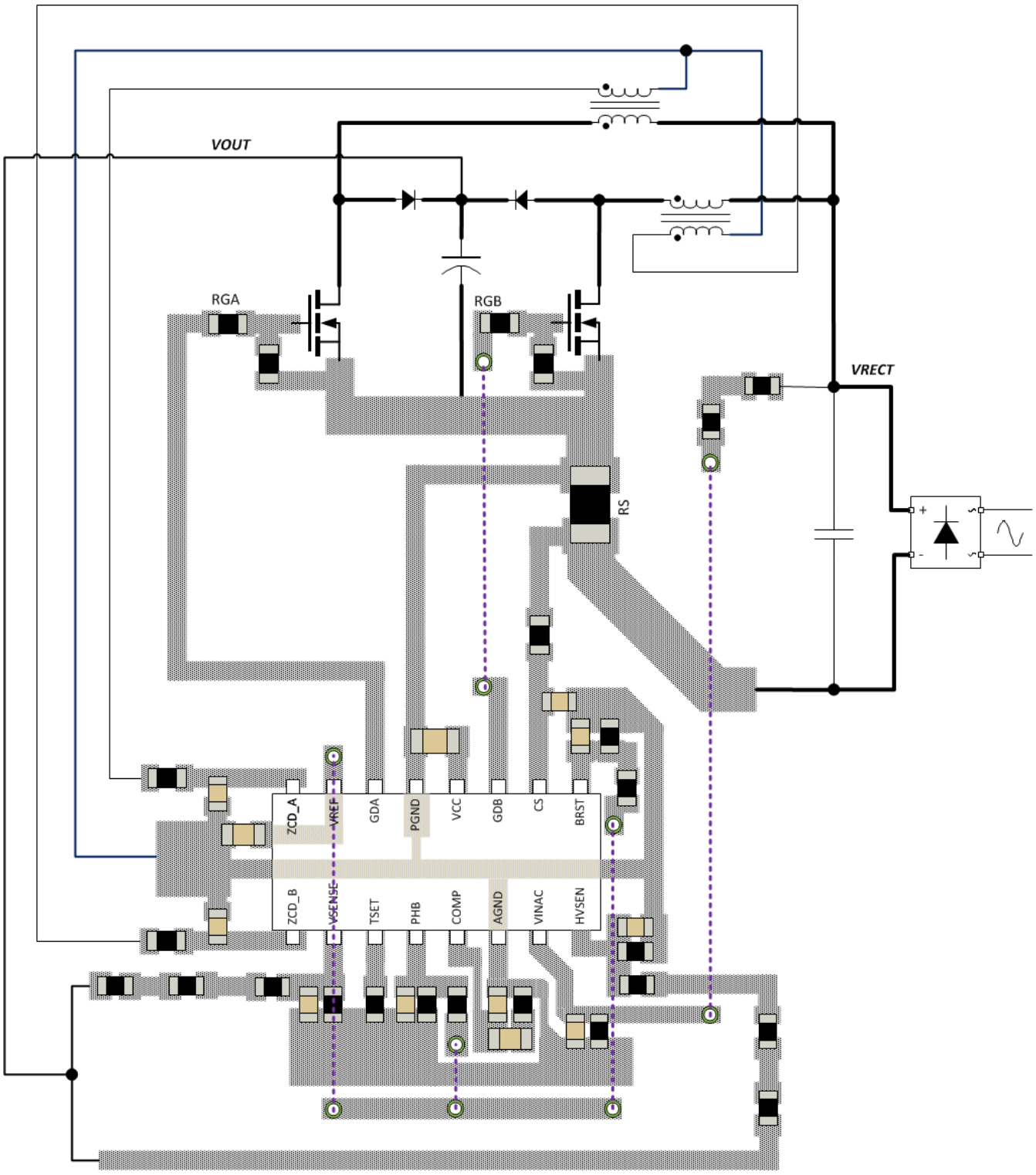
ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

Interleaved transition-mode PFC system architecture dramatically reduces input and output ripple current, allowing the circuit to use smaller and less expensive filters. To maximize the benefits of interleaving, the input and output filter capacitors should be located after the two phase currents are combined together. Similar to other power management devices, when laying out the printed circuit board (PCB) it is important to use star grounding techniques and keep filter capacitors as close to device ground as possible. To minimize the interference caused by capacitive coupling from the boost inductor, the device should be located at least 1 in (25.4 mm) away from the boost inductor. It is also recommended that the device not be placed underneath magnetic elements. Because of the precise timing requirement, timing-setting resistor R_T should be placed as close as possible to the TSET pin and returned to the analog ground pin with the shortest possible path. Figure 18 shows a recommended component placement and layout.

11.2 Layout Example



Dotted line could be or a wire mounted on the top of the board or Top layer traces, assuming device and other traces are in the bottom layer.

Figure 18. Recommended PCB Layout

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCC28064 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.1.2 Device Nomenclature

12.1.2.1 Detailed Pin Description

Analog Ground Connect analog signal bypass capacitors, compensation components, and analog signal returns to this pin. Connect the analog and power grounds at a single point to isolate high-current noise signals of the power components from interference with the low-current analog circuits.

Error Amplifier Output The error amplifier is a transconductance amplifier, so this output is a high-impedance current source. Connect voltage-regulation loop-compensation components from this pin to AGND. The on-time seen at the gate-drive outputs is proportional to the voltage at this pin minus an offset of approximately 125 mV. During normal operation, the error amplifier maintains a transconductance of 55 μS for small-signal disturbances on VSENSE, and shifts to ~290 μS when VSENSE deviates more than ±5% from VSENSEreg. During an AC-line Dropout condition, the error amplifier output is disabled and an internal 4-μA source discharges COMP for the duration of the Dropout condition. During a VSENSE-based OV event, an internal 2-kΩ resistor is applied from COMP to GND until the OV condition clears. During soft-start triggering events (UVLO, Disable, Brownout, HVSEN overvoltage, or Thermal Shutdown), the error-amp output is disabled and COMP is pulled low by an internal 2-kΩ resistor. The soft-start condition begins only after the triggering event clears and COMP has been discharged below 20 mV, ensuring that the circuit restarts with a low COMP voltage and a short on-time. (Do not connect COMP to a low-impedance source that would interfere with COMP falling below 20 mV.) During Soft-Start, the error amplifier high transconductance is enabled and COMP current is -125 μA as long as VSENSE < VREF/2. Once VSENSE exceeds VREF/2, the high gain is disabled and only the small-signal gain capability is available with a maximum COMP current of approximately –16 μA. Normal operation resumes once VSENSE > 0.983VREF (~5.9 V).

Current Sense Input Connect the current-sense resistor and the negative terminal of the diode bridge to this pin. Connect the return of the current sense resistor to the AGND pin with a separate trace. As input current increases, the voltage on CS will go more negative. This cycle-by-cycle overcurrent protection limits input current by turning off both gate driver outputs (GDx) when CS is more negative than the CS rising threshold (approximately -200 mV in two-phase operation and approximately -167 mV in single-phase and phase-fail condition). The gate drive outputs will remain low until CS falls to the CS falling threshold (approximately –15 mV). Current sense is blanked for approximately 100 ns following the rising and falling edge of either GDx output. This filters noise that may occur from gate-drive current or when inductor current switches from a power FET to a boost diode. In most cases, no additional current sense filtering is required. If external filtering is

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deemed necessary, or to prevent excessive negative voltage on the CS pin during AC-inrush conditions, a series resistor is recommended to connect the current sensing resistor to the CS pin. Due to the CS bias current, this external resistor should be less than 100 Ω to maintain accuracy.

Channel A and Channel B Gate Drive Output Connect these pins to the gate of the power FET for each phase through the shortest connection practicable. If it is necessary to use a trace longer than 0.5 inch (12.6 mm) for this connection, some ringing may occur due to trace series inductance. This ringing can be damped by adding a low-value resistor in series with GDA and GDB.

High Voltage Output Sense The UCC28064 incorporates FailSafe OVP so that any single failure does not allow the output to boost above safe levels. Output overvoltage is monitored by both VSENSE and HVSEN but their actions are different if either pin exceeds their respective overvoltage thresholds. Using two pins to monitor for overvoltage provides redundant protection and fault tolerance. When HVSEN exceeds its overvoltage threshold, it triggers a full soft-start of the controller. HVSEN can also be used to enable a downstream power converter when the voltage on HVSEN is within the operating region. When HVSEN is greater than 2.5 V, the PWMCNTL output may be driven Low (provided no other fault exists). When HVSEN falls below 2.5 V, the PWMCNTL output becomes high-impedance. Select the HVSEN divider ratio for the desired overvoltage and power-good thresholds. Select the HVSEN divider impedance for the desired power-good hysteresis based on the hysteresis current. During operation, HVSEN must never fall below 0.8 V. Dropping HVSEN below 0.8 V puts the UCC28064 into a special test mode, used only for factory testing. A bypass capacitor from HVSEN to AGND is recommended to filter noise and avoid false overvoltage shutdown.

Phase-B Enable/Disable When the voltage applied to this pin is below the Phase-B enable threshold, Phase B of the boost converter and the Phase Fail detector are disabled. The commanded on-time for Phase A is immediately doubled when Phase B is disabled, which helps keep COMP voltage constant during the phase-management transient. The PHB pin allows the user to add external phase-management control circuitry, if desired. To disable phase-management, connect the PHB pin to the VREF pin.

PWM-Control Output This open-drain output goes low when HVSEN is within the HVSEN-good region (HVSEN > 2.5 V), there is no FailSafe OV, and there is no Phase-Fail condition when operating in two-phase mode (see PHB pin). Otherwise, PWMCNTL is high-impedance.

Timing Set PWM on-time programming input. Connect a resistor from TSET to AGND to set the on-time versus COMP voltage and the minimum switching period at the gate-drive outputs.

Bias Supply Input Connect this pin to a controlled bias supply of between 14 V and 21 V. Also connect a 0.1-μF or larger ceramic bypass capacitor from this pin to PGND with the shortest possible board trace. This bias supply powers all circuits within the device and must be capable of delivering the steady-state dc current plus the transient power-MOSFET gate-charging current. Input bias current is very low during undervoltage-lockout (UVLO) or stand-by conditions (VSENSE < 1.25 V).

Input AC Voltage Sense For normal operation, connect this pin to a voltage divider across the rectified input power mains. When the voltage on VINAC remains below the brownout threshold for longer than the brownout filter time, the device enters a brownout mode, both output drivers are disabled and a full soft-start is triggered. Select the input voltage divider ratio for the desired brownout threshold. Select the divider impedance for the desired brownout hysteresis based on the hysteresis current. A dropout condition is triggered when VINAC remains below the dropout threshold for longer than the dropout filter time. The error amplifier is disabled and an internal 4-μA current source discharges COMP for the duration of the dropout condition. The dropout condition is immediately cleared and normal operation resumes when VINAC exceeds the dropout-clear threshold.

Voltage Reference Output Connect a 0.1-μF or larger ceramic bypass capacitor from this pin to AGND. VREF turns off during UVLO and VSENSE-disable to save bias current and increase stand-by efficiency. This reference output can be used to bias other circuits requiring less than a few milliamperes of non-pulsing total supply current.

Output DC Voltage Sense Connect this pin to a voltage divider across the output of the power converter. In a closed-loop system, the voltage at VSENSE is regulated to the error amplifier reference voltage. Select the output voltage divider ratio for the desired output voltage. Connect the ground side of

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this divider to analog ground (AGND) through a separate short trace for best output regulation accuracy and noise immunity. Controller operation may be enabled when VSENSE voltage exceeds the 1.25-V enable threshold. VSENSE can be pulled low by an open-drain logic output, or >6-V logic output in series with a low-leakage diode, to disable the outputs and reduce VCC current. Two levels of output overvoltage are detected at this input. If VSENSE exceeds the first-level overvoltage protection threshold V_{LOW_OV}, an internal 2-kΩ resistor is applied to COMP to quickly reduce gate-drive on-time. If VSENSE continues to rise past the second-level threshold V_{HIGH_OV}, GDA and GDB are immediately latched off. This latch is cleared when VSENSE falls below the OV-clear threshold. If VSENSE becomes disconnected, open-loop protection provides an internal current source to pull VSENSE low, which disables the controller and triggers a soft-start condition.

Zero Current Detection Inputs These inputs are used to detect a negative-going edge when the boost inductor current in each respective phase goes to zero. The inputs are clamped between 0 V and 3 V. Connect each pin through a current limiting resistor to the zero-crossing detection (ZCD) winding of the corresponding boost inductor. The resistor value should be chosen to limit the clamping currents to less than ±3 mA. The inductor winding polarity must be arranged so that this ZCD voltage falls when the inductor current decays to zero. When the inductor current falls to zero, the ZCD input must drop below the falling threshold (approximately 1 V) to cause the gate drive output to rise. Subsequently, when the power-MOSFET turns off, the ZCD input must rise above the rising threshold (approximately 1.7 V) to arm the logic for another falling ZCD edge.

ADVANCE INFORMATION

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *UCC28063EVM 300W Interleaved PFC Pre-regulator*
- *UCC38050 100-W Critical Conduction Power Factor Corrected (PFC) Pre-regulator*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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12.5 Trademarks

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PUCC28064D	ACTIVE	SOIC	D	16	40	TBD	Call TI	Call TI	-40 to 125		Samples
UCC28064DR	PREVIEW	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 125		
UCC28064DT	PREVIEW	SOIC	D	16	250	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

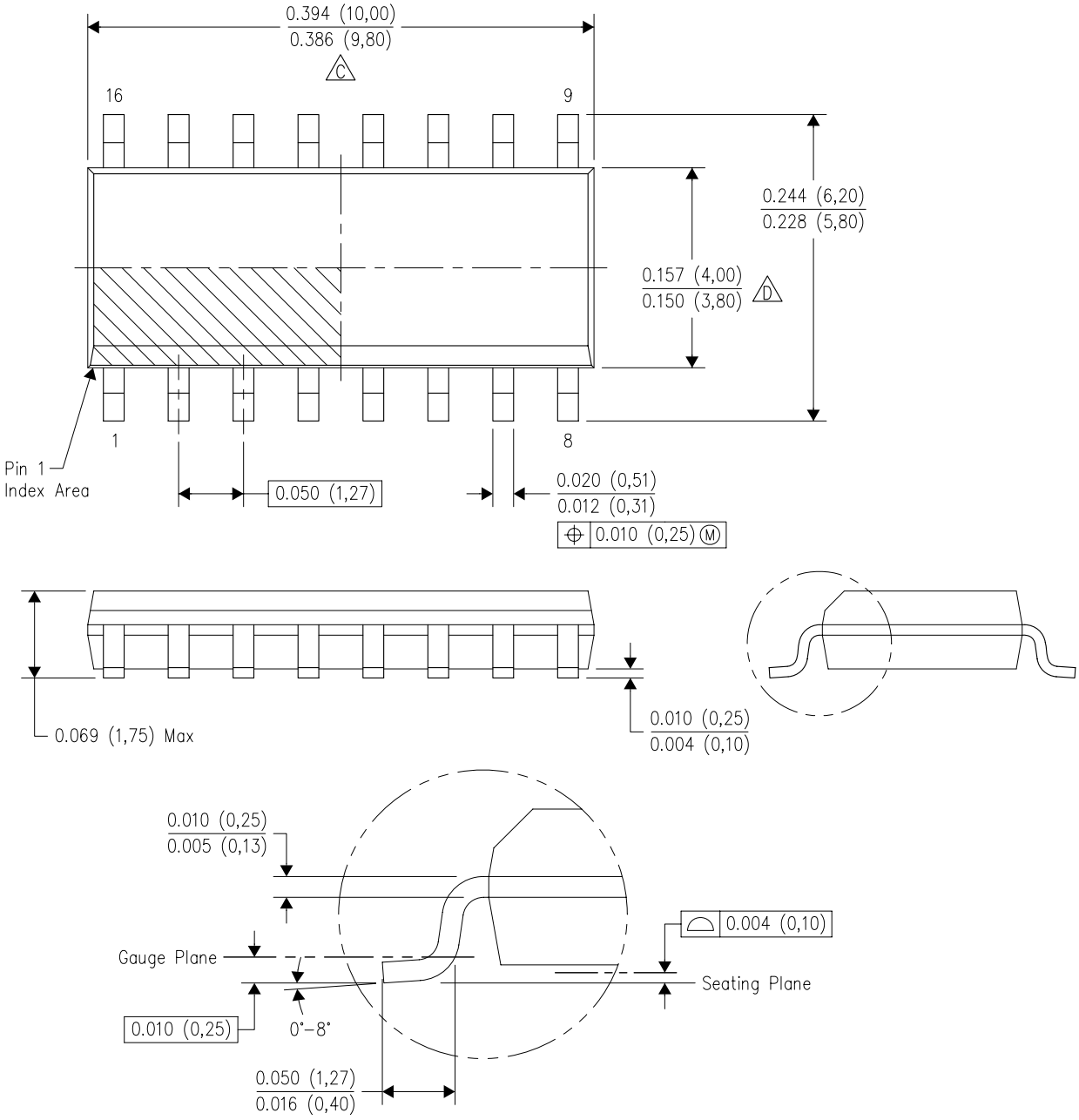
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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