SONY

CXD2304R

8-bit 20 MSPS RGB 3-Channel D/A Converter

Description

The CXD2304R is an 8-bit high-speed D/A converter for video band use. It has an input/output equivalent to 3 channels of R, G and B. It is suitable for use of digital TV, graphic display, and others.

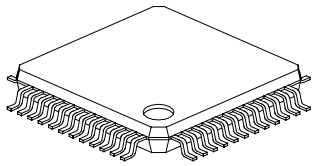
Features

- Resolution 8-bit
- Maximum conversion speed 20 MSPS
- RGB 3-channel input/output
- Differential linearity error ±0.5 LSB
- Low power consumption 50 mW
  (330 Ω load at 1.2 Vp-p output)
- Single 3.3 V power supply
- Low glitch noise
- Stand-by function

Structure

Silicon gate CMOS IC

48 pin LQFP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	AV_{DD}, DV_{DD}	7	V
• Input voltage (All pins)	V_{IN}	V_{DD}+0.5 to V_{SS}–0.5	V
• Output current (Every each channel)	I_{OUT}	0 to 15	mA
• Storage temperature	Tstg	–55 to +150	°C

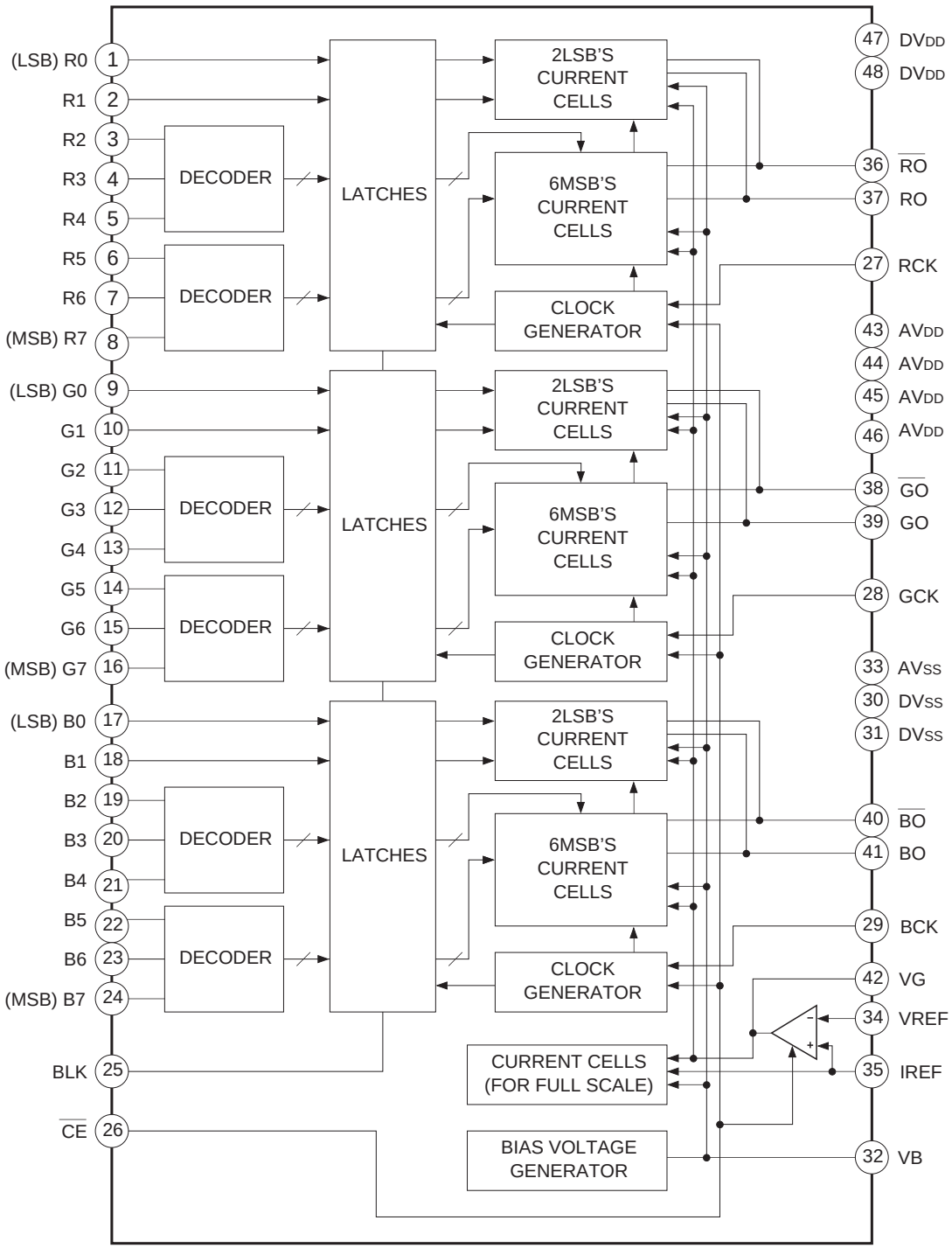
Recommended Operating Conditions

• Supply voltage	AV_{DD}, AV_{SS}	3.0 to 3.6	V
	DV_{DD}, DV_{SS}	3.0 to 3.6	V
• Reference input voltage	V_{REF}	1.2	V
• Clock pulse width	T_{PW1}, T_{PW0}	22.5 ns (min.) to 1.1 µs (max.)	
• Operating temperature	Topr	–40 to +85	°C

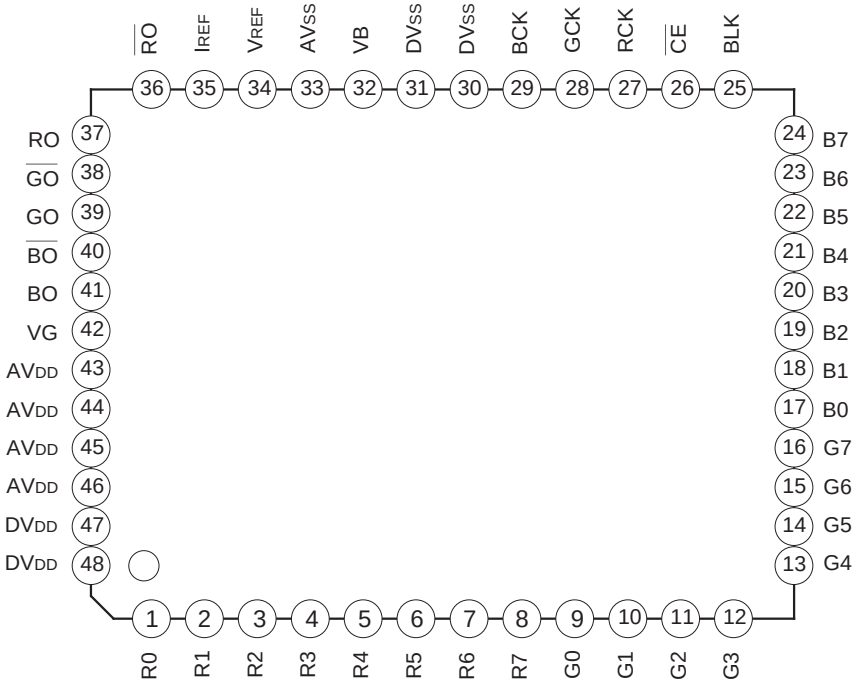
Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

E94307B01

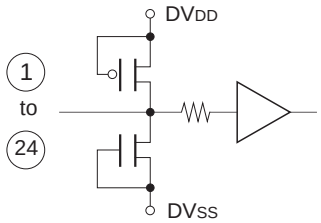
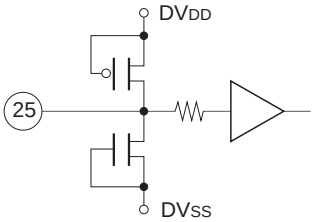
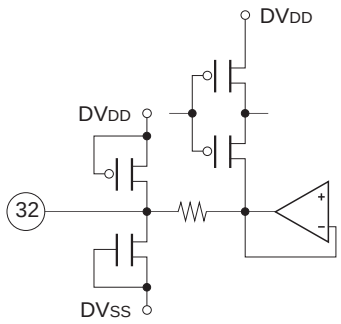
Block Diagram

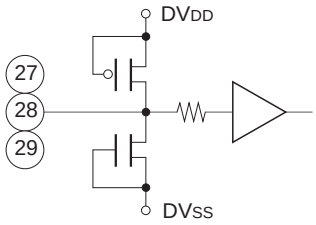
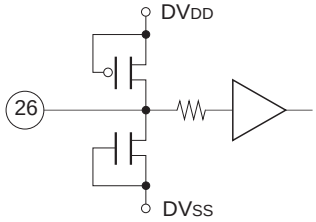
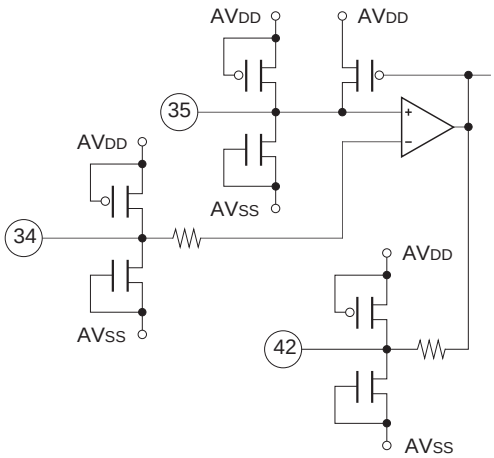


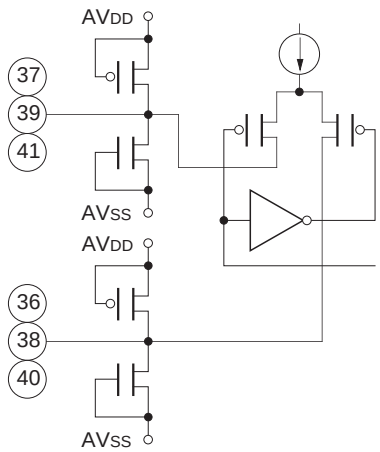
Pin Configuration



Pin Description and I/O Pins Equivalent Circuit

Pin No.	Symbol	I/O	Equivalent circuit	Description
1 to 8	R0 to R7	I		Digital input R0 (LSB) to R7 (MSB) G0 (LSB) to G7 (MSB) B0 (LSB) to B7 (MSB)
9 to 16	G0 to G7			
17 to 24	B0 to B7			
25	BLK	I		Blanking input. This is synchronized with the clock input signal for each channel. No signal at “H” (Output 0 V). Output condition at “L”.
32	VB	$\overline{O}$		Connect a capacitor of about 0.1 µF.

Pin No.	Symbol	I/O	Equivalent circuit	Description
27 28 29	RCK GCK BCK	I		Clock input.
30, 31	DVSS	—		Digital GND
33	AVSS	—		Analog GND
26	$\overline{CE}$	I		Chip enable input. This is not synchronized with the clock input signal. No signal (Output 0 V) at "H" and minimizes power consumption.
35	IREF	$\overline{O}$		Reference current output. Connect a resistance 16 times "RIR" that of output resistance value "ROUT".
34	VREF	I		Reference voltage output. Set full scale output value.
42	VG	$\overline{O}$		Connect a capacitor of about 0.1 µF.
43 to 46	AVDD	—		Analog VDD

Pin No.	Symbol	I/O	Equivalent circuit	Description
37	RO	O		Current output. Voltage output can be obtained by connecting a resistance.
39	GO			
41	BO			
36	$\overline{RO}$			Inverted current output. Normally dropped to analog GND.
38	$\overline{GO}$			
40	$\overline{BO}$			
47, 48	DV_{DD}	—		Digital V_{DD}

Electrical Characteristics (F_{CLK}=20 MHz, AV_{DD}=DV_{DD}=3.3 V, R_{OUT}=330 Ω, V_{REF}=1.2 V, R_{IR}=5.1 kΩ, Ta=25 °C)

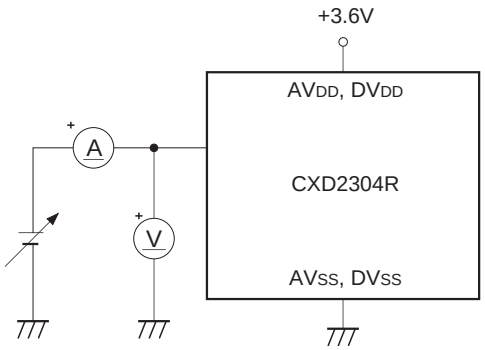
Item	Symbol	Measurement conditions		Min.	Typ.	Max.	Unit
Resolution	n				8		bit
Conversion speed	F_{CLK}	AV_{DD}=DV_{DD}=3.0 to 3.6 V Ta=–40 to 85 °C		0.5		20	MSPS
Integral non-linearity error	E_L	Endpoint		–2.5		2.5	LSB
Differential non-linearity error	E_D			–0.5		0.5	LSB
Output full-scale voltage	V_{FS}			1.12	1.24	1.36	V
Output full-scale ratio *1	F_{SR}			0	1.5	3.0	%
Output full-scale current	I_{FS}				3.8		mA
Output offset voltage	V_{OS}	When “00000000” data input				1	mV
Glitch energy	GE				150		pV•s
Crosstalk	CT	When 1 kHz sine wave input			53		dB
Supply current	I_{DD}	When 14.3 MHz color bar data input	$\overline{CE}$= “L”		15	18	mA
	I_{STB}		$\overline{CE}$= “H”			1.2	
Analog input resistance	R_{IN}	VREF		1			MΩ
Input capacitance	C_I					9	pF
Digital input voltage	V_{IH}	AV_{DD}=DV_{DD}=3.0 to 3.6 V Ta=–20 to +75 °C		2.5			V
	V_{IL}					0.5	
Digital input current	I_{IH}	AV_{DD}=DV_{DD}=3.0 to 3.6 V Ta=–20 to +75 °C		–5		5	µA
	I_{IL}						
Setup time	ts			7			ns
Hold time	th			3			ns
Propagation delay time	t_{PD}				20		ns
$\overline{CE}$ enable time *2	t_E	$\overline{CE}$=H→L			4	8	ms
$\overline{CE}$ disable time *2	t_D	$\overline{CE}$=L→H			4	8	ms

*1 Full-scale output ratio = $\left| \frac{\text{Full-scale voltage of channel}}{\text{Average of the full-scale voltage of the channels}} - 1 \right| \times 100\ (\%)$

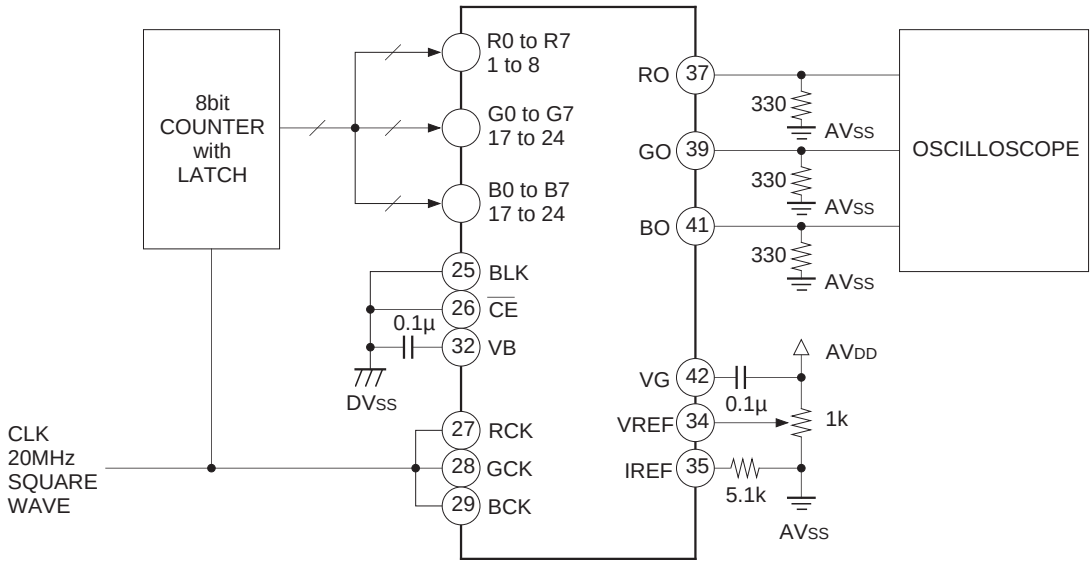
*2 When the external capacitors for the VG pins are 0.1 µF.

Electrical Characteristics Measurement Circuit

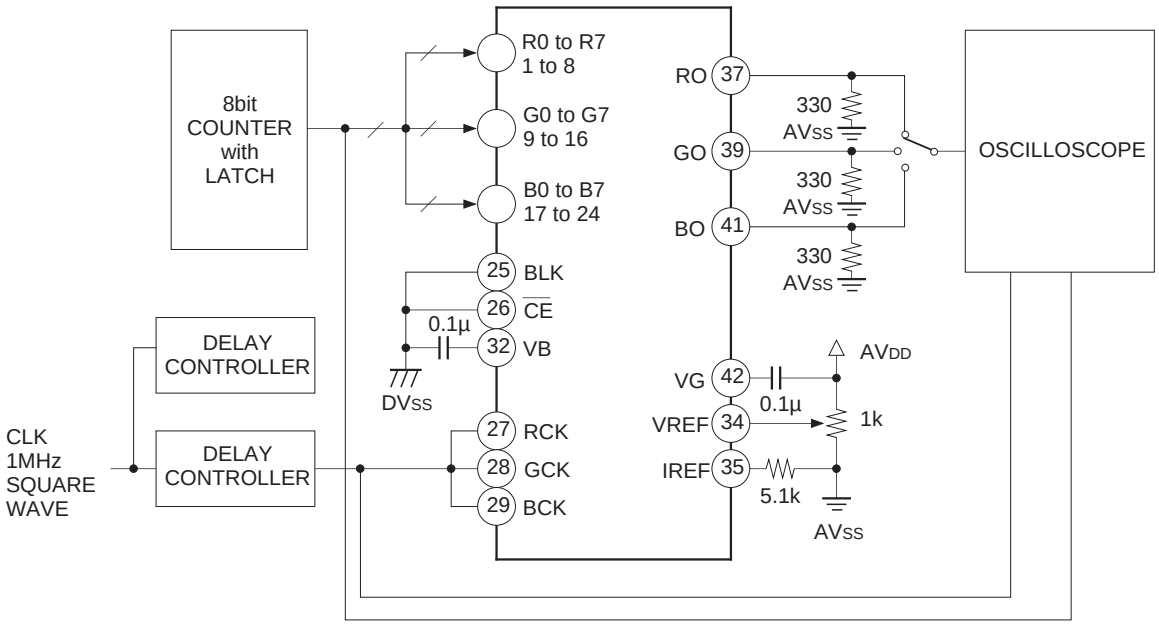
Analog Input Resistance
Digital Input Current } **Measurement Circuit**



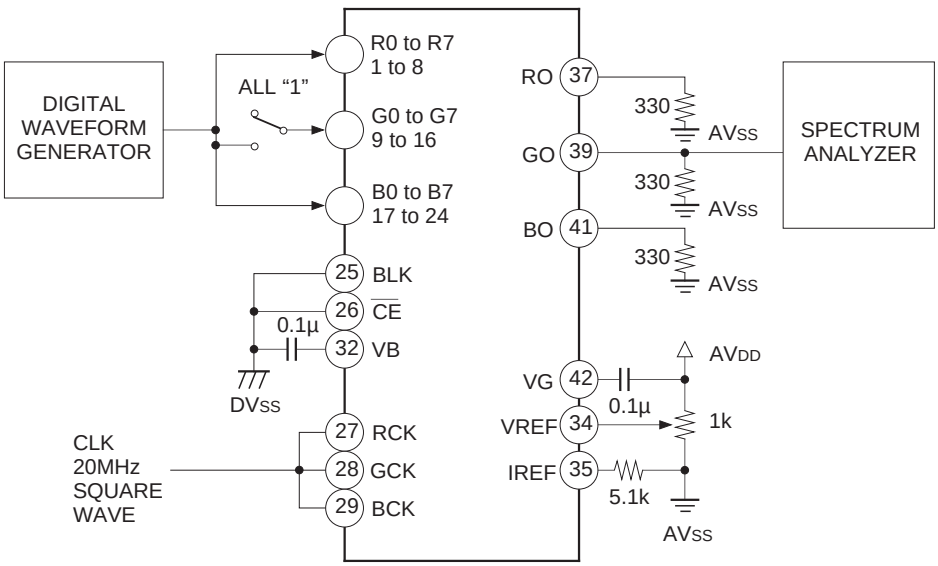
Maximum Conversion Velocity Measurement Circuit



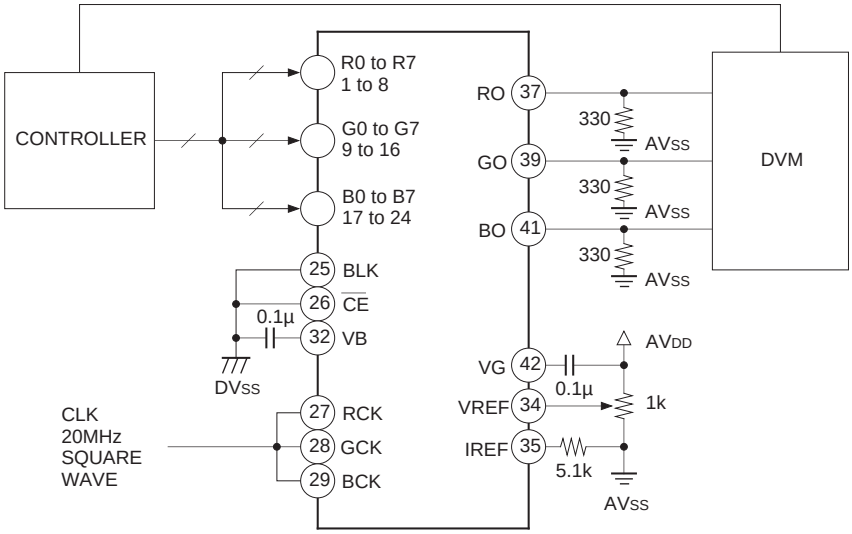
Setup Time
Hold Time } **Measurement Circuit**
Glitch Energy



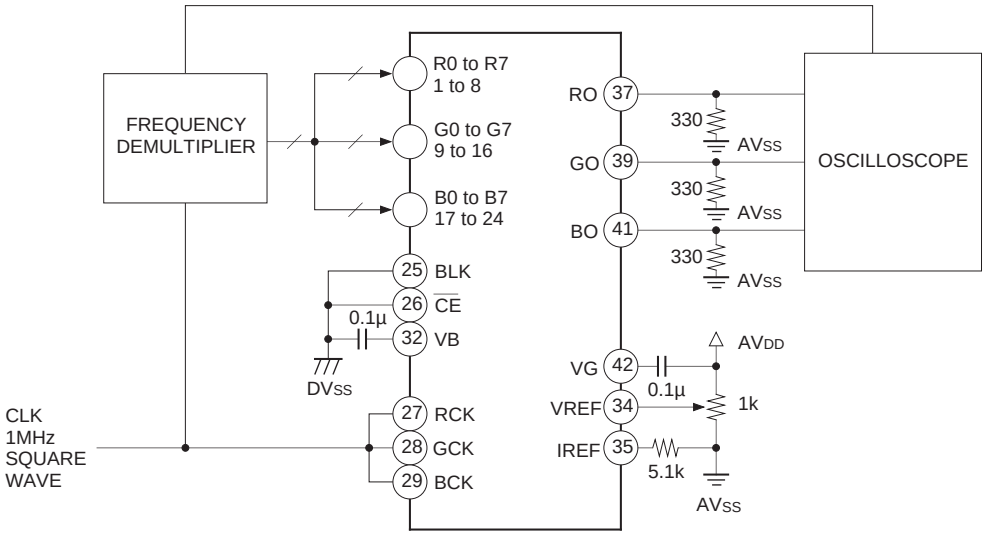
Crosstalk Measurement Circuit



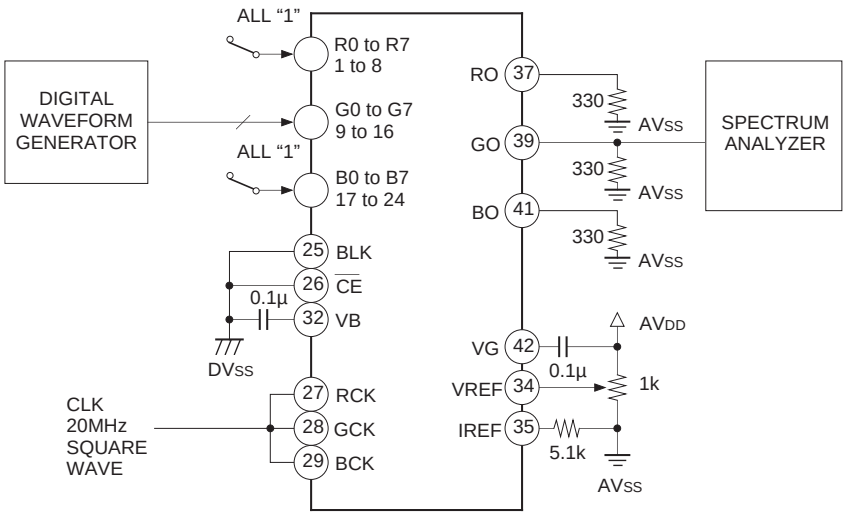
DC Characteristics Measurement Circuit



Propagation Delay Time Measurement Circuit



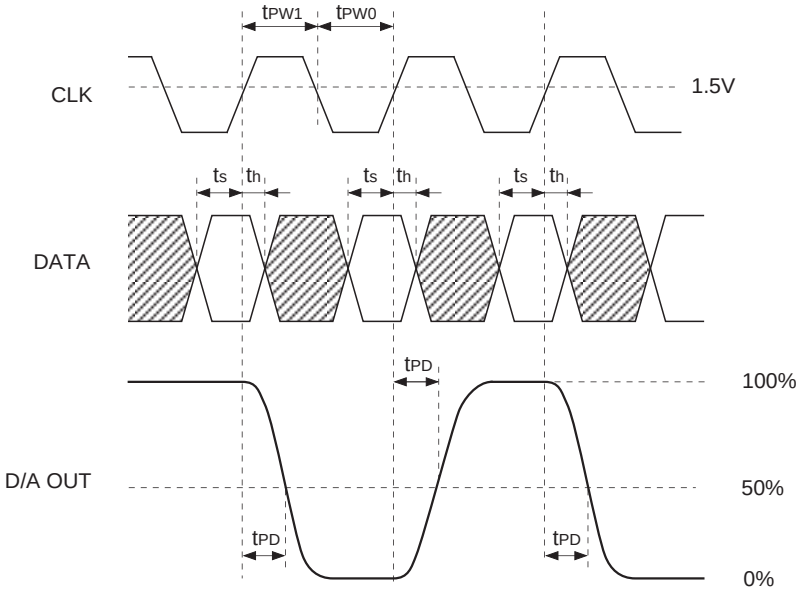
SNR Measurement Circuit



SNR : Different between primary component and secondary distortion

Description of Operation

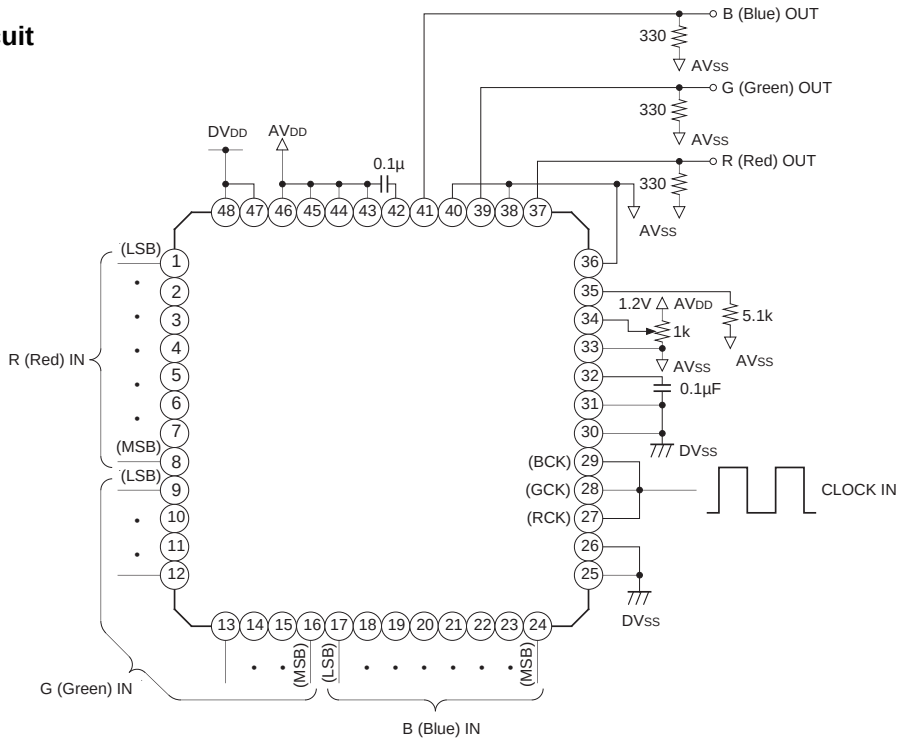
Timing Chart



I/O Chart (when full scale output voltage at 1.2 V)

Input code	Output voltage
MSB LSB	
1 1 1 1 1 1 1 1	1.2 V
:	
1 0 0 0 0 0 0 0	0.6 V
:	
0 0 0 0 0 0 0 0	0 V

Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

- How to select the output resistance

The CXD2304R is a D/A converter of the current output type. To obtain the output voltage connect the resistance to the current output pins R0, G0 and B0. For specifications we have;

Output full scale voltage V_{FS}=1.12 to 1.36 [V]

Output full scale current I_{FS}=3.8 [mA] (typ.)

Calculate the output resistance value from the relation of $V_{FS}=I_{FS} \times R_{OUT}$. Also, 16 times resistance of the output resistance R_{OUT} is connected to reference current pin IREF. In some cases, however, this turns out to be a value that does not actually exist. In such a case a value close to it can be used as a substitute.

Here please note that V_{FS} becomes

$$V_{FS}=V_{REF} \times 16R_{OUT}/R_{IR}.$$

V_{REF} is the voltage set at the reference voltage pin VREF and R_{OUT} is the resistance connected to the current output pins RO, GO and BO while R_{IR} is connected to IREF pin.

Increasing the resistance value can curb power consumption. On the other hand glitch energy and data settling time will inversely increase. Set the most suitable value according to the desired application.

- Phase relation between data and clock

To obtain the expected performance as a D/A converter, it is necessary to set properly the phase relation between data and clock applied from the exterior. Be sure to satisfy the provisions of the setup time (t_S) and hold time (t_H) as stipulated in the Electrical Characteristics.

- Power supply and ground

To reduce noise effects separate analog and digital systems in the device periphery. For power supply pins, both digital and analog, bypass respective grounds by using a ceramic capacitor of about 0.1 µF, as close as possible to the pin.

- Latch up

Digital power supply and analog power supply have to be common at the PCB power supply source. This is to prevent latch up due to voltage difference between AV_{DD} and DV_{DD} pins when power supply is turned ON.

- $\overline{RO}$, $\overline{GO}$ and $\overline{BO}$ pins

The $\overline{RO}$, $\overline{GO}$ and $\overline{BO}$ pins are the inverted current output pins described in the Pin Description. The sums shown below become the constant value for any input data.

a) The sum of the currents output form RO and $\overline{RO}$
b) The sum of the currents output form GO and $\overline{GO}$
c) The sum of the currents output form BO and $\overline{BO}$

However, the performances such as the linearity error of the inverted current output pin output current is not guaranteed.

- Output full-scale voltage

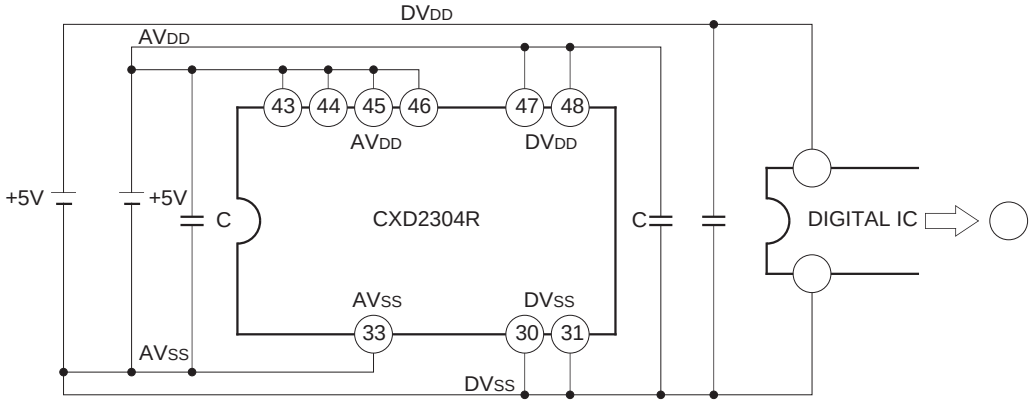
For the applications using the RGB signal, the color balance may be broken up when the no-adjusted output full-scale voltage is used.

Latch Up Prevention

The CXD2304R is a CMOS IC which required latch up precautions. Latch up is mainly generated by the lag in the voltage rising time of AV_{DD} (Pins 43 to 46) and DV_{DD} (Pins 47 and 48), when power supply is ON.

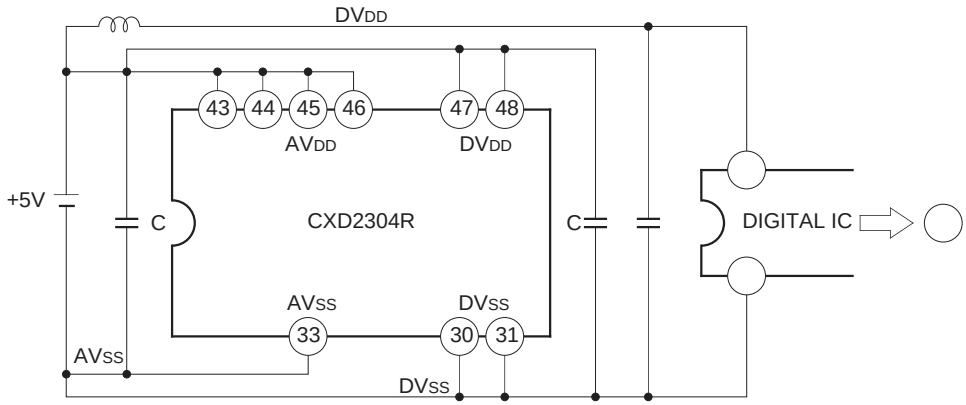
1. Correct usage

a. When analog and digital supplies are from different sources

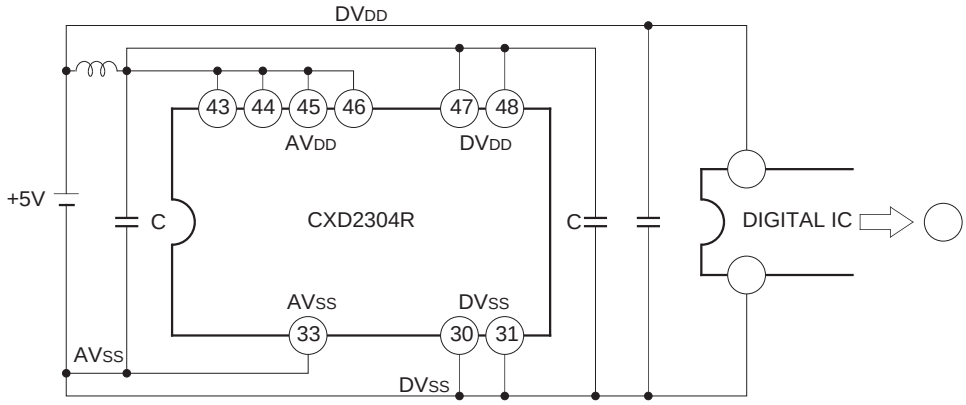


b. When analog and digital supplies are from a common source

(i)

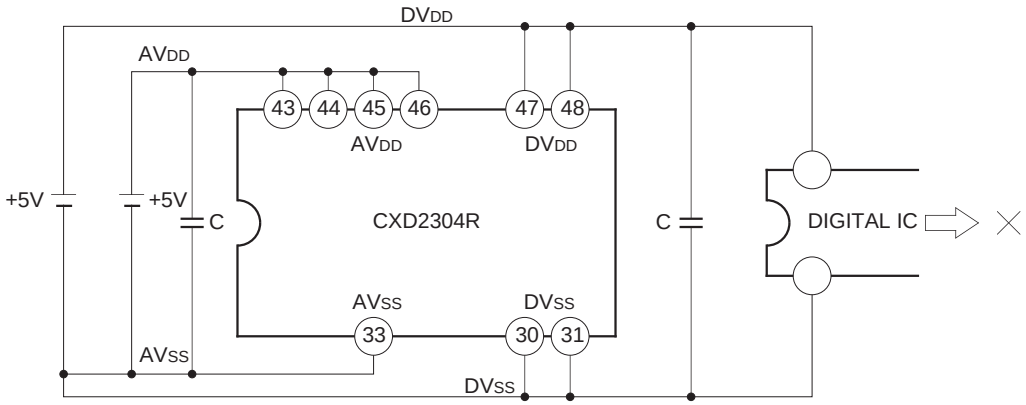


(ii)



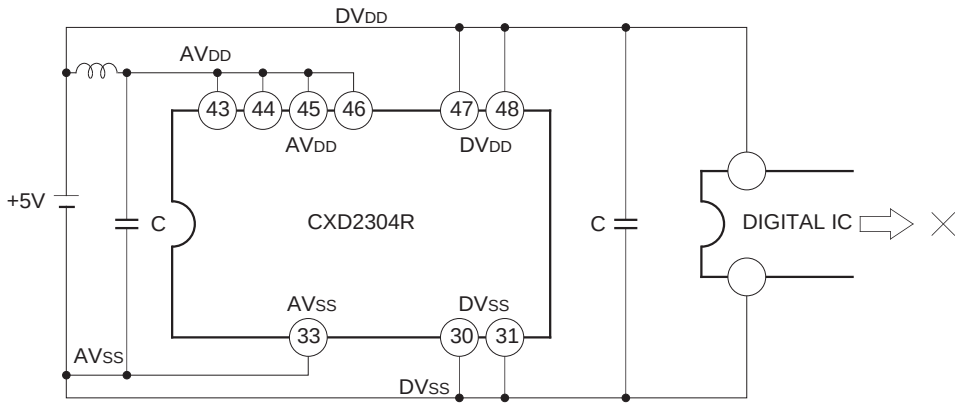
2. Example when latch up easily occurs

a. When analog and digital supplies are from different sources

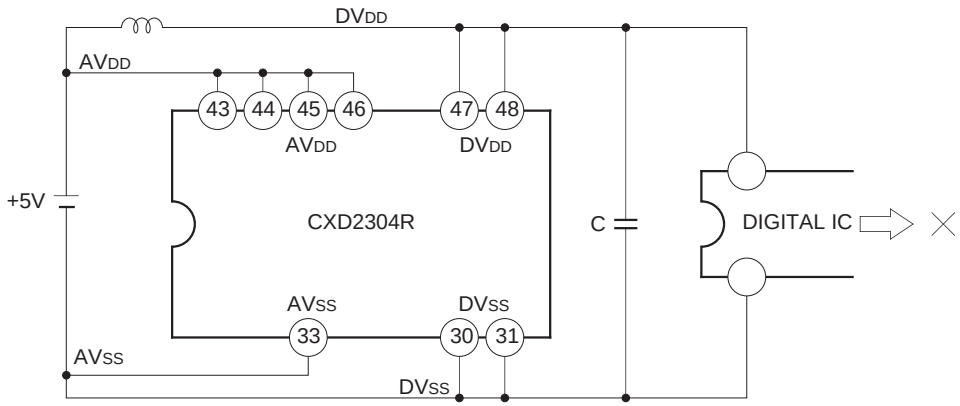


b. When analog and digital supplies are from common source

(i)



(ii)



Example of Representative Characteristics

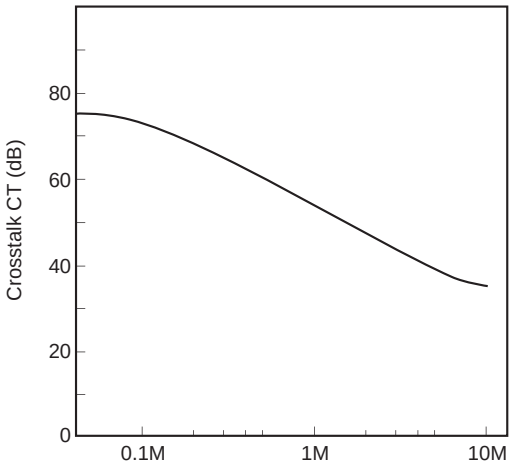


Fig. 1. Crosstalk

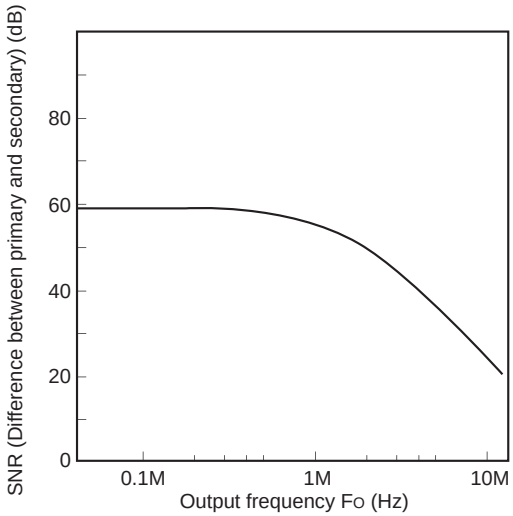


Fig. 2. SNR (Difference between primary component and secondary distortion)

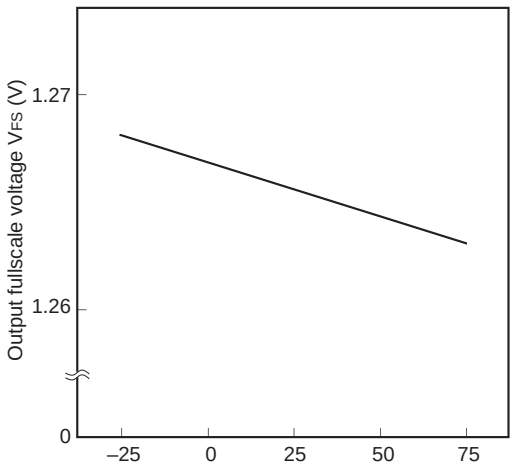


Fig. 3. Ambient temperature vs. Output full scale voltage

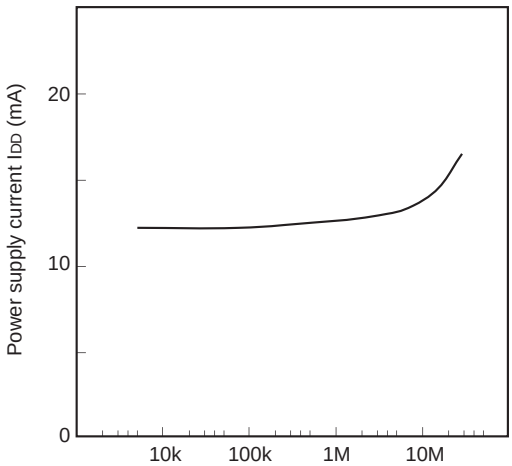


Fig. 4. Output frequency vs. Power supply current

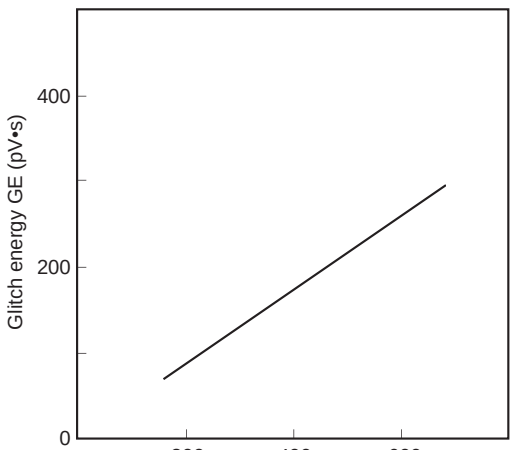


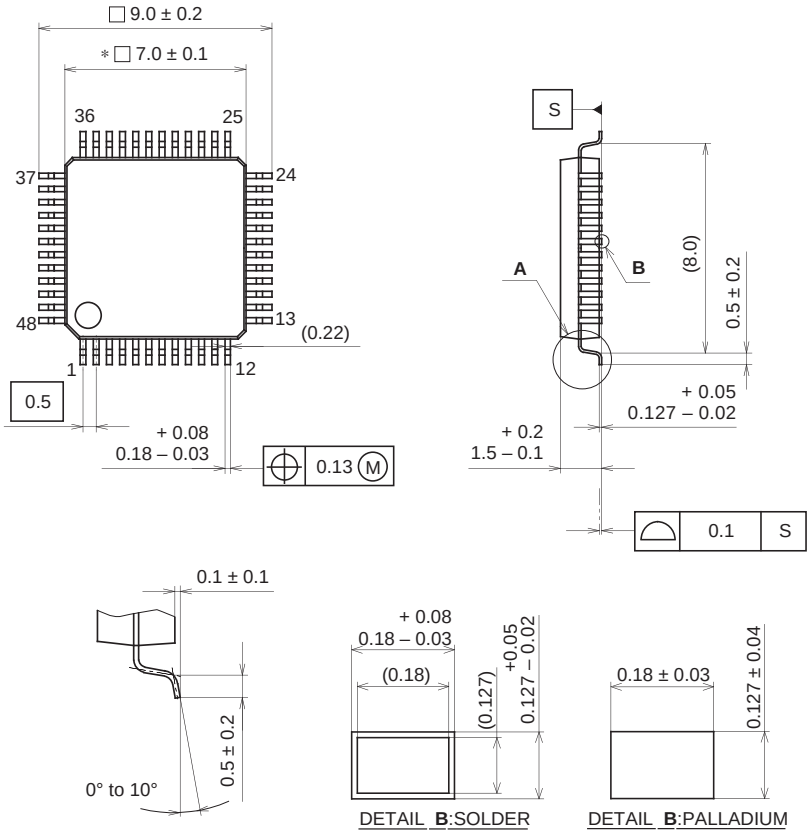
Fig. 5. Output resistance vs. Glitch energy

Reference measurement condition and description

- AV_{DD}=3.3 V
- DV_{DD}=3.3 V
- V_{REF}=1.2 V
- R_{IR}=5.1 kΩ (≈16 R_{OUT} in Fig. 5 only)
- Ta=25 °C (Except Fig. 3)
- Fig. 1, 2 Refer to the measurement circuit.
- Fig. 3 is input data=all 1
- Fig. 4 is input data=output of incremental counter.

Package Outline Unit : mm

48PIN LQFP (PLASTIC)



DETAIL **A**

DETAIL **B**:SOLDER

DETAIL **B**:PALLADIUM

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	LQFP048-P-0707
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g