

# TAS5727 25-W Digital Audio Power Amplifier With EQ and DRC

## 1 Features

- Audio Input and Output
  - 25 W Into an 8-Ω Load From a 20-V Supply
  - Wide PVDD Range, From 8 V to 26 V
  - Supports BTL Configuration With 4-Ω Load
  - Efficient Class-D Operation Eliminates Need for Heatsinks
  - One Serial Audio Input (Two Audio Channels)
  - I<sup>2</sup>C Address Selection Pin (Chip Select)
  - Single Output Filter PBTl Support
  - Supports 44.1-kHz to 48-kHz Sample Rate (LJ/RJ/I<sup>2</sup>S)
- Audio and PWM Processing
  - Independent Channel Volume Controls With Gain of 24 dB to Mute With 0.125-dB Resolution Steps
  - Programmable Two-Band Dynamic-Range Control
  - 18 Programmable Biquads for Speaker EQ and Other Audio-Processing Features
  - Programmable Coefficients for DRC Filters
  - DC Blocking Filters
- General Features
  - I<sup>2</sup>C Serial Control Interface Operational Without MCLK
  - Requires Only 3.3 V and PVDD
  - No External Oscillator: Internal Oscillator for Automatic Rate Detection
  - Surface-Mount, 48-Pin HTQFP Package
  - Thermal and Short-Circuit Protection
  - 106-dB SNR, A-Weighted

- AD, BD, and Ternary Modulation
- Up to 90% Efficient
- PWM Level Meter to Measure the Digital Power Profile
- Benefits
  - EQ: Speaker Equalization Improves Audio Performance
  - Two-Band DRC: Dynamic Range Compression. Can Be Used As Power Limiter. Enables Speaker Protection, Easy Listening, Night-Mode Listening
  - Autodetect: Automatically Detects Sample-Rate Changes. No Need for External Microprocessor Intervention

## 2 Applications

- LCD TV, LED TV, Soundbar

## 3 Description

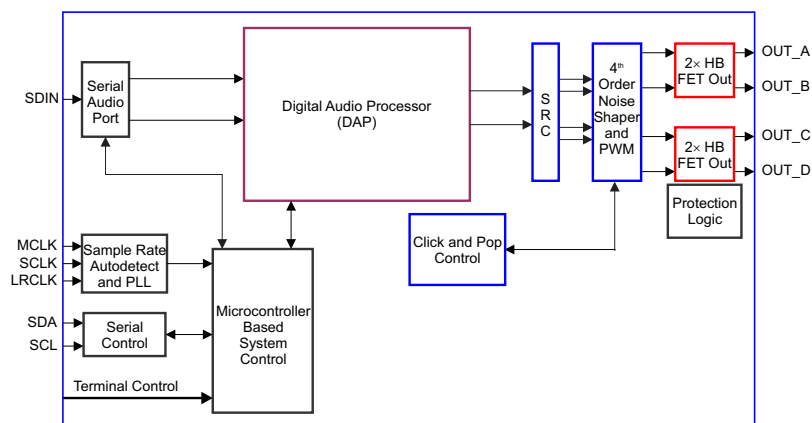
The TAS5727 is a 25-W, efficient, digital-audio power amplifier for driving stereo bridge-tied speakers. One serial data input allows processing of up to two discrete audio channels and seamless integration to most digital audio processors and MPEG decoders. The device accepts a wide range of input data and data rates. A fully programmable data path routes these channels to the internal speaker drivers.

### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE    | BODY SIZE (NOM)   |
|-------------|------------|-------------------|
| TAS5727     | HTQFP (48) | 7.00 mm x 7.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Functional View



B0262-06

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (November 2010) to Revision A                                                                                                                                                                                                                                                                                                  | Page |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. .... | 1    |
| • Changed Section: Overcurrent (OC) Protection With Current Limiting .....                                                                                                                                                                                                                                                                           | 16   |
| • Changed Section: Overcurrent (OC) Protection With Current Limiting and Overload Detection .....                                                                                                                                                                                                                                                    | 16   |

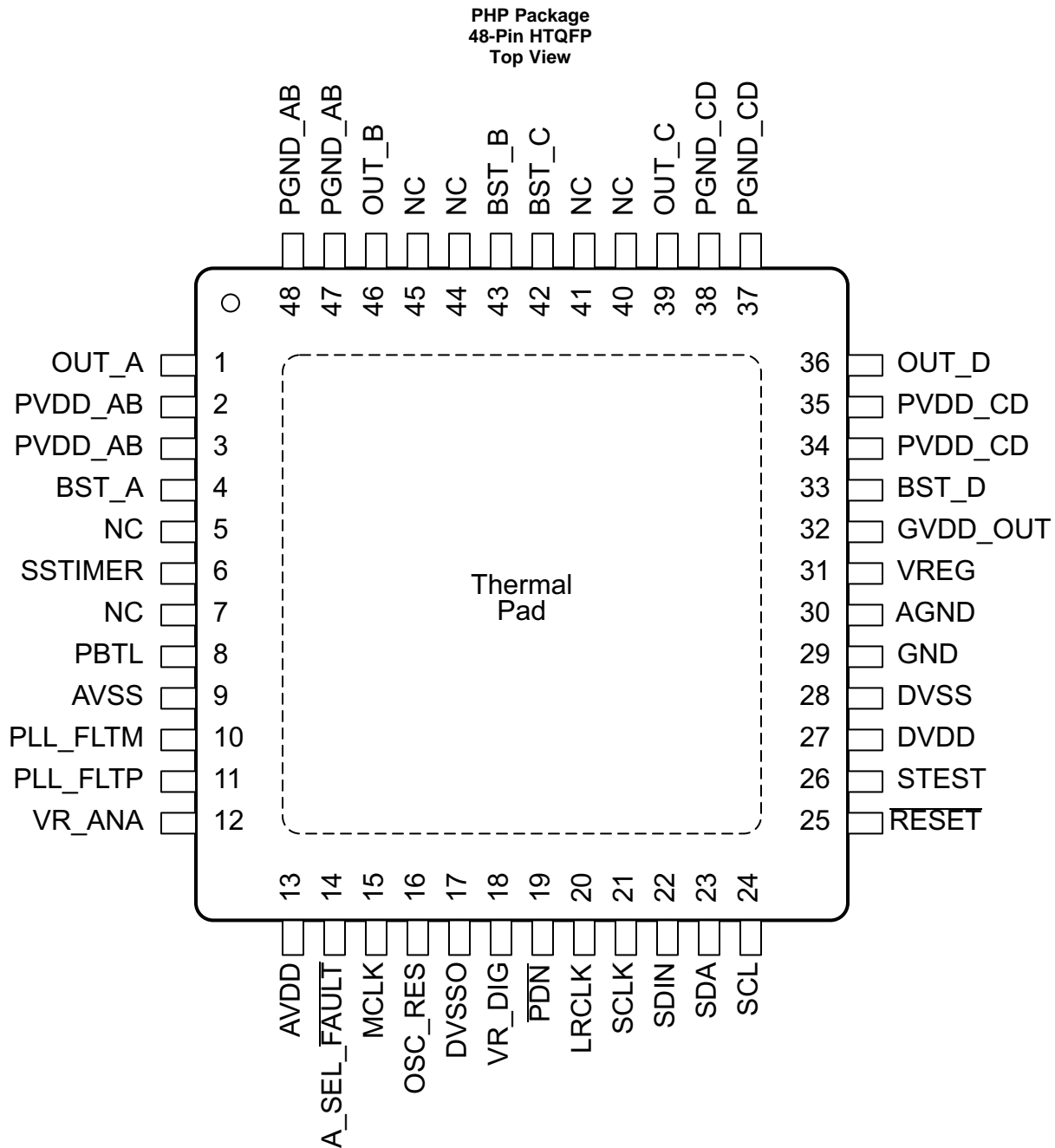
## 5 Description (continued)

The TAS5727 is a slave-only device receiving all clocks from external sources. The TAS5727 operates with a PWM carrier between a 384-kHz switching rate and a 288-KHz switching rate, depending on the input sample rate. Oversampling combined with a fourth-order noise shaper provides a flat noise floor and excellent dynamic range from 20 Hz to 20 kHz.

## 6 Device Comparison Table

|                                             | TAS5727    | TAS5729MD  | TAS5731M   | TAS5721    |
|---------------------------------------------|------------|------------|------------|------------|
| Maximum power to single-ended load          |            |            | 18         | 10         |
| Maximum power to bridge tied load           | 35         | 20         | 37         | 15         |
| Maximum power to parallel bridge tied load  | 70         | 40         | 70         | 30         |
| Minimum supported single-ended load         |            |            | 2          | 4          |
| Minimum supported bridge tied load          | 4          | 4          | 4          | 8          |
| Minimum supported parallel bridge tied load | 2          | 4          | 2          | 4          |
| Closed- or open-loop                        | Open       | Open       | Open       | Open       |
| Maximum speaker outputs (#)                 | 2          | 2          | 3          | 3          |
| Headphone channels                          | No         | Yes        | No         | Yes        |
| Architecture                                | Class D    | Class D    | Class D    | Class D    |
| Dynamic range control (DRC)                 | 2-Band AGL | 2-Band AGL | 2-Band DRC | 2-Band DRC |
| Biquads (EQ)                                | 28         | 28         | 21         | 21         |

## 7 Pin Configuration and Functions



### Pin Functions

| PIN  |     | TYPE <sup>(1)</sup> | 5-V TOLERANT | TERMINATION <sup>(2)</sup> | DESCRIPTION                         |
|------|-----|---------------------|--------------|----------------------------|-------------------------------------|
| NAME | NO. |                     |              |                            |                                     |
| AGND | 30  | P                   |              |                            | Local analog ground for power stage |

(1) TYPE: A = analog; D = 3.3-V digital; P = power/ground/decoupling; I = input; O = output

(2) All pullups are weak pullups and all pulldowns are weak pulldowns. The pullups and pulldowns are included to assure proper input logic levels if the pins are left unconnected (pullups → logic 1 input; pulldowns → logic 0 input).

**Pin Functions (continued)**

| PIN                       |                               | TYPE <sup>(1)</sup> | 5-V<br>TOLERANT | TERMINATION <sup>(2)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                                               |
|---------------------------|-------------------------------|---------------------|-----------------|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                      | NO.                           |                     |                 |                            |                                                                                                                                                                                                                                                                                                           |
| A_SEL_FAULT               | 14                            | DIO                 |                 |                            | This pin is monitored on the rising edge of $\overline{\text{RESET}}$ . A value of 0 (15-k $\Omega$ pull-down) sets the I <sup>2</sup> C device address to 0x54 and a value of 1 (15-k $\Omega$ pull-up) sets it to 0x56. this dual-function pin can be programmed to output internal power-stage errors. |
| AVDD                      | 13                            | P                   |                 |                            | 3.3-V analog power supply                                                                                                                                                                                                                                                                                 |
| AVSS                      | 9                             | P                   |                 |                            | Analog 3.3-V supply ground                                                                                                                                                                                                                                                                                |
| BST_A                     | 4                             | P                   |                 |                            | High-side bootstrap supply for half-bridge A                                                                                                                                                                                                                                                              |
| BST_B                     | 43                            | P                   |                 |                            | High-side bootstrap supply for half-bridge B                                                                                                                                                                                                                                                              |
| BST_C                     | 42                            | P                   |                 |                            | High-side bootstrap supply for half-bridge C                                                                                                                                                                                                                                                              |
| BST_D                     | 33                            | P                   |                 |                            | High-side bootstrap supply for half-bridge D                                                                                                                                                                                                                                                              |
| DVDD                      | 27                            | P                   |                 |                            | 3.3-V digital power supply                                                                                                                                                                                                                                                                                |
| DVSS                      | 28                            | P                   |                 |                            | Digital ground                                                                                                                                                                                                                                                                                            |
| DVSSO                     | 17                            | P                   |                 |                            | Oscillator ground                                                                                                                                                                                                                                                                                         |
| GND                       | 29                            | P                   |                 |                            | Analog ground for power stage                                                                                                                                                                                                                                                                             |
| GVDD_OUT                  | 32                            | P                   |                 |                            | Gate drive internal regulator output                                                                                                                                                                                                                                                                      |
| LRCLK                     | 20                            | DI                  | 5-V             | Pulldown                   | Input serial audio data left and right clock (sample-rate clock)                                                                                                                                                                                                                                          |
| MCLK                      | 15                            | DI                  | 5-V             | Pulldown                   | Master clock input                                                                                                                                                                                                                                                                                        |
| NC                        | 5, 7,<br>40,<br>41,<br>44, 45 | –                   |                 |                            | No connect                                                                                                                                                                                                                                                                                                |
| OSC_RES                   | 16                            | AO                  |                 |                            | Oscillator trim resistor. Connect an 18.2-k $\Omega$ , 1% resistor to DVSSO.                                                                                                                                                                                                                              |
| OUT_A                     | 1                             | O                   |                 |                            | Output, half-bridge A                                                                                                                                                                                                                                                                                     |
| OUT_B                     | 46                            | O                   |                 |                            | Output, half-bridge B                                                                                                                                                                                                                                                                                     |
| OUT_C                     | 39                            | O                   |                 |                            | Output, half-bridge C                                                                                                                                                                                                                                                                                     |
| OUT_D                     | 36                            | O                   |                 |                            | Output, half-bridge D                                                                                                                                                                                                                                                                                     |
| PBTL                      | 8                             | DI                  |                 |                            | Low means BTL mode; high means PBTL mode. Information goes directly to power stage.                                                                                                                                                                                                                       |
| $\overline{\text{PDN}}$   | 19                            | DI                  | 5-V             | Pullup                     | Power down, active-low. $\overline{\text{PDN}}$ prepares the device for loss of power supplies by shutting down the noise shaper and initiating the PWM stop sequence.                                                                                                                                    |
| PGND_AB                   | 47, 48                        | P                   |                 |                            | Power ground for half-bridges A and B                                                                                                                                                                                                                                                                     |
| PGND_CD                   | 37, 38                        | P                   |                 |                            | Power ground for half-bridges C and D                                                                                                                                                                                                                                                                     |
| PLL_FLTM                  | 10                            | AO                  |                 |                            | PLL negative loop-filter terminal                                                                                                                                                                                                                                                                         |
| PLL_FLTP                  | 11                            | AO                  |                 |                            | PLL positive loop-filter terminal                                                                                                                                                                                                                                                                         |
| PVDD_AB                   | 2, 3                          | P                   |                 |                            | Power-supply input for half-bridge output A                                                                                                                                                                                                                                                               |
| PVDD_CD                   | 34, 35                        | P                   |                 |                            | Power-supply input for half-bridge output D                                                                                                                                                                                                                                                               |
| $\overline{\text{RESET}}$ | 25                            | DI                  | 5-V             | Pullup                     | Reset, active-low. A system reset is generated by applying a logic low to this pin. $\overline{\text{RESET}}$ is an asynchronous control signal that restores the DAP to its default conditions and places the PWM in the hard-mute (high-impedance) state.                                               |
| SCL                       | 24                            | DI                  | 5-V             |                            | I <sup>2</sup> C serial control clock input                                                                                                                                                                                                                                                               |
| SCLK                      | 21                            | DI                  | 5-V             | Pulldown                   | Serial audio-data clock (shift clock). SCLK is the serial-audio-port input-data bit clock.                                                                                                                                                                                                                |
| SDA                       | 23                            | DIO                 | 5-V             |                            | I <sup>2</sup> C serial control data interface input/output                                                                                                                                                                                                                                               |
| SDIN                      | 22                            | DI                  | 5-V             | Pulldown                   | Serial audio data input. SDIN supports three discrete (stereo) data formats.                                                                                                                                                                                                                              |
| SSTIMER                   | 6                             | AI                  |                 |                            | Controls ramp time of OUT_x to minimize pop. Leave this pin floating for BD mode. Requires capacitor of 2.2 nF to GND in AD mode. The capacitor determines the ramp time.                                                                                                                                 |
| STEST                     | 26                            | DI                  |                 |                            | Factory test pin. Connect directly to DVSS.                                                                                                                                                                                                                                                               |

**Pin Functions (continued)**

| PIN    |     | TYPE <sup>(1)</sup> | 5-V TOLERANT | TERMINATION <sup>(2)</sup> | DESCRIPTION                                                                                             |
|--------|-----|---------------------|--------------|----------------------------|---------------------------------------------------------------------------------------------------------|
| NAME   | NO. |                     |              |                            |                                                                                                         |
| VR_ANA | 12  | P                   |              |                            | Internally regulated 1.8-V analog supply voltage. This pin must not be used to power external devices.  |
| VR_DIG | 18  | P                   |              |                            | Internally regulated 1.8-V digital supply voltage. This pin must not be used to power external devices. |
| VREG   | 31  | P                   |              |                            | Digital regulator output. Not to be used for powering external circuitry.                               |

## 8 Specifications

### 8.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                       |                                                         | MIN  | MAX                       | UNIT |
|---------------------------------------|---------------------------------------------------------|------|---------------------------|------|
| Supply voltage                        | DVDD, AVDD                                              | -0.3 | 3.6                       | V    |
|                                       | PVDD_x                                                  | -0.3 | 30                        | V    |
| Input voltage                         | 3.3-V digital input                                     | -0.5 | DVDD + 0.5                | V    |
|                                       | 5-V tolerant <sup>(2)</sup> digital input (except MCLK) | -0.5 | DVDD + 2.5 <sup>(3)</sup> |      |
|                                       | 5-V tolerant MCLK input                                 | -0.5 | AVDD + 2.5 <sup>(3)</sup> |      |
| OUT_x to PGND_x                       |                                                         |      | 32 <sup>(4)</sup>         | V    |
| BST_x to PGND_x                       |                                                         |      | 43 <sup>(4)</sup>         | V    |
| Input clamp current, I <sub>IK</sub>  |                                                         |      | ±20                       | mA   |
| Output clamp current, I <sub>OK</sub> |                                                         |      | ±20                       | mA   |
| Operating free-air temperature        |                                                         | 0    | 85                        | °C   |
| Operating junction temperature        |                                                         | 0    | 150                       | °C   |
| Storage temperature, T <sub>stg</sub> |                                                         | -40  | 125                       | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum conditions for extended periods may affect device reliability.
- (2) 5-V tolerant inputs are  $\overline{\text{PDN}}$ ,  $\overline{\text{RESET}}$ , SCLK, LRCLK, MCLK, SDIN, SDA, and SCL.
- (3) Maximum pin voltage should not exceed 6 V.
- (4) DC voltage + peak ac waveform measured at the pin should be below the allowed limit for all conditions.

### 8.2 ESD Ratings

|                                            |                                                                                | VALUE | UNIT |
|--------------------------------------------|--------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±1000 | V    |
|                                            | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±250  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 8.3 Recommended Operating Conditions

|                               |                                | MIN | NOM                                  | MAX | UNIT |     |    |
|-------------------------------|--------------------------------|-----|--------------------------------------|-----|------|-----|----|
|                               | Digital/analog supply voltage  |     | DVDD, AVDD                           | 3   | 3.3  | 3.6 | V  |
|                               | Half-bridge supply voltage     |     | PVDD_x                               | 8   |      | 26  | V  |
| V <sub>IH</sub>               | High-level input voltage       |     | 5-V tolerant                         | 2   |      |     | V  |
| V <sub>IL</sub>               | Low-level input voltage        |     | 5-V tolerant                         |     |      | 0.8 | V  |
| T <sub>A</sub>                | Operating ambient temperature  | 0   |                                      |     |      | 85  | °C |
| T <sub>J</sub> <sup>(1)</sup> | Operating junction temperature | 0   |                                      |     |      | 125 | °C |
| R <sub>L</sub> (BTL)          | Load impedance                 |     | Output filter: L = 15 μH, C = 680 nF | 4   | 8    |     | Ω  |
| R <sub>L</sub> (PBTL)         | Load impedance                 |     | Output filter: L = 15 μH, C = 680 nF | 2   | 4    |     | Ω  |

- (1) Continuous operation above the recommended junction temperature may result in reduced reliability and/or lifetime of the device.

## Recommended Operating Conditions (continued)

|                      |                          |                                                         | MIN | NOM | MAX | UNIT |
|----------------------|--------------------------|---------------------------------------------------------|-----|-----|-----|------|
| L <sub>O</sub> (BTL) | Output-filter inductance | Minimum output inductance under short-circuit condition | 10  |     |     | μH   |
|                      | Output sample rate       | 11.025/22.05/44.1-kHz data rate ±2%                     |     | 288 |     | kHz  |
|                      |                          | 48/24/12/8/16/32-kHz data rate ±2%                      |     | 384 |     |      |

## 8.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TAS5727     |      |  | UNIT |
|-------------------------------|----------------------------------------------|-------------|------|--|------|
|                               |                                              | PHP (HTQFP) |      |  |      |
|                               |                                              | 48 PINS     |      |  |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       |             | 27.9 |  | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    |             | 13   |  | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         |             | 1.1  |  | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   |             | 20.7 |  | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter |             | 0.3  |  | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance |             | 6.7  |  | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 8.5 DC Electrical Characteristics

T<sub>A</sub> = 25°, PVCC\_x = 18 V, DVDD = AVDD = 3.3 V, R<sub>L</sub> = 8 Ω, BTL AD mode, f<sub>S</sub> = 48 kHz (unless otherwise noted)

| PARAMETER                          |                                                              | TEST CONDITIONS                                                                               | MIN                             | TYP | MAX               | UNIT |    |
|------------------------------------|--------------------------------------------------------------|-----------------------------------------------------------------------------------------------|---------------------------------|-----|-------------------|------|----|
| V <sub>OH</sub>                    | High-level output voltage                                    | A_SEL_ FAULT and SDA<br>I <sub>OH</sub> = -4 mA<br>DVDD = 3 V                                 | 2.4                             |     |                   | V    |    |
| V <sub>OL</sub>                    | Low-level output voltage                                     | A_SEL_ FAULT and SDA<br>I <sub>OL</sub> = 4 mA<br>DVDD = 3 V                                  |                                 |     | 0.5               | V    |    |
| I <sub>IL</sub>                    | Low-level input current                                      | V <sub>I</sub> < V <sub>IL</sub> ; DVDD = AVDD = 3.6 V                                        |                                 |     | 75                | μA   |    |
| I <sub>IH</sub>                    | High-level input current                                     | V <sub>I</sub> > V <sub>IH</sub> ; DVDD = AVDD = 3.6 V                                        |                                 |     | 75 <sup>(1)</sup> | μA   |    |
| I <sub>DD</sub>                    | 3.3-V supply current                                         | 3.3-V supply voltage (DVDD, AVDD)                                                             | Normal mode                     |     | 49                | 68   | mA |
|                                    |                                                              |                                                                                               | Reset (RESET = low, PDN = high) |     | 23                | 38   |    |
| I <sub>PVDD</sub>                  | Supply current                                               | No load (PVDD_x)                                                                              | Normal mode                     |     | 32                | 50   | mA |
|                                    |                                                              |                                                                                               | Reset (RESET = low, PDN = high) |     | 3                 | 8    |    |
| r <sub>DS(on)</sub> <sup>(2)</sup> | Drain-to-source resistance, LS                               | T <sub>J</sub> = 25°C, includes metallization resistance                                      |                                 | 75  |                   | mΩ   |    |
|                                    | Drain-to-source resistance, HS                               | T <sub>J</sub> = 25°C, includes metallization resistance                                      |                                 | 75  |                   |      |    |
| <b>I/O Protection</b>              |                                                              |                                                                                               |                                 |     |                   |      |    |
| V <sub>UVP</sub>                   | Undervoltage protection limit                                | PVDD falling                                                                                  |                                 | 7.2 |                   | V    |    |
| V <sub>UVP,hyst</sub>              | Undervoltage protection limit                                | PVDD rising                                                                                   |                                 | 7.6 |                   | V    |    |
| O <sub>TE</sub> <sup>(3)</sup>     | Overtemperature error                                        |                                                                                               |                                 | 150 |                   | °C   |    |
| O <sub>TEHYST</sub> <sup>(3)</sup> | Extra temperature drop required to recover from error        |                                                                                               |                                 | 30  |                   | °C   |    |
| I <sub>OC</sub>                    | Overcurrent limit protection                                 |                                                                                               |                                 | 4.5 |                   | A    |    |
| I <sub>OCT</sub>                   | Overcurrent response time                                    |                                                                                               |                                 | 150 |                   | ns   |    |
| R <sub>PD</sub>                    | Internal pulldown resistor at the output of each half-bridge | Connected when drivers are in the high-impedance state to provide bootstrap capacitor charge. |                                 | 3   |                   | kΩ   |    |

(1) I<sub>IH</sub> for the PBTL pin has a maximum limit of 200 μA due to an internal pulldown on the pin.

(2) This does not include bond-wire or pin resistance.

(3) Specified by design

## 8.6 AC Electrical Characteristics (BTL, PBTL)

PVDD<sub>x</sub> = 18 V, BTL AD mode,  $f_s = 48$  KHz,  $R_L = 8 \Omega$ ,  $R_{OCP} = 22$  k $\Omega$ ,  $C_{BST} = 33$  nF, audio frequency = 1 kHz, AES17 filter,  $f_{PWM} = 384$  kHz,  $T_A = 25^\circ\text{C}$  (unless otherwise specified). All performance is in accordance with recommended operating conditions (unless otherwise specified).

| PARAMETER      |                                      | TEST CONDITIONS                                                        | MIN | TYP   | MAX | UNIT          |
|----------------|--------------------------------------|------------------------------------------------------------------------|-----|-------|-----|---------------|
| P <sub>O</sub> | Power output per channel             | PVDD = 18 V, 10% THD, 1-kHz input signal                               |     | 21.5  |     | W             |
|                |                                      | PVDD = 18 V, 7% THD, 1-kHz input signal                                |     | 20.3  |     |               |
|                |                                      | PVDD = 12 V, 10% THD, 1-kHz input signal                               |     | 9.6   |     |               |
|                |                                      | PVDD = 12 V, 7% THD, 1-kHz input signal                                |     | 9.1   |     |               |
|                |                                      | PVDD = 8 V, 10% THD, 1-kHz input signal                                |     | 4.2   |     |               |
|                |                                      | PVDD = 8 V, 7% THD, 1-kHz input signal                                 |     | 4     |     |               |
|                |                                      | PBTL mode, PVDD = 12 V, $R_L = 4 \Omega$ , 10% THD, 1-kHz input signal |     | 18.7  |     |               |
|                |                                      | PBTL mode, PVDD = 12 V, $R_L = 4 \Omega$ , 7% THD, 1-kHz input signal  |     | 17.7  |     |               |
|                |                                      | PBTL mode, PVDD = 18 V, $R_L = 4 \Omega$ , 10% THD, 1-kHz input signal |     | 41.5  |     |               |
|                |                                      | PBTL mode, PVDD = 18 V, $R_L = 4 \Omega$ , 7% THD, 1-kHz input signal  |     | 39    |     |               |
| THD+N          | Total harmonic distortion + noise    | PVDD = 18 V, P <sub>O</sub> = 1 W                                      |     | 0.07% |     |               |
|                |                                      | PVDD = 12 V, P <sub>O</sub> = 1 W                                      |     | 0.03% |     |               |
|                |                                      | PVDD = 8 V, P <sub>O</sub> = 1 W                                       |     | 0.1%  |     |               |
| V <sub>n</sub> | Output integrated noise (rms)        | A-weighted                                                             |     | 56    |     | $\mu\text{V}$ |
|                | Crosstalk                            | P <sub>O</sub> = 0.25 W, f = 1 kHz (BD Mode)                           |     | -82   |     | dB            |
|                |                                      | P <sub>O</sub> = 0.25 W, f = 1 kHz (AD Mode)                           |     | -69   |     | dB            |
| SNR            | Signal-to-noise ratio <sup>(1)</sup> | A-weighted, f = 1 kHz, maximum power at THD < 1%                       |     | 106   |     | dB            |

(1) SNR is calculated relative to 0-dBFS input level.

## 8.7 PLL Input Parameters and External Filter Components

| PARAMETER                             |                                          | TEST CONDITIONS      | MIN    | TYP    | MAX | UNIT     |
|---------------------------------------|------------------------------------------|----------------------|--------|--------|-----|----------|
| f <sub>MCLKI</sub>                    | MCLK frequency                           |                      | 2.8224 | 24.576 |     | MHz      |
|                                       | MCLK duty cycle                          |                      | 40%    | 50%    | 60% |          |
| t <sub>r</sub> / t <sub>f(MCLK)</sub> | Rise/fall time for MCLK                  |                      |        |        | 5   | ns       |
|                                       | LRCLK allowable drift before LRCLK reset |                      |        |        | 4   | MCLKs    |
|                                       | External PLL filter capacitor C1         | SMD 0603 X7R         |        | 47     |     | nF       |
|                                       | External PLL filter capacitor C2         | SMD 0603 X7R         |        | 4.7    |     | nF       |
|                                       | External PLL filter resistor R           | SMD 0603, metal film |        | 470    |     | $\Omega$ |

## 8.8 Serial Audio Ports Slave Mode

over recommended operating conditions (unless otherwise noted)

| PARAMETER           |                                                                     | TEST CONDITIONS        | MIN   | NOM    | MAX | UNIT |
|---------------------|---------------------------------------------------------------------|------------------------|-------|--------|-----|------|
| f <sub>SCLKIN</sub> | Frequency, SCLK $32 \times f_s$ , $48 \times f_s$ , $64 \times f_s$ | C <sub>L</sub> = 30 pF | 1.024 | 12.288 |     | MHz  |
| t <sub>su1</sub>    | Setup time, LRCLK to SCLK rising edge                               |                        | 10    |        |     | ns   |
| t <sub>h1</sub>     | Hold time, LRCLK from SCLK rising edge                              |                        | 10    |        |     | ns   |
| t <sub>su2</sub>    | Setup time, SDIN to SCLK rising edge                                |                        | 10    |        |     | ns   |
| t <sub>h2</sub>     | Hold time, SDIN from SCLK rising edge                               |                        | 10    |        |     | ns   |
|                     | LRCLK frequency                                                     |                        | 8     | 48     | 48  | kHz  |
|                     | SCLK duty cycle                                                     |                        | 40%   | 50%    | 60% |      |
|                     | LRCLK duty cycle                                                    |                        | 40%   | 50%    | 60% |      |

### Serial Audio Ports Slave Mode (continued)

over recommended operating conditions (unless otherwise noted)

| PARAMETER    | TEST CONDITIONS                                           | MIN  | NOM | MAX | UNIT        |
|--------------|-----------------------------------------------------------|------|-----|-----|-------------|
|              | SCLK rising edges between LRCLK rising edges              | 32   |     | 64  | SCLK edges  |
| $t_{(edge)}$ | LRCLK clock edge with respect to the falling edge of SCLK | -1/4 |     | 1/4 | SCLK period |
| $t_r/t_f$    | Rise/fall time for SCLK/LRCLK                             |      |     | 8   | ns          |

### 8.9 I<sup>2</sup>C Serial Control Port Operation

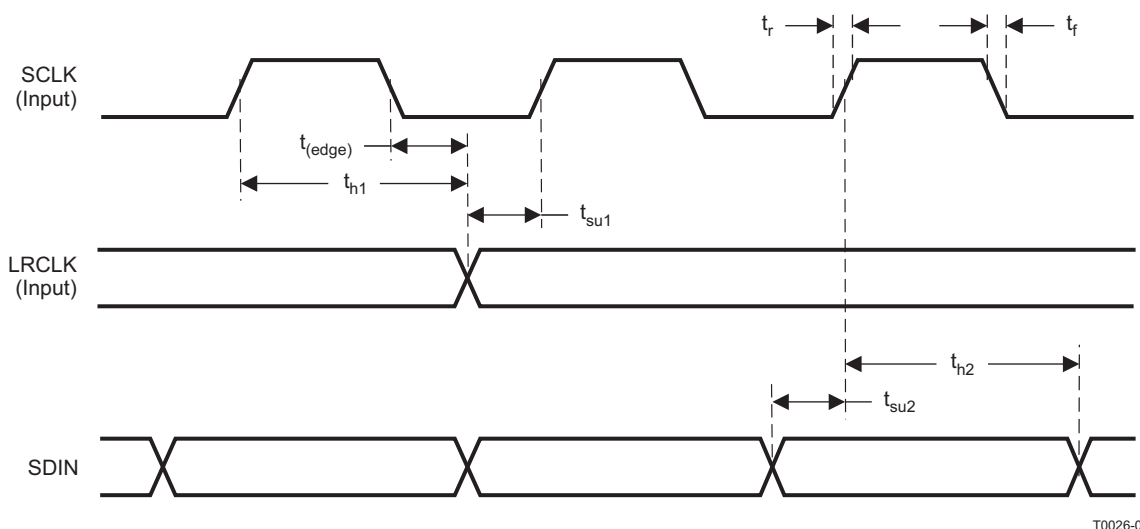
Timing characteristics for I<sup>2</sup>C Interface signals over recommended operating conditions (unless otherwise noted)

| PARAMETER                                                   | TEST CONDITIONS | MIN | MAX | UNIT    |
|-------------------------------------------------------------|-----------------|-----|-----|---------|
| $f_{SCL}$ Frequency, SCL                                    | No wait states  |     | 400 | kHz     |
| $t_{w(H)}$ Pulse duration, SCL high                         |                 | 0.6 |     | $\mu$ s |
| $t_{w(L)}$ Pulse duration, SCL low                          |                 | 1.3 |     | $\mu$ s |
| $t_r$ Rise time, SCL and SDA                                |                 |     | 300 | ns      |
| $t_f$ Fall time, SCL and SDA                                |                 |     | 300 | ns      |
| $t_{su1}$ Setup time, SDA to SCL                            |                 | 100 |     | ns      |
| $t_{h1}$ Hold time, SCL to SDA                              |                 | 0   |     | ns      |
| $t_{(buf)}$ Bus free time between stop and start conditions |                 | 1.3 |     | $\mu$ s |
| $t_{su2}$ Setup time, SCL to start condition                |                 | 0.6 |     | $\mu$ s |
| $t_{h2}$ Hold time, start condition to SCL                  |                 | 0.6 |     | $\mu$ s |
| $t_{su3}$ Setup time, SCL to stop condition                 |                 | 0.6 |     | $\mu$ s |
| $C_L$ Load capacitance for each bus line                    |                 |     | 400 | pF      |

### 8.10 Reset Timing (RESET)

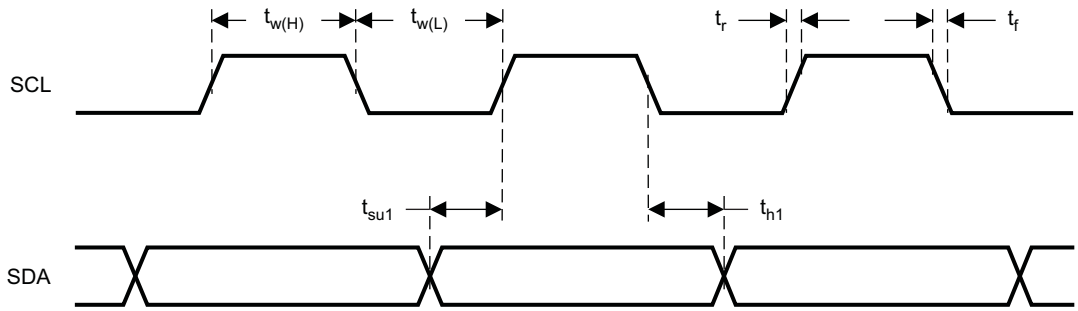
Control signal parameters over recommended operating conditions (unless otherwise noted). Please refer to Recommended Use Model section on usage of all terminals.

| PARAMETER                                           | MIN | NOM | MAX | UNIT    |
|-----------------------------------------------------|-----|-----|-----|---------|
| $t_{w(RESET)}$ Pulse duration, RESET active         | 100 |     |     | $\mu$ s |
| $t_{d(I2C\_ready)}$ Time to enable I <sup>2</sup> C |     |     | 12  | ms      |



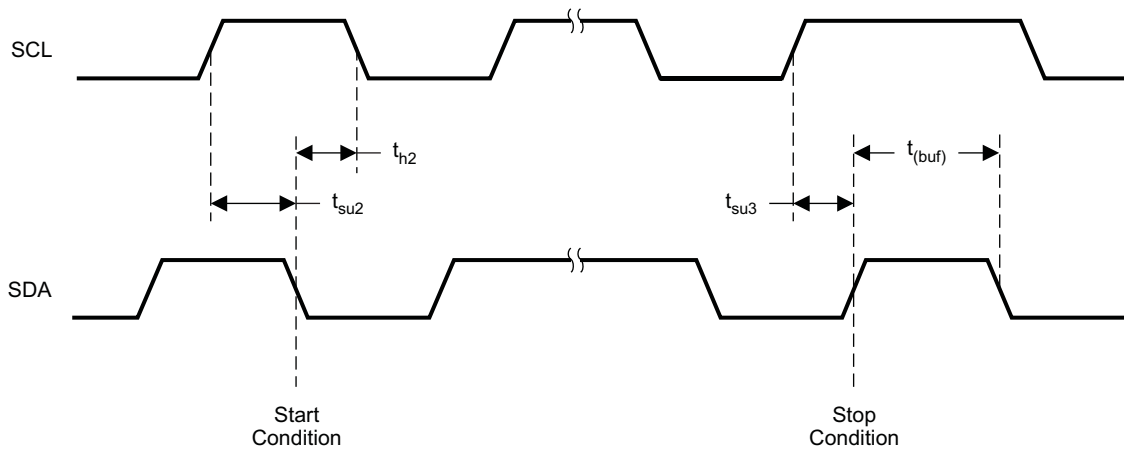
T0026-04

Figure 1. Slave-Mode Serial Data-Interface Timing



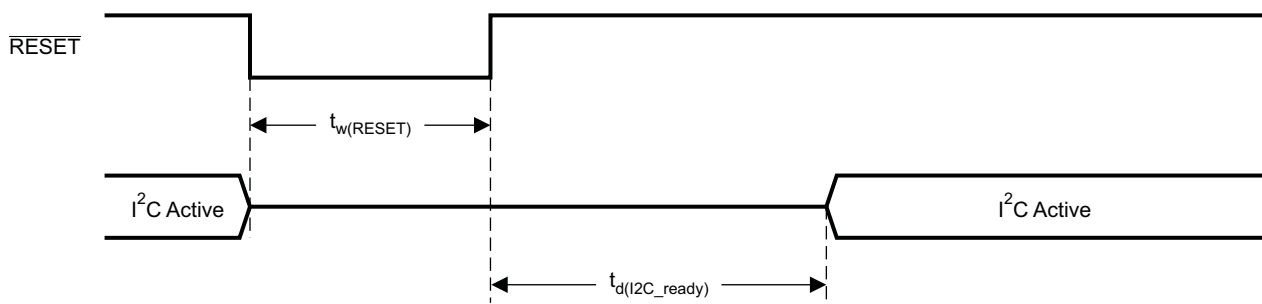
T0027-01

**Figure 2. SCL and SDA Timing**



T0028-01

**Figure 3. Start and Stop Conditions Timing**



System Initialization.  
Enable via I<sup>2</sup>C.

T0421-01

NOTES: On power up, TI recommends that the TAS5727  $\overline{RESET}$  be held LOW for at least 100  $\mu$ s after DVDD has reached 3 V.

If  $\overline{RESET}$  is asserted LOW while  $\overline{PDN}$  is LOW, then  $\overline{RESET}$  must continue to be held LOW for at least 100  $\mu$ s after  $\overline{PDN}$  is deasserted (HIGH).

**Figure 4. Reset Timing**

### 8.11 Typical Characteristics

BTL Configuration, 8 Ω

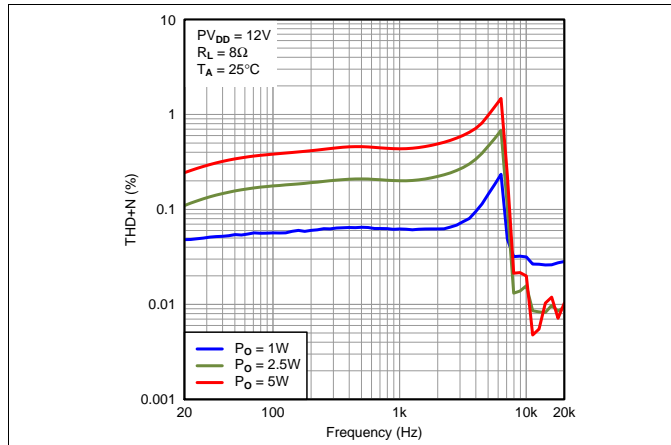


Figure 5. Total Harmonic Distortion + Noise vs Frequency

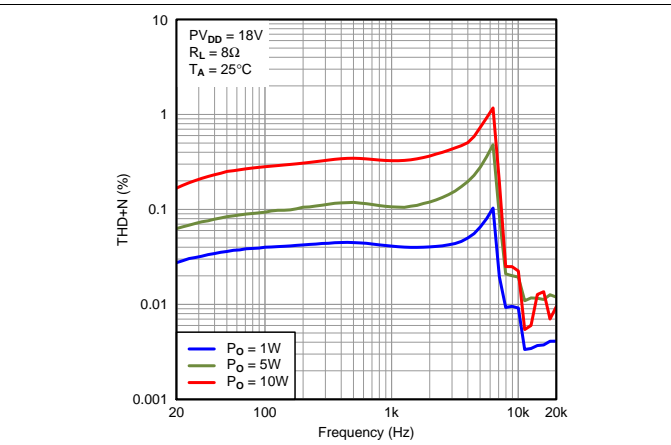


Figure 6. Total Harmonic Distortion + Noise vs Frequency

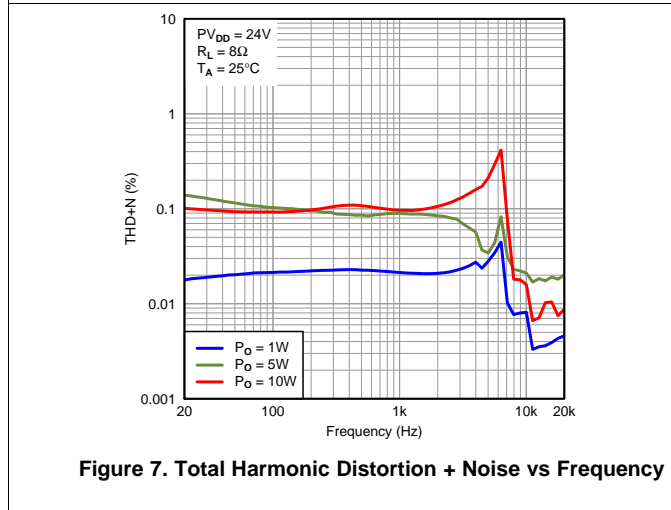


Figure 7. Total Harmonic Distortion + Noise vs Frequency

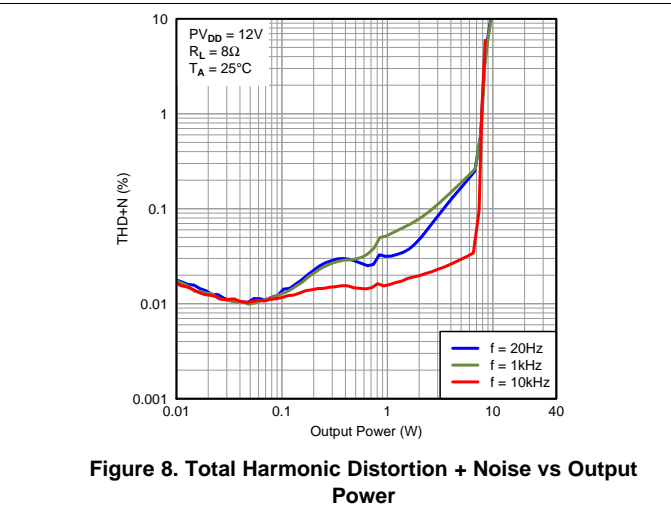


Figure 8. Total Harmonic Distortion + Noise vs Output Power

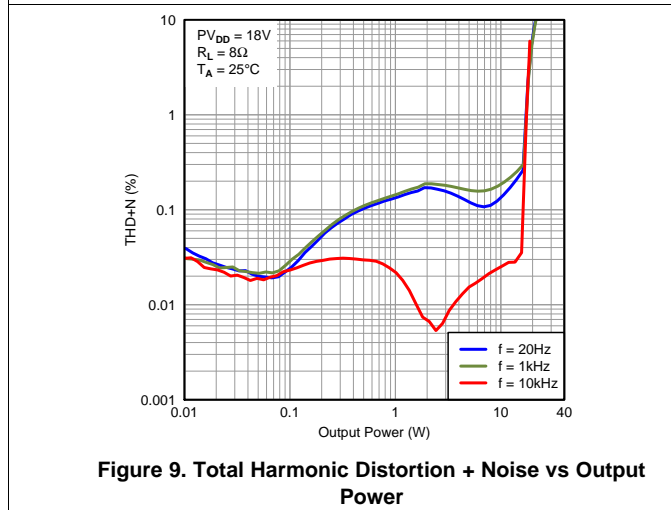


Figure 9. Total Harmonic Distortion + Noise vs Output Power

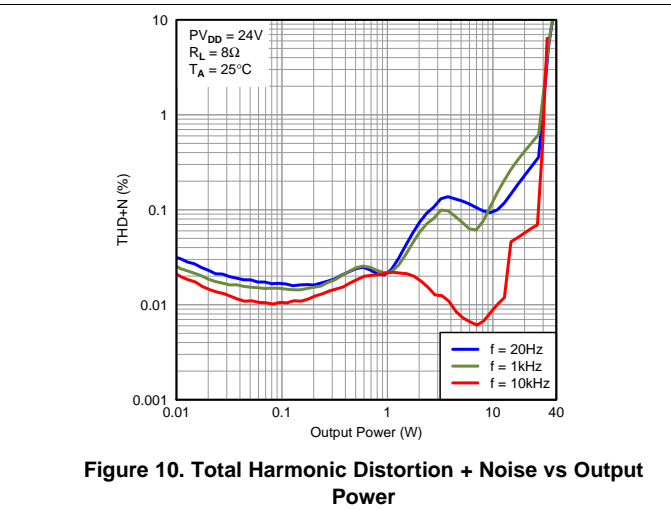
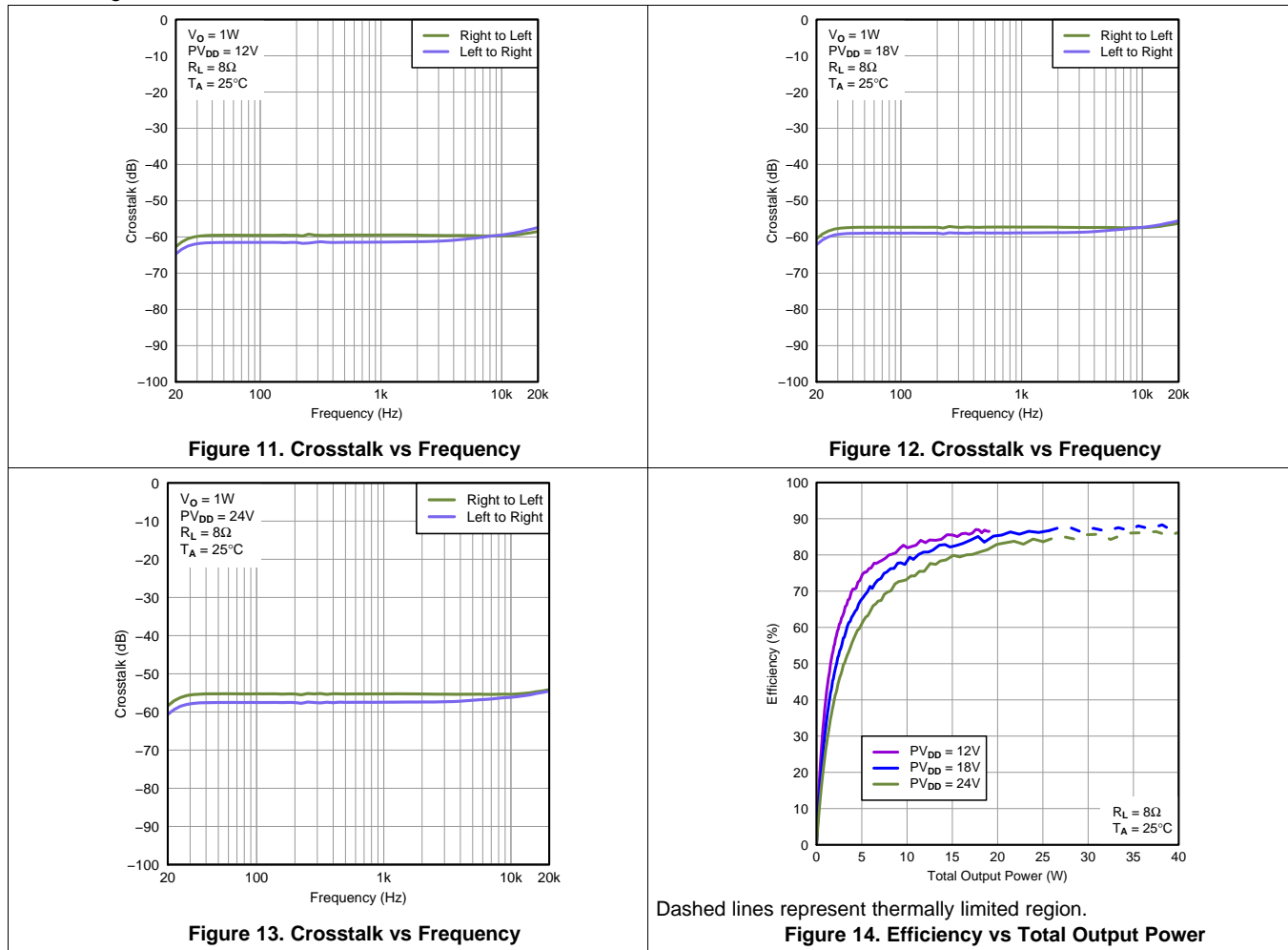


Figure 10. Total Harmonic Distortion + Noise vs Output Power

## Typical Characteristics (continued)

BTL Configuration, 8 Ω



## 9 Parameter Measurement Information

All parameters are measured according to the conditions described in the [Specifications](#).

## 10 Detailed Description

### 10.1 Overview

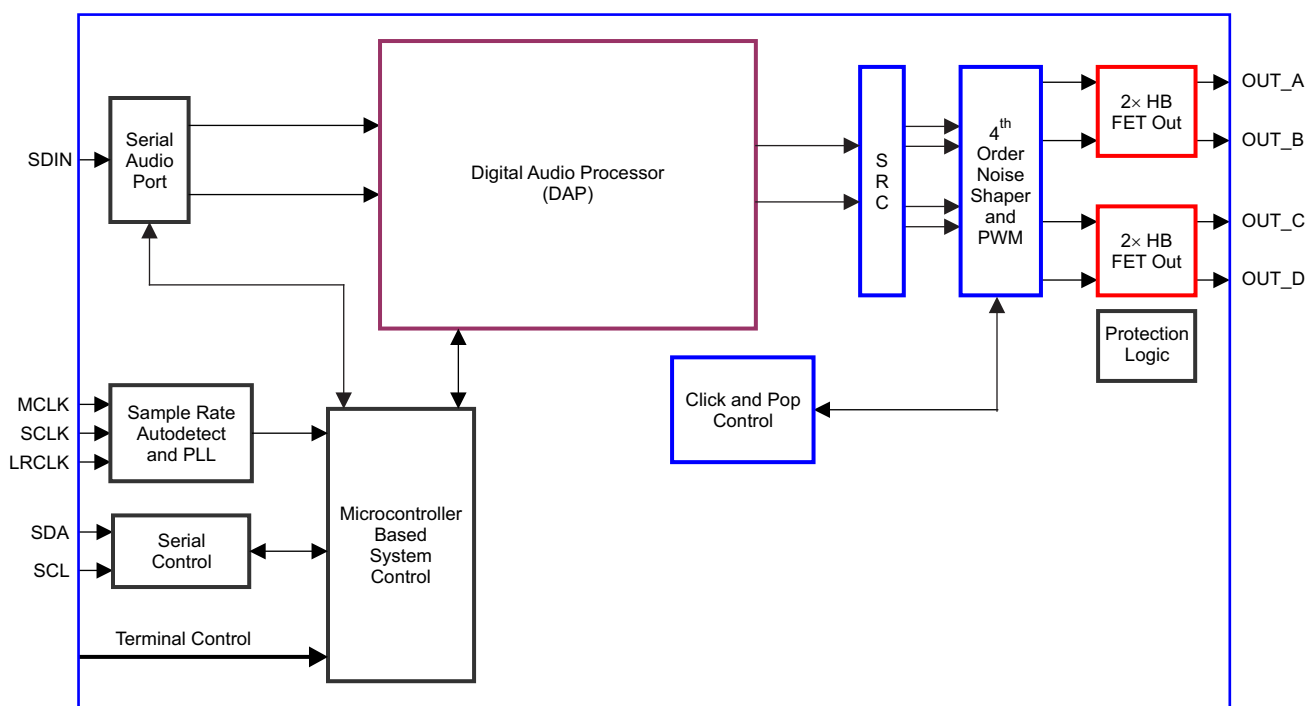
The TAS5727 is an efficient stereo I<sup>2</sup>S input Class-D audio power amplifier with a digital audio processor. The digital audio processor of the device uses noise shaping and customized correction algorithms to achieve a great power efficiency and high audio performance. Also, the device has up to eighteen equalizers and two-band advanced Automatic Gain Limiting (AGL).

The device needs only a single DVDD supply in addition to the higher-voltage PVDD power supply. An internal voltage regulator provides suitable voltage levels for the gate drive circuit. The wide PVDD power supply range of the device enables its use in a multitude of applications.

The TAS5727 is a slave-only device that is controlled by a bidirectional I<sup>2</sup>C interface that supports both 100-kHz and 400-kHz data transfer rates for single- and multiple-byte write and read operations. This control interface is used to program the registers of the device and read the device status. The PWM of this device operates with a carrier frequency between 384 kHz and 354 kHz, depending the sampling rate. This device allows the use of the same clock signal for both MCLK and BCLK (64xFs) when using a sampling frequency of 44.1 kHz or 48 kHz.

This amplifier can be configured in two different modes, stereo and mono single filter configuration is supported in mono mode.

### 10.2 Functional Block Diagrams



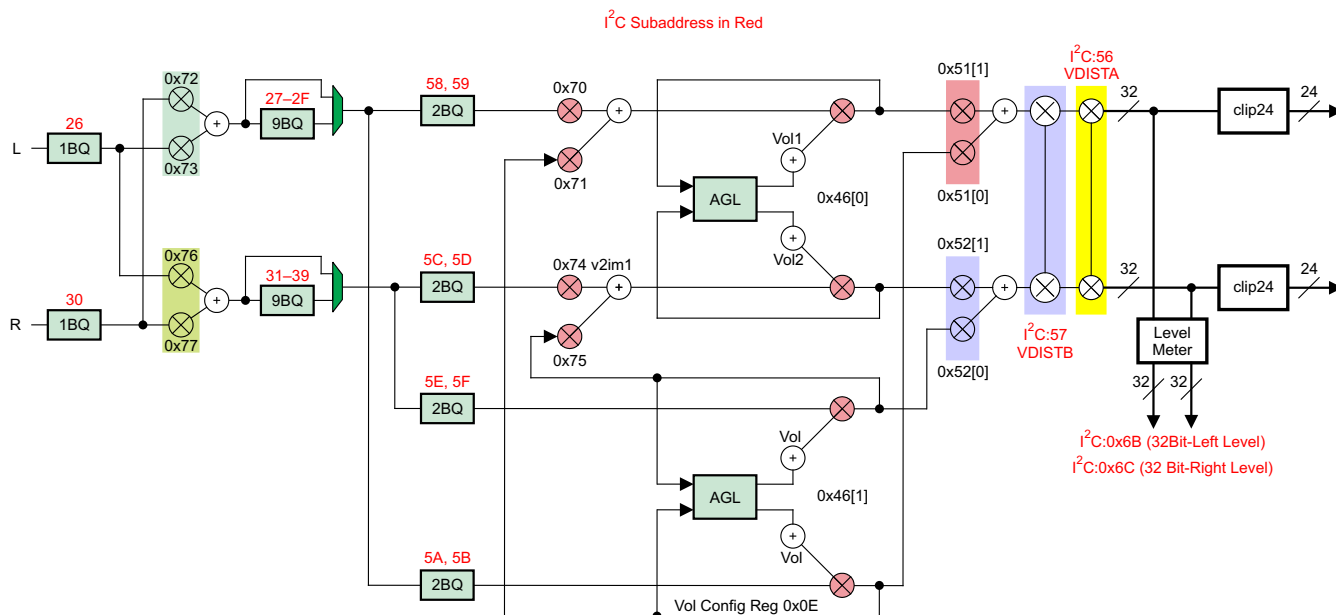
B0262-06

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Figure 15. Functional View



Functional Block Diagrams (continued)



B0321-11  
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Figure 17. DAP Process Structure

10.3 Feature Description

10.3.1 Power Supply

To facilitate system design, the TAS5727 needs only a 3.3-V supply in addition to the (typical) 18-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the gate drive circuitry. Additionally, all circuitry requiring a floating voltage supply, for example, the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors.

To provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST\_x), and power-stage supply pins (PVDD\_x). The gate-drive voltage (GVDD\_OUT) is derived from the PVDD voltage. Place all decoupling capacitors as close to their associated pins as possible. Inductance between the power-supply pins and decoupling capacitors must be avoided.

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST\_x) to the power-stage output pin (OUT\_x). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive regulator output pin (GVDD\_OUT) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 288 kHz to 384 kHz, TI recommends using 33-nF, X7R ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power-stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Pay special attention to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD\_x). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD\_x pin is decoupled with a 100-nF, X7R ceramic capacitor placed as close as possible to each supply pin.

The TAS5727 is fully protected against erroneous power-stage turnon due to parasitic gate charging.

## Feature Description (continued)

### 10.3.2 I<sup>2</sup>C Address Selection and Fault Output

#### 10.3.2.1 I<sup>2</sup>C Chip Select

A\_SEL\_FAULT is an input pin during power up. It can be pulled high (15-kΩ pullup) or low (15-kΩ pulldown). High indicates an I<sup>2</sup>C subaddress of 0x56, and low a subaddress of 0x54.

#### 10.3.2.2 I<sup>2</sup>C Device Address Change Procedure

- Write to device address change enable register, 0xF8 with a value of 0xF9A5 A5A5.
- Write to device register 0xF9 with a value of 0x0000 00XX, where XX is the new address.
- Any writes after that should use the new device address XX.

#### 10.3.2.3 Fault Indication

A\_SEL\_FAULT is an input pin during power up. This pin can be programmed after RESET to be an output by writing 1 to bit 0 of I<sup>2</sup>C register 0x05. In that mode, the A\_SEL\_FAULT pin has the definition shown in Table 1.

Any fault resulting in device shutdown is signaled by the A\_SEL\_FAULT pin going low (see Table 1). A latched version of this pin is available on D1 of register 0x02. This bit can be reset only by an I<sup>2</sup>C write.

**Table 1. A\_SEL\_FAULT Output States**

| A_SEL_FAULT | DESCRIPTION                                                                                      |
|-------------|--------------------------------------------------------------------------------------------------|
| 0           | Overcurrent (OC) or undervoltage (UVP) error or overtemperature error (OTE) or overvoltage error |
| 1           | No faults (normal operation)                                                                     |

### 10.3.3 Device Protection Systems

#### 10.3.3.1 Overcurrent (OC) Protection With Current Limiting

The device has independent, fast-reacting current detectors on all high-side and low-side power-stage FETs. The detector outputs are closely monitored by two protection systems. The first protection system controls the power stage to prevent the output current further increasing, that is, the protection system performs a cycle-by-cycle current-limiting function, rather than prematurely shutting down during combinations of high-level music transients and extreme speaker load-impedance drops. If the high-current condition situation persists, that is, the power stage is being overloaded, a second protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state. The device returns to normal operation once the fault condition (that is, a short circuit on the output) is removed. Current-limiting and overcurrent protection are not independent for half-bridges. That is, if the bridge-tied load between half-bridges A and B causes an overcurrent fault, half-bridges A, B, C, and D are shut down.

#### 10.3.3.2 Overtemperature Protection

The TAS5727 has an overtemperature-protection system. If the device junction temperature exceeds 150°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and A\_SEL\_FAULT being asserted low. The TAS5727 recovers automatically once the temperature drops approximately 30°C.

#### 10.3.3.3 Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the TAS5727 fully protect the device in any power-up, power-down, and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the PVDD and AVDD supply voltages reach 7.6 V and 2.7 V, respectively. Although PVDD and AVDD are independently monitored, a supply-voltage drop below the UVP threshold on AVDD or either PVDD pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and A\_SEL\_FAULT being asserted low.

## Feature Description (continued)

### 10.3.4 Clock, Auto Detection, and PLL

The TAS5727 is an I<sup>2</sup>S slave device. It accepts MCLK, SCLK, and LRCLK. The digital audio processor (DAP) supports all the sample rates and MCLK rates that are defined in the [Clock Control Register \(0x00\)](#).

The TAS5727 checks to verify that SCLK is a specific value of  $32 f_s$ ,  $48 f_s$ , or  $64 f_s$ . The DAP only supports a  $1 \times f_s$  LRCLK. The timing relationship of these clocks to SDIN is shown in subsequent sections. The clock section uses MCLK or the internal oscillator clock (when MCLK is unstable, out of range, or absent) to produce the internal clock (DCLK) running at 512 times the PWM switching frequency.

The DAP can autodetect and set the internal clock control logic to the appropriate settings for all supported clock rates as defined in the clock-control register.

The TAS5727 has robust clock error handling that uses the built-in trimmed oscillator clock to quickly detect changes and errors. Once the system detects a clock change or error, it mutes the audio (through a single-step mute) and then forces PLL to limp using the internal oscillator as a reference clock. Once the clocks are stable, the system autodetects the new rate and reverts to normal operation. During this process, the default volume is restored in a single step (also called hard unmute). The ramp process can be programmed to ramp back slowly (also called soft unmute) as defined in volume register (0x0E).

### 10.3.5 PWM Section

The TAS5727 DAP device uses noise-shaping and customized nonlinear correction algorithms to achieve high power efficiency and high-performance digital audio reproduction. The DAP uses a fourth-order noise shaper to increase dynamic range and SNR in the audio band. The PWM section accepts 24-bit PCM data from the DAP and outputs two BTL PWM audio output channels.

The PWM section has individual-channel DC-blocking filters that can be enabled and disabled. The filter cutoff frequency is less than 1 Hz. Individual-channel de-emphasis filters for 44.1 kHz and 48 kHz are included and can be enabled and disabled.

Finally, the PWM section has an adjustable maximum modulation limit of 93.8% to 99.2%.

For a detailed description of using audio processing features like DRC and EQ, see the User's Guide ([SLOU299](#)) and the [TAS57xx GDE](#).

### 10.3.6 SSTIMER Functionality

The SSTIMER pin uses a capacitor connected between this pin and ground to control the output duty cycle when exiting all-channel shutdown. The capacitor on the SSTIMER pin is slowly charged through an internal current source, and the charge time determines the rate at which the output transitions from a near-zero duty cycle to the desired duty cycle. This allows for a smooth transition that minimizes audible pops and clicks. When the part is shut down, the drivers are placed in the high-impedance state and transition slowly down through a 3-k $\Omega$  resistor, similarly minimizing pops and clicks. The shutdown transition time is independent of the SSTIMER pin capacitance. Larger capacitors increase the start-up time, while capacitors smaller than 2.2 nF decrease the start-up time. The SSTIMER pin should be left floating for BD modulation.

### 10.3.7 Single-Filter PBTL Mode

The TAS5727 supports parallel BTL (PBTL) mode with OUT\_A/OUT\_B (and OUT\_C/OUT\_D) connected before the LC filter. To put the part in PBTL configuration, drive PBTL (pin 8) HIGH. This synchronizes the turnoff of half-bridges A and B (and similarly C/D) if an overcurrent condition is detected in either half-bridge. There is a pulldown resistor on the PBTL pin that configures the part in BTL mode if the pin is left floating.

PWM output multiplexers should be updated to set the device in PBTL mode. Output Mux Register (0x25) should be written with a value of 0x0110 3245. Also, the PWM shutdown register (0x19) should be written with a value of 0x3A.

## Feature Description (continued)

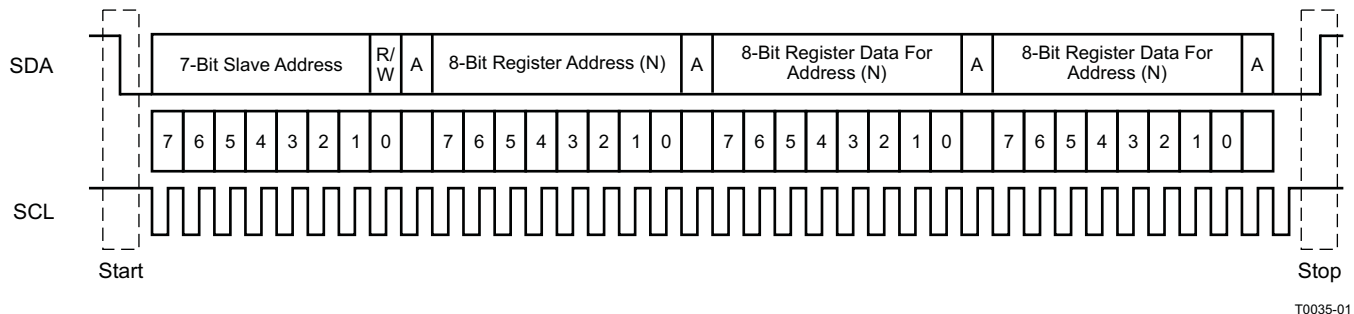
### 10.3.8 I<sup>2</sup>C Serial Control Interface

The TAS5727 DAP has a bidirectional I<sup>2</sup>C interface that is compatible with the Inter IC (I<sup>2</sup>C) bus protocol and supports both 100-kHz and 400-kHz data transfer rates for single- and multiple-byte write and read operations. This is a slave-only device that does not support a multimaster bus environment or wait-state insertion. The control interface is used to program the registers of the device and to read device status.

The DAP supports the standard-mode I<sup>2</sup>C bus operation (100 kHz maximum) and the fast I<sup>2</sup>C bus operation (400 kHz maximum). The DAP performs all I<sup>2</sup>C operations without I<sup>2</sup>C wait cycles.

#### 10.3.8.1 General I<sup>2</sup>C Operation

The I<sup>2</sup>C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 18. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The TAS5727 holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals through a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the high level for the bus.



**Figure 18. Typical I<sup>2</sup>C Sequence**

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 18.

The 7-bit address for TAS5715 is 0101 010 (0x54) or 0101 011 (0x56) defined by A\_SEL (external pulldown for 0x54 and pullup for 0x56).

#### 10.3.8.2 Single- and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte read/write operations for subaddresses 0x00 to 0x1F. However, for the subaddresses 0x20 to 0xFF, the serial control interface supports only multiple-byte read/write operations (in multiples of 4 bytes).

During multiple-byte read operations, the DAP responds with data, a byte at a time, starting at the subaddress assigned, as long as the master device continues to respond with acknowledges. If a particular subaddress does not contain 32 bits, the unused bits are read as logic 0.

## Feature Description (continued)

During multiple-byte write operations, the DAP compares the number of bytes transmitted to the number of bytes that are required for each specific subaddress. For example, if a write command is received for a biquad subaddress, the DAP must receive five 32-bit words. If fewer than five 32-bit data words have been received when a stop command (or another start command) is received, the received data is discarded.

Supplying a subaddress for each subaddress transaction is referred to as random I<sup>2</sup>C addressing. The TAS5727 also supports sequential I<sup>2</sup>C addressing. For write transactions, if a subaddress is issued followed by data for that subaddress and the 15 subaddresses that follow, a sequential I<sup>2</sup>C write transaction has taken place, and the data for all 16 subaddresses is successfully received by the TAS5727. For I<sup>2</sup>C sequential-write transactions, the subaddress then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many subaddresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last subaddress is discarded. However, all other data written is accepted; only the incomplete data is discarded.

### 10.3.8.3 Single-Byte Write

As shown in Figure 19, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I<sup>2</sup>C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a data-write transfer, the read/write bit is a 0. After receiving the correct I<sup>2</sup>C device address and the read/write bit, the DAP responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the TAS5727 internal memory address being accessed. After receiving the address byte, the TAS5727 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5727 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

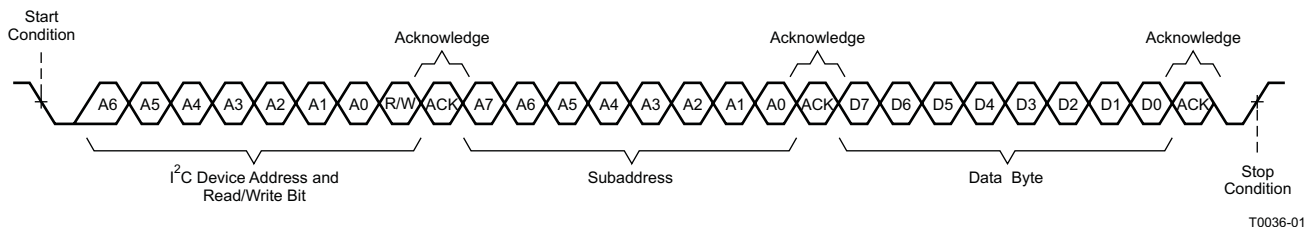


Figure 19. Single-Byte Write Transfer

### 10.3.8.4 Multiple-Byte Write

A multiple-byte data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the master device to the DAP as shown in Figure 20. After receiving each data byte, the TAS5727 responds with an acknowledge bit.

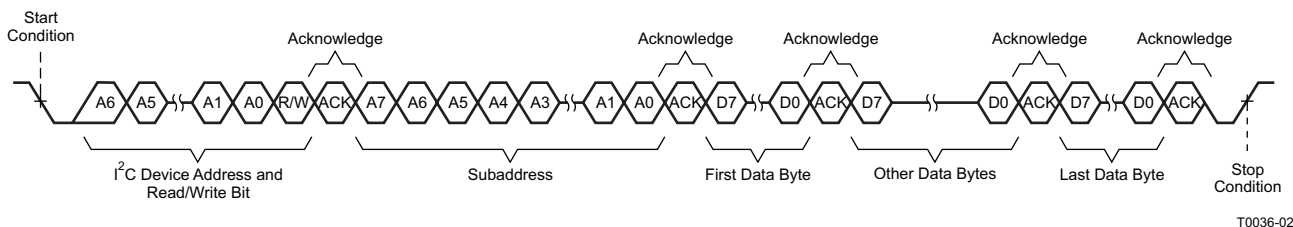


Figure 20. Multiple-Byte Write Transfer

## Feature Description (continued)

### 10.3.8.5 Single-Byte Read

As shown in Figure 21, a single-byte data-read transfer begins with the master device transmitting a start condition, followed by the I<sup>2</sup>C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit becomes a 0. After receiving the TAS5727 address and the read/write bit, TAS5727 responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5727 address and the read/write bit again. This time, the read/write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the TAS5727 again responds with an acknowledge bit. Next, the TAS5727 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

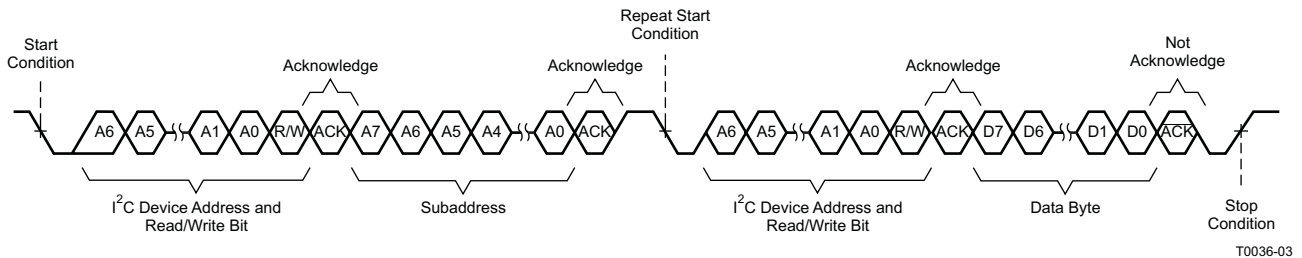


Figure 21. Single-Byte Read Transfer

### 10.3.8.6 Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the TAS5727 to the master device as shown in Figure 22. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

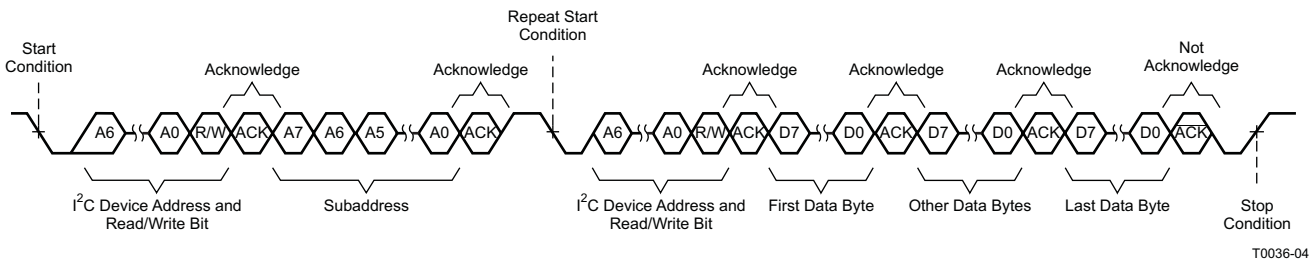


Figure 22. Multiple-Byte Read Transfer

## 10.3.9 Audio Serial Interface

Serial data is input on SDIN. The PWM outputs are derived from SDIN. The TAS5727 DAP accepts serial data in 16-, 20-, or 24-bit left-justified, right-justified, and I<sup>2</sup>S serial data formats.

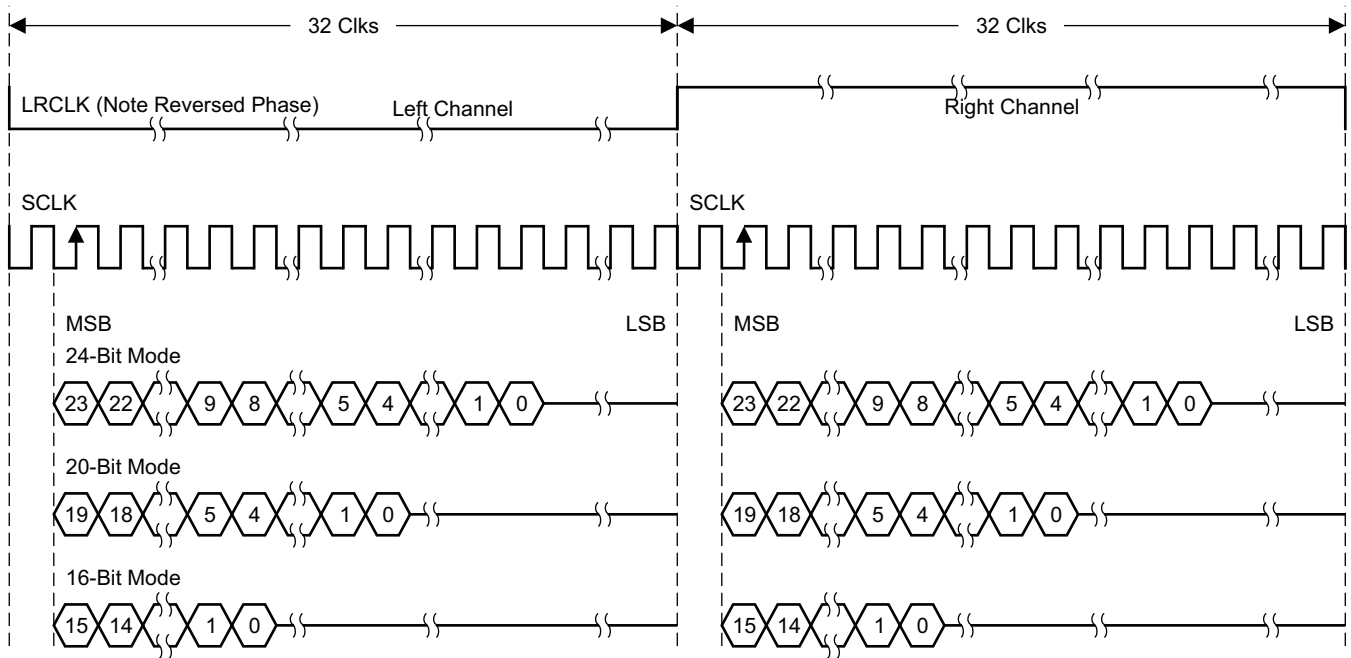
### 10.3.10 Serial Interface Control and Timing

#### 10.3.10.1 I<sup>2</sup>S Timing

I<sup>2</sup>S timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is low for the left channel and high for the right channel. A bit clock running at  $32, 48, \text{ or } 64 \times f_s$  is used to clock in the data. There is a delay of one bit clock from the time the LRCLK signal changes state to the first bit of data on the data lines. The data is written MSB-first and is valid on the rising edge of bit clock. The DAP masks unused trailing data bit positions.

**Feature Description (continued)**

2-Channel I<sup>2</sup>S (Philips Format) Stereo Input



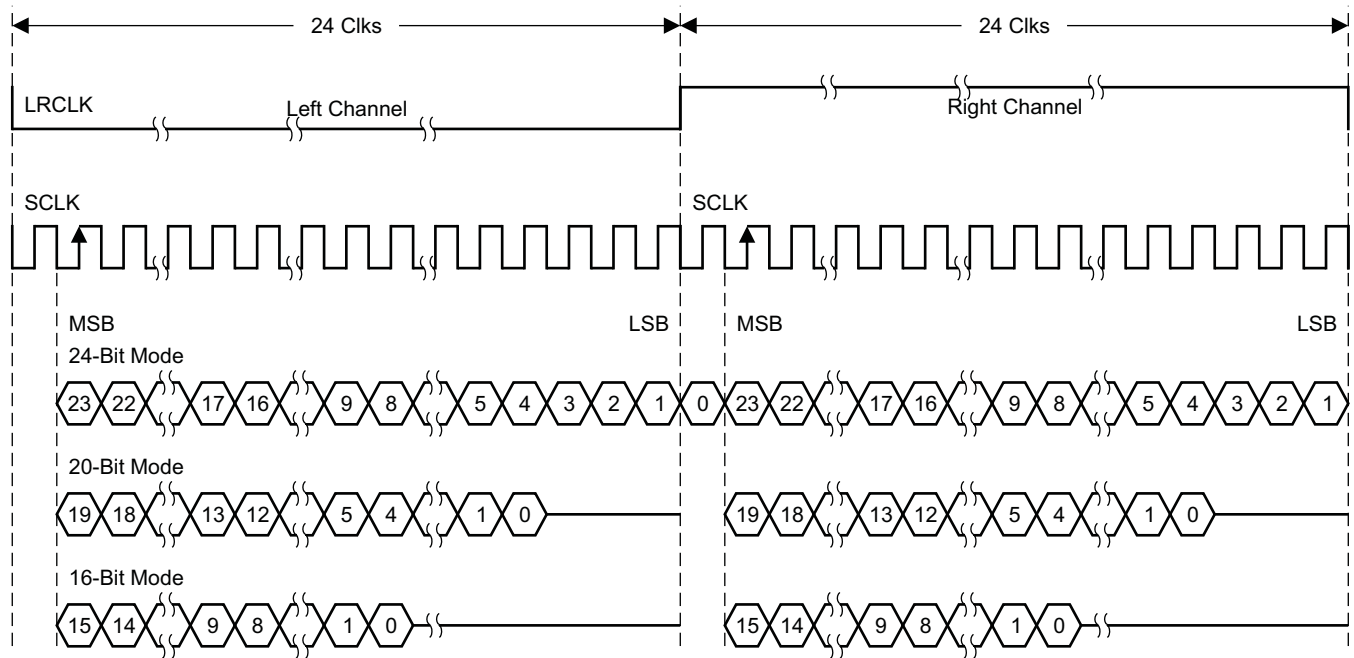
T0034-01

NOTE: All data presented in 2s-complement form with MSB first.

**Figure 23. I<sup>2</sup>S 64-f<sub>s</sub> Format**

**Feature Description (continued)**

2-Channel I<sup>2</sup>S (Philips Format) Stereo Input/Output (24-Bit Transfer Word Size)

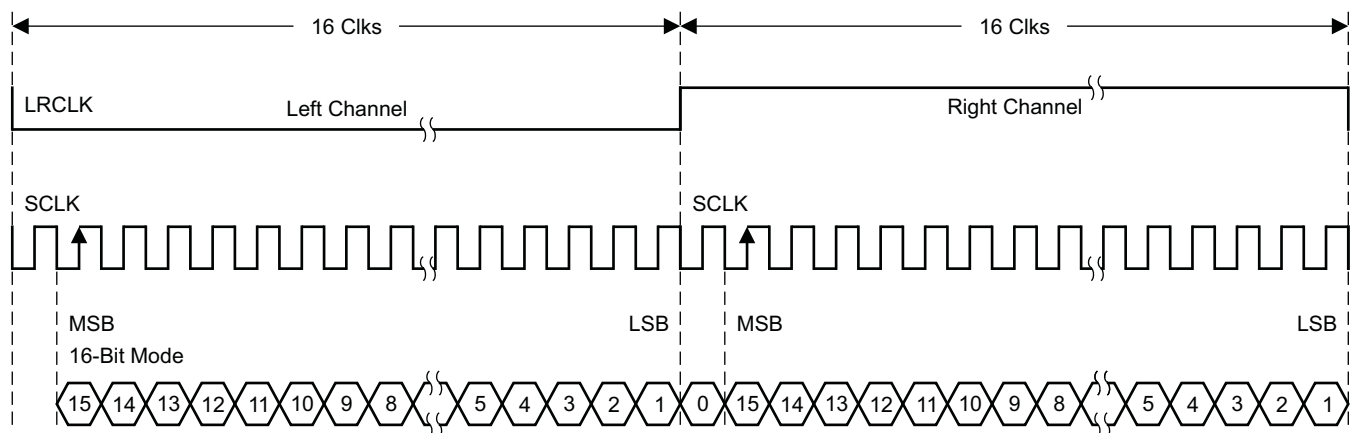


T0092-01

NOTE: All data presented in 2s-complement form with MSB first.

**Figure 24. I<sup>2</sup>S 48-f<sub>s</sub> Format**

2-Channel I<sup>2</sup>S (Philips Format) Stereo Input



T0266-01

NOTE: All data presented in 2s-complement form with MSB first.

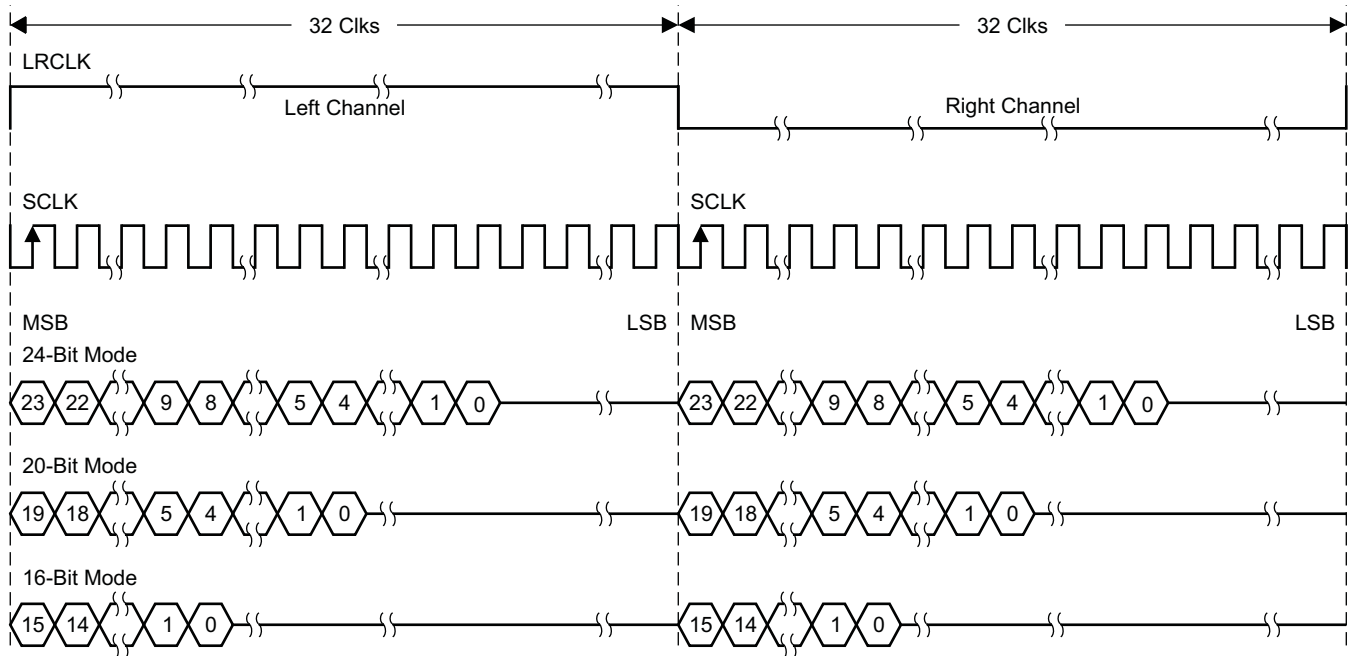
**Figure 25. I<sup>2</sup>S 32-f<sub>s</sub> Format**

**Feature Description (continued)**

**10.3.10.2 Left-Justified**

Left-justified (LJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 32, 48, or 64 × f<sub>s</sub> is used to clock in the data. The first bit of data appears on the data lines at the same time LRCLK toggles. The data is written MSB-first and is valid on the rising edge of the bit clock. The DAP masks unused trailing data bit positions.

2-Channel Left-Justified Stereo Input



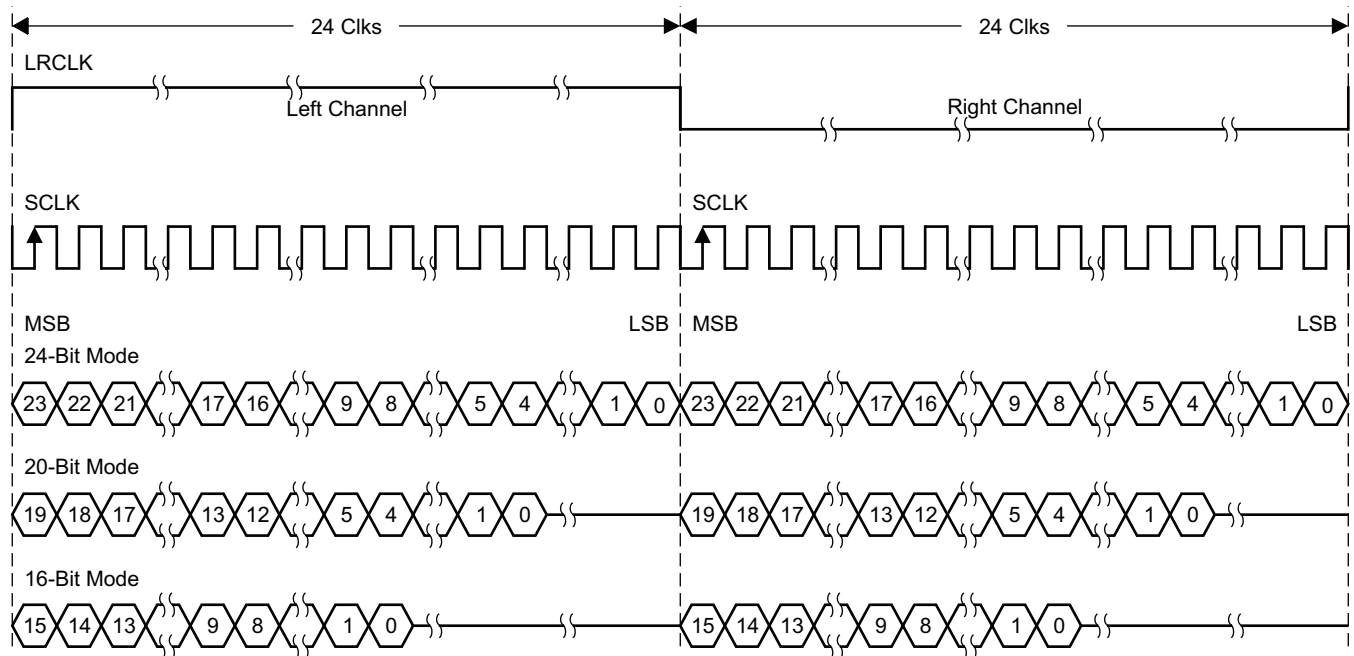
T0034-02

NOTE: All data presented in 2s-complement form with MSB first.

**Figure 26. Left-Justified 64-f<sub>s</sub> Format**

Feature Description (continued)

2-Channel Left-Justified Stereo Input (24-Bit Transfer Word Size)

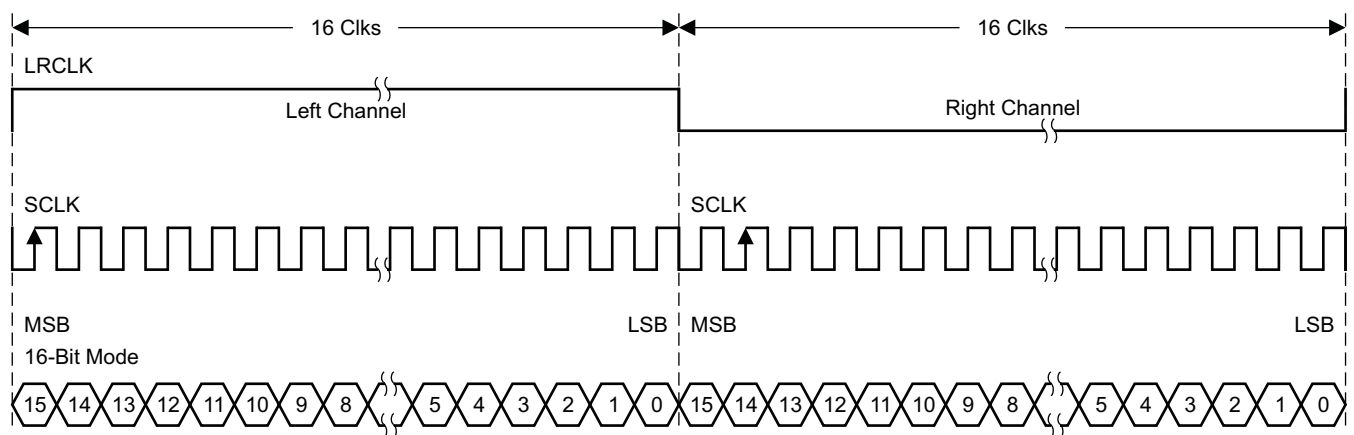


T0092-02

NOTE: All data presented in 2s-complement form with MSB first.

Figure 27. Left-Justified 48-f<sub>s</sub> Format

2-Channel Left-Justified Stereo Input



T0266-02

NOTE: All data presented in 2s-complement form with MSB first.

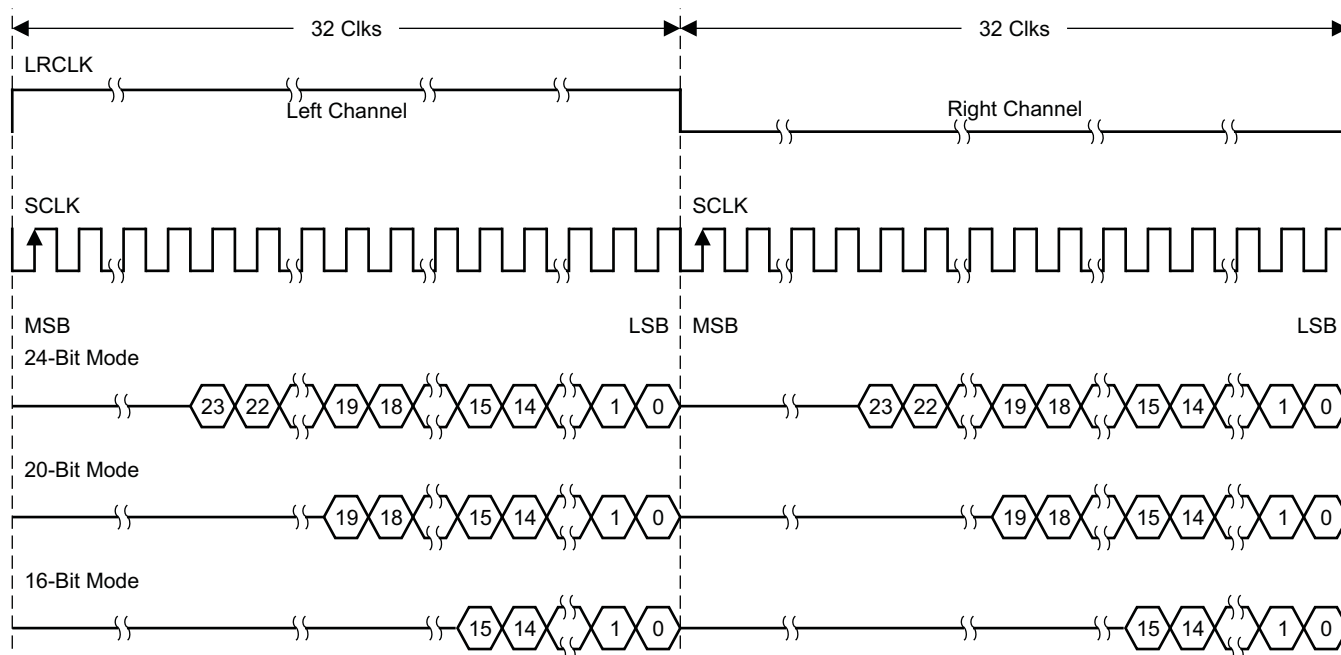
Figure 28. Left-Justified 32-f<sub>s</sub> Format

## Feature Description (continued)

### 10.3.10.3 Right-Justified

Right-justified (RJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at  $32, 48, \text{ or } 64 \times f_s$  is used to clock in the data. The first bit of data appears on the data 8 bit-clock periods (for 24-bit data) after LRCLK toggles. In RJ mode, the LSB of data is always clocked by the last bit clock before LRCLK transitions. The data is written MSB-first and is valid on the rising edge of bit clock. The DAP masks unused leading data bit positions.

2-Channel Right-Justified (Sony Format) Stereo Input



T0034-03

Figure 29. Right-Justified  $64\text{-}f_s$  Format

Feature Description (continued)

2-Channel Right-Justified Stereo Input (24-Bit Transfer Word Size)

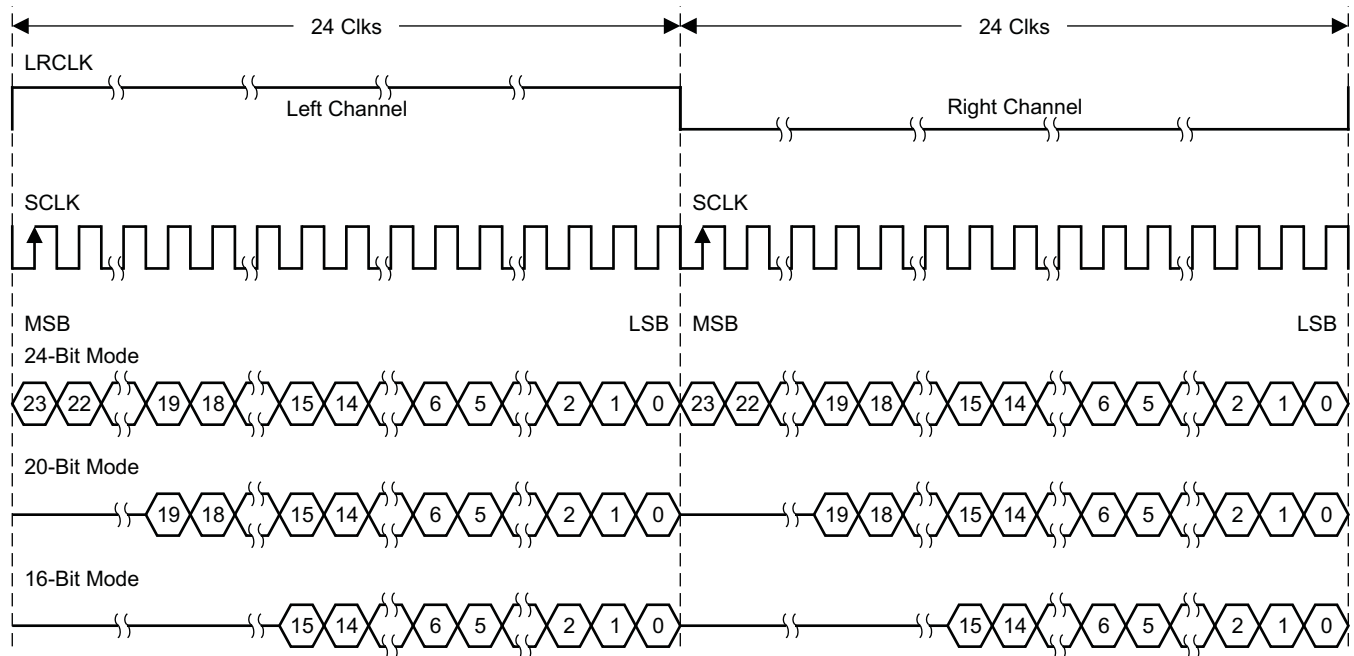


Figure 30. Right-Justified 48-f<sub>s</sub> Format

2-Channel Right-Justified (Sony Format) Stereo Input

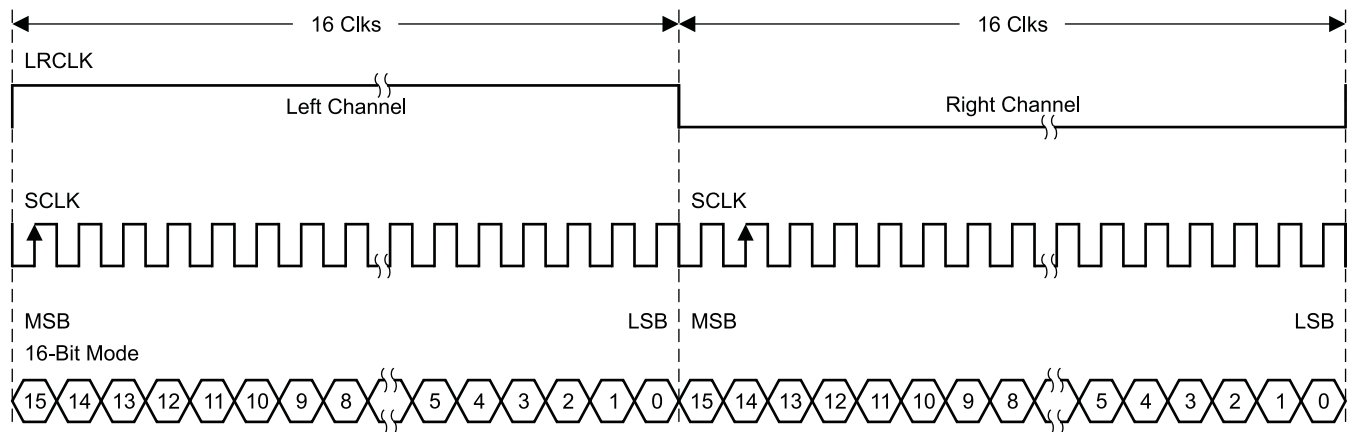


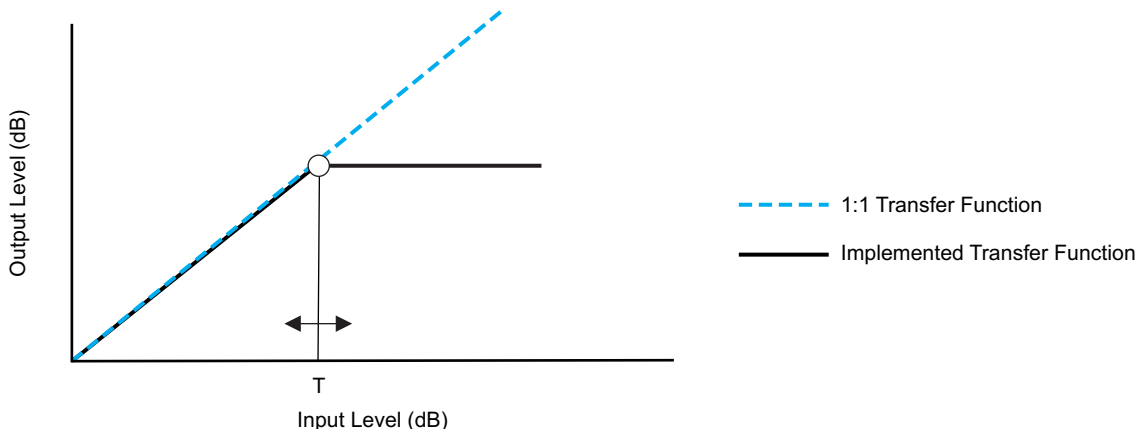
Figure 31. Right-Justified 32-f<sub>s</sub> Format

10.3.11 Dynamic Range Control (DRC)

The DRC scheme has two DRC blocks. There is one ganged DRC for the high-band left and right channels and one DRC for the low-band left and right channels.

The DRC input/output diagram is shown in [Figure 32](#).

Feature Description (continued)



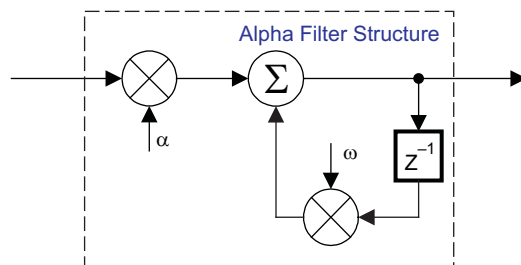
M0091-04

Professional-quality dynamic range compression automatically adjusts volume to flatten volume level.

- Each DRC has adjustable threshold levels.
- Programmable attack and decay time constants
- *Transparent compression*: compressors can attack fast enough to avoid apparent clipping before engaging, and decay times can be set slow enough to avoid pumping.

Figure 32. Dynamic Range Control

|      | $\alpha, \omega$ | T    | $\alpha_a, \omega_a / \alpha_d, \omega_d$ |
|------|------------------|------|-------------------------------------------|
| DRC1 | 0x3C             | 0x3B | 0x40                                      |
| DRC2 | 0x3F             | 0x3E | 0x43                                      |



B0265-04

T = 9.23 format, all other DRC coefficients are 3.23 format

Figure 33. DRC Structure

10.3.12 PWM Level Meter

The structure in Figure 34 shows the PWM level meter that can be used to study the power profile.

Feature Description (continued)

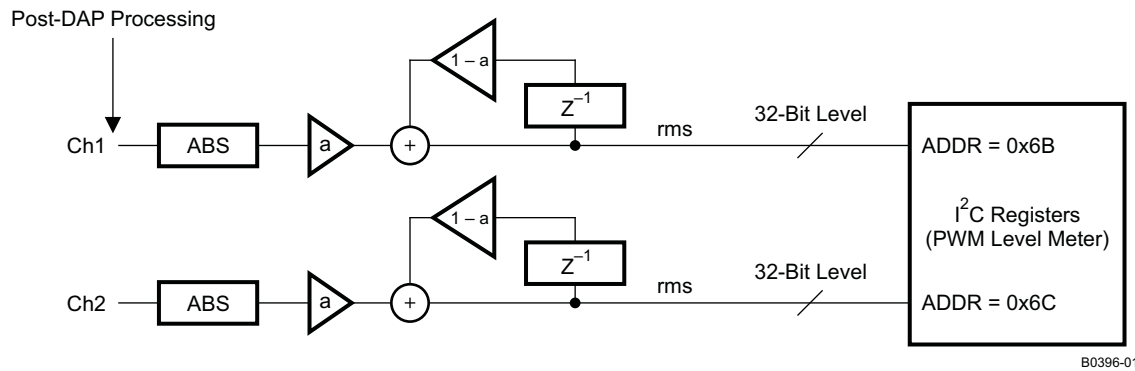


Figure 34. PWM Level Meter Structure

10.4 Device Functional Modes

10.4.1 Stereo BTL Mode

The classic stereo mode of operation uses the TAS5727 device to amplify two independent signals, which represent the left and right portions of a stereo signal. These amplified left and right audio signals are presented on differential output pairs shown as OUT\_A and OUT\_B for a channel and OUT\_C and OUT\_D for the other one. The routing of the audio data which is presented on the OUT\_x outputs can be changed according to the PWM Output Mux Register (0x25). By default, the TAS5727 device is configured to output channel 1 to the OUT\_A and OUT\_B outputs, and channel 2 to the OUT\_C and OUT\_D outputs. Stereo Mode operation outputs are shown in Figure 35.

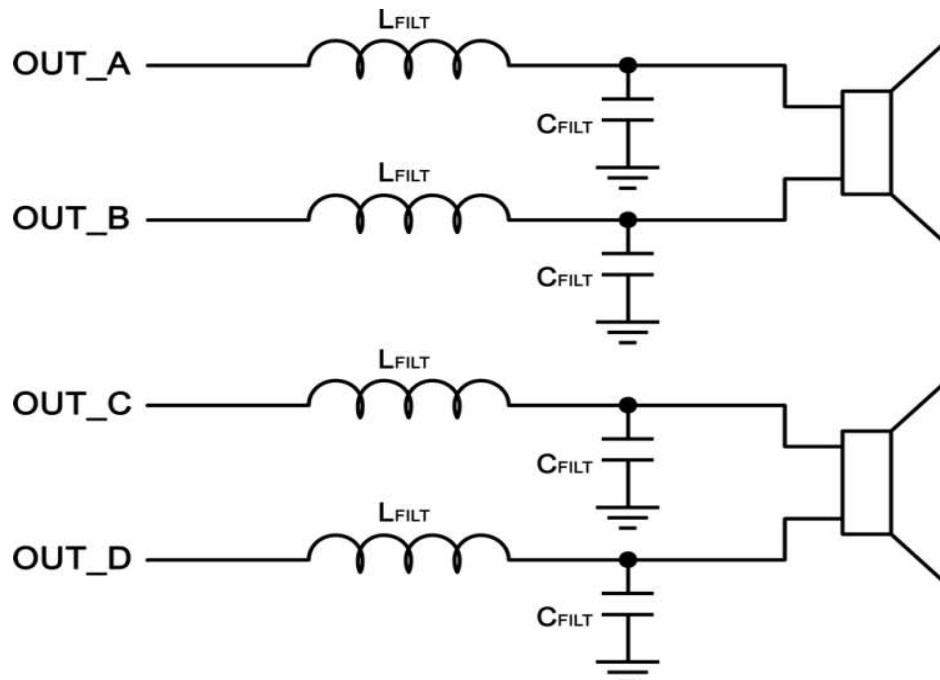


Figure 35. Stereo BTL Mode

## Device Functional Modes (continued)

### 10.4.2 Mono PBTL Mode

When this mode of operation is used, the two stereo outputs of the device are placed in parallel one with another to increase the power sourcing capabilities of the device. The TAS5727 supports parallel BTL (PBTL) mode with OUT\_A/OUT\_B (and OUT\_C/OUT\_D) connected before the LC filter. The merging of the two output channels in this device can be done before the inductor portion of the output filter. This is called *Single-Filter PBTL*, and this mono operation is shown in [Figure 36](#). More information about this can be found in [Single-Filter PBTL Mode](#).

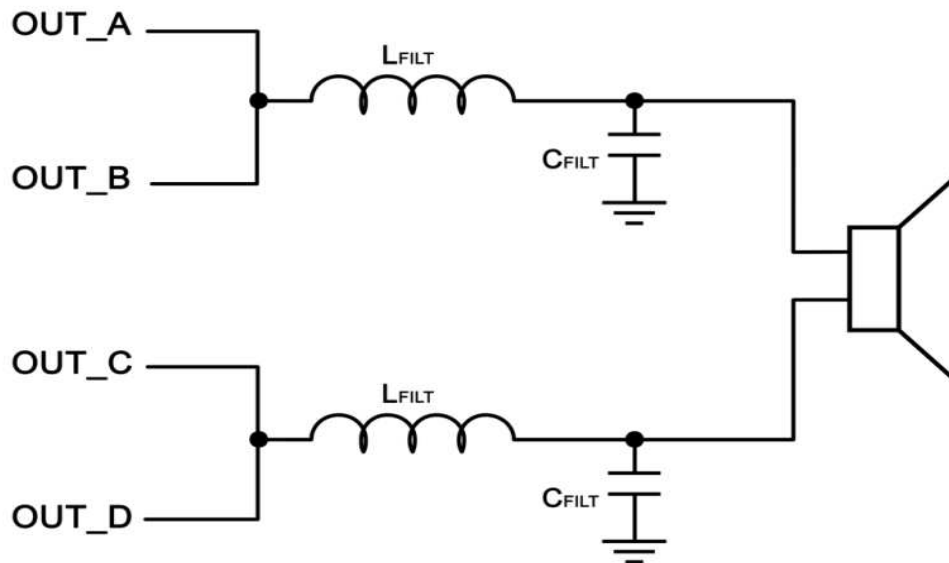


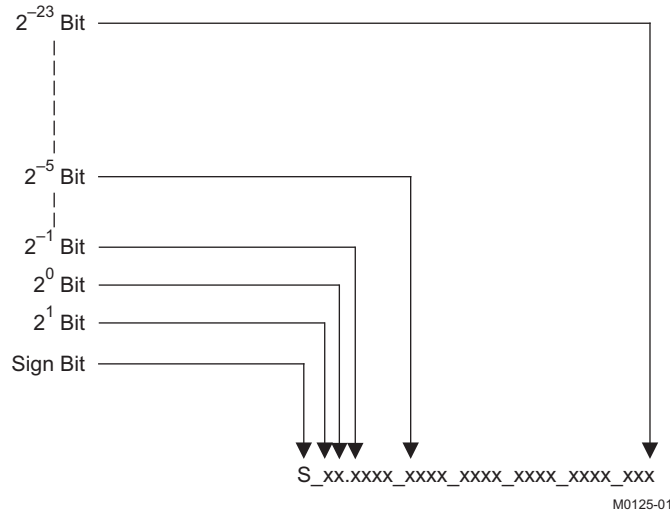
Figure 36. Mono PBTL Mode

## 10.5 Programming

### 10.5.1 26-Bit 3.23 Number Format

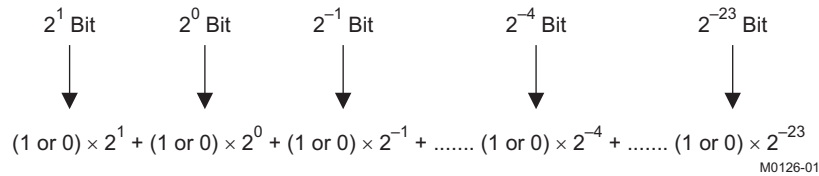
All mixer gain coefficients are 26-bit coefficients using a 3.23 number format. Numbers formatted as 3.23 numbers means that there are 3 bits to the left of the binary point and 23 bits to the right of the binary point (see [Figure 37](#)).

**Programming (continued)**



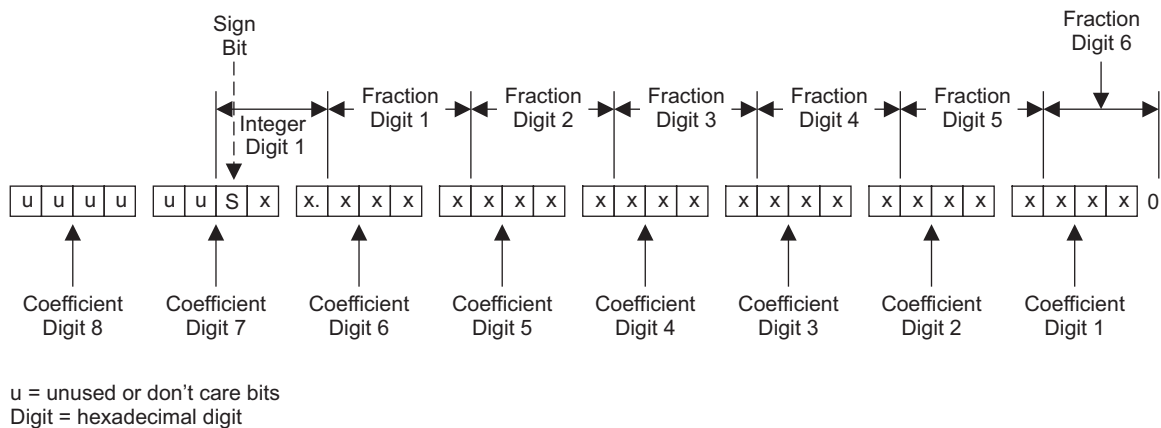
**Figure 37. 3.23 Format**

The decimal value of a 3.23 format number can be found by following the weighting shown in Figure 37. If the most significant bit is logic 0, the number is a positive number, and the weighting shown yields the correct number. If the most significant bit is a logic 1, then the number is a negative number. In this case every bit must be inverted, a 1 added to the result, and then the weighting shown in Figure 38 applied to obtain the magnitude of the negative number.



**Figure 38. Conversion Weighting Factors—3.23 Format to Floating Point**

Gain coefficients, entered through the I<sup>2</sup>C bus, must be entered as 32-bit binary numbers. Figure 39 shows the format of the 32 bit number (4 byte or 8 digit hexadecimal number).



u = unused or don't care bits  
Digit = hexadecimal digit

M0127-01

**Figure 39. Alignment of 3.23 Coefficient in 32-Bit I<sup>2</sup>C Word**

**Table 2. Sample Calculation for 3.23 Format**

| db | LINEAR            | DECIMAL                  | HEX (3.23 FORMAT)          |
|----|-------------------|--------------------------|----------------------------|
| 0  | 1                 | 8,388,608                | 80 0000                    |
| 5  | 1.77              | 14,917,288               | 00E3 9EA8                  |
| -5 | 0.56              | 4,717,260                | 0047 FACC                  |
| X  | $L = 10^{(X/20)}$ | $D = 8,388,608 \times L$ | $H = \text{dec2hex}(D, 8)$ |

**Table 3. Sample Calculation for 9.17 Format**

| db | LINEAR            | DECIMAL                | HEX (9.17 FORMAT)          |
|----|-------------------|------------------------|----------------------------|
| 0  | 1                 | 131,072                | 2 0000                     |
| 5  | 1.77              | 231,997                | 3 8A3D                     |
| -5 | 0.56              | 73,400                 | 1 1EB8                     |
| X  | $L = 10^{(X/20)}$ | $D = 131,072 \times L$ | $H = \text{dec2hex}(D, 8)$ |

## 10.6 Register Maps

**Table 4. Serial Control Interface Register Summary**

| SUBADDRESS | REGISTER NAME                  | NO. OF BYTES | CONTENTS                                | INITIALIZATION VALUE |
|------------|--------------------------------|--------------|-----------------------------------------|----------------------|
|            |                                |              | A u indicates unused bits.              |                      |
| 0x00       | Clock control register         | 1            | Description shown in subsequent section | 0x6C                 |
| 0x01       | Device ID register             | 1            | Description shown in subsequent section | 0x43                 |
| 0x02       | Error status register          | 1            | Description shown in subsequent section | 0x00                 |
| 0x03       | System control register 1      | 1            | Description shown in subsequent section | 0x80                 |
| 0x04       | Serial data interface register | 1            | Description shown in subsequent section | 0x05                 |
| 0x05       | System control register 2      | 1            | Description shown in subsequent section | 0x40                 |
| 0x06       | Soft mute register             | 1            | Description shown in subsequent section | 0x00                 |
| 0x07       | Master volume                  | 2            | Description shown in subsequent section | 0xFF (mute)          |
| 0x08       | Channel 1 vol                  | 2            | Description shown in subsequent section | 0x30 (0 dB)          |
| 0x09       | Channel 2 vol                  | 2            | Description shown in subsequent section | 0x30 (0 dB)          |
| 0x0A       | Channel 3 vol                  | 2            | Description shown in subsequent section | 0x30 (0 dB)          |
| 0x0B–0x0D  |                                | 1            | Reserved <sup>(1)</sup>                 |                      |
| 0x0E       | Volume configuration register  | 1            | Description shown in subsequent section | 0x90                 |
| 0x0F       |                                | 1            | Reserved <sup>(1)</sup>                 |                      |
| 0x10       | Modulation limit register      | 1            | Description shown in subsequent section | 0x02                 |
| 0x11       | IC delay channel 1             | 1            | Description shown in subsequent section | 0xAC                 |
| 0x12       | IC delay channel 2             | 1            | Description shown in subsequent section | 0x54                 |
| 0x13       | IC delay channel 3             | 1            | Description shown in subsequent section | 0xAC                 |
| 0x14       | IC delay channel 4             | 1            | Description shown in subsequent section | 0x54                 |
| 0x15–0x19  |                                | 1            | Reserved <sup>(1)</sup>                 |                      |
| 0x1A       | Start/stop period register     | 1            |                                         | 0x0F                 |
| 0x1B       | Oscillator trim register       | 1            |                                         | 0x82                 |
| 0x1C       | BKND_ERR register              | 1            |                                         | 0x02                 |
| 0x1D–0x1F  |                                | 1            | Reserved <sup>(1)</sup>                 |                      |
| 0x20       | Input MUX register             | 4            | Description shown in subsequent section | 0x0001 7772          |
| 0x21       | Ch 4 source select register    | 4            | Description shown in subsequent section | 0x0000 4303          |
| 0x22–0x24  |                                | 4            | Reserved <sup>(1)</sup>                 |                      |

(1) Reserved registers should not be accessed.

**Register Maps (continued)**
**Table 4. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME    | NO. OF BYTES | CONTENTS                                | INITIALIZATION VALUE |
|------------|------------------|--------------|-----------------------------------------|----------------------|
| 0x25       | PWM MUX register | 4            | Description shown in subsequent section | 0x0102 1345          |
| 0x26       | ch1_bq[0]        | 20           | u[31:26], b0[25:0]                      | 0x0080 0000          |
|            |                  |              | u[31:26], b1[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], b2[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], a1[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], a2[25:0]                      | 0x0000 0000          |
| 0x27       | ch1_bq[1]        | 20           | u[31:26], b0[25:0]                      | 0x0080 0000          |
|            |                  |              | u[31:26], b1[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], b2[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], a1[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], a2[25:0]                      | 0x0000 0000          |
| 0x28       | ch1_bq[2]        | 20           | u[31:26], b0[25:0]                      | 0x0080 0000          |
|            |                  |              | u[31:26], b1[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], b2[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], a1[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], a2[25:0]                      | 0x0000 0000          |
| 0x29       | ch1_bq[3]        | 20           | u[31:26], b0[25:0]                      | 0x0080 0000          |
|            |                  |              | u[31:26], b1[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], b2[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], a1[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], a2[25:0]                      | 0x0000 0000          |
| 0x2A       | ch1_bq[4]        | 20           | u[31:26], b0[25:0]                      | 0x0080 0000          |
|            |                  |              | u[31:26], b1[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], b2[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], a1[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], a2[25:0]                      | 0x0000 0000          |
| 0x2B       | ch1_bq[5]        | 20           | u[31:26], b0[25:0]                      | 0x0080 0000          |
|            |                  |              | u[31:26], b1[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], b2[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], a1[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], a2[25:0]                      | 0x0000 0000          |
| 0x2C       | ch1_bq[6]        | 20           | u[31:26], b0[25:0]                      | 0x0080 0000          |
|            |                  |              | u[31:26], b1[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], b2[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], a1[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], a2[25:0]                      | 0x0000 0000          |
| 0x2D       | ch1_bq[7]        | 20           | u[31:26], b0[25:0]                      | 0x0080 0000          |
|            |                  |              | u[31:26], b1[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], b2[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], a1[25:0]                      | 0x0000 0000          |
|            |                  |              | u[31:26], a2[25:0]                      | 0x0000 0000          |

**Register Maps (continued)**
**Table 4. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS           | INITIALIZATION VALUE |
|------------|---------------|--------------|--------------------|----------------------|
| 0x2E       | ch1_bq[8]     | 20           | u[31:26], b0[25:0] | 0x0080 0000          |
|            |               |              | u[31:26], b1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], b2[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a2[25:0] | 0x0000 0000          |
| 0x2F       | ch1_bq[9]     | 20           | u[31:26], b0[25:0] | 0x0080 0000          |
|            |               |              | u[31:26], b1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], b2[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a2[25:0] | 0x0000 0000          |
| 0x30       | ch2_bq[0]     | 20           | u[31:26], b0[25:0] | 0x0080 0000          |
|            |               |              | u[31:26], b1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], b2[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a2[25:0] | 0x0000 0000          |
| 0x31       | ch2_bq[1]     | 20           | u[31:26], b0[25:0] | 0x0080 0000          |
|            |               |              | u[31:26], b1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], b2[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a2[25:0] | 0x0000 0000          |
| 0x32       | ch2_bq[2]     | 20           | u[31:26], b0[25:0] | 0x0080 0000          |
|            |               |              | u[31:26], b1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], b2[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a2[25:0] | 0x0000 0000          |
| 0x33       | ch2_bq[3]     | 20           | u[31:26], b0[25:0] | 0x0080 0000          |
|            |               |              | u[31:26], b1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], b2[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a2[25:0] | 0x0000 0000          |
| 0x34       | ch2_bq[4]     | 20           | u[31:26], b0[25:0] | 0x0080 0000          |
|            |               |              | u[31:26], b1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], b2[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a2[25:0] | 0x0000 0000          |
| 0x35       | ch2_bq[5]     | 20           | u[31:26], b0[25:0] | 0x0080 0000          |
|            |               |              | u[31:26], b1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], b2[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a2[25:0] | 0x0000 0000          |
| 0x36       | ch2_bq[6]     | 20           | u[31:26], b0[25:0] | 0x0080 0000          |
|            |               |              | u[31:26], b1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], b2[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a2[25:0] | 0x0000 0000          |

**Register Maps (continued)**
**Table 4. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME               | NO. OF BYTES | CONTENTS                | INITIALIZATION VALUE |
|------------|-----------------------------|--------------|-------------------------|----------------------|
| 0x37       | ch2_bq[7]                   | 20           | u[31:26], b0[25:0]      | 0x0080 0000          |
|            |                             |              | u[31:26], b1[25:0]      | 0x0000 0000          |
|            |                             |              | u[31:26], b2[25:0]      | 0x0000 0000          |
|            |                             |              | u[31:26], a1[25:0]      | 0x0000 0000          |
|            |                             |              | u[31:26], a2[25:0]      | 0x0000 0000          |
| 0x38       | ch2_bq[8]                   | 20           | u[31:26], b0[25:0]      | 0x0080 0000          |
|            |                             |              | u[31:26], b1[25:0]      | 0x0000 0000          |
|            |                             |              | u[31:26], b2[25:0]      | 0x0000 0000          |
|            |                             |              | u[31:26], a1[25:0]      | 0x0000 0000          |
|            |                             |              | u[31:26], a2[25:0]      | 0x0000 0000          |
| 0x39       | ch2_bq[9]                   | 20           | u[31:26], b0[25:0]      | 0x0080 0000          |
|            |                             |              | u[31:26], b1[25:0]      | 0x0000 0000          |
|            |                             |              | u[31:26], b2[25:0]      | 0x0000 0000          |
|            |                             |              | u[31:26], a1[25:0]      | 0x0000 0000          |
|            |                             |              | u[31:26], a2[25:0]      | 0x0000 0000          |
| 0x3A       |                             | 4            | Reserved <sup>(1)</sup> |                      |
| 0x3B       | DRC1 softening filter alpha | 8            | u[31:26], ae[25:0]      | 0x0008 0000          |
|            | DRC1 softening filter omega |              | u[31:26], oe[25:0]      | 0x0078 0000          |
| 0x3C       | DRC1 attack rate            | 8            |                         | 0x0000 0100          |
|            | DRC1 release rate           |              |                         | 0xFFFF FF00          |

**Register Maps (continued)**
**Table 4. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME               | NO. OF BYTES | CONTENTS                                | INITIALIZATION VALUE |
|------------|-----------------------------|--------------|-----------------------------------------|----------------------|
| 0x3D       |                             | 8            | Reserved <sup>(1)</sup>                 |                      |
| 0x3E       | DRC2 softening filter alpha | 8            | u[31:26], ae[25:0]                      | 0x0008 0000          |
|            | DRC2 softening filter omega |              | u[31:26], oe[25:0]                      | 0xFFFF 0000          |
| 0x3F       | DRC2 attack rate            | 8            | u[31:26], at[25:0]                      | 0x0008 0000          |
|            | DRC2 release rate           |              | u[31:26], rt[25:0]                      | 0xFFFF 0000          |
| 0x40       | DRC1 attack threshold       | 4            | T1[31:0] (9.23 format)                  | 0x0800 0000          |
| 0x41–0x42  |                             | 4            | Reserved <sup>(1)</sup>                 |                      |
| 0x43       | DRC2 attack threshold       | 4            | T2[31:0] (9.23 format)                  | 0x0074 0000          |
| 0x44–0x45  |                             | 4            | Reserved <sup>(1)</sup>                 |                      |
| 0x46       | DRC control                 | 4            | Description shown in subsequent section | 0x0000 0000          |
| 0x47–0x4E  |                             | 4            | Reserved <sup>(1)</sup>                 |                      |
| 0x4F       | PWM switching rate control  | 4            | u[31:4], src[3:0]                       | 0x0000 0006          |
| 0x50       | Bank switch control         | 4            | Description shown in subsequent section | 0x0F70 8000          |
| 0x51       | Ch 1 output mixer           | 8            | Ch 1 output mix1[1]                     | 0x0080 0000          |
|            |                             |              | Ch 1 output mix1[0]                     | 0x0000 0000          |
| 0x52       | Ch 2 output mixer           | 8            | Ch 2 output mix2[1]                     | 0x0080 0000          |
|            |                             |              | Ch 2 output mix2[0]                     | 0x0000 0000          |
| 0x53       |                             | 16           | Reserved <sup>(1)</sup>                 |                      |
| 0x54       |                             | 16           | Reserved <sup>(1)</sup>                 |                      |
| 0x56       | Output post-scale           | 4            | u[31:26], post[25:0]                    | 0x0080 0000          |
| 0x57       | Output pre-scale            | 4            | u[31:26], pre[25:0] (9.17 format)       | 0x0002 0000          |
| 0x58       | ch1_bq[10]                  | 20           | u[31:26], b0[25:0]                      | 0x0080 0000          |
|            |                             |              | u[31:26], b1[25:0]                      | 0x0000 0000          |
|            |                             |              | u[31:26], b2[25:0]                      | 0x0000 0000          |
|            |                             |              | u[31:26], a1[25:0]                      | 0x0000 0000          |
|            |                             |              | u[31:26], a2[25:0]                      | 0x0000 0000          |
| 0x59       | ch1_bq[11]                  | 20           | u[31:26], b0[25:0]                      | 0x0080 0000          |
|            |                             |              | u[31:26], b1[25:0]                      | 0x0000 0000          |
|            |                             |              | u[31:26], b2[25:0]                      | 0x0000 0000          |
|            |                             |              | u[31:26], a1[25:0]                      | 0x0000 0000          |
|            |                             |              | u[31:26], a2[25:0]                      | 0x0000 0000          |
| 0x5A       | ch4_bq[0]                   | 20           | u[31:26], b0[25:0]                      | 0x0080 0000          |
|            |                             |              | u[31:26], b1[25:0]                      | 0x0000 0000          |
|            |                             |              | u[31:26], b2[25:0]                      | 0x0000 0000          |
|            |                             |              | u[31:26], a1[25:0]                      | 0x0000 0000          |
|            |                             |              | u[31:26], a2[25:0]                      | 0x0000 0000          |
| 0x5B       | ch4_bq[1]                   | 20           | u[31:26], b0[25:0]                      | 0x0080 0000          |
|            |                             |              | u[31:26], b1[25:0]                      | 0x0000 0000          |
|            |                             |              | u[31:26], b2[25:0]                      | 0x0000 0000          |
|            |                             |              | u[31:26], a1[25:0]                      | 0x0000 0000          |
|            |                             |              | u[31:26], a2[25:0]                      | 0x0000 0000          |

**Register Maps (continued)**
**Table 4. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME                 | NO. OF BYTES | CONTENTS                                                 | INITIALIZATION VALUE |
|------------|-------------------------------|--------------|----------------------------------------------------------|----------------------|
| 0x5C       | ch2_bq[10]                    | 20           | u[31:26], b0[25:0]                                       | 0x0080 0000          |
|            |                               |              | u[31:26], b1[25:0]                                       | 0x0000 0000          |
|            |                               |              | u[31:26], b2[25:0]                                       | 0x0000 0000          |
|            |                               |              | u[31:26], a1[25:0]                                       | 0x0000 0000          |
|            |                               |              | u[31:26], a2[25:0]                                       | 0x0000 0000          |
| 0x5D       | ch2_bq[11]                    | 20           | u[31:26], b0[25:0]                                       | 0x0080 0000          |
|            |                               |              | u[31:26], b1[25:0]                                       | 0x0000 0000          |
|            |                               |              | u[31:26], b2[25:0]                                       | 0x0000 0000          |
|            |                               |              | u[31:26], a1[25:0]                                       | 0x0000 0000          |
|            |                               |              | u[31:26], a2[25:0]                                       | 0x0000 0000          |
| 0x5E       | ch3_bq[0]                     | 20           | u[31:26], b0[25:0]                                       | 0x0080 0000          |
|            |                               |              | u[31:26], b1[25:0]                                       | 0x0000 0000          |
|            |                               |              | u[31:26], b2[25:0]                                       | 0x0000 0000          |
|            |                               |              | u[31:26], a1[25:0]                                       | 0x0000 0000          |
|            |                               |              | u[31:26], a2[25:0]                                       | 0x0000 0000          |
| 0x5F       | ch3_bq[1]                     | 20           | u[31:26], b0[25:0]                                       | 0x0080 0000          |
|            |                               |              | u[31:26], b1[25:0]                                       | 0x0000 0000          |
|            |                               |              | u[31:26], b2[25:0]                                       | 0x0000 0000          |
|            |                               |              | u[31:26], a1[25:0]                                       | 0x0000 0000          |
|            |                               |              | u[31:26], a2[25:0]                                       | 0x0000 0000          |
| 0x60–0x61  |                               | 4            | Reserved <sup>(1)</sup>                                  |                      |
| 0x62       | IDF post scale                | 4            |                                                          | 0x0000 0080          |
| 0x63–0x6A  |                               |              | Reserved <sup>(1)</sup>                                  |                      |
| 0x6B       | Left channel PWM level meter  | 4            | Data[31:0]                                               | 0x0000 0000          |
| 0x6C       | Right channel PWM level meter | 4            | Data[31:0]                                               | 0x0000 0000          |
| 0x6D–0x6F  |                               |              | Reserved <sup>(1)</sup>                                  |                      |
| 0x70       | ch1 inline mixer              | 4            | u[31:26], in_mix1[25:0]                                  | 0x0080 0000          |
| 0x71       | inline_DRC_en_mixer_ch1       | 4            | u[31:26], in_mixdrc_1[25:0]                              | 0x0000 0000          |
| 0x72       | ch1 right_channel mixer       | 4            | u[31:26], right_mix1[25:0]                               | 0x0000 0000          |
| 0x73       | ch1 left_channel_mixer        | 4            | u[31:26], left_mix_1[25:0]                               | 0x0080 0000          |
| 0x74       | ch2 inline mixer              | 4            | u[31:26], in_mix2[25:0]                                  | 0x0080 0000          |
| 0x75       | inline_DRC_en_mixer_ch2       | 4            | u[31:26], in_mixdrc_2[25:0]                              | 0x0000 0000          |
| 0x76       | ch2 left_chanel mixer         | 4            | u[31:26], left_mix1[25:0]                                | 0x0000 0000          |
| 0x77       | ch2 right_channel_mixer       | 4            | u[31:26], right_mix_1[25:0]                              | 0x0080 0000          |
| 0x78–0x7F  |                               |              | Reserved <sup>(1)</sup>                                  |                      |
| 0xF8       | Update dev address key        | 4            | Dev Id Update Key[31:0] (Key = 0xF9A5A5A5)               | 0x0000 0000          |
| 0xF9       | Update dev address reg        | 4            | u[31:8], New Dev Id[7:0] (New Dev Id = 0x38 for TAS5727) | 0x0000 0036          |
| 0xFA–0xFF  |                               | 4            | Reserved <sup>(1)</sup>                                  |                      |

All DAP coefficients are 3.23 format unless specified otherwise.

Registers 0x3B through 0x46 should be altered only during the initialization phase.

### 10.6.1 Clock Control Register (0x00)

The clocks and data rates are automatically determined by the TAS5727. The clock control register contains the autodetected clock status. Bits D7–D5 reflect the sample rate. Bits D4–D2 reflect the MCLK frequency.

**Table 5. Clock Control Register (0x00)**

| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                                                               |
|----------|----------|----------|----------|----------|----------|----------|----------|------------------------------------------------------------------------|
| 0        | 0        | 0        | –        | –        | –        | –        | –        | $f_S = 32\text{-kHz}$ sample rate                                      |
| 0        | 0        | 1        | –        | –        | –        | –        | –        | Reserved                                                               |
| 0        | 1        | 0        | –        | –        | –        | –        | –        | Reserved                                                               |
| <b>0</b> | <b>1</b> | <b>1</b> | –        | –        | –        | –        | –        | <b><math>f_S = 44.1/48\text{-kHz}</math> sample rate<sup>(1)</sup></b> |
| 1        | 0        | 0        | –        | –        | –        | –        | –        | $f_S = 16\text{-kHz}$ sample rate                                      |
| 1        | 0        | 1        | –        | –        | –        | –        | –        | $f_S = 22.05/24\text{-kHz}$ sample rate                                |
| 1        | 1        | 0        | –        | –        | –        | –        | –        | $f_S = 8\text{-kHz}$ sample rate                                       |
| 1        | 1        | 1        | –        | –        | –        | –        | –        | $f_S = 11.025/12\text{-kHz}$ sample rate                               |
| –        | –        | –        | 0        | 0        | 0        | –        | –        | MCLK frequency = $64 \times f_S$ <sup>(2)</sup>                        |
| –        | –        | –        | 0        | 0        | 1        | –        | –        | MCLK frequency = $128 \times f_S$ <sup>(2)</sup>                       |
| –        | –        | –        | 0        | 1        | 0        | –        | –        | MCLK frequency = $192 \times f_S$ <sup>(3)</sup>                       |
| –        | –        | –        | <b>0</b> | <b>1</b> | <b>1</b> | –        | –        | <b>MCLK frequency = <math>256 \times f_S</math><sup>(1)(4)</sup></b>   |
| –        | –        | –        | 1        | 0        | 0        | –        | –        | MCLK frequency = $384 \times f_S$                                      |
| –        | –        | –        | 1        | 0        | 1        | –        | –        | MCLK frequency = $512 \times f_S$                                      |
| –        | –        | –        | 1        | 1        | 0        | –        | –        | Reserved                                                               |
| –        | –        | –        | 1        | 1        | 1        | –        | –        | Reserved                                                               |
| –        | –        | –        | –        | –        | –        | <b>0</b> | –        | <b>Reserved<sup>(1)</sup></b>                                          |
| –        | –        | –        | –        | –        | –        | –        | <b>0</b> | <b>Reserved<sup>(1)</sup></b>                                          |

(1) Default values are in **bold**.

(2) Only available for 44.1-kHz and 48-kHz rates

(3) Rate only available for 32/44.1/48-KHz sample rates

(4) Not available at 8 kHz

### 10.6.2 Device Id Register (0x01)

The device ID register contains the ID code for the firmware revision.

**Table 6. General Status Register (0x01)**

| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                                 |
|----------|----------|----------|----------|----------|----------|----------|----------|------------------------------------------|
| <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>Identification code<sup>(1)</sup></b> |

(1) Default values are in **bold**.

### 10.6.3 Error Status Register (0x02)

The error bits are sticky and are not cleared by the hardware. This means that the software must clear the register (write zeroes) and then read them to determine if they are persistent errors.

Error definitions:

- MCLK error: MCLK frequency is changing. The number of MCLKs per LRCLK is changing.
- SCLK error: The number of SCLKs per LRCLK is changing.
- LRCLK error: LRCLK frequency is changing.
- Frame slip: LRCLK phase is drifting with respect to internal frame sync.

**Table 7. Error Status Register (0x02)**

| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                                                         |
|----------|----------|----------|----------|----------|----------|----------|----------|------------------------------------------------------------------|
| 1        | -        | -        | -        | -        | -        | -        | -        | MCLK error                                                       |
| -        | 1        | -        | -        | -        | -        | -        | -        | PLL autolock error                                               |
| -        | -        | 1        | -        | -        | -        | -        | -        | SCLK error                                                       |
| -        | -        | -        | 1        | -        | -        | -        | -        | LRCLK error                                                      |
| -        | -        | -        | -        | 1        | -        | -        | -        | Frame slip                                                       |
| -        | -        | -        | -        | -        | 1        | -        | -        | Clip indicator                                                   |
| -        | -        | -        | -        | -        | -        | 1        | -        | Overcurrent, overtemperature, overvoltage, or undervoltage error |
| 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        | Reserved                                                         |
| <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>No errors</b> <sup>(1)</sup>                                  |

(1) Default values are in **bold**.

### 10.6.4 System Control Register 1 (0x03)

System control register 1 has several functions:

Bit D7: If 0, the DC-blocking filter for each channel is disabled.

If 1, the DC-blocking filter (-3 dB cutoff <1 Hz) for each channel is enabled.

Bit D5: If 0, use soft unmute on recovery from a clock error. This is a slow recovery. Unmute takes the same time as the volume ramp defined in register 0x0E.

If 1, use hard unmute on recovery from clock error. This is a fast recovery, a single-step volume ramp.

Bits D1–D0: Select de-emphasis

**Table 8. System Control Register 1 (0x03)**

| D7 | D6       | D5       | D4 | D3 | D2 | D1 | D0 | FUNCTION                                                       |
|----|----------|----------|----|----|----|----|----|----------------------------------------------------------------|
| 0  | -        | -        | -  | -  | -  | -  | -  | PWM high-pass (dc blocking) disabled                           |
| 1  | -        | -        | -  | -  | -  | -  | -  | <b>PWM high-pass (dc blocking) enabled</b> <sup>(1)</sup>      |
| -  | <b>0</b> | -        | -  | -  | -  | -  | -  | <b>Reserved</b> <sup>(1)</sup>                                 |
| -  | -        | <b>0</b> | -  | -  | -  | -  | -  | <b>Soft unmute on recovery from clock error</b> <sup>(1)</sup> |
| -  | -        | 1        | -  | -  | -  | -  | -  | Hard unmute on recovery from clock error                       |
| -  | -        | -        | 1  | -  | -  | -  | -  | <b>Reserved</b> <sup>(1)</sup>                                 |
| -  | -        | -        | -  | 0  | -  | -  | -  | <b>Reserved</b> <sup>(1)</sup>                                 |
| -  | -        | -        | -  | -  | 0  | -  | -  | <b>Reserved</b> <sup>(1)</sup>                                 |
| -  | -        | -        | -  | -  | -  | 0  | 0  | <b>No de-emphasis</b> <sup>(1)</sup>                           |
| -  | -        | -        | -  | -  | -  | 0  | 1  | De-emphasis for $f_S = 32$ kHz                                 |
| -  | -        | -        | -  | -  | -  | 1  | 0  | De-emphasis for $f_S = 44.1$ kHz                               |
| -  | -        | -        | -  | -  | -  | 1  | 1  | De-emphasis for $f_S = 48$ kHz                                 |

(1) Default values are in **bold**.

### 10.6.5 Serial Data Interface Register (0x04)

As shown in [Table 9](#), the TAS5727 supports nine serial data modes. The default is 24-bit, I<sup>2</sup>S mode.

**Table 9. Serial Data Interface Control Register (0x04) Format**

| RECEIVE SERIAL DATA INTERFACE FORMAT | WORD LENGTH | D7–D4       | D3       | D2       | D1       | D0       |
|--------------------------------------|-------------|-------------|----------|----------|----------|----------|
| Right-justified                      | 16          | 0000        | 0        | 0        | 0        | 0        |
| Right-justified                      | 20          | 0000        | 0        | 0        | 0        | 1        |
| Right-justified                      | 24          | 0000        | 0        | 0        | 1        | 0        |
| I <sup>2</sup> S                     | 16          | 000         | 0        | 0        | 1        | 1        |
| I <sup>2</sup> S                     | 20          | 0000        | 0        | 1        | 0        | 0        |
| <b>I<sup>2</sup>S</b> <sup>(1)</sup> | <b>24</b>   | <b>0000</b> | <b>0</b> | <b>1</b> | <b>0</b> | <b>1</b> |
| Left-justified                       | 16          | 0000        | 0        | 1        | 1        | 0        |
| Left-justified                       | 20          | 0000        | 0        | 1        | 1        | 1        |
| Left-justified                       | 24          | 0000        | 1        | 0        | 0        | 0        |
| Reserved                             |             | 0000        | 1        | 0        | 0        | 1        |
| Reserved                             |             | 0000        | 1        | 0        | 1        | 0        |
| Reserved                             |             | 0000        | 1        | 0        | 1        | 1        |
| Reserved                             |             | 0000        | 1        | 1        | 0        | 0        |
| Reserved                             |             | 0000        | 1        | 1        | 0        | 1        |
| Reserved                             |             | 0000        | 1        | 1        | 1        | 0        |
| Reserved                             |             | 0000        | 1        | 1        | 1        | 1        |

(1) Default values are in **bold**.

### 10.6.6 System Control Register 2 (0x05)

When bit D6 is set low, the system exits all-channel shutdown and starts playing audio; otherwise, the outputs are shut down (hard mute).

**Table 10. System Control Register 2 (0x05)**

| D7       | D6       | D5       | D4       | D3       | D2       | D1 | D0       | FUNCTION                                                         |
|----------|----------|----------|----------|----------|----------|----|----------|------------------------------------------------------------------|
| <b>0</b> | –        | –        | –        | –        | –        | –  | –        | <b>Mid-Z ramp disabled</b> <sup>(1)</sup>                        |
| 1        | –        | –        | –        | –        | –        | –  | –        | Mid-Z ramp enabled                                               |
| –        | <b>0</b> | –        | –        | –        | –        | –  | –        | Exit all-channel shutdown (normal operation)                     |
| –        | <b>1</b> | –        | –        | –        | –        | –  | –        | <b>Enter all-channel shutdown (hard mute)</b> <sup>(1)</sup>     |
| –        | –        | <b>0</b> | <b>0</b> | –        | –        | –  | –        | <b>Reserved</b> <sup>(1)</sup>                                   |
| –        | –        | –        | –        | <b>0</b> | –        | –  | –        | <b>Ternary modulation disabled</b> <sup>(1)</sup>                |
| –        | –        | –        | –        | 1        | –        | –  | –        | Ternary modulation enabled                                       |
| –        | –        | –        | –        | –        | <b>0</b> | –  | –        | <b>Reserved</b> <sup>(1)</sup>                                   |
| –        | –        | –        | –        | –        | –        | 0  | –        | A_SEL_FAULT configured as input                                  |
| –        | –        | –        | –        | –        | –        | 1  | –        | A_SEL_FAULT configured as output to function as A_SEL_FAULT pin. |
| –        | –        | –        | –        | –        | –        | –  | <b>0</b> | <b>Reserved</b> <sup>(1)</sup>                                   |

(1) Default values are in **bold**.

Ternary modulation is disabled by default. To enable ternary modulation, the following writes are required before bringing the system out of shutdown:

1. Set bit D3 of register 0x05 to 1.
2. Write the following ICD settings:
  - (a) 0x11= 80
  - (b) 0x12= 7C
  - (c) 0x13= 80
  - (d) 0x24 =7C
3. Set the input mux register as follows:
  - (a) 0x20 = 00 89 77 72

### 10.6.7 Soft Mute Register (0x06)

Writing a 1 to any of the following bits sets the output of the respective channel to 50% duty cycle (soft mute).

**Table 11. Soft Mute Register (0x06)**

| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                                    |
|----------|----------|----------|----------|----------|----------|----------|----------|---------------------------------------------|
| <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | –        | –        | –        | <b>Reserved</b> <sup>(1)</sup>              |
| –        | –        | –        | –        | –        | 1        | –        | –        | Soft mute channel 3                         |
| –        | –        | –        | –        | –        | <b>0</b> | –        | –        | <b>Soft unmute channel 3</b> <sup>(1)</sup> |
| –        | –        | –        | –        | –        | –        | 1        | –        | Soft mute channel 2                         |
| –        | –        | –        | –        | –        | –        | <b>0</b> | –        | <b>Soft unmute channel 2</b> <sup>(1)</sup> |
| –        | –        | –        | –        | –        | –        | –        | 1        | Soft mute channel 1                         |
| –        | –        | –        | –        | –        | –        | –        | <b>0</b> | <b>Soft unmute channel 1</b> <sup>(1)</sup> |

(1) Default values are in **bold**.

### 10.6.8 Volume Registers (0x07, 0x08, 0x09)

Step size is 0.125 dB and volume registers are 2 bytes.

- Master volume – 0x07 (default is mute)
- Channel-1 volume – 0x08 (default is 0 dB)
- Channel-2 volume – 0x09 (default is 0 dB)

**Table 12. Master Volume Table**

| VALUE  | LEVEL  | VALUE  | LEVEL  | VALUE  | LEVEL  | VALUE  | LEVEL | VALUE  | LEVEL  | VALUE  | LEVEL  |
|--------|--------|--------|--------|--------|--------|--------|-------|--------|--------|--------|--------|
| 0x0000 | 24.000 | 0x0027 | 19.250 | 0x004E | 14.250 | 0x0075 | 9.375 | 0x009C | 4.500  | 0x00C3 | -0.375 |
| 0x0001 | 23.875 | 0x0028 | 19.000 | 0x004F | 14.125 | 0x0076 | 9.250 | 0x009D | 4.375  | 0x00C4 | -0.500 |
| 0x0002 | 23.750 | 0x0029 | 18.875 | 0x0050 | 14.000 | 0x0077 | 9.125 | 0x009E | 4.250  | 0x00C5 | -0.625 |
| 0x0003 | 23.625 | 0x002A | 18.750 | 0x0051 | 13.875 | 0x0078 | 9.000 | 0x009F | 4.125  | 0x00C6 | -0.750 |
| 0x0004 | 23.500 | 0x002B | 18.625 | 0x0052 | 13.750 | 0x0079 | 8.875 | 0x00A0 | 4.000  | 0x00C7 | -0.875 |
| 0x0005 | 23.375 | 0x002C | 18.500 | 0x0053 | 13.625 | 0x007A | 8.750 | 0x00A1 | 3.875  | 0x00C8 | -1.000 |
| 0x0006 | 23.250 | 0x002D | 18.375 | 0x0054 | 13.500 | 0x007B | 8.625 | 0x00A2 | 3.750  | 0x00C9 | -1.125 |
| 0x0007 | 23.125 | 0x002E | 18.250 | 0x0055 | 13.375 | 0x007C | 8.500 | 0x00A3 | 3.625  | 0x00CA | -1.250 |
| 0x0008 | 23.000 | 0x002F | 18.125 | 0x0056 | 13.250 | 0x007D | 8.375 | 0x00A4 | 3.500  | 0x00CB | -1.375 |
| 0x0009 | 22.875 | 0x0030 | 18.000 | 0x0057 | 13.125 | 0x007E | 8.250 | 0x00A5 | 3.375  | 0x00CC | -1.500 |
| 0x000A | 22.750 | 0x0031 | 17.875 | 0x0058 | 13.000 | 0x007F | 8.125 | 0x00A6 | 3.250  | 0x00CD | -1.625 |
| 0x000B | 22.625 | 0x0032 | 17.750 | 0x0059 | 12.875 | 0x0080 | 8.000 | 0x00A7 | 3.125  | 0x00CE | -1.750 |
| 0x000C | 22.500 | 0x0033 | 17.625 | 0x005A | 12.750 | 0x0081 | 7.875 | 0x00A8 | 3.000  | 0x00CF | -1.875 |
| 0x000D | 22.375 | 0x0034 | 17.500 | 0x005B | 12.625 | 0x0082 | 7.750 | 0x00A9 | 2.875  | 0x00D0 | -2.000 |
| 0x000E | 22.250 | 0x0035 | 17.375 | 0x005C | 12.500 | 0x0083 | 7.625 | 0x00AA | 2.750  | 0x00D1 | -2.125 |
| 0x000F | 22.125 | 0x0036 | 17.250 | 0x005D | 12.375 | 0x0084 | 7.500 | 0x00AB | 2.625  | 0x00D2 | -2.250 |
| 0x0010 | 22.000 | 0x0037 | 17.125 | 0x005E | 12.250 | 0x0085 | 7.375 | 0x00AC | 2.500  | 0x00D3 | -2.375 |
| 0x0011 | 21.875 | 0x0038 | 17.000 | 0x005F | 12.125 | 0x0086 | 7.250 | 0x00AD | 2.375  | 0x00D4 | -2.500 |
| 0x0012 | 21.750 | 0x0039 | 16.875 | 0x0060 | 12.000 | 0x0087 | 7.125 | 0x00AE | 2.250  | 0x00D5 | -2.625 |
| 0x0013 | 21.625 | 0x003A | 16.750 | 0x0061 | 11.875 | 0x0088 | 7.000 | 0x00AF | 2.125  | 0x00D6 | -2.750 |
| 0x0014 | 21.500 | 0x003B | 16.625 | 0x0062 | 11.750 | 0x0089 | 6.875 | 0x00B0 | 2.000  | 0x00D7 | -2.875 |
| 0x0015 | 21.375 | 0x003C | 16.500 | 0x0063 | 11.625 | 0x008A | 6.750 | 0x00B1 | 1.875  | 0x00D8 | -3.000 |
| 0x0016 | 21.250 | 0x003D | 16.375 | 0x0064 | 11.500 | 0x008B | 6.625 | 0x00B2 | 1.750  | 0x00D9 | -3.125 |
| 0x0017 | 21.125 | 0x003E | 16.250 | 0x0065 | 11.375 | 0x008C | 6.500 | 0x00B3 | 1.625  | 0x00DA | -3.250 |
| 0x0018 | 21.000 | 0x003F | 16.125 | 0x0066 | 11.250 | 0x008D | 6.375 | 0x00B4 | 1.500  | 0x00DB | -3.375 |
| 0x0019 | 20.875 | 0x0040 | 16.000 | 0x0067 | 11.125 | 0x008E | 6.250 | 0x00B5 | 1.375  | 0x00DC | -3.500 |
| 0x001A | 20.750 | 0x0041 | 15.875 | 0x0068 | 11.000 | 0x008F | 6.125 | 0x00B6 | 1.250  | 0x00DD | -3.625 |
| 0x001B | 20.625 | 0x0042 | 15.750 | 0x0069 | 10.875 | 0x0090 | 6.000 | 0x00B7 | 1.125  | 0x00DE | -3.750 |
| 0x001C | 20.500 | 0x0043 | 15.625 | 0x006A | 10.750 | 0x0091 | 5.875 | 0x00B8 | 1.000  | 0x00DF | -3.875 |
| 0x001D | 20.375 | 0x0044 | 15.500 | 0x006B | 10.625 | 0x0092 | 5.750 | 0x00B9 | 0.875  | 0x00E0 | -4.000 |
| 0x001E | 20.250 | 0x0045 | 15.375 | 0x006C | 10.500 | 0x0093 | 5.625 | 0x00BA | 0.750  | 0x00E1 | -4.125 |
| 0x001F | 20.125 | 0x0046 | 15.250 | 0x006D | 10.375 | 0x0094 | 5.500 | 0x00BB | 0.625  | 0x00E2 | -4.250 |
| 0x0020 | 20.000 | 0x0047 | 15.125 | 0x006E | 10.250 | 0x0095 | 5.375 | 0x00BC | 0.500  | 0x00E3 | -4.375 |
| 0x0021 | 19.875 | 0x0048 | 15.000 | 0x006F | 10.125 | 0x0096 | 5.250 | 0x00BD | 0.375  | 0x00E4 | -4.500 |
| 0x0022 | 19.750 | 0x0049 | 14.875 | 0x0070 | 10.000 | 0x0097 | 5.125 | 0x00BE | 0.250  | 0x00E5 | -4.625 |
| 0x0023 | 19.625 | 0x004A | 14.750 | 0x0071 | 9.875  | 0x0098 | 5.000 | 0x00BF | 0.125  | 0x00E6 | -4.750 |
| 0x0024 | 19.500 | 0x004B | 14.625 | 0x0072 | 9.750  | 0x0099 | 4.875 | 0x00C0 | 0.000  | 0x00E7 | -4.875 |
| 0x0025 | 19.375 | 0x004C | 14.500 | 0x0073 | 9.625  | 0x009A | 4.750 | 0x00C1 | -0.125 | 0x00E8 | -5.000 |
| 0x0026 | 19.125 | 0x004D | 14.375 | 0x0074 | 9.500  | 0x009B | 4.625 | 0x00C2 | -0.250 | 0x00E9 | -5.125 |

**Table 12. Master Volume Table (continued)**

| VALUE  | LEVEL   | VALUE  | LEVEL   | VALUE  | LEVEL   | VALUE  | LEVEL   | VALUE  | LEVEL   | VALUE  | LEVEL   |
|--------|---------|--------|---------|--------|---------|--------|---------|--------|---------|--------|---------|
| 0x00EA | -5.250  | 0x0119 | -11.125 | 0x0148 | -17.000 | 0x0177 | -22.875 | 0x01A6 | -28.750 | 0x01D5 | -34.625 |
| 0x00EB | -5.375  | 0x011A | -11.250 | 0x0149 | -17.125 | 0x0178 | -23.000 | 0x01A7 | -28.875 | 0x01D6 | -34.750 |
| 0x00EC | -5.500  | 0x011B | -11.375 | 0x014A | -17.250 | 0x0179 | -23.125 | 0x01A8 | -29.000 | 0x01D7 | -34.875 |
| 0x00ED | -5.625  | 0x011C | -11.500 | 0x014B | -17.375 | 0x017A | -23.250 | 0x01A9 | -29.125 | 0x01D8 | -35.000 |
| 0x00EE | -5.750  | 0x011D | -11.625 | 0x014C | -17.500 | 0x017B | -23.375 | 0x01AA | -29.250 | 0x01D9 | -35.125 |
| 0x00EF | -5.875  | 0x011E | -11.750 | 0x014D | -17.625 | 0x017C | -23.500 | 0x01AB | -29.375 | 0x01DA | -35.250 |
| 0x00F0 | -6.000  | 0x011F | -11.875 | 0x014E | -17.750 | 0x017D | -23.625 | 0x01AC | -29.500 | 0x01DB | -35.375 |
| 0x00F1 | -6.125  | 0x0120 | -12.000 | 0x014F | -17.875 | 0x017E | -23.750 | 0x01AD | -29.625 | 0x01DC | -35.500 |
| 0x00F2 | -6.250  | 0x0121 | -12.125 | 0x0150 | -18.000 | 0x017F | -23.875 | 0x01AE | -29.750 | 0x01DD | -35.625 |
| 0x00F3 | -6.375  | 0x0122 | -12.250 | 0x0151 | -18.125 | 0x0180 | -24.000 | 0x01AF | -29.875 | 0x01DE | -35.750 |
| 0x00F4 | -6.500  | 0x0123 | -12.375 | 0x0152 | -18.250 | 0x0181 | -24.125 | 0x01B0 | -30.000 | 0x01DF | -35.875 |
| 0x00F5 | -6.625  | 0x0124 | -12.500 | 0x0153 | -18.375 | 0x0182 | -24.250 | 0x01B1 | -30.125 | 0x01E0 | -36.000 |
| 0x00F6 | -6.750  | 0x0125 | -12.625 | 0x0154 | -18.500 | 0x0183 | -24.375 | 0x01B2 | -30.250 | 0x01E1 | -36.125 |
| 0x00F7 | -6.875  | 0x0126 | -12.750 | 0x0155 | -18.625 | 0x0184 | -24.500 | 0x01B3 | -30.375 | 0x01E2 | -36.250 |
| 0x00F8 | -7.000  | 0x0127 | -12.875 | 0x0156 | -18.750 | 0x0185 | -24.625 | 0x01B4 | -30.500 | 0x01E3 | -36.375 |
| 0x00F9 | -7.125  | 0x0128 | -13.000 | 0x0157 | -18.875 | 0x0186 | -24.750 | 0x01B5 | -30.625 | 0x01E4 | -36.500 |
| 0x00FA | -7.250  | 0x0129 | -13.125 | 0x0158 | -19.000 | 0x0187 | -24.875 | 0x01B6 | -30.750 | 0x01E5 | -36.625 |
| 0x00FB | -7.375  | 0x012A | -13.250 | 0x0159 | -19.125 | 0x0188 | -25.000 | 0x01B7 | -30.875 | 0x01E6 | -36.750 |
| 0x00FC | -7.500  | 0x012B | -13.375 | 0x015A | -19.250 | 0x0189 | -25.125 | 0x01B8 | -31.000 | 0x01E7 | -36.875 |
| 0x00FD | -7.625  | 0x012C | -13.500 | 0x015B | -19.375 | 0x018A | -25.250 | 0x01B9 | -31.125 | 0x01E8 | -37.000 |
| 0x00FE | -7.750  | 0x012D | -13.625 | 0x015C | -19.500 | 0x018B | -25.375 | 0x01BA | -31.250 | 0x01E9 | -37.125 |
| 0x00FF | -7.875  | 0x012E | -13.750 | 0x015D | -19.625 | 0x018C | -25.500 | 0x01BB | -31.375 | 0x01EA | -37.250 |
| 0x0100 | -8.000  | 0x012F | -13.875 | 0x015E | -19.750 | 0x018D | -25.625 | 0x01BC | -31.500 | 0x01EB | -37.375 |
| 0x0101 | -8.125  | 0x0130 | -14.000 | 0x015F | -20.875 | 0x018E | -25.750 | 0x01BD | -31.625 | 0x01EC | -37.500 |
| 0x0102 | -8.250  | 0x0131 | -14.125 | 0x0160 | -20.000 | 0x018F | -25.875 | 0x01BE | -31.750 | 0x01ED | -37.625 |
| 0x0103 | -8.375  | 0x0132 | -14.250 | 0x0161 | -20.125 | 0x0190 | -26.000 | 0x01BF | -31.875 | 0x01EE | -37.750 |
| 0x0104 | -8.500  | 0x0133 | -14.375 | 0x0162 | -20.250 | 0x0191 | -26.125 | 0x01C0 | -32.000 | 0x01EF | -37.875 |
| 0x0105 | -8.625  | 0x0134 | -14.500 | 0x0163 | -20.375 | 0x0192 | -26.250 | 0x01C1 | -32.125 | 0x01F0 | -38.000 |
| 0x0106 | -8.750  | 0x0135 | -14.625 | 0x0164 | -20.500 | 0x0193 | -26.375 | 0x01C2 | -32.250 | 0x01F1 | -38.125 |
| 0x0107 | -8.875  | 0x0136 | -14.750 | 0x0165 | -20.625 | 0x0194 | -26.500 | 0x01C3 | -32.375 | 0x01F2 | -38.250 |
| 0x0108 | -9.000  | 0x0137 | -14.875 | 0x0166 | -20.750 | 0x0195 | -26.625 | 0x01C4 | -32.500 | 0x01F3 | -38.375 |
| 0x0109 | -9.125  | 0x0138 | -15.000 | 0x0167 | -20.875 | 0x0196 | -26.750 | 0x01C5 | -32.625 | 0x01F4 | -38.500 |
| 0x010A | -9.250  | 0x0139 | -15.125 | 0x0168 | -21.000 | 0x0197 | -26.875 | 0x01C6 | -32.750 | 0x01F5 | -38.625 |
| 0x010B | -9.375  | 0x013A | -15.250 | 0x0169 | -21.125 | 0x0198 | -27.000 | 0x01C7 | -32.875 | 0x01F6 | -38.750 |
| 0x010C | -9.500  | 0x013B | -15.375 | 0x016A | -21.250 | 0x0199 | -27.125 | 0x01C8 | -33.000 | 0x01F7 | -38.875 |
| 0x010D | -9.625  | 0x013C | -15.500 | 0x016B | -21.375 | 0x019A | -27.250 | 0x01C9 | -33.125 | 0x01F8 | -39.000 |
| 0x010E | -9.750  | 0x013D | -15.625 | 0x016C | -21.500 | 0x019B | -27.375 | 0x01CA | -33.250 | 0x01F9 | -39.125 |
| 0x010F | -9.875  | 0x013E | -15.750 | 0x016D | -21.625 | 0x019C | -27.500 | 0x01CB | -33.375 | 0x01FA | -39.250 |
| 0x0110 | -10.000 | 0x013F | -15.875 | 0x016E | -21.750 | 0x019D | -27.625 | 0x01CC | -33.500 | 0x01FB | -39.375 |
| 0x0111 | -10.125 | 0x0140 | -16.000 | 0x016F | -21.875 | 0x019E | -27.750 | 0x01CD | -33.625 | 0x01FC | -39.500 |
| 0x0112 | -10.250 | 0x0141 | -16.125 | 0x0170 | -22.000 | 0x019F | -27.875 | 0x01CE | -33.750 | 0x01FD | -39.625 |
| 0x0113 | -10.375 | 0x0142 | -16.250 | 0x0171 | -22.125 | 0x01A0 | -28.000 | 0x01CF | -33.875 | 0x01FE | -39.750 |
| 0x0114 | -10.500 | 0x0143 | -16.375 | 0x0172 | -22.250 | 0x01A1 | -28.125 | 0x01D0 | -34.000 | 0x01FF | -39.875 |
| 0x0115 | -10.625 | 0x0144 | -16.500 | 0x0173 | -22.375 | 0x01A2 | -28.250 | 0x01D1 | -34.125 | 0x0200 | -40.000 |
| 0x0116 | -10.750 | 0x0145 | -16.625 | 0x0174 | -22.500 | 0x01A3 | -28.375 | 0x01D2 | -34.250 | 0x0201 | -40.125 |
| 0x0117 | -10.875 | 0x0146 | -16.750 | 0x0175 | -22.625 | 0x01A4 | -28.500 | 0x01D3 | -34.375 | 0x0202 | -40.250 |
| 0x0118 | -11.000 | 0x0147 | -16.875 | 0x0176 | -22.750 | 0x01A5 | -28.625 | 0x01D4 | -34.500 | 0x0203 | -40.375 |

**Table 12. Master Volume Table (continued)**

| VALUE  | LEVEL   | VALUE  | LEVEL   | VALUE  | LEVEL   | VALUE  | LEVEL   | VALUE  | LEVEL   | VALUE  | LEVEL   |
|--------|---------|--------|---------|--------|---------|--------|---------|--------|---------|--------|---------|
| 0x0204 | -40.500 | 0x0233 | -46.375 | 0x0262 | -52.250 | 0x0291 | -58.250 | 0x02C0 | -64.000 | 0x02EF | -69.875 |
| 0x0205 | -40.625 | 0x0234 | -46.500 | 0x0263 | -52.375 | 0x0292 | -58.125 | 0x02C1 | -64.125 | 0x02F0 | -70.000 |
| 0x0206 | -40.750 | 0x0235 | -46.625 | 0x0264 | -52.500 | 0x0293 | -58.375 | 0x02C2 | -64.250 | 0x02F1 | -70.125 |
| 0x0207 | -40.875 | 0x0236 | -46.750 | 0x0265 | -52.625 | 0x0294 | -58.500 | 0x02C3 | -64.375 | 0x02F2 | -70.250 |
| 0x0208 | -41.000 | 0x0237 | -46.875 | 0x0266 | -52.750 | 0x0295 | -58.625 | 0x02C4 | -64.500 | 0x02F3 | -70.375 |
| 0x0209 | -41.125 | 0x0238 | -47.000 | 0x0267 | -52.875 | 0x0296 | -58.750 | 0x02C5 | -64.625 | 0x02F4 | -70.500 |
| 0x020A | -41.250 | 0x0239 | -47.125 | 0x0268 | -53.000 | 0x0297 | -58.875 | 0x02C6 | -64.750 | 0x02F5 | -70.625 |
| 0x020B | -41.375 | 0x023A | -47.250 | 0x0269 | -53.125 | 0x0298 | -59.000 | 0x02C7 | -64.875 | 0x02F6 | -70.750 |
| 0x020C | -41.500 | 0x023B | -47.375 | 0x026A | -53.250 | 0x0299 | -59.125 | 0x02C8 | -65.000 | 0x02F7 | -70.875 |
| 0x020D | -41.625 | 0x023C | -47.500 | 0x026B | -53.375 | 0x029A | -59.250 | 0x02C9 | -65.125 | 0x02F8 | -71.000 |
| 0x020E | -41.750 | 0x023D | -47.625 | 0x026C | -53.500 | 0x029B | -59.375 | 0x02CA | -65.250 | 0x02F9 | -71.125 |
| 0x020F | -41.875 | 0x023E | -47.750 | 0x026D | -53.625 | 0x029C | -59.500 | 0x02CB | -65.375 | 0x02FA | -71.250 |
| 0x0210 | -42.000 | 0x023F | -47.875 | 0x026E | -53.750 | 0x029D | -59.625 | 0x02CC | -65.500 | 0x02FB | -71.375 |
| 0x0211 | -42.125 | 0x0240 | -48.000 | 0x026F | -53.875 | 0x029E | -59.750 | 0x02CD | -65.625 | 0x02FC | -71.500 |
| 0x0212 | -42.250 | 0x0241 | -48.125 | 0x0270 | -54.000 | 0x029F | -59.875 | 0x02CE | -65.750 | 0x02FD | -71.625 |
| 0x0213 | -42.375 | 0x0242 | -48.250 | 0x0271 | -54.125 | 0x02A0 | -60.000 | 0x02CF | -65.875 | 0x02FE | -71.750 |
| 0x0214 | -42.500 | 0x0243 | -48.375 | 0x0272 | -54.250 | 0x02A1 | -60.125 | 0x02D0 | -66.000 | 0x02FF | -71.875 |
| 0x0215 | -42.625 | 0x0244 | -48.500 | 0x0273 | -54.375 | 0x02A2 | -60.250 | 0x02D1 | -66.125 | 0x0300 | -72.000 |
| 0x0216 | -42.750 | 0x0245 | -48.625 | 0x0274 | -54.500 | 0x02A3 | -60.375 | 0x02D2 | -66.250 | 0x0301 | -72.125 |
| 0x0217 | -42.875 | 0x0246 | -48.750 | 0x0275 | -54.625 | 0x02A4 | -60.500 | 0x02D3 | -66.375 | 0x0302 | -72.250 |
| 0x0218 | -43.000 | 0x0247 | -48.875 | 0x0276 | -54.750 | 0x02A5 | -60.625 | 0x02D4 | -66.500 | 0x0303 | -72.375 |
| 0x0219 | -43.125 | 0x0248 | -49.000 | 0x0277 | -54.875 | 0x02A6 | -60.750 | 0x02D5 | -66.625 | 0x0304 | -72.500 |
| 0x021A | -43.250 | 0x0249 | -49.125 | 0x0278 | -55.000 | 0x02A7 | -60.875 | 0x02D6 | -66.750 | 0x0305 | -72.625 |
| 0x021B | -43.375 | 0x024A | -49.250 | 0x0279 | -55.125 | 0x02A8 | -61.000 | 0x02D7 | -66.875 | 0x0306 | -72.750 |
| 0x021C | -43.500 | 0x024B | -49.375 | 0x027A | -55.250 | 0x02A9 | -61.125 | 0x02D8 | -67.000 | 0x0307 | -72.875 |
| 0x021D | -43.625 | 0x024C | -49.500 | 0x027B | -55.375 | 0x02AA | -61.250 | 0x02D9 | -67.125 | 0x0308 | -73.000 |
| 0x021E | -43.750 | 0x024D | -49.625 | 0x027C | -55.500 | 0x02AB | -61.375 | 0x02DA | -67.250 | 0x0309 | -73.125 |
| 0x021F | -43.875 | 0x024E | -49.750 | 0x027D | -55.625 | 0x02AC | -61.500 | 0x02DB | -67.375 | 0x030A | -73.250 |
| 0x0220 | -44.000 | 0x024F | -49.875 | 0x027E | -55.750 | 0x02AD | -61.625 | 0x02DC | -67.500 | 0x030B | -73.375 |
| 0x0221 | -44.125 | 0x0250 | -50.000 | 0x027F | -55.875 | 0x02AE | -61.750 | 0x02DD | -67.625 | 0x030C | -73.500 |
| 0x0222 | -44.250 | 0x0251 | -50.125 | 0x0280 | -56.000 | 0x02AF | -61.875 | 0x02DE | -67.750 | 0x030D | -73.625 |
| 0x0223 | -44.375 | 0x0252 | -50.250 | 0x0281 | -56.250 | 0x02B0 | -62.000 | 0x02DF | -67.875 | 0x030E | -73.750 |
| 0x0224 | -44.500 | 0x0253 | -50.375 | 0x0282 | -56.125 | 0x02B1 | -62.125 | 0x02E0 | -68.000 | 0x030F | -73.875 |
| 0x0225 | -44.625 | 0x0254 | -50.500 | 0x0283 | -56.375 | 0x02B2 | -62.250 | 0x02E1 | -68.125 | 0x0310 | -74.000 |
| 0x0226 | -44.750 | 0x0255 | -50.625 | 0x0284 | -56.500 | 0x02B3 | -62.375 | 0x02E2 | -68.250 | 0x0311 | -74.250 |
| 0x0227 | -44.875 | 0x0256 | -50.750 | 0x0285 | -56.625 | 0x02B4 | -62.500 | 0x02E3 | -68.375 | 0x0312 | -74.125 |
| 0x0228 | -45.000 | 0x0257 | -50.875 | 0x0286 | -56.750 | 0x02B5 | -62.625 | 0x02E4 | -68.500 | 0x0313 | -74.375 |
| 0x0229 | -45.125 | 0x0258 | -51.000 | 0x0287 | -56.875 | 0x02B6 | -62.750 | 0x02E5 | -68.625 | 0x0314 | -74.500 |
| 0x022A | -45.250 | 0x0259 | -51.125 | 0x0288 | -57.000 | 0x02B7 | -62.875 | 0x02E6 | -68.750 | 0x0315 | -74.625 |
| 0x022B | -45.375 | 0x025A | -51.250 | 0x0289 | -57.125 | 0x02B8 | -63.000 | 0x02E7 | -68.875 | 0x0316 | -74.750 |
| 0x022C | -45.500 | 0x025B | -51.375 | 0x028A | -57.250 | 0x02B9 | -63.125 | 0x02E8 | -69.000 | 0x0317 | -74.875 |
| 0x022D | -45.625 | 0x025C | -51.500 | 0x028B | -57.375 | 0x02BA | -63.250 | 0x02E9 | -69.125 | 0x0318 | -75.000 |
| 0x022E | -45.750 | 0x025D | -51.625 | 0x028C | -57.500 | 0x02BB | -63.375 | 0x02EA | -69.250 | 0x0319 | -75.125 |
| 0x022F | -45.875 | 0x025E | -51.750 | 0x028D | -57.625 | 0x02BC | -63.500 | 0x02EB | -69.375 | 0x031A | -75.250 |
| 0x0230 | -46.000 | 0x025F | -51.875 | 0x028E | -57.750 | 0x02BD | -63.625 | 0x02EC | -69.500 | 0x031B | -75.375 |
| 0x0231 | -46.125 | 0x0260 | -52.000 | 0x028F | -57.875 | 0x02BE | -63.750 | 0x02ED | -69.625 | 0x031C | -75.500 |
| 0x0232 | -46.250 | 0x0261 | -52.125 | 0x0290 | -58.000 | 0x02BF | -63.875 | 0x02EE | -69.750 | 0x031D | -75.625 |

**Table 12. Master Volume Table (continued)**

| VALUE  | LEVEL   | VALUE  | LEVEL   | VALUE  | LEVEL   | VALUE  | LEVEL   | VALUE  | LEVEL   | VALUE  | LEVEL    |
|--------|---------|--------|---------|--------|---------|--------|---------|--------|---------|--------|----------|
| 0x031E | -75.750 | 0x0344 | -80.500 | 0x036A | -85.250 | 0x0390 | -90.000 | 0x03B6 | -94.750 | 0x03DC | -99.500  |
| 0x031F | -75.875 | 0x0345 | -80.625 | 0x036B | -85.375 | 0x0391 | -90.125 | 0x03B7 | -94.875 | 0x03DD | -99.625  |
| 0x0320 | -76.000 | 0x0346 | -80.750 | 0x036C | -85.500 | 0x0392 | -90.250 | 0x03B8 | -95.000 | 0x03DE | -99.750  |
| 0x0321 | -76.125 | 0x0347 | -80.875 | 0x036D | -85.625 | 0x0393 | -90.375 | 0x03B9 | -95.125 | 0x03DF | -99.875  |
| 0x0322 | -76.250 | 0x0348 | -81.000 | 0x036E | -85.750 | 0x0394 | -90.500 | 0x03BA | -95.250 | 0x03E0 | -100.000 |
| 0x0323 | -76.375 | 0x0349 | -81.125 | 0x036F | -85.875 | 0x0395 | -90.625 | 0x03BB | -95.375 | 0x03E1 | -100.125 |
| 0x0324 | -76.500 | 0x034A | -81.250 | 0x0370 | -86.000 | 0x0396 | -90.750 | 0x03BC | -95.500 | 0x03E2 | -100.250 |
| 0x0325 | -76.625 | 0x034B | -81.375 | 0x0371 | -86.125 | 0x0397 | -90.875 | 0x03BD | -95.625 | 0x03E3 | -100.375 |
| 0x0326 | -76.750 | 0x034C | -81.500 | 0x0372 | -86.250 | 0x0398 | -91.000 | 0x03BE | -95.750 | 0x03E4 | -100.500 |
| 0x0327 | -76.875 | 0x034D | -81.625 | 0x0373 | -86.375 | 0x0399 | -91.125 | 0x03BF | -95.875 | 0x03E5 | -100.625 |
| 0x0328 | -77.000 | 0x034E | -81.750 | 0x0374 | -86.500 | 0x039A | -91.250 | 0x03C0 | -96.000 | 0x03E6 | -100.750 |
| 0x0329 | -77.125 | 0x034F | -81.875 | 0x0375 | -86.625 | 0x039B | -91.375 | 0x03C1 | -96.125 | 0x03E7 | -100.875 |
| 0x032A | -77.250 | 0x0350 | -82.000 | 0x0376 | -86.750 | 0x039C | -91.500 | 0x03C2 | -96.250 | 0x03E8 | -101.000 |
| 0x032B | -77.375 | 0x0351 | -82.125 | 0x0377 | -86.875 | 0x039D | -91.625 | 0x03C3 | -96.375 | 0x03E9 | -101.125 |
| 0x032C | -77.500 | 0x0352 | -82.250 | 0x0378 | -87.000 | 0x039E | -91.750 | 0x03C4 | -96.500 | 0x03EA | -101.250 |
| 0x032D | -77.625 | 0x0353 | -82.375 | 0x0379 | -87.125 | 0x039F | -91.875 | 0x03C5 | -96.625 | 0x03EB | -101.375 |
| 0x032E | -77.750 | 0x0354 | -82.500 | 0x037A | -87.250 | 0x03A0 | -92.000 | 0x03C6 | -96.750 | 0x03EC | -101.500 |
| 0x032F | -77.875 | 0x0355 | -82.625 | 0x037B | -87.375 | 0x03A1 | -92.125 | 0x03C7 | -96.875 | 0x03ED | -101.625 |
| 0x0330 | -78.000 | 0x0356 | -82.750 | 0x037C | -87.500 | 0x03A2 | -92.250 | 0x03C8 | -97.000 | 0x03EE | -101.750 |
| 0x0331 | -78.125 | 0x0357 | -82.875 | 0x037D | -87.625 | 0x03A3 | -92.375 | 0x03C9 | -97.125 | 0x03EF | -101.875 |
| 0x0332 | -78.250 | 0x0358 | -83.000 | 0x037E | -87.750 | 0x03A4 | -92.500 | 0x03CA | -97.250 | 0x03F0 | -102.000 |
| 0x0333 | -78.375 | 0x0359 | -83.125 | 0x037F | -87.875 | 0x03A5 | -92.625 | 0x03CB | -97.375 | 0x03F1 | -102.125 |
| 0x0334 | -78.500 | 0x035A | -83.250 | 0x0380 | -88.000 | 0x03A6 | -92.750 | 0x03CC | -97.500 | 0x03F2 | -102.250 |
| 0x0335 | -78.625 | 0x035B | -83.375 | 0x0381 | -88.125 | 0x03A7 | -92.875 | 0x03CD | -97.625 | 0x03F3 | -102.375 |
| 0x0336 | -78.750 | 0x035C | -83.500 | 0x0382 | -88.250 | 0x03A8 | -93.000 | 0x03CE | -97.750 | 0x03F4 | -102.500 |
| 0x0337 | -78.875 | 0x035D | -83.625 | 0x0383 | -88.375 | 0x03A9 | -93.125 | 0x03CF | -97.875 | 0x03F5 | -102.625 |
| 0x0338 | -79.000 | 0x035E | -83.750 | 0x0384 | -88.500 | 0x03AA | -93.250 | 0x03D0 | -98.000 | 0x03F6 | -102.750 |
| 0x0339 | -79.125 | 0x035F | -83.875 | 0x0385 | -88.625 | 0x03AB | -93.375 | 0x03D1 | -98.125 | 0x03F7 | -102.875 |
| 0x033A | -79.250 | 0x0360 | -84.000 | 0x0386 | -88.750 | 0x03AC | -93.500 | 0x03D2 | -98.250 | 0x03F8 | -103.000 |
| 0x033B | -79.375 | 0x0361 | -84.125 | 0x0387 | -88.875 | 0x03AD | -93.625 | 0x03D3 | -98.375 | 0x03F9 | -103.125 |
| 0x033C | -79.500 | 0x0362 | -84.250 | 0x0388 | -89.000 | 0x03AE | -93.750 | 0x03D4 | -98.500 | 0x03FA | -103.250 |
| 0x033D | -79.625 | 0x0363 | -84.375 | 0x0389 | -89.125 | 0x03AF | -93.875 | 0x03D5 | -98.625 | 0x03FB | -103.375 |
| 0x033E | -79.750 | 0x0364 | -84.500 | 0x038A | -89.250 | 0x03B0 | -94.000 | 0x03D6 | -98.750 | 0x03FC | -103.500 |
| 0x033F | -79.875 | 0x0365 | -84.625 | 0x038B | -89.375 | 0x03B1 | -94.125 | 0x03D7 | -98.875 | 0x03FD | -103.625 |
| 0x0340 | -80.000 | 0x0366 | -84.750 | 0x038C | -89.500 | 0x03B2 | -94.250 | 0x03D8 | -99.000 | 0x03FE | -103.750 |
| 0x0341 | -80.250 | 0x0367 | -84.875 | 0x038D | -89.625 | 0x03B3 | -94.375 | 0x03D9 | -99.125 | 0x03FF | Mute     |
| 0x0341 | -80.250 | 0x0368 | -85.000 | 0x038E | -89.750 | 0x03B4 | -94.500 | 0x03DA | -99.250 |        |          |
| 0x0343 | -80.375 | 0x0369 | -85.125 | 0x038F | -89.875 | 0x03B5 | -94.625 | 0x03DB | -99.375 |        |          |

### 10.6.9 Volume Configuration Register (0x0E)

Bits D2–D0: Volume slew rate (used to control volume change and MUTE ramp rates). These bits control the number of steps in a volume ramp. Volume steps occur at a rate that depends on the sample rate of the I<sup>2</sup>S data as follows:

| Sample rate (kHz) | Approximate ramp rate |
|-------------------|-----------------------|
| 8/16/32           | 125 µs/step           |
| 11.025/22.05/44.1 | 90.7 µs/step          |
| 12/24/48          | 83.3 µs/step          |

In two-band DRC, register 0x0A should be set to 0x30 and register 0x0E bits 6 and 5 should be set to 1.

**Table 13. Volume Configuration Register (0x0E)**

| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                                                                      |
|----------|----------|----------|----------|----------|----------|----------|----------|-------------------------------------------------------------------------------|
| <b>1</b> | –        | –        | –        | –        | –        | –        | –        | Reserved <sup>(1)</sup>                                                       |
| –        | <b>0</b> | –        | –        | –        | –        | –        | –        | DRC2 volume 1 (ch4) from I <sup>2</sup> C register 0x08                       |
| –        | <b>1</b> | –        | –        | –        | –        | –        | –        | <b>DRC2 volume 1 (ch4) from I<sup>2</sup>C register 0x0A<sup>(1)</sup></b>    |
| –        | –        | <b>0</b> | –        | –        | –        | –        | –        | DRC2 volume 2 (ch3) from I <sup>2</sup> C register 0x09                       |
| –        | –        | <b>1</b> | –        | –        | –        | –        | –        | <b>DRC2 volume 2 (ch3) from I<sup>2</sup>C register 0x0A<sup>(1)</sup></b>    |
| –        | –        | –        | <b>1</b> | <b>0</b> | –        | –        | –        | Reserved <sup>(1)</sup>                                                       |
| –        | –        | –        | –        | –        | <b>0</b> | <b>0</b> | <b>0</b> | <b>Volume slew 512 steps (43 ms volume ramp time at 48 kHz)<sup>(1)</sup></b> |
| –        | –        | –        | –        | –        | 0        | 0        | 1        | Volume slew 1024 steps (85-ms volume ramp time at 48 kHz)                     |
| –        | –        | –        | –        | –        | 0        | 1        | 0        | Volume slew 2048 steps (171-ms volume ramp time at 48 kHz)                    |
| –        | –        | –        | –        | –        | 0        | 1        | 1        | Volume slew 256 steps (21-ms volume ramp time at 48 kHz)                      |
| –        | –        | –        | –        | –        | 1        | X        | X        | Reserved                                                                      |

(1) Default values are in **bold**.

### 10.6.10 Modulation Limit Register (0x10)

**Table 14. Modulation Limit Register (0x10)**

| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | MODULATION LIMIT           |
|----------|----------|----------|----------|----------|----------|----------|----------|----------------------------|
| <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | –        | –        | –        | Reserved                   |
| –        | –        | –        | –        | –        | 0        | 0        | 0        | 99.2%                      |
| –        | –        | –        | –        | –        | 0        | 0        | 1        | 98.4%                      |
| –        | –        | –        | –        | –        | <b>0</b> | <b>1</b> | <b>0</b> | <b>97.7%<sup>(1)</sup></b> |
| –        | –        | –        | –        | –        | 0        | 1        | 1        | 96.9%                      |
| –        | –        | –        | –        | –        | 1        | 0        | 0        | 96.1%                      |
| –        | –        | –        | –        | –        | 1        | 0        | 1        | 95.3%                      |
| –        | –        | –        | –        | –        | 1        | 1        | 0        | 94.5%                      |
| –        | –        | –        | –        | –        | 1        | 1        | 1        | 93.8%                      |

(1) Default values are in **bold**.

### 10.6.11 Interchannel Delay Registers (0x11, 0x12, 0x13, and 0x14)

Internal PWM channels 1, 2,  $\bar{1}$ , and  $\bar{2}$  are mapped into registers 0x11, 0x12, 0x13, and 0x14.

**Table 15. Channel Interchannel Delay Register Format**

| BITS DEFINITION | D7       | D6       | D5       | D4       | D3       | D2       | D1 | D0 | FUNCTION                                           |
|-----------------|----------|----------|----------|----------|----------|----------|----|----|----------------------------------------------------|
|                 | 0        | 0        | 0        | 0        | 0        | 0        | –  | –  | Minimum absolute delay, 0 DCLK cycles              |
|                 | 0        | 1        | 1        | 1        | 1        | 1        | –  | –  | Maximum positive delay, $31 \times 4$ DCLK cycles  |
|                 | 1        | 0        | 0        | 0        | 0        | 0        | –  | –  | Maximum negative delay, $-32 \times 4$ DCLK cycles |
|                 |          |          |          |          |          |          | 0  | 0  | Reserved                                           |
| SUBADDRESS      | D7       | D6       | D5       | D4       | D3       | D2       | D1 | D0 | Delay = (value) $\times$ 4 DCLKs                   |
| <b>0x11</b>     | <b>1</b> | <b>0</b> | <b>1</b> | <b>0</b> | <b>1</b> | <b>1</b> | –  | –  | <b>Default value for channel 1<sup>(1)</sup></b>   |
| <b>0x12</b>     | <b>0</b> | <b>1</b> | <b>0</b> | <b>1</b> | <b>0</b> | <b>1</b> | –  | –  | <b>Default value for channel 2<sup>(1)</sup></b>   |
| <b>0x13</b>     | <b>1</b> | <b>0</b> | <b>1</b> | <b>0</b> | <b>1</b> | <b>1</b> | –  | –  | <b>Default value for channel 1<sup>(1)</sup></b>   |
| <b>0x14</b>     | <b>0</b> | <b>1</b> | <b>0</b> | <b>1</b> | <b>0</b> | <b>1</b> | –  | –  | <b>Default value for channel 2<sup>(1)</sup></b>   |

(1) Default values are in **bold**.

ICD settings have high impact on audio performance (for example, dynamic range, THD, crosstalk, and so forth). Therefore, appropriate ICD settings must be used. By default, the device has ICD settings for the AD mode. If used in BD mode, then update these registers before coming out of all-channel shutdown.

**Table 16. ICD Settings**

| MODE | AD MODE | BD MODE |
|------|---------|---------|
| 0x11 | AC      | B8      |
| 0x12 | 54      | 60      |
| 0x13 | AC      | A0      |
| 0x14 | 54      | 48      |

### 10.6.12 PWM Shutdown Group Register (0x19)

Settings of this register determine which PWM channels are active. The value should be 0x30 for BTL mode and 0x3A for PBTTL mode. The default value of this register is 0x30. The functionality of this register is tied to the state of bit D5 in the system control register.

This register defines which channels belong to the shutdown group (SDG). If a 1 is set in the shutdown group register, that particular channel is **not** started following an exit *out of all-channel shutdown* command (if bit D5 is set to 0 in system control register 2, 0x05).

**Table 17. PWM Shutdown Group Register (0x19)**

| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                                                        |
|----------|----------|----------|----------|----------|----------|----------|----------|-----------------------------------------------------------------|
| <b>0</b> | –        | –        | –        | –        | –        | –        | –        | Reserved <sup>(1)</sup>                                         |
| –        | <b>0</b> | –        | –        | –        | –        | –        | –        | Reserved <sup>(1)</sup>                                         |
| –        | –        | <b>1</b> | –        | –        | –        | –        | –        | Reserved <sup>(1)</sup>                                         |
| –        | –        | –        | <b>1</b> | –        | –        | –        | –        | Reserved <sup>(1)</sup>                                         |
| –        | –        | –        | –        | <b>0</b> | –        | –        | –        | PWM channel 4 does not belong to shutdown group. <sup>(1)</sup> |
| –        | –        | –        | –        | 1        | –        | –        | –        | PWM channel 4 belongs to shutdown group.                        |
| –        | –        | –        | –        | –        | <b>0</b> | –        | –        | PWM channel 3 does not belong to shutdown group. <sup>(1)</sup> |
| –        | –        | –        | –        | –        | 1        | –        | –        | PWM channel 3 belongs to shutdown group.                        |
| –        | –        | –        | –        | –        | –        | <b>0</b> | –        | PWM channel 2 does not belong to shutdown group. <sup>(1)</sup> |
| –        | –        | –        | –        | –        | –        | 1        | –        | PWM channel 2 belongs to shutdown group.                        |
| –        | –        | –        | –        | –        | –        | –        | <b>0</b> | PWM channel 1 does not belong to shutdown group. <sup>(1)</sup> |
| –        | –        | –        | –        | –        | –        | –        | 1        | PWM channel 1 belongs to shutdown group.                        |

(1) Default values are in **bold**.

### 10.6.13 Start/Stop Period Register (0x1A)

This register is used to control the soft-start and soft-stop period following an enter or exit all-channel shutdown command or change in the PDN state. This helps reduce pops and clicks at start-up and shutdown. The times are only approximate and vary depending on device activity level and I<sup>2</sup>S clock stability.

**Table 18. Start/Stop Period Register (0x1A)**

| D7 | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                                                       |
|----|----------|----------|----------|----------|----------|----------|----------|----------------------------------------------------------------|
| 0  | –        | –        | –        | –        | –        | –        | –        | SSTIMER enabled <sup>(1)</sup>                                 |
| 1  | –        | –        | –        | –        | –        | –        | –        | SSTIMER disabled                                               |
| –  | <b>0</b> | <b>0</b> | –        | –        | –        | –        | –        | <b>Reserved<sup>(2)</sup></b>                                  |
| –  | –        | –        | 0        | 0        | –        | –        | –        | No 50% duty cycle start/stop period                            |
| –  | –        | –        | 0        | 1        | 0        | 0        | 0        | 16.5-ms 50% duty cycle start/stop period                       |
| –  | –        | –        | 0        | 1        | 0        | 0        | 1        | 23.9-ms 50% duty cycle start/stop period                       |
| –  | –        | –        | 0        | 1        | 0        | 1        | 0        | 31.4-ms 50% duty cycle start/stop period                       |
| –  | –        | –        | 0        | 1        | 0        | 1        | 1        | 40.4-ms 50% duty cycle start/stop period                       |
| –  | –        | –        | 0        | 1        | 1        | 0        | 0        | 53.9-ms 50% duty cycle start/stop period                       |
| –  | –        | –        | 0        | 1        | 1        | 0        | 1        | 70.3-ms 50% duty cycle start/stop period                       |
| –  | –        | –        | 0        | 1        | 1        | 1        | 0        | 94.2-ms 50% duty cycle start/stop period                       |
| –  | –        | –        | <b>0</b> | <b>1</b> | <b>1</b> | <b>1</b> | <b>1</b> | <b>125.7-ms 50% duty cycle start/stop period<sup>(2)</sup></b> |
| –  | –        | –        | 1        | 0        | 0        | 0        | 0        | 164.6-ms 50% duty cycle start/stop period                      |
| –  | –        | –        | 1        | 0        | 0        | 0        | 1        | 239.4-ms 50% duty cycle start/stop period                      |
| –  | –        | –        | 1        | 0        | 0        | 1        | 0        | 314.2-ms 50% duty cycle start/stop period                      |
| –  | –        | –        | 1        | 0        | 0        | 1        | 1        | 403.9-ms 50% duty cycle start/stop period                      |
| –  | –        | –        | 1        | 0        | 1        | 0        | 0        | 538.6-ms 50% duty cycle start/stop period                      |
| –  | –        | –        | 1        | 0        | 1        | 0        | 1        | 703.1-ms 50% duty cycle start/stop period                      |
| –  | –        | –        | 1        | 0        | 1        | 1        | 0        | 942.5-ms 50% duty cycle start/stop period                      |
| –  | –        | –        | 1        | 0        | 1        | 1        | 1        | 1256.6-ms 50% duty cycle start/stop period                     |
| –  | –        | –        | 1        | 1        | 0        | 0        | 0        | 1728.1-ms 50% duty cycle start/stop period                     |
| –  | –        | –        | 1        | 1        | 0        | 0        | 1        | 2513.6-ms 50% duty cycle start/stop period                     |
| –  | –        | –        | 1        | 1        | 0        | 1        | 0        | 3299.1-ms 50% duty cycle start/stop period                     |
| –  | –        | –        | 1        | 1        | 0        | 1        | 1        | 4241.7-ms 50% duty cycle start/stop period                     |
| –  | –        | –        | 1        | 1        | 1        | 0        | 0        | 5655.6-ms 50% duty cycle start/stop period                     |
| –  | –        | –        | 1        | 1        | 1        | 0        | 1        | 7383.7-ms 50% duty cycle start/stop period                     |
| –  | –        | –        | 1        | 1        | 1        | 1        | 0        | 9897.3-ms 50% duty cycle start/stop period                     |
| –  | –        | –        | 1        | 1        | 1        | 1        | 1        | 13,196.4-ms 50% duty cycle start/stop period                   |

(1) Default values are in **bold**.

(2) Default values are in **bold**.

### 10.6.14 Oscillator Trim Register (0x1B)

The TAS5727 PWM processor contains an internal oscillator to support autodetect of I<sup>2</sup>S clock rates. This reduces system cost because an external reference is not required. Currently, TI recommends a reference resistor value of 18.2 kΩ (1%). This should be connected between OSC\_RES and DVSSO.

Writing 0x00 to register 0x1B enables the trim that was programmed at the factory.

Note that trim must always be run following reset of the device.

**Table 19. Oscillator Trim Register (0x1B)**

| D7       | D6       | D5       | D4       | D3       | D2       | D1 | D0       | FUNCTION                                                              |
|----------|----------|----------|----------|----------|----------|----|----------|-----------------------------------------------------------------------|
| <b>1</b> | –        | –        | –        | –        | –        | –  | –        | Reserved <sup>(1)</sup>                                               |
| –        | <b>0</b> | –        | –        | –        | –        | –  | –        | Oscillator trim not done (read-only) <sup>(1)</sup>                   |
| –        | 1        | –        | –        | –        | –        | –  | –        | Oscillator trim done (read only)                                      |
| –        | –        | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | –  | –        | Reserved <sup>(1)</sup>                                               |
| –        | –        | –        | –        | –        | –        | 0  | –        | Select factory trim (Write a 0 to select factory trim; default is 1.) |
| –        | –        | –        | –        | –        | –        | 1  | –        | Factory trim disabled <sup>(1)</sup>                                  |
| –        | –        | –        | –        | –        | –        | –  | <b>0</b> | Reserved <sup>(1)</sup>                                               |

(1) Default values are in **bold**.

### 10.6.15 BKND\_ERR Register (0x1C)

When a back-end error signal is received from the internal power stage, the power stage is reset, stopping all PWM activity. Subsequently, the modulator waits approximately for the time listed in [Table 20](#) before attempting to re-start the power stage.

**Table 20. BKND\_ERR Register (0x1C)<sup>(1)</sup>**

| D7 | D6 | D5 | D4 | D3       | D2       | D1       | D0       | FUNCTION                                           |
|----|----|----|----|----------|----------|----------|----------|----------------------------------------------------|
| 0  | 0  | 0  | 0  | 0        | 0        | 0        | X        | Reserved                                           |
| –  | –  | –  | –  | <b>0</b> | <b>0</b> | <b>1</b> | <b>0</b> | Set back-end reset period to 299 ms <sup>(2)</sup> |
| –  | –  | –  | –  | 0        | 0        | 1        | 1        | Set back-end reset period to 449 ms                |
| –  | –  | –  | –  | 0        | 1        | 0        | 0        | Set back-end reset period to 598 ms                |
| –  | –  | –  | –  | 0        | 1        | 0        | 1        | Set back-end reset period to 748 ms                |
| –  | –  | –  | –  | 0        | 1        | 1        | 0        | Set back-end reset period to 898 ms                |
| –  | –  | –  | –  | 0        | 1        | 1        | 1        | Set back-end reset period to 1047 ms               |
| –  | –  | –  | –  | 1        | 0        | 0        | 0        | Set back-end reset period to 1197 ms               |
| –  | –  | –  | –  | 1        | 0        | 0        | 1        | Set back-end reset period to 1346 ms               |
| –  | –  | –  | –  | 1        | 0        | 1        | X        | Set back-end reset period to 1496 ms               |
| –  | –  | –  | –  | 1        | 1        | X        | X        | Set back-end reset period to 1496 ms               |

(1) This register can be written only with a non-reserved value. Also this register can be written once after the reset.

(2) Default values are in **bold**.

**10.6.16 Input Multiplexer Register (0x20)**

This register controls the modulation scheme (AD or BD mode) as well as the routing of I<sup>2</sup>S audio to the internal channels.

**Table 21. Input Multiplexer Register (0x20)**

| D31      | D30      | D29      | D28      | D27      | D26      | D25      | D24      | FUNCTION                                  |
|----------|----------|----------|----------|----------|----------|----------|----------|-------------------------------------------|
| <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | Reserved <sup>(1)</sup>                   |
| D23      | D22      | D21      | D20      | D19      | D18      | D17      | D16      | FUNCTION                                  |
| <b>0</b> | –        | –        | –        | –        | –        | –        | –        | <b>Channel-1 AD mode</b> <sup>(1)</sup>   |
| 1        | –        | –        | –        | –        | –        | –        | –        | Channel-1 BD mode                         |
| –        | <b>0</b> | <b>0</b> | <b>0</b> | –        | –        | –        | –        | <b>SDIN-L to channel 1</b> <sup>(1)</sup> |
| –        | 0        | 0        | 1        | –        | –        | –        | –        | SDIN-R to channel 1                       |
| –        | 0        | 1        | 0        | –        | –        | –        | –        | Reserved                                  |
| –        | 0        | 1        | 1        | –        | –        | –        | –        | Reserved                                  |
| –        | 1        | 0        | 0        | –        | –        | –        | –        | Reserved                                  |
| –        | 1        | 0        | 1        | –        | –        | –        | –        | Reserved                                  |
| –        | 1        | 1        | 0        | –        | –        | –        | –        | Ground (0) to channel 1                   |
| –        | 1        | 1        | 1        | –        | –        | –        | –        | Reserved                                  |
| –        | –        | –        | –        | <b>0</b> | –        | –        | –        | <b>Channel 2 AD mode</b> <sup>(1)</sup>   |
| –        | –        | –        | –        | 1        | –        | –        | –        | Channel 2 BD mode                         |
| –        | –        | –        | –        | –        | 0        | 0        | 0        | SDIN-L to channel 2                       |
| –        | –        | –        | –        | –        | <b>0</b> | <b>0</b> | <b>1</b> | <b>SDIN-R to channel 2</b> <sup>(1)</sup> |
| –        | –        | –        | –        | –        | 0        | 1        | 0        | Reserved                                  |
| –        | –        | –        | –        | –        | 0        | 1        | 1        | Reserved                                  |
| –        | –        | –        | –        | –        | 1        | 0        | 0        | Reserved                                  |
| –        | –        | –        | –        | –        | 1        | 0        | 1        | Reserved                                  |
| –        | –        | –        | –        | –        | 1        | 1        | 0        | Ground (0) to channel 2                   |
| –        | –        | –        | –        | –        | 1        | 1        | 1        | Reserved                                  |
| D15      | D14      | D13      | D12      | D11      | D10      | D9       | D8       | FUNCTION                                  |
| <b>0</b> | <b>1</b> | <b>1</b> | <b>1</b> | <b>0</b> | <b>1</b> | <b>1</b> | <b>1</b> | Reserved <sup>(1)</sup>                   |
| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                                  |
| <b>0</b> | <b>1</b> | <b>1</b> | <b>1</b> | <b>0</b> | <b>0</b> | <b>1</b> | <b>0</b> | Reserved <sup>(1)</sup>                   |

(1) Default values are in **bold**.

### 10.6.17 Channel 4 Source Select Register (0x21)

This register selects the channel 4 source.

**Table 22. Subchannel Control Register (0x21)**

| D31      | D30      | D29      | D28      | D27      | D26      | D25      | D24      | FUNCTION                            |
|----------|----------|----------|----------|----------|----------|----------|----------|-------------------------------------|
| <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | Reserved <sup>(1)</sup>             |
| D23      | D22      | D21      | D20      | D19      | D18      | D17      | D16      | FUNCTION                            |
| <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | Reserved <sup>(1)</sup>             |
| D15      | D14      | D13      | D12      | D11      | D10      | D9       | D8       | FUNCTION                            |
| <b>0</b> | <b>1</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>1</b> | –        | Reserved <sup>(1)</sup>             |
| –        | –        | –        | –        | –        | –        | –        | 0        | (L + R)/2                           |
| –        | –        | –        | –        | –        | –        | –        | 1        | Left-channel post-BQ <sup>(1)</sup> |
| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                            |
| <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>1</b> | <b>1</b> | Reserved <sup>(1)</sup>             |

(1) Default values are in **bold**.

### 10.6.18 PWM Output MUX Register (0x25)

This DAP output mux selects which internal PWM channel is output to the external pins. Any channel can be output to any external output pin.

Bits D21–D20: Selects which PWM channel is output to OUT\_A

Bits D17–D16: Selects which PWM channel is output to OUT\_B

Bits D13–D12: Selects which PWM channel is output to OUT\_C

Bits D09–D08: Selects which PWM channel is output to OUT\_D

Note that channels are encoded so that channel 1 = 0x00, channel 2 = 0x01, ..., channel 4 = 0x03.

**Table 23. PWM Output Mux Register (0x25)**

| D31      | D30      | D29      | D28      | D27      | D26      | D25      | D24      | FUNCTION                                    |
|----------|----------|----------|----------|----------|----------|----------|----------|---------------------------------------------|
| <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>1</b> | Reserved <sup>(1)</sup>                     |
| D23      | D22      | D21      | D20      | D19      | D18      | D17      | D16      | FUNCTION                                    |
| <b>0</b> | <b>0</b> | –        | –        | –        | –        | –        | –        | Reserved <sup>(1)</sup>                     |
| –        | –        | <b>0</b> | <b>0</b> | –        | –        | –        | –        | Multiplex channel 1 to OUT_A <sup>(1)</sup> |
| –        | –        | 0        | 1        | –        | –        | –        | –        | Multiplex channel 2 to OUT_A                |
| –        | –        | 1        | 0        | –        | –        | –        | –        | Multiplex channel 1 to OUT_A                |
| –        | –        | 1        | 1        | –        | –        | –        | –        | Multiplex channel 2 to OUT_A                |
| –        | –        | –        | –        | <b>0</b> | <b>0</b> | –        | –        | Reserved <sup>(1)</sup>                     |
| –        | –        | –        | –        | –        | –        | 0        | 0        | Multiplex channel 1 to OUT_B                |
| –        | –        | –        | –        | –        | –        | 0        | 1        | Multiplex channel 2 to OUT_B                |
| –        | –        | –        | –        | –        | –        | <b>1</b> | <b>0</b> | Multiplex channel 1 to OUT_B <sup>(1)</sup> |
| –        | –        | –        | –        | –        | –        | 1        | 1        | Multiplex channel 2 to OUT_B                |

(1) Default values are in **bold**.

**Table 23. PWM Output Mux Register (0x25) (continued)**

| D15      | D14      | D13      | D12      | D11      | D10      | D9       | D8       | FUNCTION                                          |
|----------|----------|----------|----------|----------|----------|----------|----------|---------------------------------------------------|
| <b>0</b> | <b>0</b> | –        | –        | –        | –        | –        | –        | Reserved <sup>(1)</sup>                           |
| –        | –        | 0        | 0        | –        | –        | –        | –        | Multiplex channel 1 to OUT_C                      |
| –        | –        | <b>0</b> | <b>1</b> | –        | –        | –        | –        | <b>Multiplex channel 2 to OUT_C<sup>(1)</sup></b> |
| –        | –        | 1        | 0        | –        | –        | –        | –        | Multiplex channel 1 to OUT_C                      |
| –        | –        | 1        | 1        | –        | –        | –        | –        | Multiplex channel 2 to OUT_C                      |
| –        | –        | –        | –        | <b>0</b> | <b>0</b> | –        | –        | Reserved <sup>(1)</sup>                           |
| –        | –        | –        | –        | –        | –        | 0        | 0        | Multiplex channel 1 to OUT_D                      |
| –        | –        | –        | –        | –        | –        | 0        | 1        | Multiplex channel 2 to OUT_D                      |
| –        | –        | –        | –        | –        | –        | 1        | 0        | Multiplex channel 1 to OUT_D                      |
| –        | –        | –        | –        | –        | –        | 1        | 1        | <b>Multiplex channel 2 to OUT_D<sup>(1)</sup></b> |
| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                                          |
| <b>0</b> | <b>1</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>1</b> | <b>0</b> | <b>1</b> | Reserved <sup>(1)</sup>                           |

**10.6.19 DRC Control Register (0x46)**
**Table 24. DRC Control Register (0x46)**

| D31      | D30      | D29      | D28      | D27      | D26      | D25      | D24      | FUNCTION                             |
|----------|----------|----------|----------|----------|----------|----------|----------|--------------------------------------|
| <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | Reserved <sup>(1)</sup>              |
| D23      | D22      | D21      | D20      | D19      | D18      | D17      | D16      | FUNCTION                             |
| <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | Reserved <sup>(1)</sup>              |
| D15      | D14      | D13      | D12      | D11      | D10      | D9       | D8       | FUNCTION                             |
| <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | Reserved <sup>(1)</sup>              |
| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                             |
| <b>0</b> | <b>0</b> | –        | –        | –        | –        | –        | –        | Reserved <sup>(1)</sup>              |
| –        | –        | 0        | –        | –        | –        | –        | –        | Reserved                             |
| –        | –        | 1        | –        | –        | –        | –        | –        | Reserved                             |
| –        | –        | –        | <b>0</b> | –        | –        | –        | –        | Reserved <sup>(1)</sup>              |
| –        | –        | –        | –        | <b>0</b> | –        | –        | –        | Reserved <sup>(1)</sup>              |
| –        | –        | –        | –        | –        | <b>0</b> | –        | –        | Reserved <sup>(1)</sup>              |
| –        | –        | –        | –        | –        | –        | <b>0</b> | –        | <b>DRC2 turned OFF<sup>(1)</sup></b> |
| –        | –        | –        | –        | –        | –        | –        | 1        | DRC2 turned ON                       |
| –        | –        | –        | –        | –        | –        | –        | <b>0</b> | <b>DRC1 turned OFF<sup>(1)</sup></b> |
| –        | –        | –        | –        | –        | –        | –        | 1        | DRC1 turned ON                       |

 (1) Default values are in **bold**.

### 10.6.20 PWM Switching Rate Control Register (0x4F)

PWM switching rate should be selected through the register 0x4F before coming out of all-channel shutdown.

**Table 25. PWM Switching Rate Control Register (0x4F)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION                |
|-----|-----|-----|-----|-----|-----|-----|-----|-------------------------|
| 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | Reserved <sup>(1)</sup> |
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | FUNCTION                |
| 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | Reserved <sup>(1)</sup> |
| D15 | D14 | D13 | D12 | D11 | D10 | D9  | D8  | FUNCTION                |
| 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | Reserved <sup>(1)</sup> |
| D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  | FUNCTION                |
| –   | –   | 0   | 0   | –   | –   | –   | –   | Reserved <sup>(1)</sup> |
| –   | –   | –   | –   | 0   | 1   | 1   | 0   | SRC = 6 <sup>(1)</sup>  |
| –   | –   | –   | –   | 0   | 1   | 1   | 1   | SRC = 7                 |
| –   | –   | –   | –   | 1   | 0   | 0   | 0   | SRC = 8                 |
| –   | –   | –   | –   | 1   | 0   | 0   | 1   | SRC = 9                 |
| –   | –   | –   | –   | 1   | 0   | 1   | 0   | Reserved                |
| –   | –   | –   | –   | 1   | 1   | –   | –   | Reserved                |

(1) Default values are in **bold**.

### 10.6.21 Bank Switch and EQ Control (0x50)

**Table 26. Bank Switching Command (0x50)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION                                                                                                                                                                                      |
|-----|-----|-----|-----|-----|-----|-----|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | Reserved <sup>(1)</sup>                                                                                                                                                                       |
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | FUNCTION                                                                                                                                                                                      |
| 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | Reserved <sup>(1)</sup>                                                                                                                                                                       |
| D15 | D14 | D13 | D12 | D11 | D10 | D9  | D8  | FUNCTION                                                                                                                                                                                      |
| 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | Reserved <sup>(1)</sup>                                                                                                                                                                       |
| D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  | FUNCTION                                                                                                                                                                                      |
| 0   |     |     |     |     |     |     |     | EQ ON <sup>(1)</sup>                                                                                                                                                                          |
| 1   | –   | –   | –   | –   | –   | –   | –   | EQ OFF (bypass BQ 0–7 of channels 1 and 2)                                                                                                                                                    |
| –   | 0   | –   | –   | –   | –   | –   | –   | Reserved <sup>(1)</sup>                                                                                                                                                                       |
| –   | –   | 0   | –   | –   | –   | –   | –   | Ignore bank-mapping in bits D31–D8. Use default mapping. <sup>(1)</sup>                                                                                                                       |
| –   | –   | 1   | –   | –   | –   | –   | –   | Use bank-mapping in bits D31–D8.                                                                                                                                                              |
| –   | –   | –   | 0   | –   | –   | –   | –   | L and R can be written independently. <sup>(1)</sup>                                                                                                                                          |
| –   | –   | –   | 1   | –   | –   | –   | –   | L and R are ganged for EQ biquads; a write to the left-channel biquad is also written to the right-channel biquad. (0x29–0x2F is ganged to 0x30–0x36. Also, 0x58–0x5B is ganged to 0x5C–0x5F. |
| –   | –   | –   | –   | 0   | –   | –   | –   | Reserved <sup>(1)</sup>                                                                                                                                                                       |
| –   | –   | –   | –   | –   | 0   | 0   | 0   | No bank switching. All updates to DAP <sup>(1)</sup>                                                                                                                                          |
| –   | –   | –   | –   | –   | 0   | 0   | 1   | Configure bank 1 (32 kHz by default)                                                                                                                                                          |
| –   | –   | –   | –   | –   | 0   | 1   | X   | Reserved                                                                                                                                                                                      |
| –   | –   | –   | –   | –   | 1   | X   | X   | Reserved                                                                                                                                                                                      |

(1) Default values are in **bold**.

## 11 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

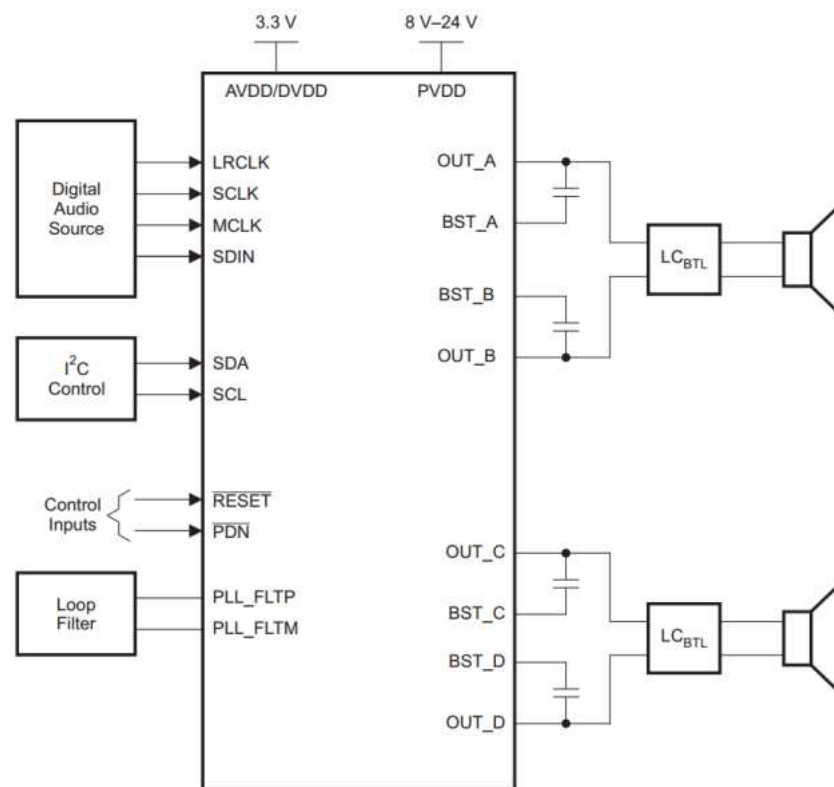
### 11.1 Application Information

The typical connection diagram highlights the required external components and system level connections for proper operation of the device in several popular system examples.

Each of these configurations can be realized using the Evaluation Module (EVM) for the device. These flexible modules allow full evaluation of the device in the most common modes of operation. Any design variation can be supported by TI through schematic and layout reviews. Visit <http://e2e.ti.com> for design assistance and join the audio amplifier discussion forum for additional information.

### 11.2 Typical Applications

#### 11.2.1 Stereo Stereo Bridge Tied Load Application



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**Figure 40. TAS5727 Stereo Application**

#### 11.2.1.1 Design Requirements

Table 27 lists the design parameters for this example.

Table 27. Design Parameters

| PARAMETER         | EXAMPLE                                           |
|-------------------|---------------------------------------------------|
| Low Power Supply  | 3.3 V                                             |
| High Power Supply | 8 V to 26 V                                       |
| Host Processor    | I <sup>2</sup> S Compliant Master                 |
|                   | I <sup>2</sup> C Compliant Master                 |
|                   | GPIO Control                                      |
| Output Filters    | Inductor-Capacitor Low-Pass Filter <sup>(1)</sup> |
| Speaker           | 4-Ω minimum                                       |

(1) Refer to SLOA119 for a detailed description of the filter design.

11.2.1.2 Detailed Design Procedure

11.2.1.2.1 Component Selection and Hardware Connections

The typical connections required for proper operation of the device can be found on the TAS5727 User's Guide (SLOU346). The device was tested this list of components, deviation from this typical application components unless recommended by this document may produce unwanted results, which could range from degradation of audio performance to destructive failure of the device. The application report Class-D LC Filter Design (SLOA119) offers a detailed description on proper component selection and design of the output filter based upon the modulation used, desired load, and response.

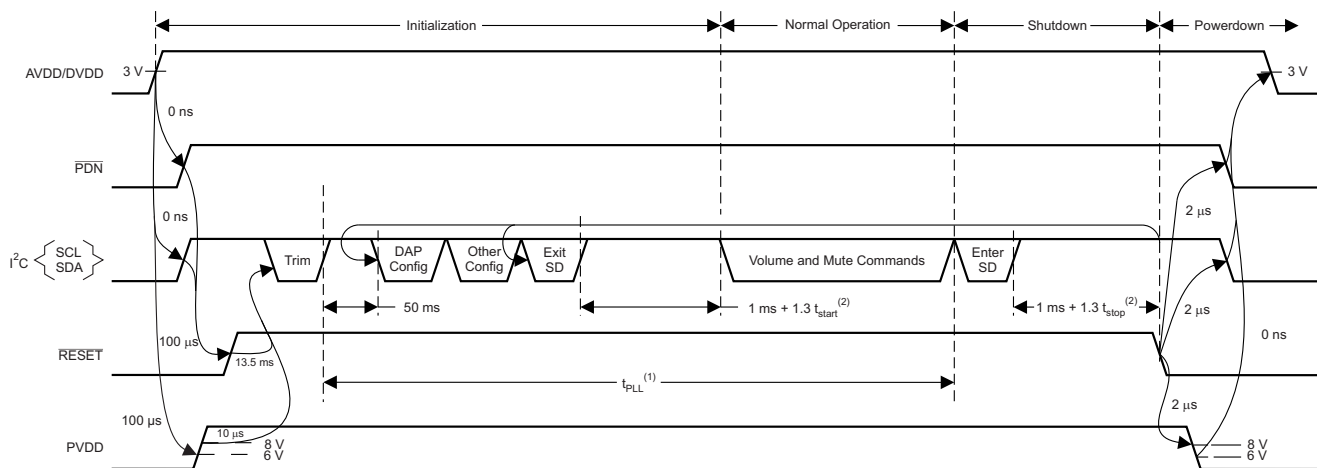
11.2.1.2.2 I<sup>2</sup>C Pullup Resistors

Customary pullup resistors are required on the SCL and SDA signal lines. These pullups are not shown in the typical application circuits, because they are shared by all of the devices on the I<sup>2</sup>C bus, and are considered to be part of the associated passive components for the System Processor. These resistor values should be chosen per the guidance provided in the I<sup>2</sup>C Specification.

11.2.1.2.3 Digital I/O Connectivity

The digital I/O lines of the TAS5727 are described in previous sections. As discussed, whenever a static digital pin (that is a pin that is hardwired to be HIGH or LOW) is required to be pulled HIGH, it should be connected to DVDD through a pullup resistor to control the slew rate of the voltage presented to the digital I/O pins. It is not, however, necessary to have a separate pullup resistor for each static digital I/O line. Instead, a single resistor can be used to tie all static I/O lines HIGH to reduce BOM count.

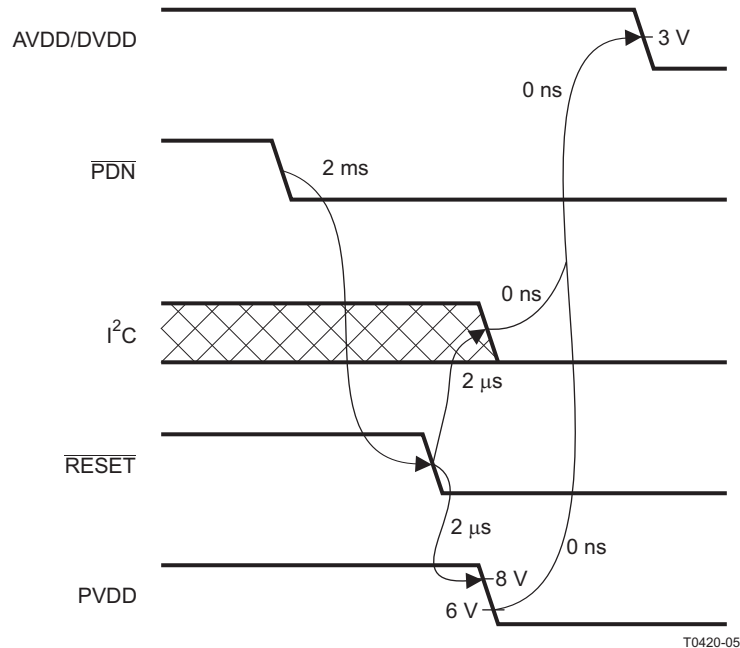
11.2.1.2.4 Recommended Start-Up and Shutdown Procedures



(1)  $t_{PLL}$  has to be greater than  $240\text{ ms} + 1.3 t_{start}$ . This constraint only applies to the first trim command following AVDD/DVDD power-up. It does not apply to trim commands following subsequent resets.  
 (2)  $t_{start}/t_{stop}$  = PWM start/stop time as defined in register 0X1A

T0419-06

Figure 41. Recommended Command Sequence


**Figure 42. Power-Loss Sequence**

#### 11.2.1.2.4.1 Initialization Sequence

Use the following sequence to power up and initialize the device:

1. Hold all digital inputs low and ramp up AVDD/DVDD to at least 3 V.
2. Initialize digital inputs and PVDD supply as follows:
  - Drive  $\overline{\text{RESET}} = 0$ ,  $\overline{\text{PDN}} = 1$ , and other digital inputs to their desired state while ensuring that all are never more than 2.5 V above AVDD/DVDD. Wait at least 100 μs, drive  $\overline{\text{RESET}} = 1$ , and wait at least another 13.5 ms.
  - Ramp up PVDD to at least 8 V while ensuring that it remains below 6 V for at least 100 μs after AVDD/DVDD reaches 3 V. Then wait at least another 10 μs.
3. Trim oscillator (write 0x00 to register 0x1B) and wait at least 50 ms.
4. Configure the DAP through I<sup>2</sup>C (see User's Guide for typical values).
5. Configure remaining registers.
6. Exit shutdown (sequence defined below).

#### 11.2.1.2.4.2 Normal Operation

The following are the only events supported during normal operation:

1. Writes to master/channel volume registers
2. Writes to soft-mute register
3. Enter and exit shutdown (sequence defined below)

#### NOTE

Event 3 is not supported for  $240 \text{ ms} + 1.3 \times t_{\text{start}}$  after trim following AVDD/DVDD power-up ramp (where  $t_{\text{start}}$  is specified by register 0x1A).

#### 11.2.1.2.4.3 Shutdown Sequence

Enter:

1. Write 0x40 to register 0x05.
2. Wait at least  $1 \text{ ms} + 1.3 \times t_{\text{stop}}$  (where  $t_{\text{stop}}$  is specified by register 0x1A).

3. If desired, reconfigure by returning to step 4 of initialization sequence.

Exit:

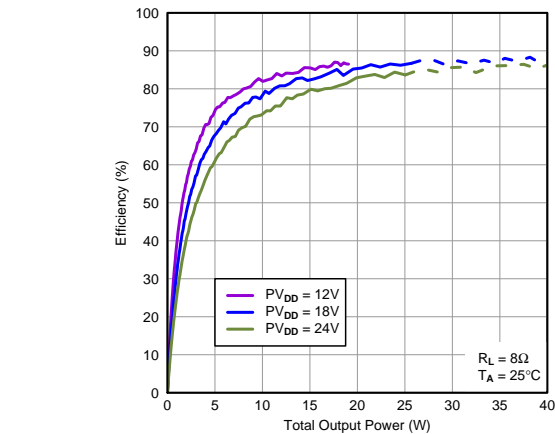
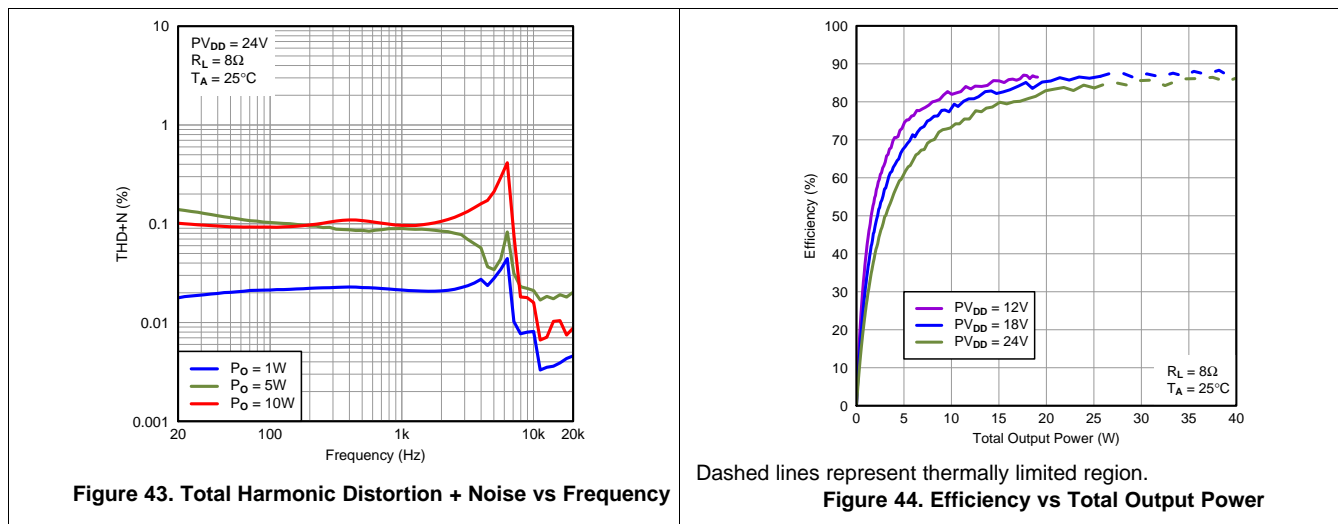
1. Write 0x00 to register 0x05 (exit shutdown command may not be serviced for as much as 240 ms after trim following AVDD/DVDD power-up ramp).
2. Wait at least 1 ms + 1.3 ×  $t_{start}$  (where  $t_{start}$  is specified by register 0x1A).
3. Proceed with normal operation.

#### 11.2.1.2.4.4 Power-Down Sequence

Use the following sequence to power down the device and its supplies:

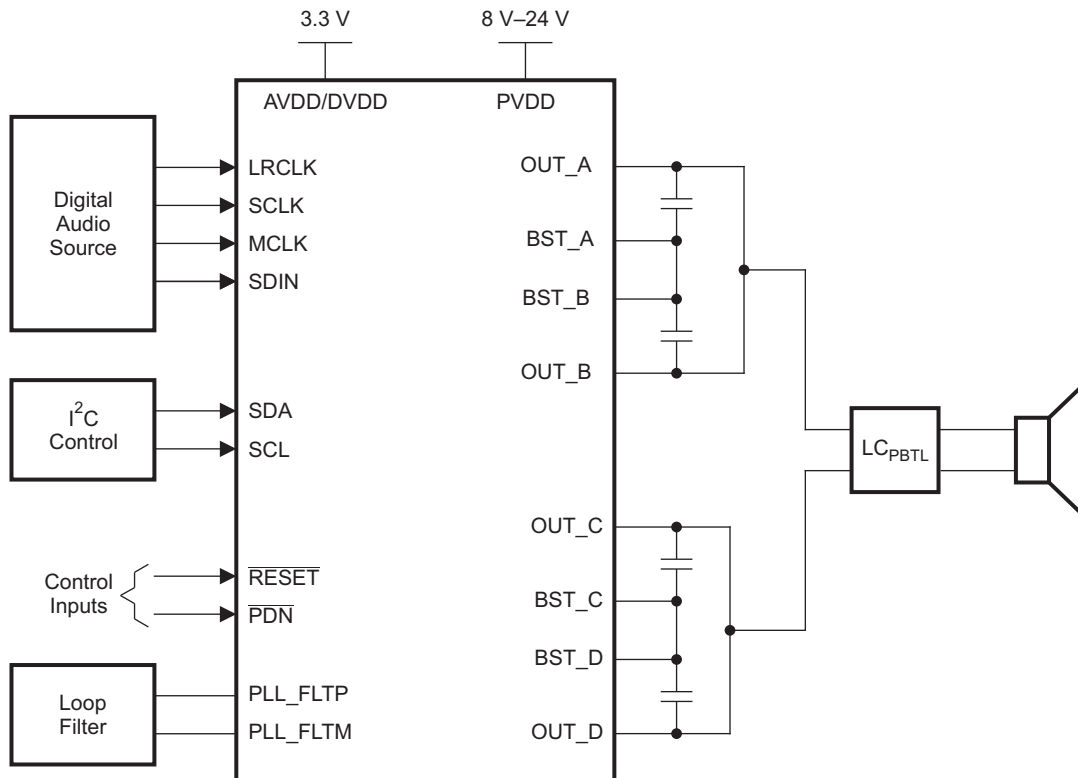
1. If time permits, enter shutdown (sequence defined above); else, in case of sudden power loss, assert  $\overline{PDN} = 0$  and wait at least 2 ms.
2. Assert  $\overline{RESET} = 0$ .
3. Drive digital inputs low and ramp down PVDD supply as follows:
  - Drive all digital inputs low after  $\overline{RESET}$  has been low for at least 2  $\mu$ s.
  - Ramp down PVDD while ensuring that it remains above 8 V until  $\overline{RESET}$  has been low for at least 2  $\mu$ s.
4. Ramp down AVDD/DVDD while ensuring that it remains above 3 V until PVDD is below 6 V and that it is never more than 2.5 V below the digital inputs.

#### 11.2.1.3 Application Curves



Dashed lines represent thermally limited region.

## 11.2.2 Mono Parallel Bridge Tied Load Application



B0264-26

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**Figure 45. TAS5727 Mono Application**

### 11.2.2.1 Design Requirements

Table 28 lists the design parameters for this example.

**Table 28. Design Parameters**

| PARAMETER         | EXAMPLE                                           |
|-------------------|---------------------------------------------------|
| Low Power Supply  | 3.3 V                                             |
| High Power Supply | 8 V to 26 V                                       |
| Host Processor    | I <sup>2</sup> S Compliant Master                 |
|                   | I <sup>2</sup> C Compliant Master                 |
|                   | GPIO Control                                      |
| Output Filters    | Inductor-Capacitor Low-Pass Filter <sup>(1)</sup> |
| Speaker           | 2-Ω minimum                                       |

(1) Refer to [SLOA119](#) for a detailed description of the filter design.

### 11.2.2.2 Detailed Design Procedure

Refer to [Detailed Design Procedure](#).

### 11.2.2.3 Application Curves

Refer to [Application Curves](#).

## 12 Power Supply Recommendations

The TAS5727 requires two power supplies: a low voltage, 3.3 V nominal for the pins DVDD, AVDD, and DRVDD, and a high power supply of 8 V to 24 V for the pin PVDD. There is no requirement for power-up sequencing of low and high power supplies; however, TI recommends putting the PDN pin to low before removing the low voltage power supplies to protect the outputs.

### 12.1 DVDD and AVDD Supplies

The AVDD Supply is used to power the analog internal circuit of the device, and needs a well-regulated and filtered 3.3-V supply voltage. The DVDD Supply is used to power the digital circuitry. DVDD needs a well-regulated and filtered 3.3-V supply voltage.

### 12.2 PVDD Power Supply

The TAS5727 class-D audio amplifier requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) and noise is as low as possible. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1  $\mu\text{F}$ , placed as close as possible to the device PVDD leads works best. For filtering lower-frequency noise signals, TI recommends placing a 10  $\mu\text{F}$  or greater capacitor near the audio power amplifier.

## 13 Layout

### 13.1 Layout Guidelines

Class-D switching edges are fast and switched currents are high, so it is necessary to take care when planning the layout of the printed-circuit board. The following suggestions help meet audio, thermal, and EMC requirements.

- TAS5727 uses the PCB for heat sinking; therefore, the PowerPAD™ needs to be soldered to the PCB and adequate copper area and copper vias connecting the top, bottom and internal layers should be used.
- Decoupling capacitors: the high-frequency decoupling capacitors should be placed as close to the supply pins as possible; on the TAS5727, a 1- $\mu\text{F}$  high-quality ceramic capacitor is used. Large (10- $\mu\text{F}$  or greater) bulk power supply decoupling capacitors should be placed near the TAS5727 on the PVDD supplies.
- Keep the current loop from each of the outputs through the output inductor and the small filter capacitor and back to GND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding: TI recommends a big common GND plane. The PVDD decoupling capacitors should connect to GND. The TAS5727 PowerPAD should be connected to GND.
- Output filter: remember to select inductors that can handle the high short-circuit current of the device. The LC filter should be placed close to the outputs.

The [EVM product folder](#) and User's Guide available on [www.ti.com](http://www.ti.com) shows schematic, bill of material, gerber files, and more detailed layout plots.

### 13.2 Layout Example

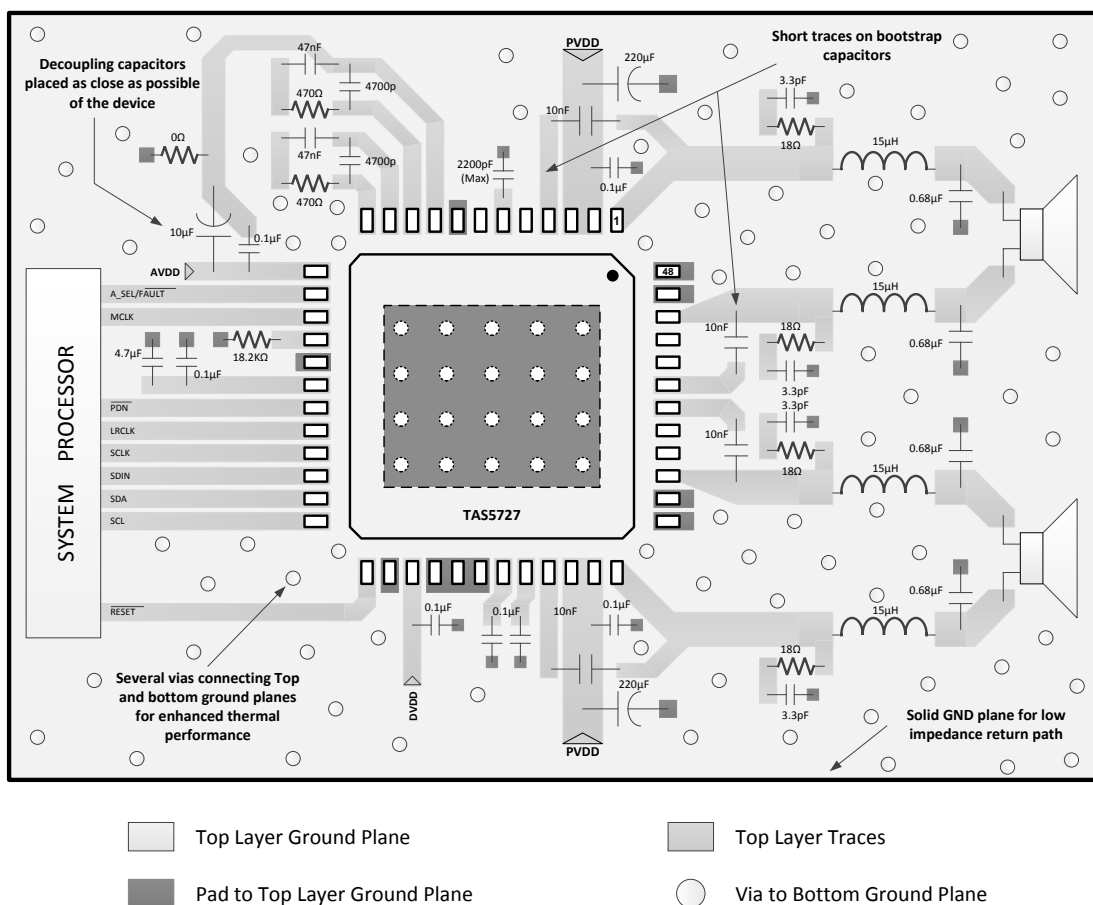


Figure 46. Layout Example

## 14 Device and Documentation Support

### 14.1 Device Support

#### 14.1.1 Development Support

For development support, see the following:

[TAS57xx GDE](#)

### 14.2 Documentation Support

#### 14.2.1 Related Documentation

For related documentation, see the following:

- *TAS5727 25-W Digital Input Amplifier With EQ and 2-Band DRC*, [SLOU299](#)
- *TAS5721-TAS5723EVM User's Guide*, [SLOU346](#)
- *Class-D LC Filter Design*, [SLOA119](#)

### 14.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 14.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 14.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 14.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TAS5727PHP       | ACTIVE        | HTQFP        | PHP             | 48   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | 0 to 85      | TAS5727                 | <a href="#">Samples</a> |
| TAS5727PHPR      | ACTIVE        | HTQFP        | PHP             | 48   | 1000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | 0 to 85      | TAS5727                 | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

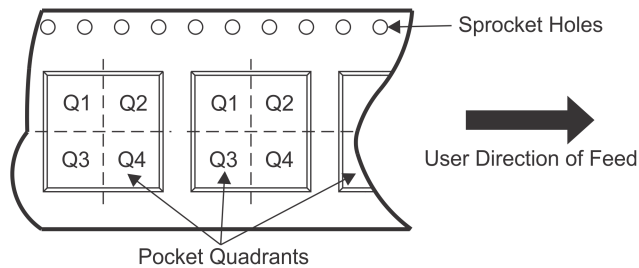
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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



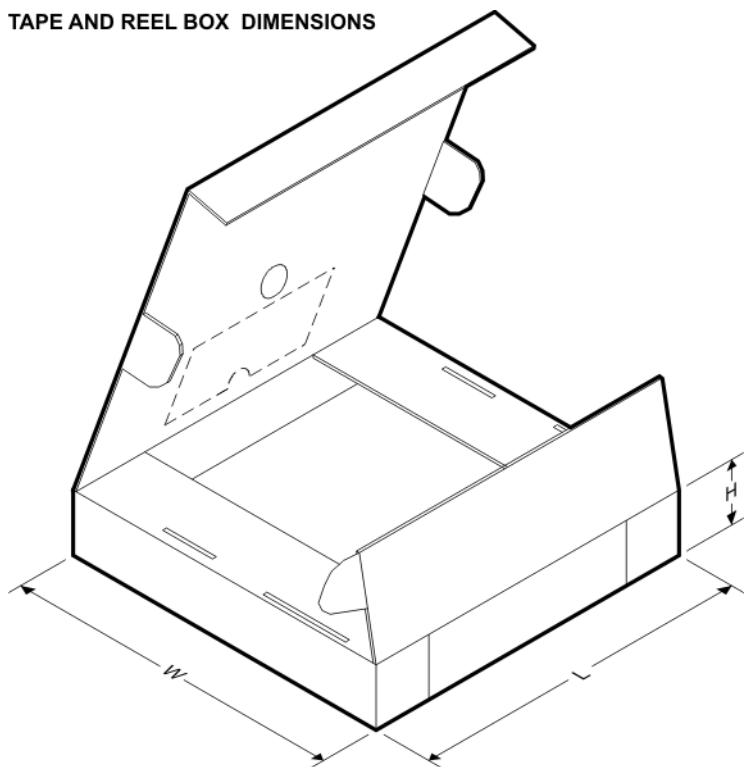
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TAS5727PHPR | HTQFP        | PHP             | 48   | 1000 | 330.0              | 16.4               | 9.6     | 9.6     | 1.5     | 12.0    | 16.0   | Q2            |

**TAPE AND REEL BOX DIMENSIONS**

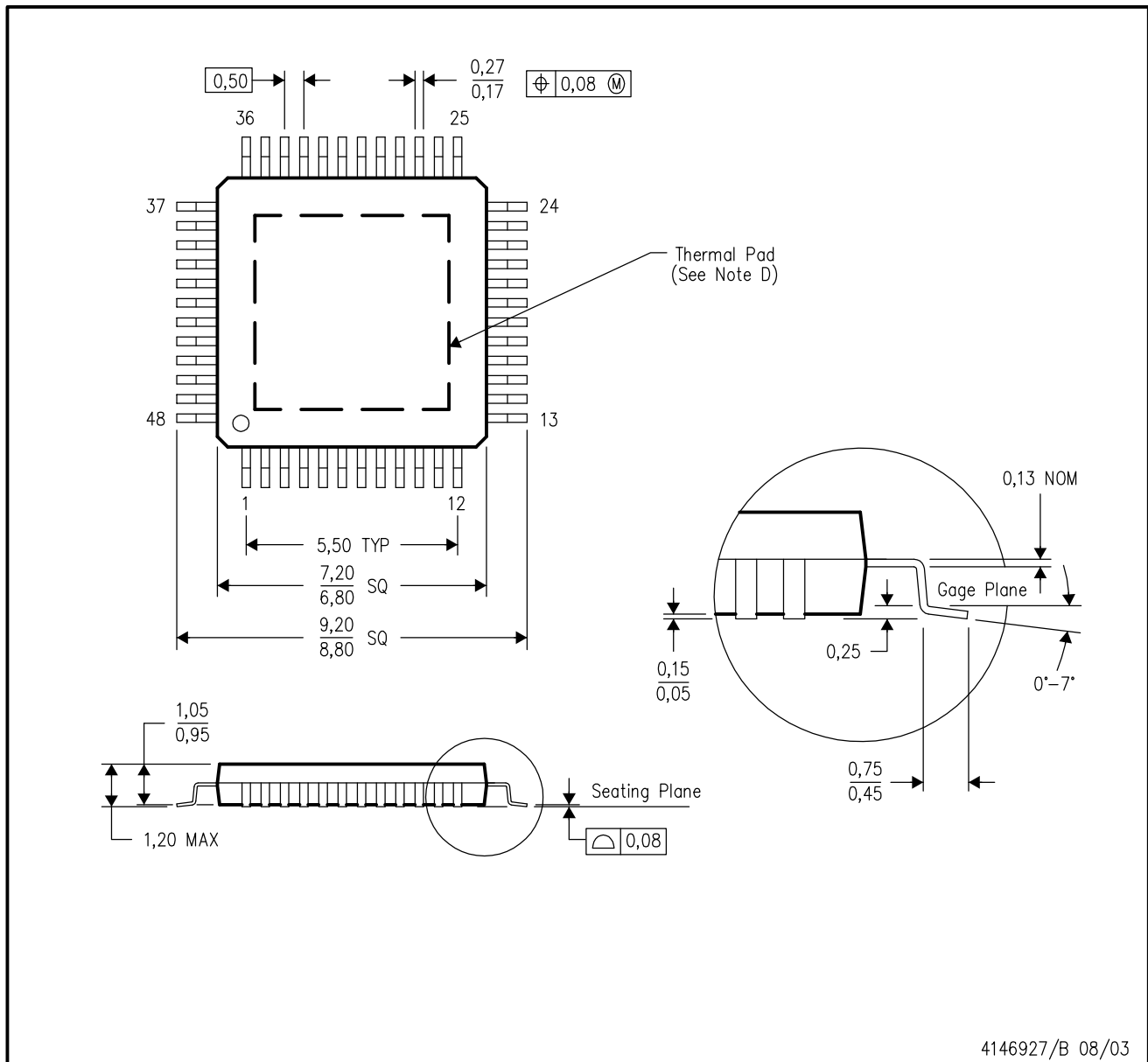


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TAS5727PHPR | HTQFP        | PHP             | 48   | 1000 | 367.0       | 367.0      | 38.0        |

PHP (S-PQFP-G48)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

# THERMAL PAD MECHANICAL DATA

PHP (S-PQFP-G48)

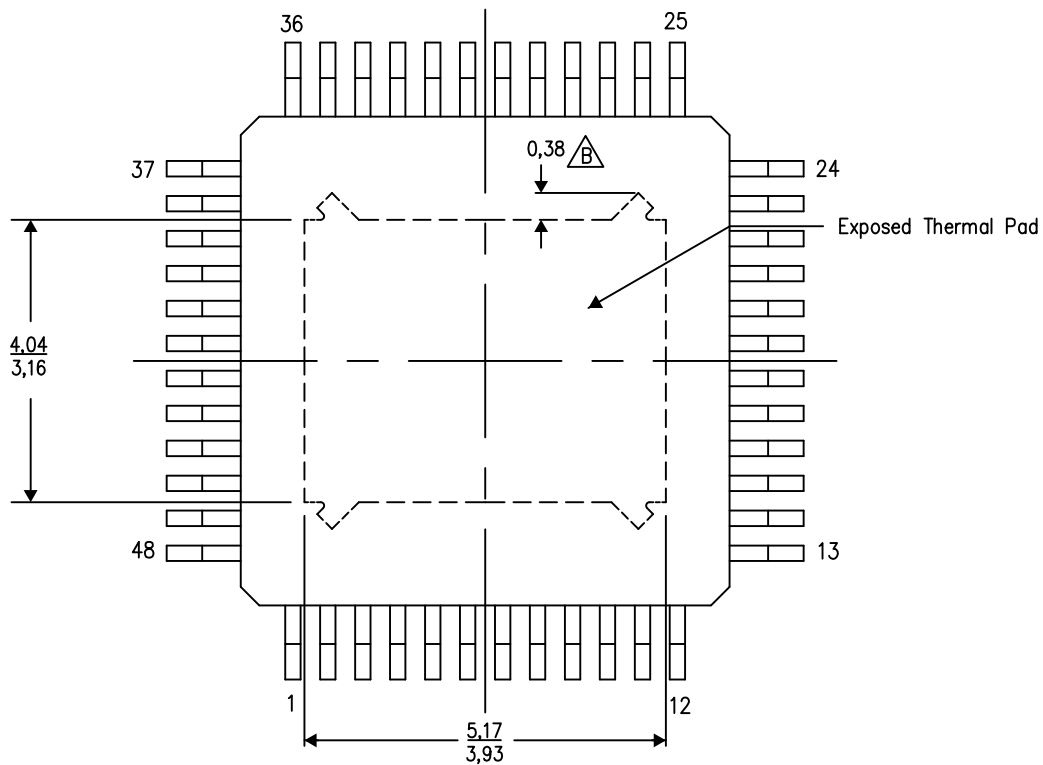
PowerPAD™ PLASTIC QUAD FLATPACK

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206329-9/P 03/15

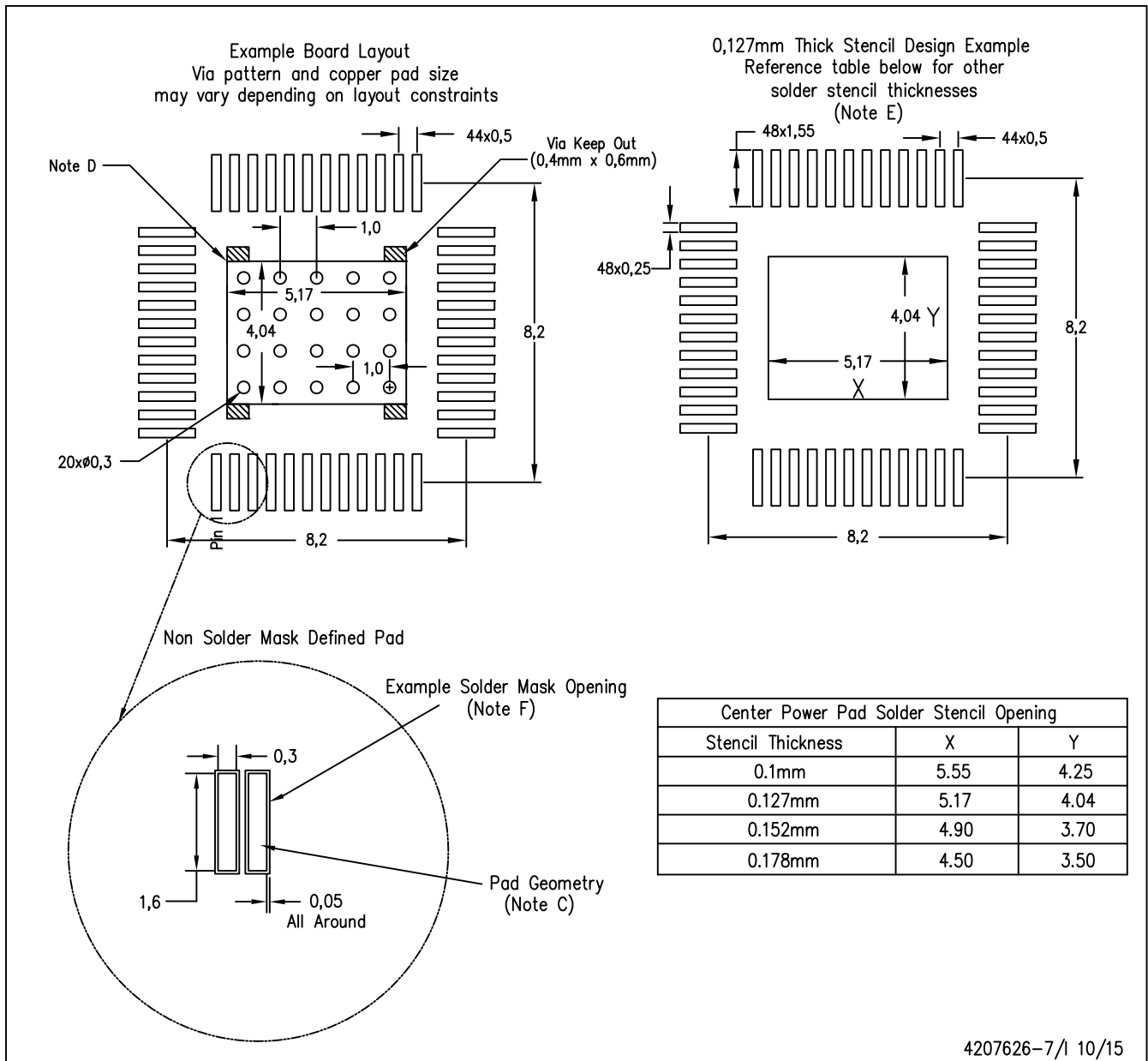
NOTE: A. All linear dimensions are in millimeters

Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PHP (S-PQFP-G48)

PowerPAD™ PLASTIC QUAD FLATPACK



4207626-7/1 10/15

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting options for vias placed in the thermal pad.

PowerPAD is a trademark of Texas Instruments

# THERMAL PAD MECHANICAL DATA

PHP (S-PQFP-G48)

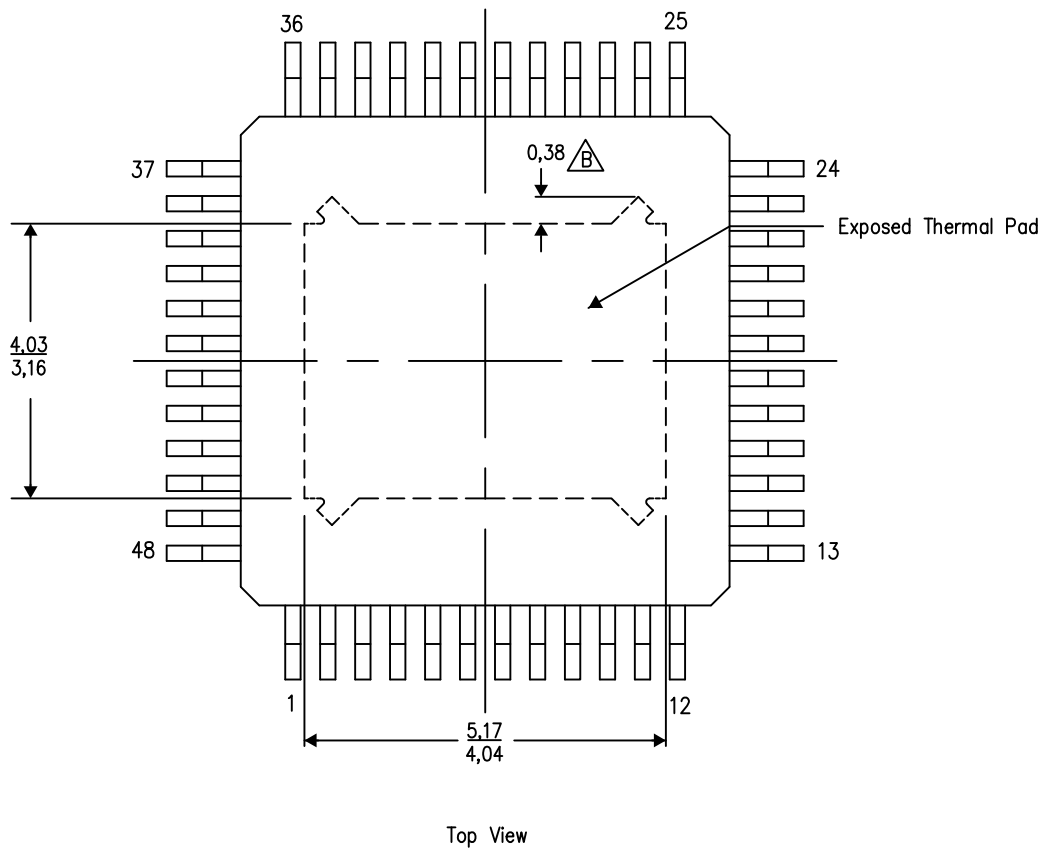
PowerPAD™ PLASTIC QUAD FLATPACK

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).


The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206329-18/P 03/15

NOTE: A. All linear dimensions are in millimeters

 B. Tie strap features may not be present.

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| Data Converters              | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>                       |
| DLP® Products                | <a href="http://www.dlp.com">www.dlp.com</a>                                         |
| DSP                          | <a href="http://dsp.ti.com">dsp.ti.com</a>                                           |
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| Interface                    | <a href="http://interface.ti.com">interface.ti.com</a>                               |
| Logic                        | <a href="http://logic.ti.com">logic.ti.com</a>                                       |
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|                               |                                                                                          |
|-------------------------------|------------------------------------------------------------------------------------------|
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| Computers and Peripherals     | <a href="http://www.ti.com/computers">www.ti.com/computers</a>                           |
| Consumer Electronics          | <a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>                   |
| Energy and Lighting           | <a href="http://www.ti.com/energy">www.ti.com/energy</a>                                 |
| Industrial                    | <a href="http://www.ti.com/industrial">www.ti.com/industrial</a>                         |
| Medical                       | <a href="http://www.ti.com/medical">www.ti.com/medical</a>                               |
| Security                      | <a href="http://www.ti.com/security">www.ti.com/security</a>                             |
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