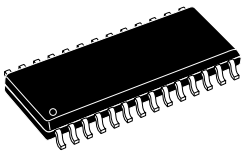
STA120

DIGITAL AUDIO INTERFACE RECEIVER

- MONOLITHIC CMOS RECEIVER
- 3.3V SUPPLY VOLTAGE
- LOW-JITTER, ON-CHIP CLOCK RECOVERY 256xFs OUTPUT CLOCK PROVIDED
- SUPPORTS: AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340/1201 PROFESSIONAL AND CONSUMER FORMATS
- EXTENSIVE ERROR REPORTING REPEAT LAST SAMPLE ON ERROR OPTION



SO28

ORDERING NUMBER: STA120D

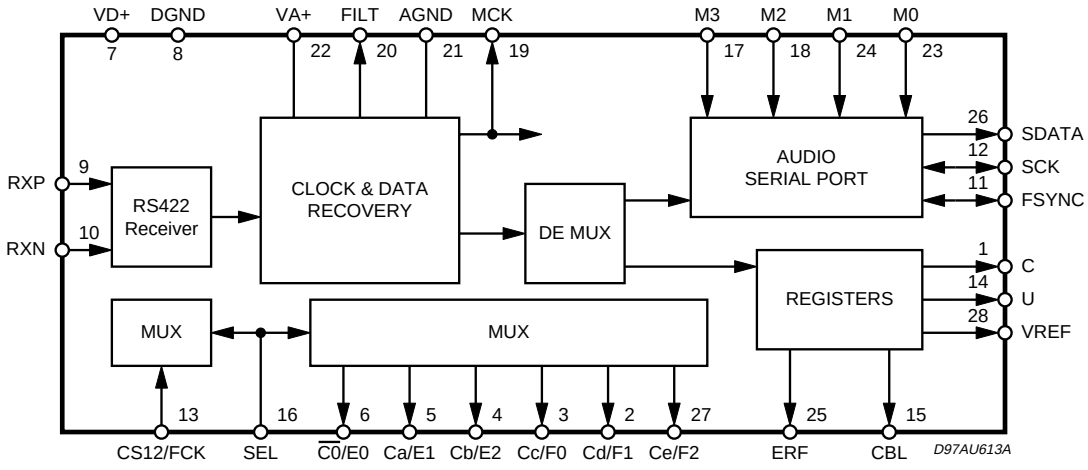
DESCRIPTION

The STA120 is a monolithic CMOS device that receives and decodes audio data according to the AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340/1201 interface standards.

The STA120 recovers the clock and synchronization signals and de-multiplexes the audio and digital data. Differential or single ended inputs can be decoded.

The STA120 de-multiplexes the channel, user and validity data directly to serial output pins with dedicated output pins for the most important channel status bits.

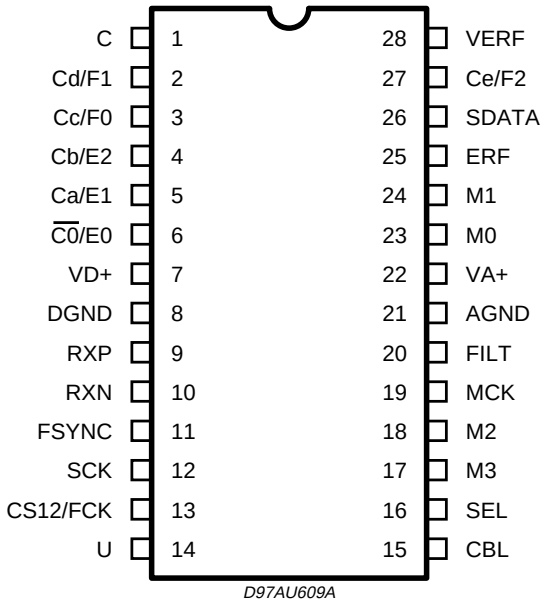
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{D+}, V_{A+}	Power Supply Voltage	4	V
V_{IN}	Input Voltage (excluding pins 9, 10)	-0.3 to V_D+ +0.3	V
T_{amb}	Ambient Operating Temperature (power applied)	-30 to +85	°C
T_{stg}	Storage Temperature	-40 to 150	°C

PIN CONNECTIONS (Top view)



PINS DESCRIPTION

N.	Name	Description
Power Supply		
7	V_{D+}	Positive Digital Power.Positive supply for the digital section. Nominally 3.3V.
8	DGND	Digital Ground.Ground for the digital section.
21	AGND	Analog Ground.Ground for the analog section. AGND should be connected to same ground as DGND.
22	V_{A+}	Positive Analog Power.Positive supply for the analog section. Nominally 3.3V.
Audio Output Interface		
11	FSYNC	Frame Sync.Delineates the serial data and may indicate the particular channel, left or right and may be an input or output. The format is based on M0, M1, M2 and M3 pins.
12	SCK	Serial Clock.Serial clock for SDATA pin which can be configured (via the M0, M1, M2 and M3 pins) as an input or output and can sample data on the rising or falling edge. As an output, SCK will generate 32 clocks for every audio sample. As an input, 32 SCK periods per audio sample must be provided in all normal modes.
17, 18, 23, 24	M2, M3, M1, M0	Serial Port Mode Selects.Selects the format of Fsync and the sample edge of SCK with respect to SDATA.
26	SDATA	Serial Data. Audio data serial output pin.

PINS DESCRIPTION (continued)

N.	Name	Description
Control Pins		
1	C	Channel Status Output. Received channel status bit serial output port. FSYNC may be used to latch this bit externally. Except in I^2S modes when this pin is updated at the active edge off Fsync.
2	Cd	Channel Status Output Bits.These pin are dual Function with the "C" bits selected when SEL is high. Channel status information is displayed for the channel selected by CS12. $\overline{C0}$, which is channel status bit 0, defines professional ($\overline{C0}$ = 0) or consumer ($\overline{C0}$ = 1) mode and further controls the definition of the Ca-Ce pins. These pins are updated with the rising edge of CBL.
	F1	Frequency reporting Bits.Encoder sample frequency information that is enabled by bringing SEL low. A proper clock on FCK must be input for at least two thirds of a channel status block for these pins to be valid. They are updated three times per block, starting at the block boundary.
3	Cc	Channel Status Output Bits.These pin are dual Function with the "C" bits selected when SEL is high. Channel status information is displayed for the channel selected by CS12. $\overline{C0}$, which is channel status bit 0, defines professional ($\overline{C0}$ = 0) or consumer ($\overline{C0}$ = 1) mode and further controls the definition of the Ca-Ce pins. These pins are updated with the rising edge of CBL.
	F0	Frequency reporting Bits.Encoded sample frequency information that is enabled by bringing SEL low. A proper clock on FCK must be input for at least two thirds of a channel status block for these pins to be valid. They are updated three times per block, starting at the block boundary.
4	Cb	Channel Status Output Bits.These pin are dual Function with the "C" bits selected when SEL is high. Channel status information is displayed for the channel selected by CS12. $\overline{C0}$, which is channel status bit 0, defines professional ($\overline{C0}$ = 0) or consumer ($\overline{C0}$ = 1) mode and further controls the definition of the Ca-Ce pins. These pins are updated with the rising edge of CBL.
	E2	Error Condition.Encoded error information that is enabled by bringing SEL low. The error codes are prioritized and latched so that the error code displayed is the highest level of error since the last clearing of the error pins. Clearing is accomplished by bringing SEL high for more than 8 MCK cycles.
5	Ca	Channel Status Output Bits.These pin are dual Function with the "C" bits selected when SEL is high. Channel status information is displayed for the channel selected by CS12. $\overline{C0}$, which is channel status bit 0, defines professional ($\overline{C0}$ = 0) or consumer ($\overline{C0}$ = 1) mode and further controls the definition of the Ca-Ce pins. These pins are updated with the rising edge of CBL.
5	E2	Error Condition.Encoded error information that is enabled by bringing SEL low. The error codes are prioritized and latched so that the error code displayed is the highest level of error since the last clearing of the error pins. Clearing is accomplished by bringing SEL high for more than 8 MCK cycles.
6	$\overline{C0}$	Channel Status Output Bits.These pin are dual Function with the "C" bits selected when SEL is high. Channel status information is displayed for the channel selected by CS12. $\overline{C0}$, which is channel status bit 0, defines professional ($\overline{C0}$ = 0) or consumer ($\overline{C0}$ = 1) mode and further controls the definition of the Ca-Ce pins. These pins are updated with the rising edge of CBL.
	E0	Error Condition.Encoded error information that is enabled by bringing SEL low. The error codes are prioritized and latched so that the error code displayed is the highest level of error since the last clearing of the error pins. Clearing is accomplished by bringing SEL high for more than 8 MCK cycles.
13	CS12	Channel Select.This pin is also dual function and is selected by bringing SEL high. CS12 selects sub-frame1 (when low) or sub-frame2 (when high) to be displayed by channel status pins $\overline{C0}$ an Ca through Ce.
	FCK	Frequency Clock.Frequency Clock input that is enabled by bringing SEL low. FCK is compared to the received clock frequency with the value displayed on F2 through F0. Nominal input value is 6.144MHz.
14	U	User Bit.Received user bit serial output port, FSYNC may be used to latch this bit externally. Except in I2S modes when this pin is updated at the active edge off Fsync.
15	CBL	Channel Status Block Start.The channel status block output is high for the first four bytes of channel status and low for the last 20 bytes.

PINS DESCRIPTION (continued)

N.	Name	Description
16	SEL	Select.Control pin that selects either channel status information (SEL = 1) or error and frequency information (SEL = 0) to be displayed on six ($\overline{C0}$, Ca Cb, Cc, Cd, Ce) pins.
27	Ce	Channel Status Output Bits.These pin are dual Function with the "C" bits selected when SEL is high. Channel status information is displayed for the channel selected by CS12. $\overline{C0}$, which is channel status bit 0, defines professional ($\overline{C0}$ = 0) or consumer ($\overline{C0}$ = 1) mode and further controls the definition of the Ca-Ce pins. These pins are updated with the rising edge of CBL.
	F2	Frequency reporting Bits.Encoded sample frequency information that is enabled by bringing SEL low. A proper clock on FCK must be input for at least two thirds of a channel status block for these pins to be valid. They are updated three times per block, starting at the block boundary.
28	VERF	Validity + Error Flag. A logical OR'ing of the validity bit from the received data and the error flag. May be used by interpolation filters to interpolate through errors.
Receiver Interface		
9	RXP	Line Receiver. (RS422 compatible)
10	RXN	Line Receiver. (RS422 compatible)
Phase Locked Loop		
19	MCK	Master Clock.Low Jitter clock output of 256 times the received sample frequency.
20	FILT	Filter.An external 330 Ohm resistor and 0.47µF capacitor in parallel with a 15nF capacitor is required from FILT pin to analog ground.
25	ERF	Error Flag,Signals that an error has occurred while receiving the audio sample currently being read from the serial port. Three errors cause ERF to go high: a parity or biphase coding violation during the current sample, or an out of lock PLL receiver.

DIGITAL CHARACTERISTICS (T_{amb} = 25°C; V_{D+}, V_{A+} = 3.3V ±10%)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{D+},V_{A+}	Power supply voltage Range		3.0	3.3	3.6	V
V_{IH}	High-Level Input Voltage		2.0			V
V_{IL}	Low-Level Input Voltage				+0.8	V
V_{OH}	High-Level Output Voltage	I_O = 200µA	V_{DD}-1.0			V
V_{OL}	Low-Level Output Voltage	I_O = 3.2mA			0.4	V
I_{in}	Input Leakage Current			1.0	10	µA
F_S	Input Sample Frequency	(Note 1)	25		96	kHz
MCK	Master Clock frequency	(Note 1)	6.4	256xFS	25	MHz
t_j	MCK Clock Jitter			300		ps RMS
	MCK Duty Cycle	(high time/cycle time)		50		%
I_{dd_ST}	Static I_{dd} (MCK = 0)			0.1	1	mA
I_{dd_DYN}	Dynamic Idd			6	15	mA

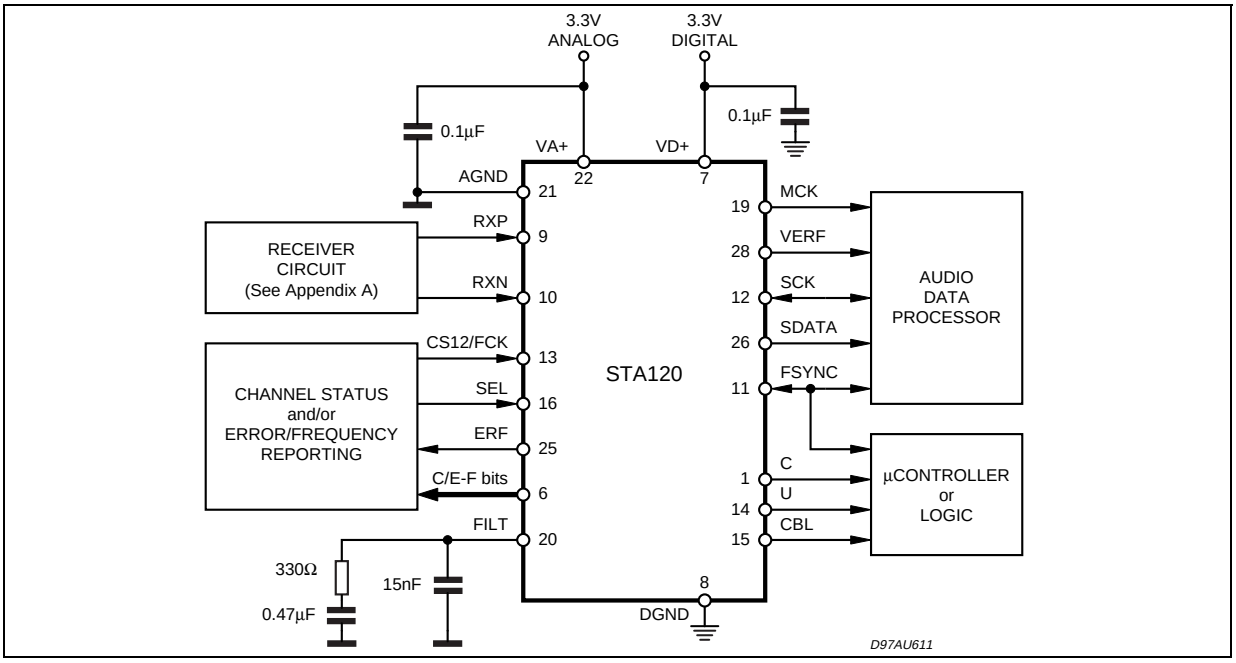
Note 1: FS is defined as the incoming audio sample frequency per channel.

SWITCHING CHARACTERISTICS - SERIAL PORTS (T_{amb} = 25°C; V_{D+}, V_{A+} = 3.3V ±10%)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{sck}	SCK Frequency	(Note 2)		OWRx32		Hz

Note 2: The output word rate, OWR, refers to the frequency at which an audio sample is output from the part. (A stereo pair is two audio samples). Therefore, in Master mode, there are always 32 SCK periods in one audio sample. In Slave mode 32 SCK periods must be provided in most serial port formats.

Figure 1. Circuit Diagram



GENERAL DESCRIPTION

The STA120 is a monolithic CMOS circuit that receives and decodes audio and digital data according to the AES/EBU, IEC 958, S/PDIF, and EIAJ CP-340/1201 interface standards.

It contains a RS422 line receiver and Phase-Locked Loops (PLL) that recovers the clock and synchronization signals and de-multiplexes the audio and digital data. The STA120 de-multiplexes the channel status, user and validity information directly to serial output pins with dedicated pins for the most important channel status bits.

Line Receiver

The line receiver can decode differential as well as single ended inputs. The receiver consits of a differential input Schmitt trigger with 50mV of hysteresis. The hysteresis prevents noisy signals from corrupting the phase detector. Appendix A contains more information on how to configure the line receivers for differential and single ended signals.

Clocks and Jitter Attenuation

The primary function of this chip is to recover audio data and low jitter clocks from a digital audio transmission line. The clocks that can be generated are MCK (256xFS), SCK (64xFS), and FSYNC (FS or 2xFS). MCK is the output of the voltage controlled oscillator which is a component of the PLL. The PLL consists of phase and frequency detectors, a second-order loop filter, and a voltage controlled oscillator.

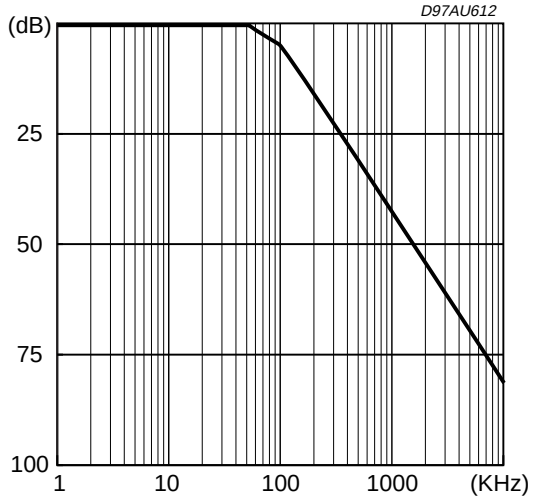
All components of the PLL are on chip with the exception of a resistor and capacitors used in the loop filter. This filter is connected between the FILT pin and AGND. The closed-loop transfer function, which specifies the PLL's jitter attenuation characteristics, is shown in Figure 2.

The loop will begin to attenuate jitter at approximately 25kHz with another pole at 80kHz and will have 50dB of attenuation by 1MHz. Since most data jitter introduced by the transmission line is high in frequency, it will be strongly attenuated.

Multiple frequency detectors are used to minimize the time it takes the PLL to lock to the incoming data stream and to prevent false lock conditions. When the PLL is not locked to the incoming data stream, the

frequency detectors pull the VCO frequency within the lock range of the PLL. When no digital audio data is present, the VCO frequency is pulled to its minimum value.

Figure 2. Jitter Attenuator Characteristics.



As a master, SCK is always MCK divided by four, producing a frequency of 64 x FS. In the STA120, FSYNC is always generated from the incoming data stream. When FSYNC is generated from the data its edges are extracted at times when intersymbol interference is at a minimum. This provides a sample frequency clock that is as spectrally pure as the digital audio source clock for moderate length transmission lines.

STA120 DESCRIPTION

The STA120 does not need a microprocessor to handle the non-audio data (although a micro may be used with the C and U serial ports). Instead, dedicated pins are available for the most important channel status bits. The STA120 is a monolithic CMOS circuits that receives and decodes digital audio data which was encoded according to the digital audio interface standards. It contains a clock and data recovery utilizing an on-chip phase-locked loop. The output data is output through a configurable serial port that supports 14 formats.

The channel status and user data have their own serial pins and the validity flag is OR'ed with the ERF flag to provide a single pin, VERF, indicating that the audio output may not be valid. This pin may be used by interpolation filters that provide error correction.

Audio Serial Port

The audio serial port is used primarily to output audio data and consists of three pins: SCK, FSYNC and SDATA. These pins are configured via four control pins: M0, M1,M2,and M3.M3 selects between eight normal serial formats (M3 = 0), and six special formats (M3 = 1).

Normal Modes (M3 = 0)

When M3 is low, the normal serial port formats shown in Figure 3 are selected using M2, M1 and M0. These formats are also listed in Table 1 wherein the first word part the format number (Out-In) indicates whether FSYNC and SCK are outputs from the STA120 or are inputs.

The next word (L/R-WSYNC) indicates whether FSYNC indicates the particular channel or just delineates each word. If an error occurs (ERF=1) while using one of these formats, the previous valid audio data for that channel will be output.

If the STA120 is not locked, the last sample is repeated at the output. In some modes FSYNC and SCK are outputs and in others they are inputs. In Table 3, LSBJ is short for LSB justified where the LSB is justified to the end of the audio frame and the MSB varies with word length. As outputs the STA120 generates 32 SCK periods per audio sample (64 per stereo sample) and, as inputs, 32 SCK periods must be provided per audio sample.

When FSYNC and SCK are inputs, one stereo sample is double buffered. For those modes which output 24 bits of audio data, the auxiliary bits will be included. If the auxiliary bits are not used for audio data, they must be masked off.

Table 1. Normal Audio Port Modes (M3 = 0)

M2	M1	M0	Format
0	0	0	0 - Out, L/R, 16-24 Bits
0	0	1	1 - In, L/R, 16-24 Bits
0	1	0	2 - Out, L/R, I^2S Compatible
0	1	1	3 - In, L/R, I^2S Compatible
1	0	0	4 - Out, WSYNC, 16-24 Bits
1	0	1	5 - Out, L/R, 16 Bits LSBJ
1	1	0	6 - Out, L/R, 18 Bits LSBJ
1	1	1	7 - Out, L/R, MSB Last

Special Modes (M3 = 1)

When M3 is high, the special audio modes described in Table 2 are selected via M2, M1, and M0. In formats 8, 9, and 10, SCK, FSYNC, and SDATA are the same as in formats 0, 1, and 2 respectively; however, the recovered data is output as is even if ERF is high, indicating an error. (In modes 0-2 the previous valid sample is output).
When out of lock invalid data are sent to the output and the ERF pin goes high.
Format 11 is similar to format 0 except that SCK is an input and FSYNC is an output.
In this mode FSYNC and SDATA are synchronized to the incoming SCK, This mode may be useful when writing data to storage.

Table 2. Special Audio Port Modes (M3 = 1)

M2	M1	M0	Format
0	0	0	8 - Format 0 - No repeat on error
0	0	1	9 - Format 1 - No repeat on error
0	1	0	10 - Format 2 - No repeat on error
0	1	1	11 - Format 0 - Async. SCK input
1	0	0	12 - Received NRZ Data
1	0	1	13 - Received Bi-phase Data
1	1	0	14 - Reserved
1	1	1	15 - STA120 Reset

Format 12 is similar to format 7 except that SDATA is the entire data word received from the transmission line including the C, U, V, and P bits, with zeros in place of the preamble. In format 13 SDATA contains the entire biphase encoded data from the transmission line including the preamble, and SCK is twice the normal frequency.

The normal two frame delay of data from input to output is reduced to only a few bit periods in formats 12 and 13. However, the C, U, V bits and error codes follow their normal pathways and therefore follow the output data by nearly two frames. Figure 4.... illustrates formats 12 and 13. Format 14 is reserved and not presently used, and format 15 causes the STA120 to go into a reset state. While in reset all outputs will be inactive except MCK. The STA120 incorporates a Power-on Reset to avoid a Reset at power-up.

C, U, VERF, ERF, and CBL Serial Outputs

The C and U bits and CBL are output one SCK period prior to the active edge of FSYNC in all serial port formats except 2, 3 and 10 (I^2S modes). The active edge of FSYNC may be used to latch C, U, and CBL externally. In formats 2, 3 and 10, the C and U bits and CBL are updated with the active edge of FSYNC. The validity + error flag (VERF) and the error flag (ERF) are always updated at the active edge of FSYNC.

This timing is illustrated in Figure 5.

The C output contains the channel status bits with CBL rising indicating the start of a new channel status block. CBL is high for the first four bytes of channel status (32 frames or 64 samples) and low for the last 20 bytes of channel status (160 frames or 320 samples).

The U output contains the User Channel data. The V bit is OR'ed with the ERF flag and output on the VERF pin. This indicates that the audio sample may be in error and can be used by interpolation filters to interpolate through the error.

ERF being high indicates a serious error occurred on the transmission line. There are three errors that cause ERF to go high: a parity error or biphase coding violation during that sample, or an out of lock PLL receiver. Timing for the above pins is illustrated in Figure 5.

Multifunction Pins

There are seven multifunction pins which contain either error and received frequency information, or channel status information, selectable by SEL.

Figure 3. Audio Serial Port Formats

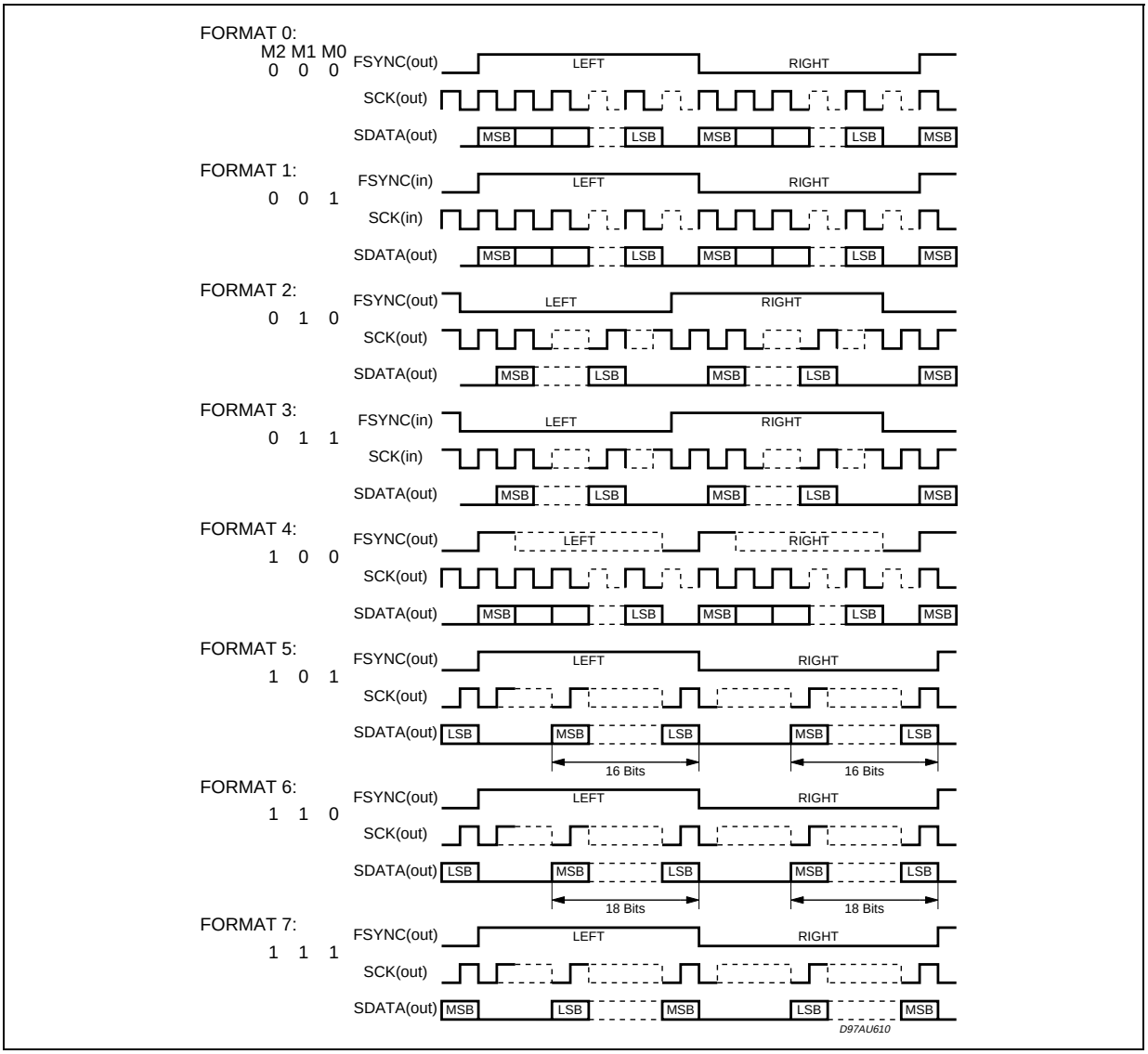
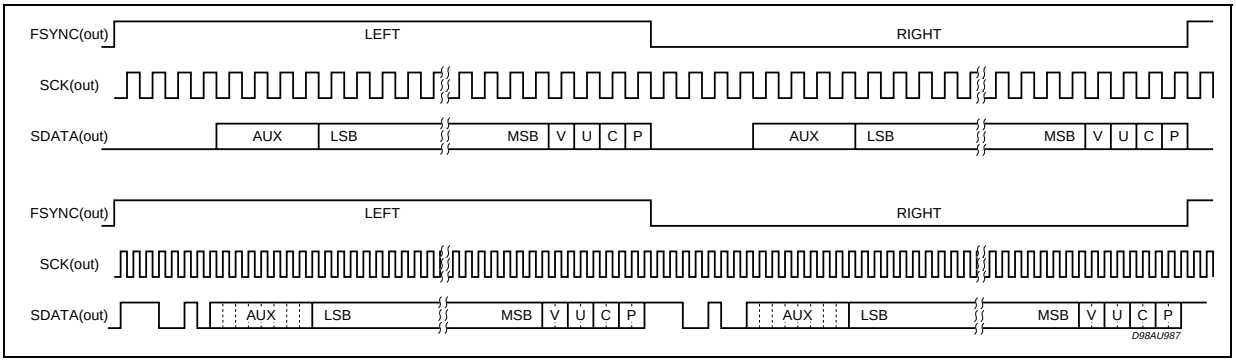


Figure 4. Special Audio Port Formats 12 and 13



Error And Frequency Reporting

When SEL is low, error and received frequency information are selected.

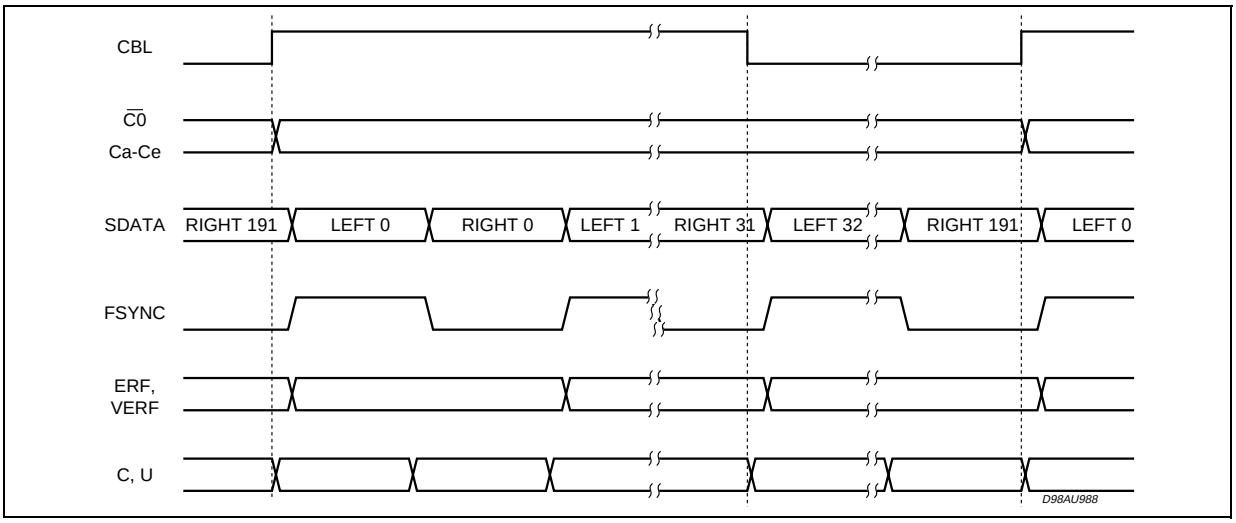
The error information is encoded on pins E2, E1, and E0, and is decoded as shown in Table 3. When an error occurs, the corresponding error code is latched.

Clearing is then accomplished by bringing SEL high for more than eight MCK cycles. The errors have a priority associated with their error code, with validity having the lowest priority that occurred since the last clearing will be selected.

Table 3. Error Decoding

E2	E1	E0	Error
0	0	0	No Error
0	0	1	Validity Bit High
0	1	0	Confidence flag
0	1	1	Slipped Sample
1	0	0	CRC Error (PRO only)
1	0	1	Parity Error
1	1	0	Bi-Phase Coding Error
1	1	1	No Lock

Figure 5. CBL Timing



The validity flag indicates that the validity bit for a previous sample was high since the last clearing of the error codes. The slipped sample error can only occur when FSYNC and SCK of the audio serial port are inputs. In this case, if FSYNC is asynchronous to the received data rate, periodically a stereo sample will be dropped or reread depending on whether the read rate is slower or faster than the received data rate . When this occurs, the slipped sample error code will appear on the "E" pins.

The CRC error is updated at the beginning of a channel status block, and is only valid when the professional format of channel status data is received. This error is indicated when the STA120 calculated CRC value does not match the CRC byte of the channel status block or when a block boundary changes (as in removing samples while editing).

The parity error occurs when the incoming sub-frame does not have even parity as specified by the standards. The biphase coding error indicates a biphase coding violation occurred. The no lock error indicates that the PLL is not locked onto the incoming data stream. Lock is achieved after receiving three frame preambles then one block preamble, and is lost after not receiving four consecutive frame preambles.

The receive frequency information is encoded on pins F2, F1 and F0, and is decoded as shown in Table 6. The on-chip frequency comparator compares the received clock frequency to an externally supplied 6.144MHz clock which is input on the FCK pin. The "F" pins. The clock on FCK must be valid for two thirds of a block for the "F" pins to be accurate.

Table 4. Sample Frequency Decoding

F2	F1	F0	Error
0	0	0	Out of Range
0	0	1	48KHz ±4%
0	1	0	44.1KHz ±4%
0	1	1	32KHz ±4%
1	0	0	48KHz ±400ppm
1	0	1	44.1KHz ±400ppm
1	1	0	44.056KHz ±400ppm
1	1	1	32KHz ±400ppm

Channel Status Reporting

When SEL is high, channel status is displayed on C0, and Ca-Ce for the channel selected by CS12. If CS12 is low, channel status for sub-frame1 is displayed, and if CS12 is high, channel status for subframe 2 is displayed. the contents of Ca-Ce depend upon the C0 professional/consumer bit. The information report is shown in Table 5.

Table 5. Channel Status Pins

Pin	Professional	Consumer
C0	0 (low)	1 (high)
Ca	C1	C1
Cb	EM0	C2
Cc	EM1	C3
Cd	C9	ORIG
Ce	CRCE	IGCAT

Professional Channel Status (C0 = 0)

When C0 is low, the received channel status block is encoded according to the professional / broadcast format. The Ca through Ce pins are defined for some of the more important professional bits. As listed in Table 5, Ca is the inverse of channel status bit1. Therefore, if the incoming channel status bit1. Therefore, if the incoming channel status bit 1 is 1, Ca, defined as C1, will be 0. C1 indicates whether audio (C1 = 1) or non-audio (C1 = 0) data is being received. Cb and Cc, defined as EM0 and EM1 respectively, indicate emphasis and are encoded version of channel status bits 2, 3, and 4. The decoding is listed in Table 6. Cd, defined as C9, is the inverse of channel status bit 9, which gives some indication of channel status bit 9, which gives some indication of channel mode. (Bit 9 is also defined as bit 1 of byte 1). When Ce, defined as CRCE, is low, the STA120 calculated CRC value does not match the received CRC value. This signal may be used to qualify Ca through Cd. If Ca through Ce are being displayed, Ce going low can indicate not to update the display.

Table 6. Emphasis Encoding

EM1	EM0	C2	C3	C4	Emphasis
0	0	1	1	1	CCITT J.17 emphasis
0	1	1	1	0	50/15ms emphasis
1	0	1	0	0	No emphasis
1	1	0	0	0	Not indicated

Consumer Channel Status (C0 = 1)

When C0 is high, the received channel status block is encoded according to the consumer format. In this case Ca through Ce are defined differently as shown in Table 5.

Ca is the inverse of channel status bit 1, C1, indicating audio (C1 = 1) or non-audio (C1 = 0). Cb is defined as the inverse of channel status bit 2, C2, which indicates copy inhibit/copyright information Cc, defined as C3, is the emphasis bit of channel status, with C3 low indicating the data has had pre-emphasis added.

The audio standards, in consumer mode, describe bit 15, L, as the generation status which indicates whether the audio data is an original work or a copy (1st generation or higher). The definition of the Lbit is reversed for three category codes: two broadcast codes, and laser-optical (CD's). Therefore, to interpret the L bit properly, the category code must be decoded. The STA120 does this decoding internally and provides the ORIG signal that, when low, indicates that the audio data is original over all category codes.

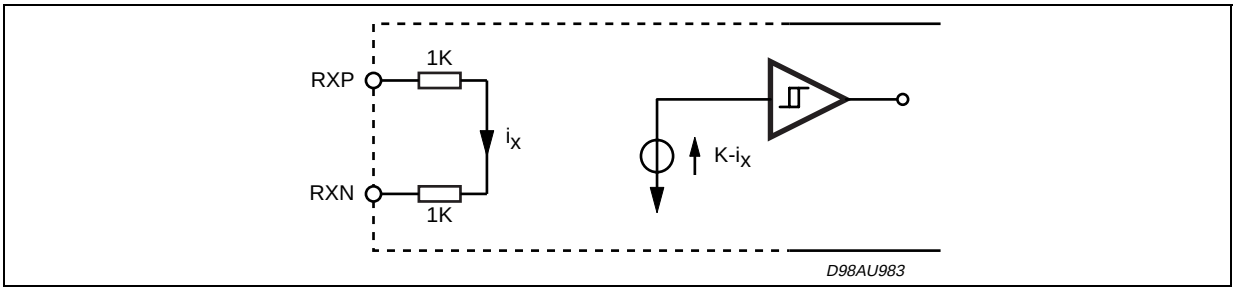
SCMS

The consumer audio standards also mention a serial copy management system, SCMS, for dealing with copy protection of copyrighted works. SCMS is designed to allow unlimited duplication of the original work, but no duplication of any copies of the original. This system utilizes the channel status bit 2, Copy, and channel status bit 15, L or generation status, along with the category codes. If the Copy bit is 0, copyright protection is asserted over the material is an original or a duplication. (As mentioned in the previous paragraph, the definition of the L bit can be reversed based on the category codes.) There are two category codes that get special attention: general and A/D converters without C or L bit information. For these two categories the SCMS standard requires that equipment interfacing to these categories set the C bit to 0 (copyright protection asserted) and the L bit to 1 (original). To support this feature, Ce, in the consumer mode, is defined as IGCAT (ignorant category) which is low for the "general" (0000000) and "A/D converter without copyright information" (01100xx) categories.

APPENDIX A: RS422 RECEIVER INFORMATION

The RS422 receivers on the STA120 is designed to receive both the professional and consumer interfaces, and meet all specifications listed in the digital audio standards. Figure 6 illustrates the internal schematic of the receiver portion of both chips. The receiver has a differential input. A Schmitt trigger is incorporated to add hysteresis which prevents noisy signals from corrupting the phase detector.

Figure 6. RS422 Receiver Internal Circuit



Professional Interface

The digital audio specifications for professional use call for a balanced receiver, using XLR connectors, with 110Ω ±20% impedance. (The XLR connector on the receiver should have female pins with a male shell.) Since the receiver has a very high impedance, a 110Ω resistor should be placed across the receiver terminals to match the line impedance, as shown in figure 7, and, since the part has internal biasing, no external biasing network is needed. If some isolation is desired without the use of transformers, a 0.01µF capacitor should be placed on the input of esch pin (RXP and RXN) as shown in Figure 8. However, if transformers are not used, high frequency energy could be coupled between transmitter and receiver causing degradation in analog performance.

Although transformers are not required by AES they are strongly recommended. The EBU requires transformers. Figure 7 and 8 show an optional DC blocking capacitor on the transmission line. A 0.1 to 0.47µF ceramic capacitor may be used to block any DC voltage that is accidentally connected to the digital audio receiver. The use of this capacitor is an issue of robustness s the digital audio transmission line does not have a DC voltage component.

Figure 7. Professional Input Circuit

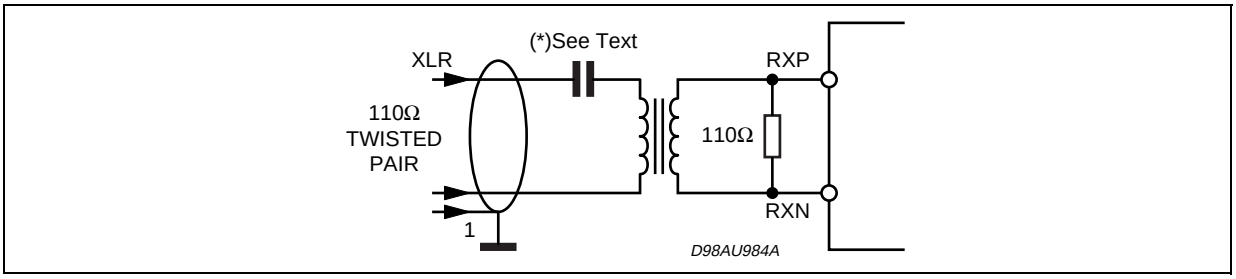
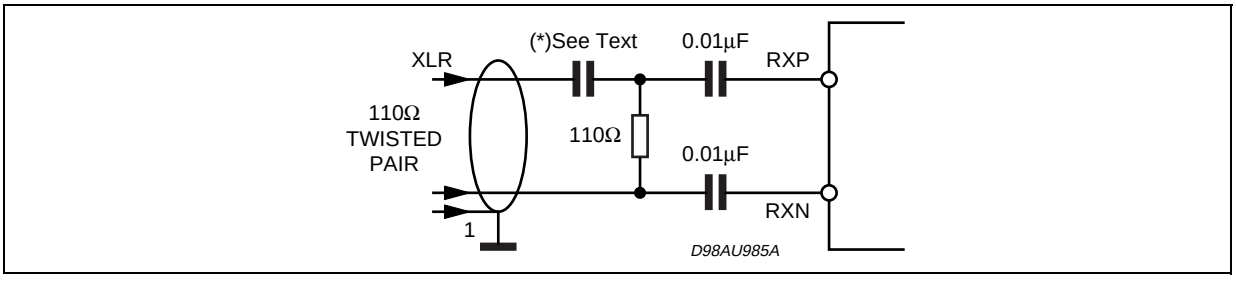


Figure 8. Transformerless Professional Circuit



Grounding the shield of the cables a tricky issue. In the configuration of systems, it is important to avoid ground loops and DC current flowing down the shield of the cable that could results when boxes with different ground potentials are connected.

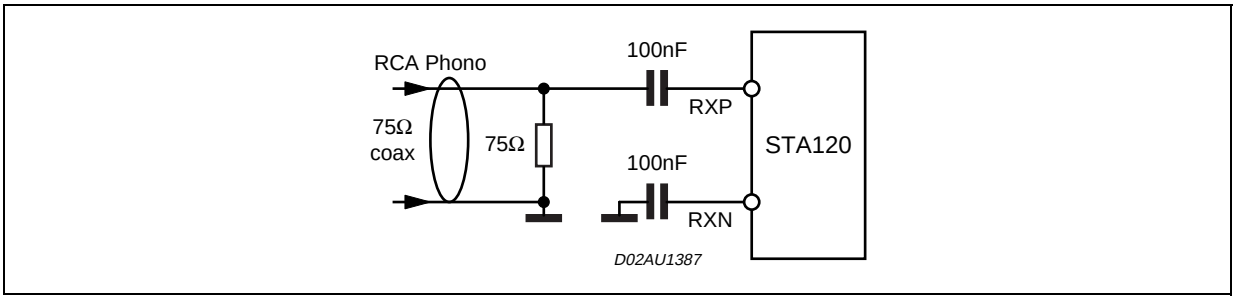
Generally, it is good practice to ground the shield to the chassis of the transmitting unit, and connect the shield through a capacitor to chassis ground at the receiver. However, in some cases it is advantageous to have the ground of two boxes help to the same potential, and the cable shield might be depended upon to make that electrical connection.

Generally, it may be a good idea to provide the option of grounding or capacitively coupling to ground with a "ground-lift" circuit.

Consumer Interface

In the case of the consumer interface, the standards call for an unbalanced circuit having a receiver impedance of 75Ω ±5%. The connector for the consumer interface is an RCA phono plug (fixed socket described in Table IV of IEC268-11). The receiver circuit for the consumer interface is shown in Figure 9.

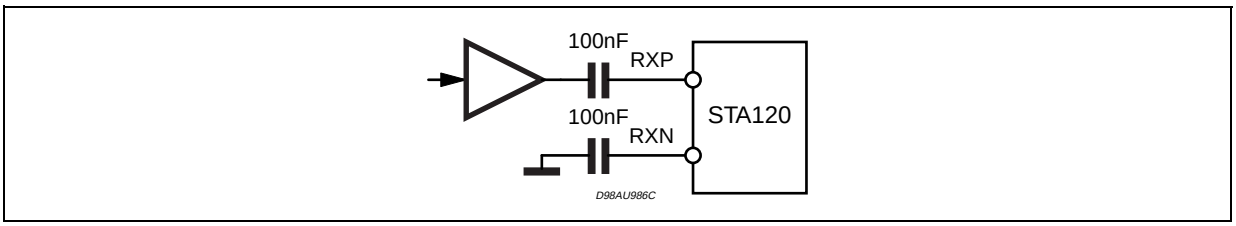
Figure 9. Consumer Input Circuit



TTL/CMOS Levels

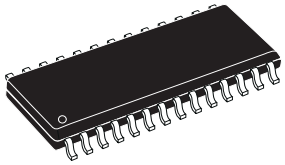
The circuit shown in Figure 10 may be used when external RS422 receivers or TTL/CMOS logic drive the STA120 receiver section.

Figure 10. TTL/CMOS Interface

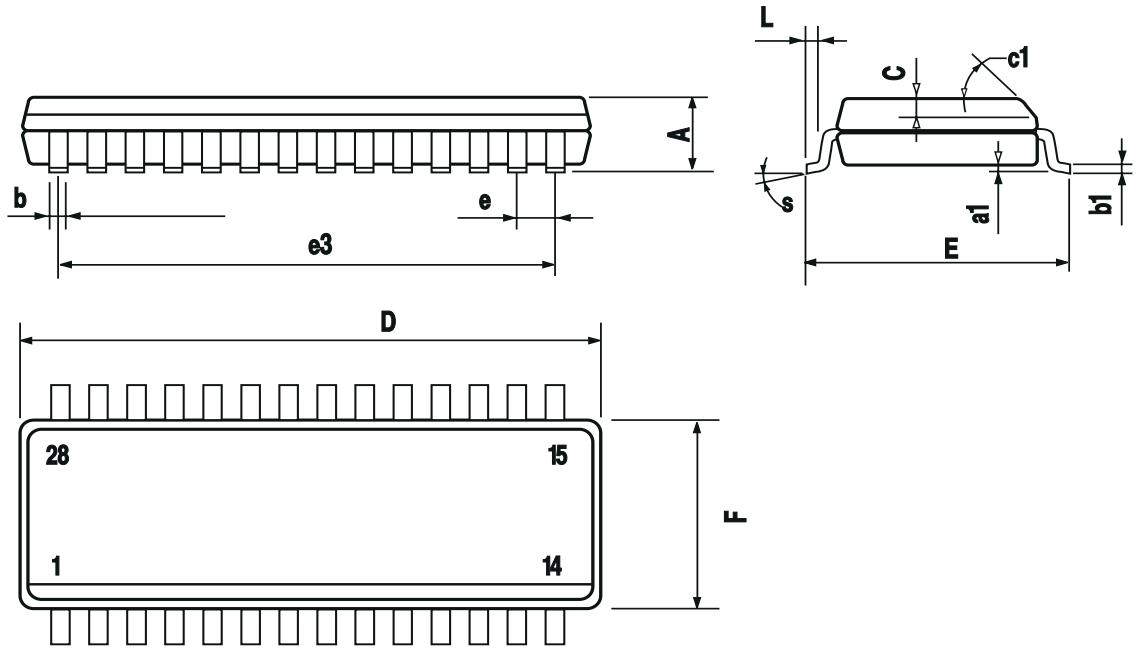


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8 ° (max.)					

OUTLINE AND MECHANICAL DATA



SO28



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