AU6984

USB2.0 Universal Flash Disk Controller

Technical Reference Manual

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1. Introduction

1.1 Description

The AU6984 USB 2.0 Flash Disk Controller is the best high performance solutions for SLC (Single- Level Cell), MLC (Multi-Level Cell) NAND and AG-AND with multiple dies data flash. Its high-speed read (30MB/Sec) and write access performance enable users to transfer and backup data effectively. Besides, AU6984 is certified by USB-IF (USB Implementers Forum), WHQL (Window Hardware Quality Labs) and EMI tests to guarantee the quality and reliability for end-users.
With multiple functions integrated into one chip and external components built inside, AU6984 is pledged to deliver the best performance benchmark and to further reduce the BOM cost of end products adopting this solution. It provides dual channel access and ISP (In-System Programming) technologies, which are the most important features to allow manufacturers building high performance UFD easily and to have the flexibility of adopting different source of flash chips. Same as its siblings of product family, AU6984 features the auto-run function to prompt the designated AP automatically when plugging into PC. In addition to being as a removable storage device, AU6984 can also be configured as a bootable disk for system recovery. Also, its random access performance exceed the minimum requirement of Read Boost feature found in Microsoft Vista operating system, in which randomly access blocks of information are saved into UFD for boosting up the average performance.
To enhance the usefulness and manageability of UFD further, Alcor Micro develops a smart application program iStar (Partition/Password Operation Tool) as a handy utility in managing partition, password and security. Having iStar as the companion of UFD, the data in a UFD could be protected from unauthorized access successfully.

1.2 Features

- PCBs are pin compatible in AU6980, AU6981, AU6982, AU6983, AU6984.
- Integrate build-in regulator
- Supports SLC and MLC dual channel with high performance
- Supports 4K/Page SLC and MLC dual channel with high performance Integrates hardware DMA engine to tune up the operation performance
- Improve read performance reach 30MB/Sec
- Supports firmware upgrade mechanism(ISP,In-System Programming)
- Integrates hardware DMA engine to tune up the operation performance
- Integrates multi-bit ECC correction mechanism
- Complies with the standards defined in USB v2.0, USB Device Class Definition for Mass Storage and Bulk-Transport v1.0
- Works with default driver under the environments of Windows ME, Windows 2000, Windows XP, Mac 9.2, Mac OS X. Using Alcor Micro's vendor driver for the environment under Windows 98SE
- Concurrent bus operation using multiple FIFO for better performance
- Integrates into flash memory power control switch
- Supports bad block management
- Supports dynamic serial number modification via mass production software
- Supports software write protection
- Support Auto Run function
- Support erasable and read-only mode AP Disk
- Companion application program with UFD – iStar available for users

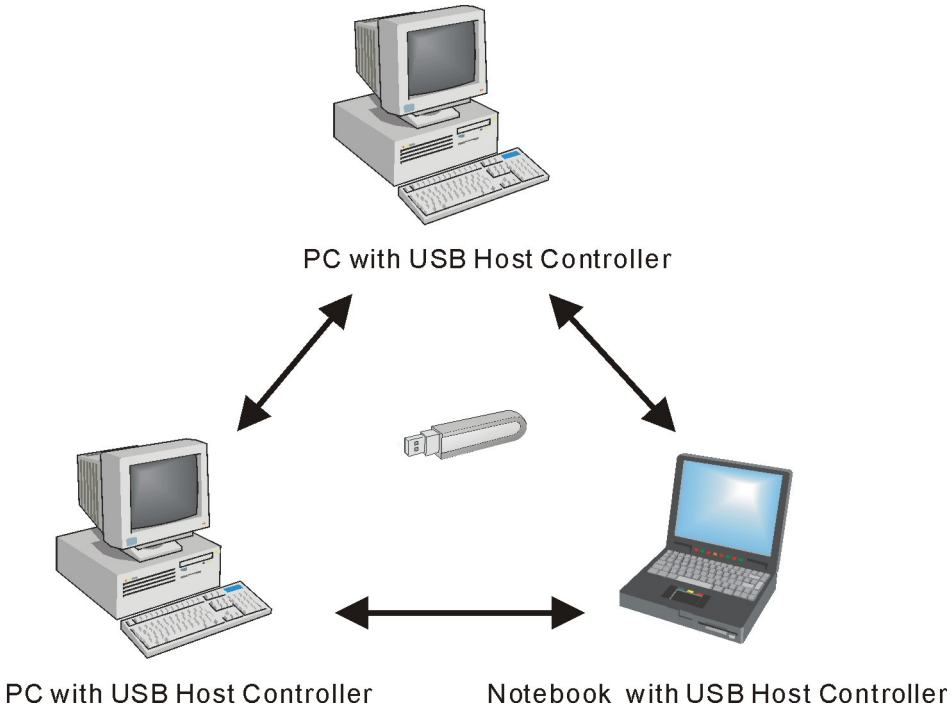
- To have UFD partition management function
- To do password protection for the security in data access
- To guard data files with software write protection function
- To lock up PC by UFD as the key

- Available in 48-pin LQFP 7x7mm package to support 4CE pin flashx2pcs
- Available in 64-pin LQFP 7x7mm package to support 4CE pin flashx4pcs

2. Application Block Diagram

The following figure shows the application diagram of a typical flash disk product with AU6984. By connecting the flash disk to a desktop or notebook PC through USB bus, AU6984 is then turned into a bus-powered, high speed USB disk, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.

Figure 2.1 Block Diagram



3. Pin Assignment

Depending on the application, the AU6984 is available in two different packages. Below figure shows signal name for each pin and the table in the page after describes each pin in detail.

Figure 3.1 AU6984-MHL Pin Assignment Diagram

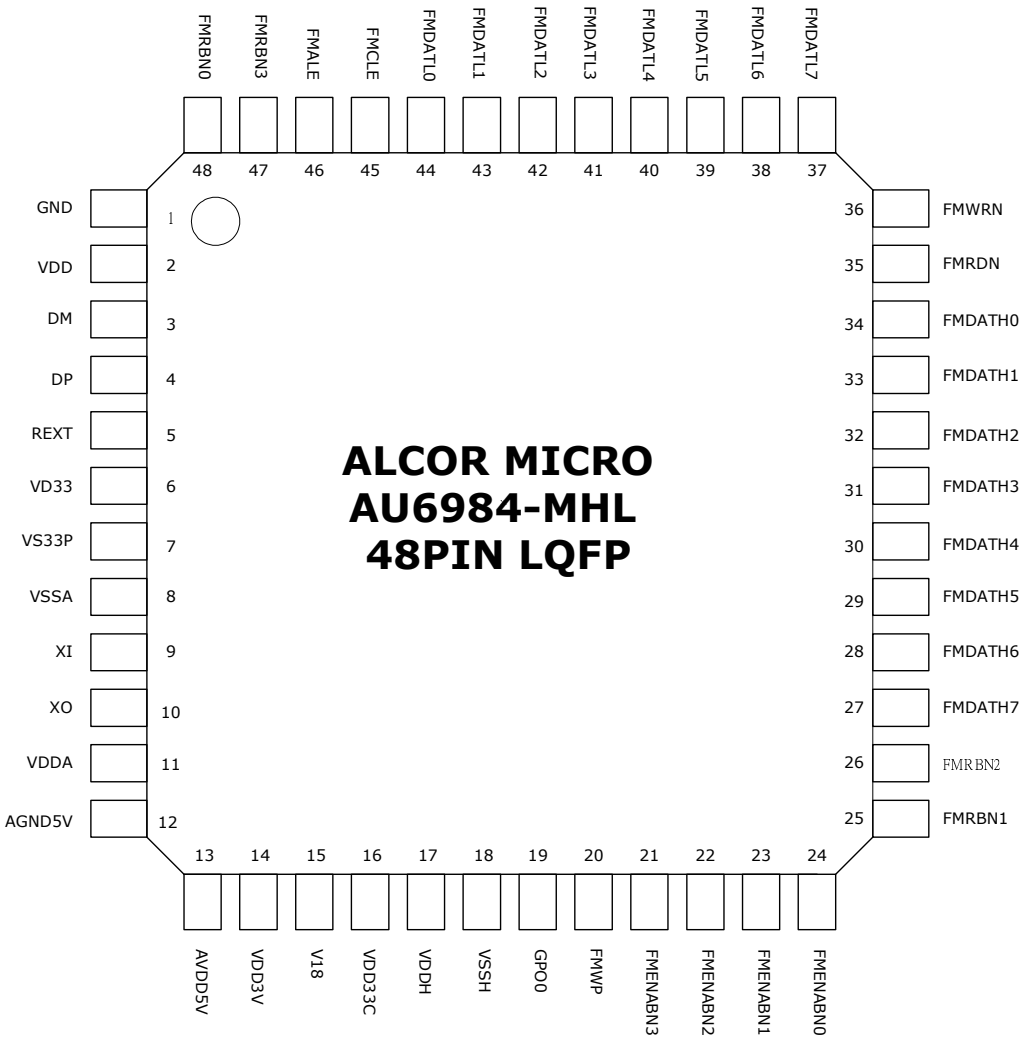


Table 3.1 AU6984-MHL Pin Descriptions

Pin #	Pin Name	I/O	Description
1	GND	I/ GND	"1" Force Chip into USB 1.1 operation mode Ground
2	VDD	I	1.8V power
3	DM	I/O	USB DM
4	DP	I/O	USB DP
5	REXT	I	External resistor 330 to ground
6	VD33	I	3.3V power
7	VS33P	GND	Ground
8	VSSA	GND	Ground
9	XI	I	12 MHz oscillator input
10	XO	O	12 MHz oscillator output
11	VDDA	I	1.8V power for PLL
12	AGND5V	I	Ground
13	AVDD5V	I	5V input power pin
14	VDD3V	O	3.3V output power pin
15	V18	O	1.8V output for Core
16	VDD33C	O	3.3V output for flash chip
17	VDDH	I	3.3V input power pin
18	VSSH	I	Ground '1' AND Flash, '0' NAND flash
19	GPO0	O	blanking when system access
20	FMWP	I	Reserved for firmware
21	FMENABN3	O	Flash 3 select pin
22	FMENABN2	O	Flash 2 select pin
23	FMENABN1	O	Flash 1 select pin
24	FMENABN0	O	Flash 0 select pin
25	FMRBN1	I	Flash 1 ready pin
26	FMRBN2	I	Flash 2 ready pin
27	FMDATH7	I/O	Flash high data 7 pin
28	FMDATH6	I/O	Flash high data 6 pin
29	FMDATH5	I/O	Flash high data 5 pin
30	FMDATH4	I/O	Flash high data 4 pin
31	FMDATH3	I/O	Flash high data 3 pin

Pin #	Pin Name	I/O	Description
32	FMDATH2	I/O	Flash high data 2 pin
33	FMDATH1	I/O	Flash high data 1 pin
34	FMDATH0	I/O	Flash high data 0 pin
35	FMRDN	O	Flash read signal
36	FMWRN	O	Flash write signal
37	FMDATL7	I/O	Flash low data 7 pin
38	FMDATL6	I/O	Flash low data 6 pin
39	FMDATL5	I/O	Flash low data 5 pin
40	FMDATL4	I/O	Flash low data 4 pin
41	FMDATL3	I/O	Flash low data 3 pin
42	FMDATL2	I/O	Flash low data 2 pin
43	FMDATL1	I/O	Flash low data 1 pin
44	FMDATL0	I/O	Flash low data 0 pin
45	FMCLE	O	Flash command latch pin
46	FMALE	O	Flash address latch pin
47	FMRBN3	I	Flash 3 ready pin
48	FMRBN0	I	Flash 0 ready pin

The following figure shows signal name of each pin in 64-pin package and the table in the page after describes each pin in detail.

Figure 3.2 AU6984-MIL Pin Assignment Diagram

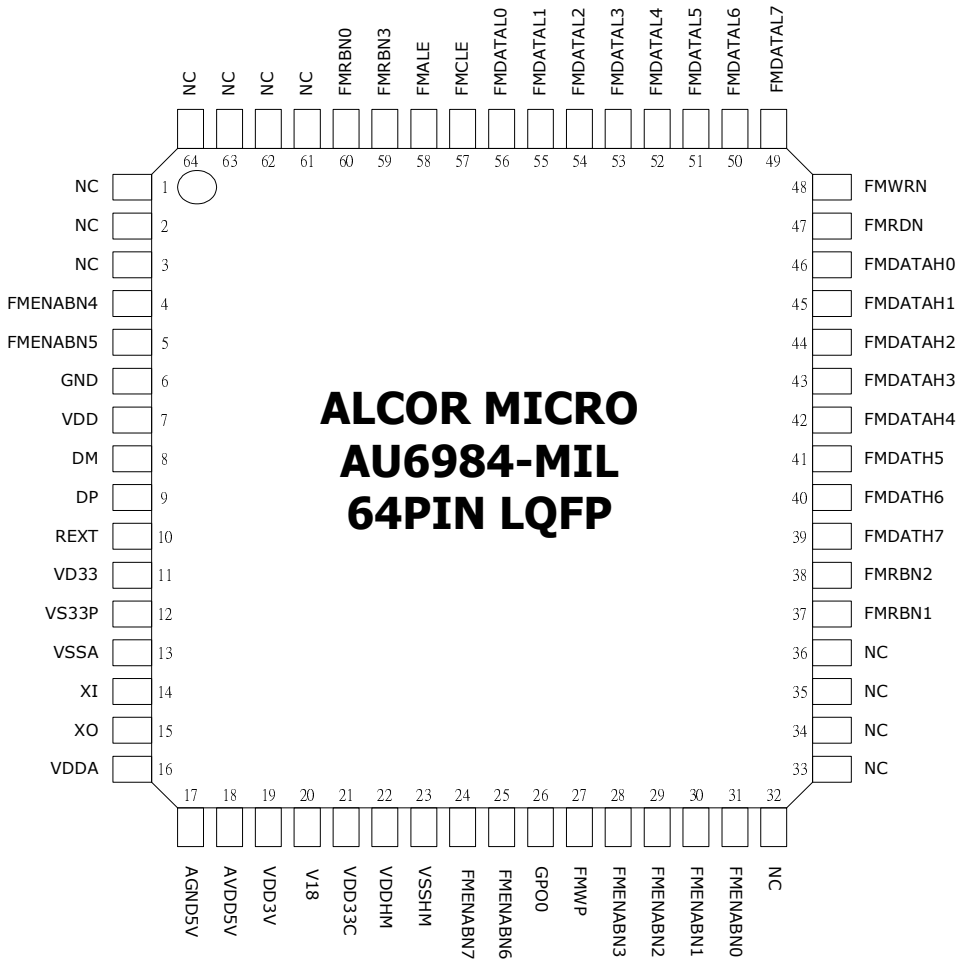


Table 3.2 AU6984-MIL Pin Descriptions

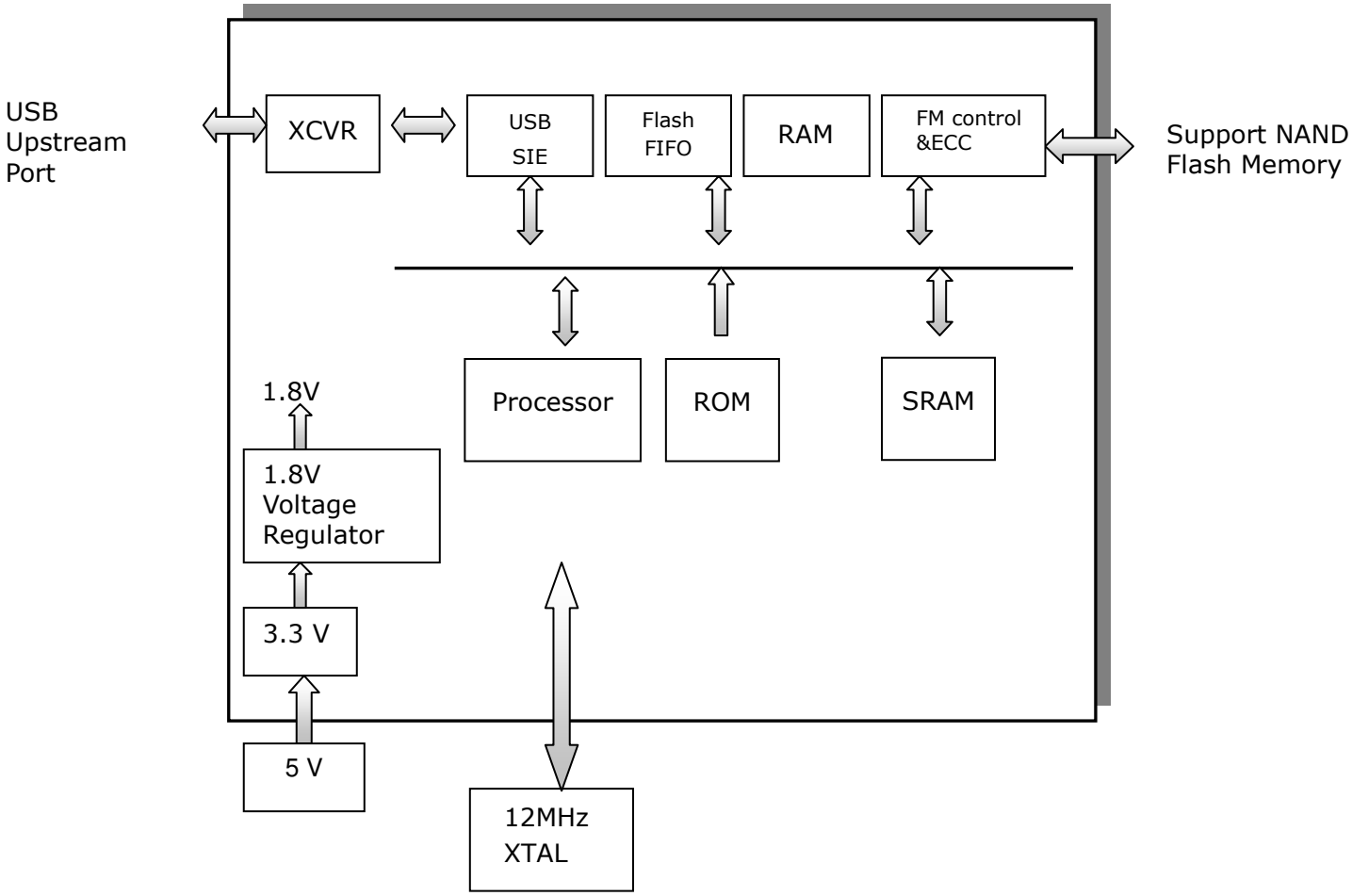
Pin #	Pin Name	I/O	Description
1	NC		NC
2	NC		NC
3	NC		NC
4	FMENABN4	O	Flash 4 select pin
5	FMENABN5	O	Flash 5 select pin
6	GND	I/GND	"1" Force Chip into USB 1.1 operation mode/Ground
7	VDD	I	1.8V power
8	DM	I/O	USB DM
9	DP	I/O	USB DP
10	REXT	I	External resistor 330 to ground
11	VD33	I	3.3V power
12	VS33P	GND	Ground
13	VSSA	GND	Ground
14	XI	I	12 MHz oscillator input
15	XO	O	12 MHz oscillator output
16	VDDA	I	1.8V power for PLL
17	AGND5V	I	Ground
18	AVDD5V	I	5V input power pin
19	VDD3V	O	3.3V output power pin
20	V18	O	1.8V output for Core
21	VDD33C	O	3.3V output for flash chip
22	VDDHM	I	3.3V input power pin
23	VSSHM	I	Ground/ '1' AND Flash, '0' NAND flash
24	FMENABN7	O	Flash 7 select pin
25	FMENABN6	O	Flash 6 select pin
26	GPO0	O	blanking when system access
27	FMWP	I	Reserved for firmware
28	FMENABN3	O	Flash 3 select pin
29	FMENABN2	O	Flash 2 select pin
30	FMENABN1	O	Flash 1 select pin
31	FMENABN0	O	Flash 0 select pin
32	NC		NC
33	NC	I	Hardware test T0
34	NC	I	Hardware test T1
35	NC	I	Hardware test T2

Pin #	Pin Name	I/O	Description
36	NC		
37	FMRBN1	I	Flash 1 ready pin
38	FMRBN2	I	Flash 2 ready pin
39	FMDATH7	I/O	Flash high data 7 pin
40	FMDATH6	I/O	Flash high data 6 pin
41	FMDATH5	I/O	Flash high data 5 pin
42	FMDATH4	I/O	Flash high data 4 pin
43	FMDATH3	I/O	Flash high data 3 pin
44	FMDATH2	I/O	Flash high data 2 pin
45	FMDATH1	I/O	Flash high data 1 pin
46	FMDATH0	I/O	Flash high data 0 pin
47	FMRDN	O	Flash read signal
48	FMWRN	O	Flash write signal
49	FMDATL7	I/O	Flash low data 7 pin
50	FMDATL6	I/O	Flash low data 6 pin
51	FMDATL5	I/O	Flash low data 5 pin
52	FMDATL4	I/O	Flash low data 4 pin
53	FMDATL3	I/O	Flash low data 3 pin
54	FMDATL2	I/O	Flash low data 2 pin
55	FMDATL1	I/O	Flash low data 1 pin
56	FMDATL0	I/O	Flash low data 0 pin
57	FMCLE	O	Flash command latch pin
58	FMALE	O	Flash address latch pin
59	FMRBN3	I	Flash 3 ready pin
60	FMRBN0	I	Flash 0 ready pin
61	NC		NC
62	NC		NC
63	NC		NC
64	NC		NC

4. System Architecture and Reference Design

4.1 AU6984 Block Diagram

Figure 4.1 AU6984 Block Diagram



5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DDH}	Power Supply	-0.3 to V_{DDH} +0.3	V
V_{IN}	Input Signal Voltage	-0.3 to 3.6	V
V_{OUT}	Output Signal Voltage	-0.3 to V_{DDH} +0.3	V
T_{STG}	Storage Temperature	-40 to 150	^{O}C

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
A_{DD}	5V Power Supply	4.75	5.0	5.0	V
V_{DDH}	Power Supply	3.0	3.3	3.6	V
V_{DD}	Digital Supply	1.62	1.8	1.98	V
V_{IN}	Input Signal Voltage	0	3.3	3.6	V
T_{OPR}	Operating Temperature	0		70	^{O}C

5.3 General DC Characteristics

Table 5.3 General DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IN}	Input current	No pull-up or pull-down	-10	±1	10	µA
I_{OZ}	Tri-state leakage current		-10	±1	10	µA
C_{IN}	Input capacitance	Pad Limit		2.8		ρF
C_{OUT}	Output capacitance	Pad Limit		2.8		ρF
C_{BID}	Bi-directional buffer capacitance	Pad Limit		2.8		ρF

5.4 DC Electrical Characteristics of 3.3V I/O Cells

Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DDH}	Power supply	3.3V I/O	3.0	3.3	3.6	V
V_{il}	Input low voltage	LVTTL			0.8	V
V_{ih}	Input high voltage		2.0			V
V_{ol}	Output low voltage	$\lvert I_{ol} \rvert$ =2~16mA			0.4	V
V_{oh}	Output high voltage	$\lvert I_{oh} \rvert$ =2~16mA	2.4			V
R_{pu}	Input pull-up resistance	PU=high, PD=low	55	75	110	KΩ
R_{pd}	Input pull-down resistance	PU=low, PD=high	40	75	150	KΩ
I_{in}	Input leakage current	V_{in}= V_{DDH} or 0	-10	±1	10	μA
I_{oz}	Tri-state output leakage current		-10	±1	10	μA

5.5 USB Transceiver Characteristics

Table 5.5 Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VD33	Analog supply Voltage		3.0	3.3	3.6	V
VDDU VDDA	Digital supply Voltage		1.62	1.8	1.98	V
I_{CC}	Operating supply current	High speed operating at 480 MHz			55	mA
$I_{CC\ (susp)}$	Suspend supply current	In suspend mode, current with 1.5kΩ pull-up resistor on pin RPU disconnected			120	μA

Table 5.6 Static characteristic：Digital pin

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input levels						
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2.0			V
Output levels						
V_{OL}	Low-level output voltage				0.2	V
V_{OH}	High-level output voltage		VDDH-0.2			V

VD33=3.0V~3.6V；VDDU,VDDA=1.62V~1.98V；Temp=0℃~70℃

Table 5.7 Static characteristic：Analog I/O pins（DP/DM）

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB2.0 Transceiver（HS）						
Input Levels（differential receiver）						
V_{HSDIFF}	High speed differential input sensitivity	$\lvert V_{I(DP)}-V_{I(DM)} \rvert$ measured at the connection as application circuit	300			mV
V_{HSCM}	High speed data signaling common mode voltage range		-50		500	mV
V_{HSSQ}	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
V_{HSDSC}	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
V_{HSOI}	High speed idle level output voltage(differential)		-10		10	mV
V_{HSOL}	High speed low level output voltage(differential)		-10		10	mV
V_{HSOH}	High speed high level output voltage(differential)		-360		400	mV
V_{CHIRPJ}	Chirp-J output voltage（differential）		700		1100	mV
V_{CHIRPK}	Chirp-K output voltage（differential）		-900		-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	Ω

		Overall resistance including external resistor	40.5	45	49.5	
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver（FS/LS）						
Input Levels（differential receiver）						
V_{DI}	Differential input sensitivity	$\lvert V_{I(DP)}-V_{I(DM)} \rvert$	0.2			V
V_{CM}	Differential common mode voltage		0.8		2.5	V
Input Levels（single-ended receivers）						
V_{SE}	Single ended receiver threshold		0.8		2.0	V
Output levels						
V_{OL}	Low-level output voltage		0		0.3	V
V_{OH}	High-level output voltage		2.8		3.6	V

VD33=3.0V~3.6V；VDDU,VDDA=1.62V~1.98V；Temp=0℃~70℃

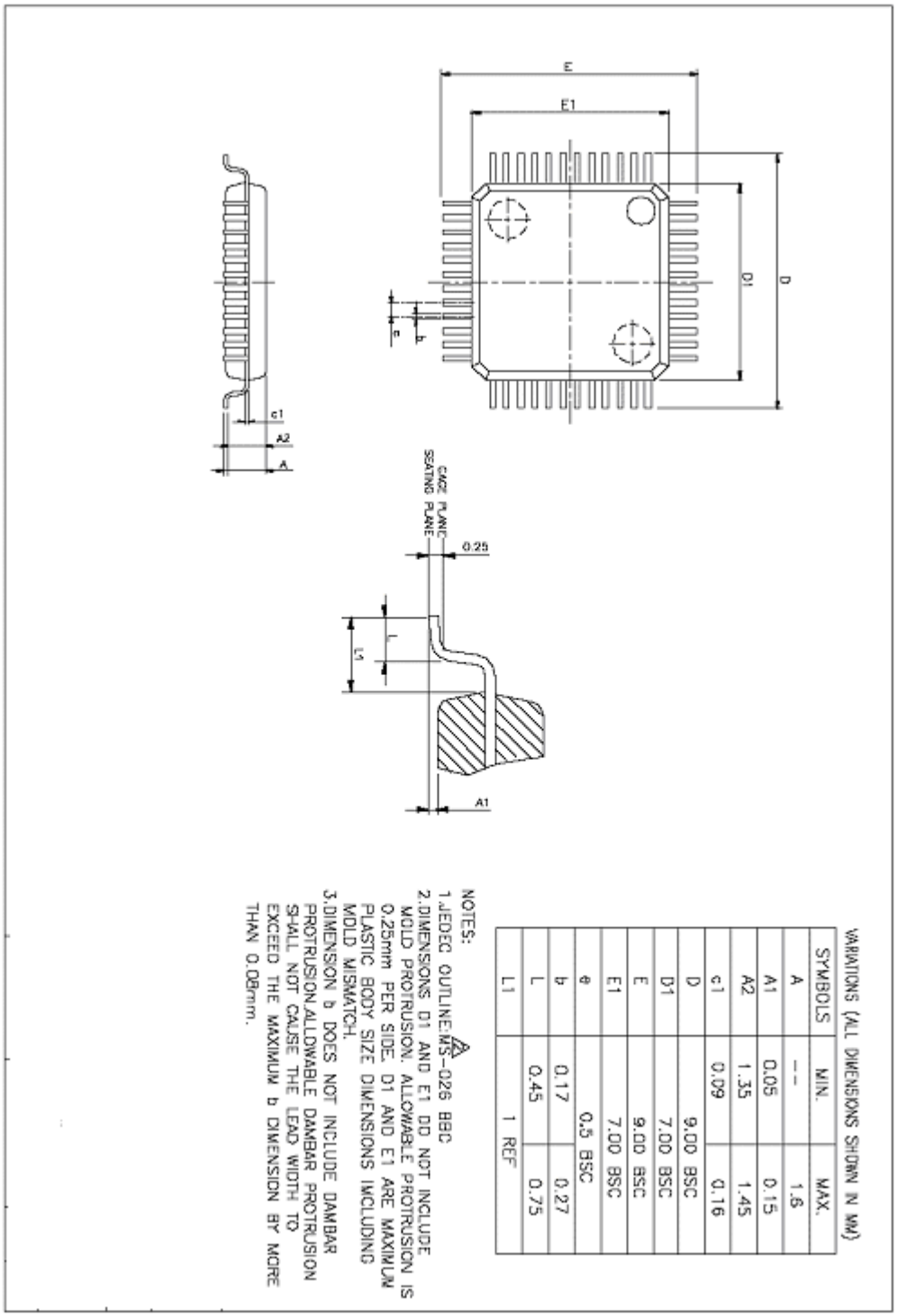
Table 5.8 Dynamic characteristic：Analog I/O pins（DP/DM）

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver Characteristics						
High-Speed Mode						
t_{HSR}	High-speed differential rise time		500			ps
t_{HSF}	High-speed differential fall time		500			ps
Full-Speed Mode						
t_{FR}	Rise time	CL=50pF；10 to 90% of $\lvert V_{OH}-V_{OL} \rvert$ ；	4		20	ns
t_{FF}	Fall time	CL=50pF；90 to 10% of $\lvert V_{OH}-V_{OL} \rvert$ ；	4		20	ns
t_{FRMA}	Differential rise/fall time matching（t_{FR} / t_{FF}）	Excluding the first transition from idle mode	90		110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
Low-Speed Mode						
t_{LR}	Rise time	CL=200pF-600pF；10 to 90% of $\lvert V_{OH}-V_{OL} \rvert$ ；	75		300	ns

t_{LF}	Fall time	CL=200pF-600pF；90 to 10% of $\lvert V_{OH}-V_{OL} \rvert$；	75		300	ns
t_{LRMA}	Differential rise/fall time matching（t_{LR} / t_{LF}）	Excluding the first transition from idle mode	80		125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
V_{OH}	High-level output voltage		2.8		3.6	V

6. Mechanical Information

Figure 6.1 48 LQFP Mechanical Information Diagram

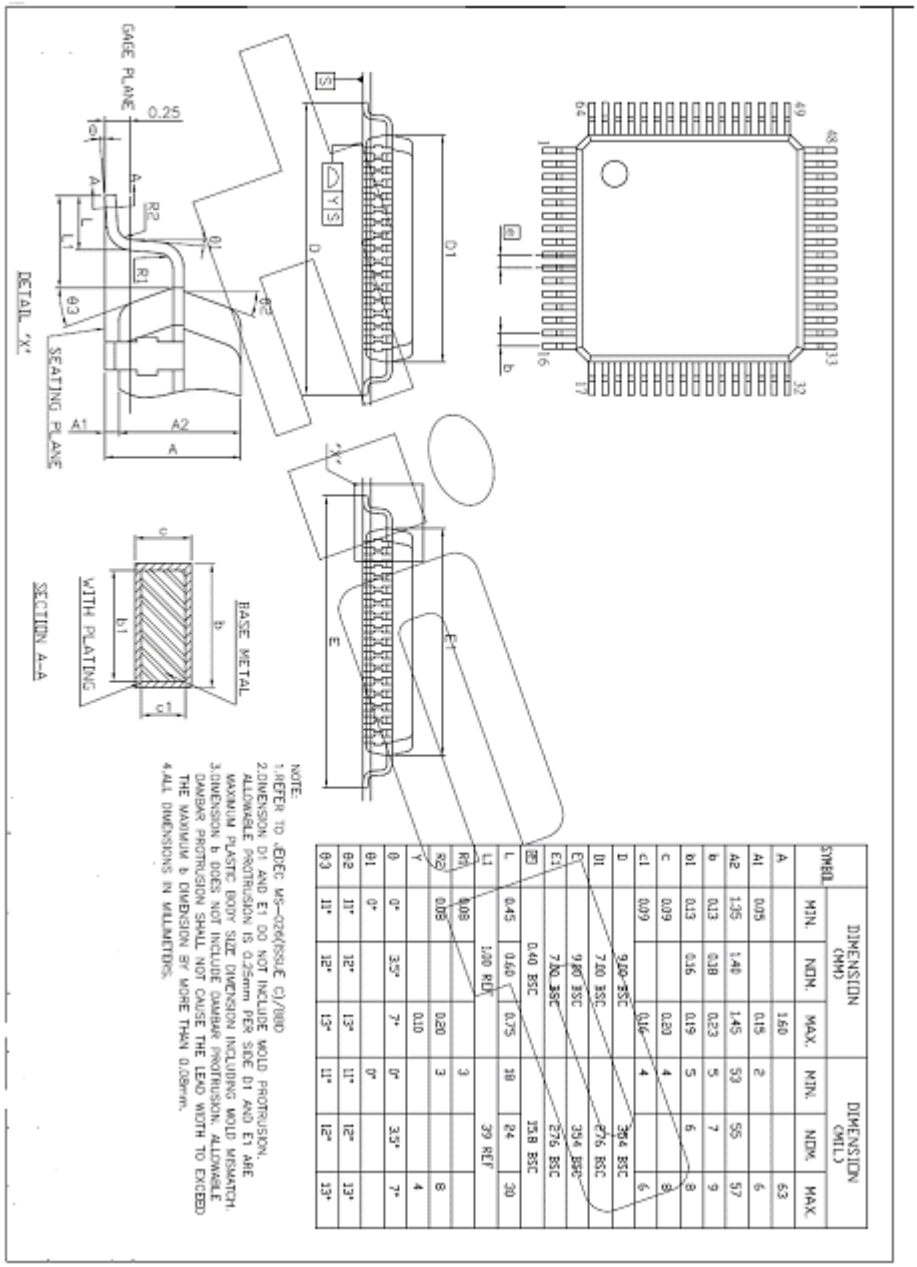


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:
1.JEDEC OUTLINE:MS-026 BBC
2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

Figure 6.2 64 LQFP Mechanical Information Diagram



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.13	0.18	0.23	5	7	9
b1	0.13	0.16	0.19	5	6	8
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D		9.00 BSC			354 BSC	
D1		7.00 BSC			276 BSC	
E		9.00 BSC			354 BSC	
E1		7.00 BSC			276 BSC	
e		0.40 BSC			15.8 BSC	
L	0.45	0.60	0.75	18	24	30
L1		1.00 REF			39 REF	
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.10			4
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°		0°			
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

7. Abbreviations

In this chapter some of the terms and abbreviations used throughout the technical reference manual are listed as follows.

DC Electrical	Direct Current Electrical
PLL	Phase Lock Loop, which is a closed-loop frequency control system.
ECC	Error Checking and Correcting
XTAL	Crystal
UFD	USB Flash Disk
iStar	Partition/Password Operation Tool - the smart application program developed by Alcor Micro as a companion handy tool for managing the UFD.

About Alcor Micro, Corp.

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader…etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California. Alcor Micro is distinguished by its ability to provide innovative solutions for spec-driven products. Innovations like single chip solutions for traditional multiple chip products and on-board voltage regulators enable the company to provide cost-efficiency solutions for the computer peripheral device OEM customers worldwide.