ELPIDA

PRELIMINARY DATA SHEET

256MB DDR SDRAM S.O.DIMM

HB54A2568KN-A75B/B75B/10B (32M words × 64 bits, 2 Banks)

Description

The HB54A2568KN is Double Data Rate (DDR) SDRAM Module, mounted 256M bits DDR SDRAM (HM5425161BTT) sealed in TSOP package, and 1 piece of serial EEPROM (2k bits EEPROM) for Presence Detect (PD). The HB54A2568KN is organized as 16M × 64 × 2 bank mounted 8 pieces of 256M bits DDR SDRAM. Read and write operations are performed at the cross points of the CK and the /CK. This high-speed data transfer is realized by the 2 bits prefetch-pipelined architecture. Data strobe (DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode register, the on-chip Delay Locked Loop (DLL) can be set enable or disable. An outline of the products is 200-pin socket type package (dual lead out). Therefore, it makes high density mounting possible without surface mount technology. It provides common data inputs and outputs. Decoupling capacitors are mounted beside each TSOP on the module board.

Features

- 200-pin socket type package (dual lead out)
  - Outline: 67.6mm (Length) × 31.75mm (Height) × 3.80mm (Thickness)
  - Lead pitch: 0.6mm
- 2.5V power supply (VCC)
- SSTL-2 interface for all inputs and outputs
- Clock frequency: 133 MHz (max) (-A75B/B75B)
  : 100 MHz (max) (-10B)
- Data inputs, outputs and DM are synchronized with DQS
- 4 banks can operate simultaneously and independently (Component)
- Burst read/write operation
- Programmable burst length: 2, 4, 8
  - Burst read stop capability
- Programmable burst sequence
  - Sequential
  - Interleave
- Start addressing capability
  - Even and Odd
- Programmable /CAS latency (CL): 2, 2.5
- 8192 refresh cycles: 7.8μs (8192row /64ms)
- 2 variations of refresh
  - Auto refresh
  - Self refresh

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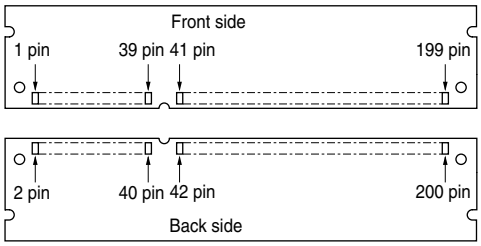
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Ordering Information

Part number	Clock frequency MHz (max.)	/CAS latency	Package	Contact pad
HB54A2568KN-A75B*1	133 MHz	2.0	200-pin dual lead out socket type	Gold
HB54A2568KN-B75B*2	133 MHz	2.5		
HB54A2568KN-10B*3	100 MHz	2.0		

Notes: 1. 143 MHz operation at /CAS latency = 2.5.
2. 100 MHz operation at /CAS latency = 2.0.
3. 125 MHz operation at /CAS latency = 2.5.

Pin Configurations



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VREF	51	VSS	2	VREF	52	VSS
3	VSS	53	DQ19	4	VSS	54	DQ23
5	DQ0	55	DQ24	6	DQ4	56	DQ28
7	DQ1	57	VCC	8	DQ5	58	VCC
9	VCC	59	DQ25	10	VCC	60	DQ29
11	DQS0	61	DQS3	12	DM0	62	DM3
13	DQ2	63	VSS	14	DQ6	64	VSS
15	VSS	65	DQ26	16	VSS	66	DQ30
17	DQ3	67	DQ27	18	DQ7	68	DQ31
19	DQ8	69	VCC	20	DQ12	70	VCC
21	VCC	71	NC	22	VCC	72	NC
23	DQ9	73	NC	24	DQ13	74	NC
25	DQS1	75	VSS	26	DM1	76	VSS
27	VSS	77	NC	28	VSS	78	NC
29	DQ10	79	NC	30	DQ14	80	NC
31	DQ11	81	VCC	32	DQ15	82	VCC
33	VCC	83	NC	34	VCC	84	NC
35	CK0	85	NC	36	VCC	86	NC
37	/CK0	87	VSS	38	VSS	88	VSS
39	VSS	89	CK2	40	VSS	90	VSS
41	DQ16	91	/CK2	42	DQ20	92	VCC
43	DQ17	93	VCC	44	DQ21	94	VCC
45	VCC	95	CKE1	46	VCC	96	CKE0
47	DQS2	97	NC	48	DM2	98	NC
49	DQ18	99	A12	50	DQ22	100	A11

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
101	A9	151	DQ42	102	A8	152	DQ46
103	VSS	153	DQ43	104	VSS	154	DQ47
105	A7	155	VCC	106	A6	156	VCC
107	A5	157	VCC	108	A4	158	/CK1
109	A3	159	VSS	110	A2	160	CK1
111	A1	161	VSS	112	A0	162	VSS
113	VCC	163	DQ48	114	VCC	164	DQ52
115	A10/AP	165	DQ49	116	BA1	166	DQ53
117	BA0	167	VCC	118	/RAS	168	VCC
119	/WE	169	DQS6	120	/CAS	170	DM6
121	/S0	171	DQ50	122	/S1	172	DQ54
123	NC	173	VSS	124	NC	174	VSS
125	VSS	175	DQ51	126	VSS	176	DQ55
127	DQ32	177	DQ56	128	DQ36	178	DQ60
129	DQ33	179	VCC	130	DQ37	180	VCC
131	VCC	181	DQ57	132	VCC	182	DQ61
133	DQS4	183	DQS7	134	DM4	184	DM7
135	DQ34	185	VSS	136	DQ38	186	VSS
137	VSS	187	DQ58	138	VSS	188	DQ62
139	DQ35	189	DQ59	140	DQ39	190	DQ63
141	DQ40	191	VCC	142	DQ44	192	VCC
143	VCC	193	SDA	144	VCC	194	SA0
145	DQ41	195	SCL	146	DQ45	196	SA1
147	DQS5	197	VCCSPD	148	DM5	198	SA2
149	VSS	199	VCCID	150	VSS	200	NC

Pin Description

Pin name	Function
A0 to A12	Address input Row address A0 to A12 Column address A0 to A8
BA0, BA1	Bank select address
DQ0 to DQ63	Data input/output
/RAS	Row address strobe command
/CAS	Column address strobe command
/WE	Write enable
/S0, /S1	Chip select
CKE0, CKE1	Clock enable
CK0 to CK2	Clock input
/CK0 to /CK2	Differential clock input
DQS0 to DQS7	Input and output data strobe
DM0 to DM7	Input mask
SCL	Clock input for serial PD
SDA	Data input/output for serial PD
SA0 to SA2	Serial address input
VCC	Power for internal circuit
VCCSPD	Power for serial EEPROM
VREF	Input reference voltage
VSS	Ground
VCCID	VCC identification flag
NC	No connection

Serial PD Matrix*[1]

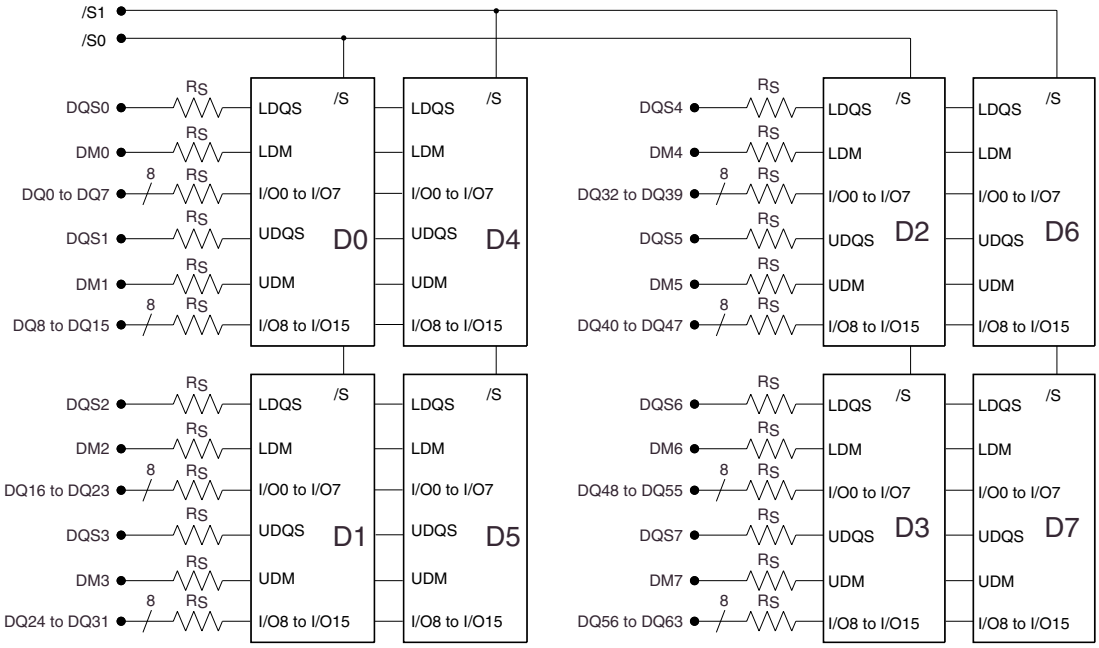
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes utilized by module manufacturer	1	0	0	0	0	0	0	0	80	128
1	Total number of bytes in serial PD device	0	0	0	0	1	0	0	0	08	256 byte
2	Memory type	0	0	0	0	0	1	1	1	07	SDRAM DDR
3	Number of row address	0	0	0	0	1	1	0	1	0D	13
4	Number of column address	0	0	0	0	1	0	0	1	09	9
5	Number of DIMM banks	0	0	0	0	0	0	1	0	02	2
6	Module data width	0	1	0	0	0	0	0	0	40	64 bits
7	Module data width continuation	0	0	0	0	0	0	0	0	00	0 (+)
8	Voltage interface level of this assembly	0	0	0	0	0	1	0	0	04	SSTL 2.5V
9	DDR SDRAM cycle time, CL = X -A75B	0	1	1	1	0	0	0	0	70	CL = 2.5*[5]
	-B75B	0	1	1	1	0	1	0	1	75	
	-10B	1	0	0	0	0	0	0	0	80	
10	SDRAM access from clock (tAC) -A75B/B75B	0	1	1	1	0	0	0	0	70	0.7ns*[5]
	-10B	1	0	0	0	0	0	0	0	80	0.8ns*[5]
11	DIMM configuration type	0	0	0	0	0	0	0	0	00	Non-parity
12	Refresh rate/type	1	0	0	0	0	0	1	0	82	7.8 µs Self refresh
13	Primary SDRAM width	0	0	0	1	0	0	0	0	10	× 16
14	Error checking SDRAM width	0	0	0	0	0	0	0	0	00	Not used
15	SDRAM device attributes: Minimum clock delay back-to-back column access	0	0	0	0	0	0	0	1	01	1 CLK
16	SDRAM device attributes: Burst length supported	0	0	0	0	1	1	1	0	0E	2, 4, 8
17	SDRAM device attributes: Number of banks on SDRAM device	0	0	0	0	0	1	0	0	04	4
18	SDRAM device attributes: /CAS latency	0	0	0	0	1	1	0	0	0C	2, 2.5
19	SDRAM device attributes: /CS latency	0	0	0	0	0	0	0	1	01	0
20	SDRAM device attributes: /WE latency	0	0	0	0	0	0	1	0	02	1
21	SDRAM module attributes	0	0	1	0	0	0	0	0	20	Unbuffered
22	SDRAM device attributes: General	1	0	0	0	0	0	0	0	80	± 0.2V
23	Minimum clock cycle time at CLX - 0.5 -A75B	0	1	1	1	0	1	0	1	75	CL = 2*[5]
	-B75B/10B	1	0	1	0	0	0	0	0	A0	
24	Maximum data access time (tAC) from clock at CLX - 0.5 -A75B/B75B	0	1	1	1	0	0	0	0	70	0.7ns*[5]
	-10B	1	0	0	0	0	0	0	0	80	0.8ns*[5]
25	Minimum clock cycle time at CLX - 1	0	0	0	0	0	0	0	0	00	
26	Maximum data access time (tAC) from clock at CLX - 1	0	0	0	0	0	0	0	0	00	
27	Minimum row precharge time (tRP)	0	1	0	1	0	0	0	0	50	20ns

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
28	Minimum row active to row active delay (tRRD)	0	0	1	1	1	1	0	0	3C	15ns
29	Minimum /RAS to /CAS delay (tRCD)	0	1	0	1	0	0	0	0	50	20ns
30	Minimum active to precharge time (tRAS) -A75B/B75B	0	0	1	0	1	1	0	1	2D	45ns
	-10B	0	0	1	1	0	0	1	0	32	50ns
31	Module bank density	0	0	1	0	0	0	0	0	20	1 bank/ 2 bank 128 MB
32	Address and command setup time before clock (tIS) -A75B/B75B	1	0	1	1	0	0	0	0	B0	1.1ns*5
	-10B	1	1	0	0	0	0	0	0	C0	1.2ns*5
33	Address and command hold time after clock (tIH) -A75B/B75B	1	0	1	1	0	0	0	0	B0	1.1ns*5
	-10B	1	1	0	0	0	0	0	0	C0	1.2ns*5
34	Data input setup time before clock (tDS) -A75B/B75B	0	1	0	1	0	0	0	0	50	0.5ns*5
	-10B	0	1	1	0	0	0	0	0	60	0.6ns*5
35	Data input hold time after clock (tDH) -A75B/B75B	0	1	0	1	0	0	0	0	50	0.5ns*5
	-10B	0	1	1	0	0	0	0	0	60	0.6ns*5
36 to 40	Superset information	0	0	0	0	0	0	0	0	00	Future use
41	Active command period (tRC) -A75B/B75B	0	1	0	0	0	0	0	1	41	65ns*5
	-10B	0	1	0	0	0	1	1	0	46	70ns*5
42	Auto refresh to active/ Auto refresh command cycle (tRFC) -A75B/B75B	0	1	0	0	1	0	1	1	4B	75ns*5
	-10B	0	1	0	1	0	0	0	0	50	80ns*5
43	SDRAM tCK cycle max. (tCK max.)	0	0	1	1	1	1	0	0	3C	15ns*5
44	Dout to DQS skew -A75B/B75B	0	0	1	1	0	0	1	0	32	500ps*5
	-10B	0	0	1	1	1	1	0	0	3C	600ps*5
45	Data hold skew (tQHS) -A75B/B75B	0	1	1	1	0	1	0	1	75	750ps*5
	-10B	1	0	1	0	0	0	0	0	A0	1000ps*5
46 to 61	Superset information	0	0	0	0	0	0	0	0	00	Future use
62	SPD revision	0	0	0	0	0	0	0	0	00	Initial

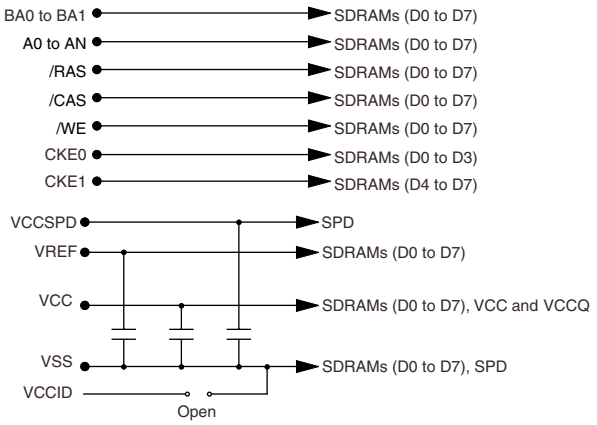
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
63	Checksum for bytes 0 to 62 -A75B	1	0	0	1	1	1	0	0	9C	156
	-B75B	1	1	0	0	1	1	0	0	CC	204
	-10B	0	1	1	1	1	0	1	1	7B	123
64	Manufacturer's JEDEC ID code	0	0	0	0	0	1	1	1	07	HITACHI
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00	
72	Manufacturing location	×	×	×	×	×	×	×	×	××	*2 (ASCII-8bit code)
73	Module part number	0	1	0	0	1	0	0	0	48	H
74	Module part number	0	1	0	0	0	0	1	0	42	B
75	Module part number	0	0	1	1	0	1	0	1	35	5
76	Module part number	0	0	1	1	0	1	0	0	34	4
77	Module part number	0	1	0	0	0	0	0	1	41	A
78	Module part number	0	0	1	1	0	0	1	0	32	2
79	Module part number	0	0	1	1	0	1	0	1	35	5
80	Module part number	0	0	1	1	0	1	1	0	36	6
81	Module part number	0	0	1	1	1	0	0	0	38	8
82	Module part number	0	1	0	0	1	0	1	1	4B	K
83	Module part number	0	1	0	0	1	1	1	0	4E	N
84	Module part number	0	0	1	0	1	1	0	1	2D	—
85	Module part number -A75B	0	1	0	0	0	0	0	1	41	A
	-B75B	0	1	0	0	0	0	1	0	42	B
	-10B	0	0	1	1	0	0	0	1	31	1
86	Module part number -A75B/B75B	0	0	1	1	0	1	1	1	37	7
	-10B	0	0	1	1	0	0	0	0	30	0
87	Module part number -A75B/B75B	0	0	1	1	0	1	0	1	35	5
	-10B	0	1	0	0	0	0	1	0	42	B
88	Module part number -A75B/B75B	0	1	0	0	0	0	1	0	42	B
	-10B	0	0	1	0	0	0	0	0	20	(Space)
89 to 90	Module part number	0	0	1	0	0	0	0	0	20	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30	Initial
92	Revision code	0	0	1	0	0	0	0	0	20	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	××	Year code (BCD)
94	Manufacturing date	×	×	×	×	×	×	×	×	××	Week code (BCD)
95 to 98	Module serial number	*3									
99 to 127	Manufacturer specific data	*4									

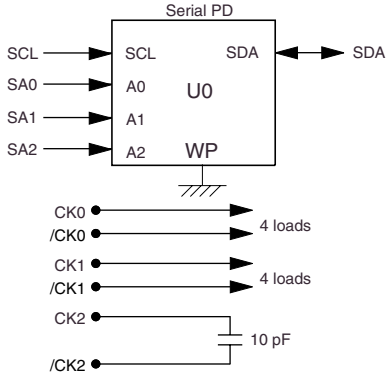
Notes: 1. All serial PD data are not protected. 0: Serial data, “driven Low”, 1: Serial data, “driven High” These SPD are based on JEDEC Committee Ballot JC-42.5-99-129.
2. Byte72 is manufacturing location code. (ex: In case of Japan, byte72 is 4AH. 4AH shows “J” on ASCII code.)
3. Bytes 95 through 98 are assembly serial number.
4. All bits of 99 through 127 are not defined (“1” or “0”).
5. These specifications are defined based on component specification, not module.

Block Diagram



* D0 to D7 : 256M bits DDR SDRAM
U0 : 2k bits EEPROM
Rs : 22Ω

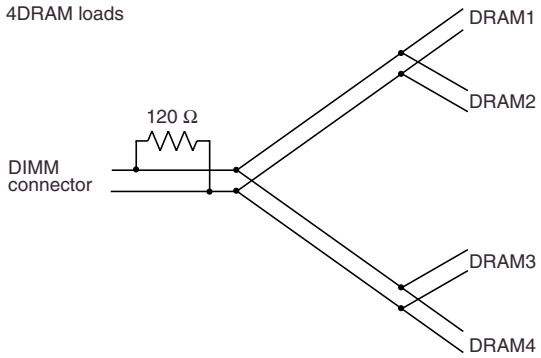




Notes :

1. DQ wiring may differ from that described in this drawing; however DQ/DM/DQS relationships are maintained as shown.
   VCCID strap connections:
   (for memory device VCC, VCCQ)
   Strap out (open): VCC = VCCQ
   Strap in (closed): VCC ≠ VCCQ
2. The SDA pull-up registor is reguired due to the open-drain/open-collector output.
3. The SCL pull-up registor is recommended, because of the normal SCL lime inactive "high" state.

Logical Clock Net Structure



Pin Functions (1)

CK (CLK), /CK (/CLK) (input pin): The CK and the /CK are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CK rising edge and the VREF level. When a read operation, DQSs and DQs are referred to the cross point of the CK and the /CK. When a write operation, DMs and DQs are referred to the cross point of the DQS and the VREF level. DQSs for write operation are referred to the cross point of the CK and the /CK.

/S (/CS) (input pin): When /S is Low, commands and data can be input. When /S is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

/RAS, /CAS, and /WE (input pins): These pins define operating commands (read, write, etc.) depending on the combinations of their voltage levels. See "Command operation".

A0 to A12 (input pins): Row address (AX0 to AX12) is determined by the A0 to the A12 level at the cross point of the CK rising edge and the VREF level in a bank active command cycle. Column address (AY0 to AY8) is loaded via the A0 to the A8 at the cross point of the CK rising edge and the VREF level in a read or a write command cycle. This column address becomes the starting address of a burst operation.

A10 (AP) (input pin): A10 defines the precharge mode when a precharge command, a read command or a write command is issued. If A10 = High when a precharge command is issued, all banks are precharged. If A10 = Low when a precharge command is issued, only the bank that is selected by BA1, BA0 is precharged. If A10 = High when read or write command, auto-precharge function is enabled. While A10 = Low, auto-precharge function is disabled.

BA0, BA1 (input pin): BA0/BA1 are bank select signals. The memory array is divided into bank 0, bank 1, bank 2 and bank 3. If BA1 = Low and BA0 = Low, bank 0 is selected. If BA1 = High and BA0 = Low, bank 1 is selected. If BA1 = Low and BA0 = High, bank 2 is selected. If BA1 = High and BA0 = High, bank 3 is selected.

CKE (input pin): CKE controls power down and self-refresh. The power down and the self-refresh commands are entered when the CKE is driven Low and exited when it resumes to High.

The CKE level must be kept for 1 CK cycle (= LCKEPW) at least, that is, if CKE changes at the cross point of the CK rising edge and the VREF level with proper setup time tIS, at the next CK rising edge CKE level must be kept with proper hold time tIH.

Pin Functions (2)

DQ (input and output pins): Data are input to and output from these pins.

DQS (input and output pin): DQS provide the read data strobes (as output) and the write data strobes (as input).

DM (input pins): DM is the reference signal of the data input mask function. DMs are sampled at the cross point of DQS and VREF

VCC and VCCQ (power supply pins): 2.5V is applied. (VCC is for the internal circuit and VCCQ is for the output buffer.)

VCCSPD (power supply pin): 2.5V is applied (For serial EEPROM).

VSS (power supply pin): Ground is connected.

Detailed Operation Part, AC Characteristics and Timing Waveforms

Refer to the HM5425161B/HM5425801B/HM5425401B Series datasheet (E0086H).

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to VSS	VT	–1.0 to +4.6	V	1
Supply voltage relative to VSS	VCC, VCCQ	–1.0 to +4.6	V	1
Short circuit output current	IOUT	50	mA	
Power dissipation	PT	8	W	
Operating temperature	Topr	0 to +65	°C	
Storage temperature	Tstg	–50 to +100	°C	

Notes: 1. Respect to VSS.

DC Operating Conditions (TA = 0 to +65°C)

Parameter	Symbol	min.	Typ	max.	Unit	Notes
Supply voltage	VCC, VCCQ	2.3	2.5	2.7	V	1, 2
	VSS	0	0	0	V	
Input reference voltage	VREF	1.15	1.25	1.35	V	1
Termination voltage	VTT	VREF – 0.04	VREF	VREF + 0.04	V	1
DC Input high voltage	VIH	VREF + 0.18	—	VCCQ + 0.3	V	1, 3
DC Input low voltage	VIL	–0.3	—	VREF – 0.18	V	1, 4
DC Input signal voltage	VIN (dc)	–0.3	—	VCCQ + 0.3	V	5
DC differential input voltage	VSWING (dc)	0.36	—	VCCQ + 0.6	V	6

Notes: 1. All parameters are referred to VSS, when measured.
2. VCCQ must be lower than or equal to VCC.
3. VIH is allowed to exceed VCC up to 4.6V for the period shorter than or equal to 5ns.
4. VIL is allowed to outreach below VSS down to –1.0V for the period shorter than or equal to 5ns.
5. VIN (dc) specifies the allowable dc execution of each differential input.
6. VSWING (dc) specifies the input differential voltage required for switching.

DC Characteristics 1 (TA = 0 to 65°C, VCC, VCCQ = 2.5V ± 0.2V, VSS = 0V)

Parameter	Symbol	Grade	max.	Unit	Test condition	Notes
Operating current (ACTV-PRE)	ICC0	-A75B -B75B -10B	600 560 480	mA	CKE ≥ VIH, tRC = min.	1, 2, 5
Operating current (ACTV-READ-PRE)	ICC1	-A75B -B75B -10B	820 760 680	mA	CKE ≥ VIH, BL = 2, CL = 2.5, tRC = min.	1, 2, 5
Idle power down standby current	ICC2P	-A75B -B75B -10B	144 120 96	mA	CKE ≤ VIL	4
Idle standby current	ICC2N	-A75B -B75B -10B	320 280 240	mA	CKE ≥ VIH, /CS ≥ VIH	4
Active power down standby current	ICC3P	-A75B -B75B -10B	200 160 120	mA	CKE ≤ VIL	3
Active standby current	ICC3N	-A75B -B75B -10B	400 360 320	mA	CKE ≥ VIH, /CS ≥ VIH tRAS = max.	3
Operating current (Burst read operation)	ICC4R	-A75B -B75B -10B	1220 1160 1100	mA	CKE ≥ VIH, BL = 2, CL = 2.5	1, 2, 5, 6
Operating current (Burst write operation)	ICC4W	-A75B -B75B -10B	1160 1100 1040	mA	CKE ≥ VIH, BL = 2, CL = 2.5	1, 2, 5, 6
Auto refresh current	ICC5	-A75B -B75B -10B	1020 980 880	mA	tRFC = min., Input ≤ VIL or ≥ VIH	
Self refresh current	ICC6		24	mA	Input ≥ VCC – 0.2V Input ≤ 0.2V.	

Notes. 1. These ICC data are measured under condition that DQ pins are not connected.
2. One bank operation.
3. One bank active.
4. All banks idle.
5. Command/Address transition once per one cycle.
6. Data/Data mask transition twice per one cycle.
7. The ICC data on this table are measured with regard to tCK = min. in general.

DC Characteristics 2 (TA = 0 to 65°C, VCC, VCCQ = 2.5V ± 0.2V, VSS = 0V)

Parameter	Symbol	min.	max.	Unit	Test condition	Notes
Input leakage current	ILI	–10	10	µA	VCC ≥ VIN ≥ VSS	
Output leakage current	ILO	–10	10	µA	VCC ≥ VOUT ≥ VSS	
Output high voltage	VOH	VTT + 0.76	—	V	IOH (max.) = –15.2mA	
Output low voltage	VOL	—	VTT – 0.76	V	IOL (min.) = 15.2mA	

Pin Capacitance (TA = 25°C, VCC, VCCQ = 2.5V ± 0.2V)

[Parameter	Symbol	Pins	min.	max.	Unit	Notes
Input capacitance	CI1	Address, /RAS, /CAS, /WE	—	60	pF	1
Input capacitance	CI2	CKE, /S CK, /CK	—	40	pF	1
Data and DQS input/output capacitance	CO	DQ, DQS, DM	—	27	pF	1, 2

Notes: 1.These parameters are measured on conditions: f = 100MHz, VOUT = VCCQ/2, ΔVOUT = 0.2V.

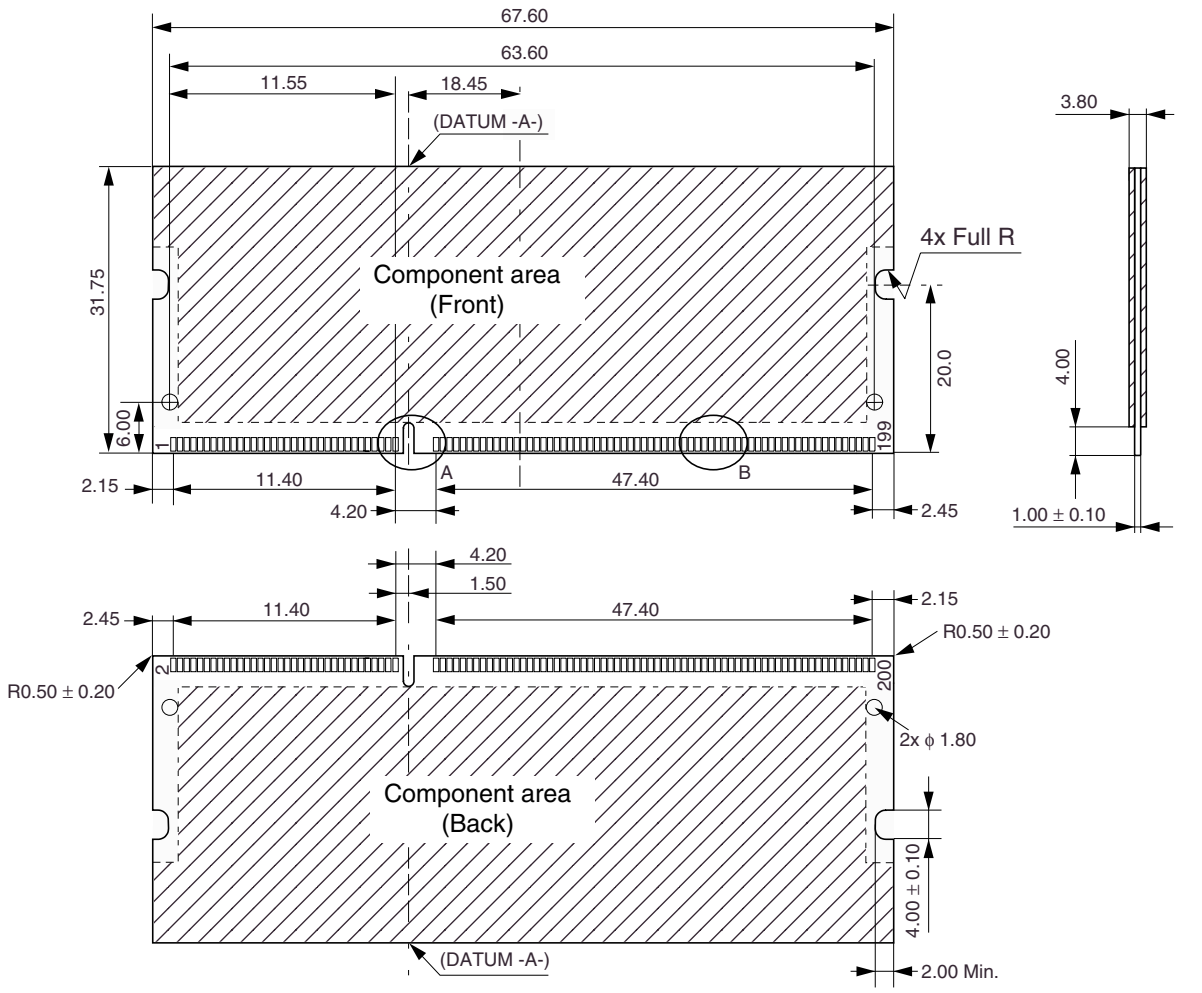
2. Dout circuits are disabled.

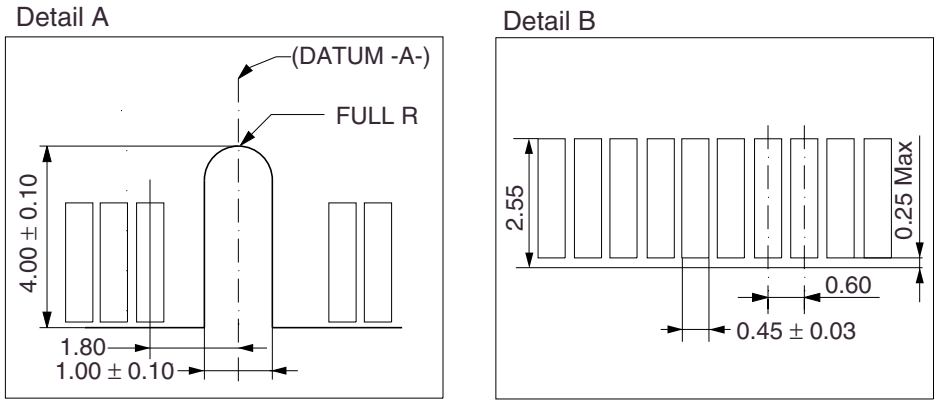
Timing Parameter Measured in Clock Cycle for Unbuffered DIMM

		Number of clock cycle	
Parameter	Symbol	min.	max.
Write to pre-charge command delay (same bank)	tWPD	3 + BL/2	
Read to pre-charge command delay (same bank)	tRPD	BL/2	
Write to read command delay (to input all data)	tWRD	2 + BL/2	
Burst stop command to write command delay (CL = 2)	tBSTW	2	
(CL = 2.5)	tBSTW	3	
Burst stop command to DQ High-Z (CL = 2)	tBSTZ	2	
(CL = 2.5)	tBSTZ	2.5	
Read command to write command delay (to output all data) (CL = 2)	tRWD	2 + BL/2	
(CL = 2.5)	tRWD	3 + BL/2	
Pre-charge command to High-Z (CL = 2)	tHZP	2	
(CL = 2.5)	tHZP	2.5	
Write command to data in latency	tWCD	1	
Write recovery	tWR	2	
DM to data in latency	tDMD	0	
Register set command to active or register set command	tMRD	2	
Self refresh exit to non-read command	tSNR	10	
Self refresh exit to read command	tSRD	200	
Power down entry	tPDEN	1	
Power down exit to command input	tPDEX	1	
CKE minimum pulse width	tCKEPW	1	

Physical Outline

Unit: mm





ECA-TS2-0019-01

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.
In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other.
Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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