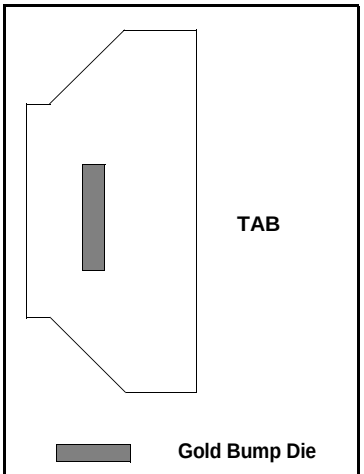
SSD1812

Product Preview

LCD Segment / Common Driver with Controller

CMOS



ORDERING INFORMATION

SSD1812Z	Gold Bump Die
SSD1812TR	TAB

SSD1812 is a single-chip CMOS LCD driver with controller for liquid crystal dot-matrix graphic display system. It consists of 187 high voltage driving output pins for driving 132 Segments, 54 Commons and 1 Icon Driving-Common.

SSD1812 displays data directly from its internal 132 X 65 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through a software selectable 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface.

SSD1812 embeds a DC-DC Converter, an On-Chip Bias Divider and an On-Chip Oscillator which reduce the number of external components. With the special design on minimizing power consumption and die/package layout, SSD1812 is suitable for any portable battery-driven applications requiring a long operation period and a compact size.

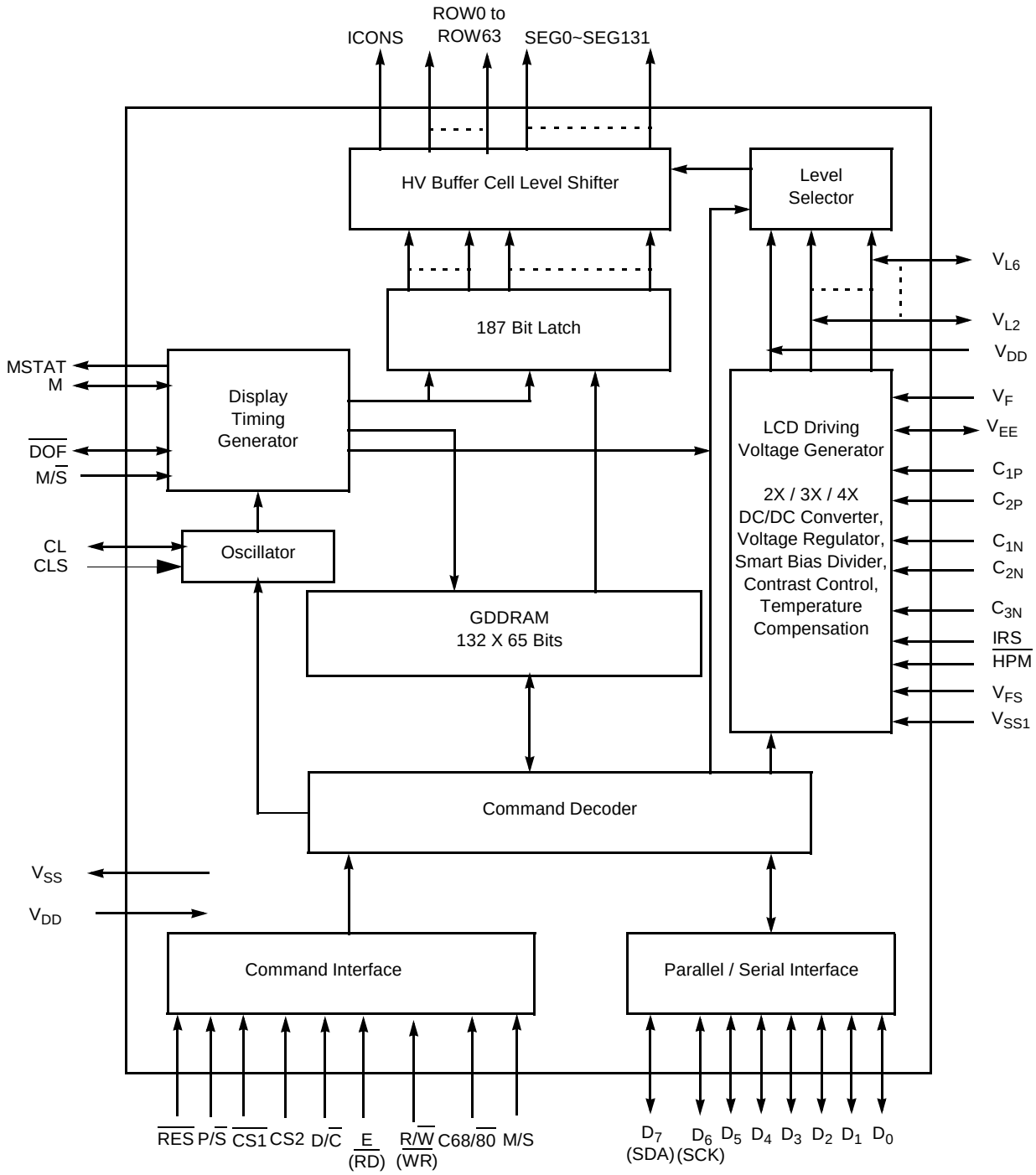
- Single Supply Operation, 1.8 V - 3.5V
- Minimum -12.0V LCD Driving Output Voltage
- Low Current Sleep Mode
- On-Chip Voltage Generator / External Power Supply
- 2X / 3X / 4X On-Chip DC-DC Converter
- On-Chip Oscillator
- Programmable Multiplex ratio [1Mux - 55Mux]
- On-Chip Smart Bias Divider
- Programmable 1/4, 1/5, 1/6, 1/7, 1/8 and 1/9 bias ratio
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface and Serial Peripheral Interface
- On-Chip 132 x 65 Graphic Display Data RAM
- Re-mapping of Row and Column Drivers
- Vertical Scrolling
- Display Offset Control
- RAM Page Blinking
- 64 Level Internal Contrast Control
- External Contrast Control
- Selectable LCD Driving Voltage Temperature Coefficients (8 settings)
- Available in Gold Bump Die and Standard TAB (Tape Automated Bonding) Package

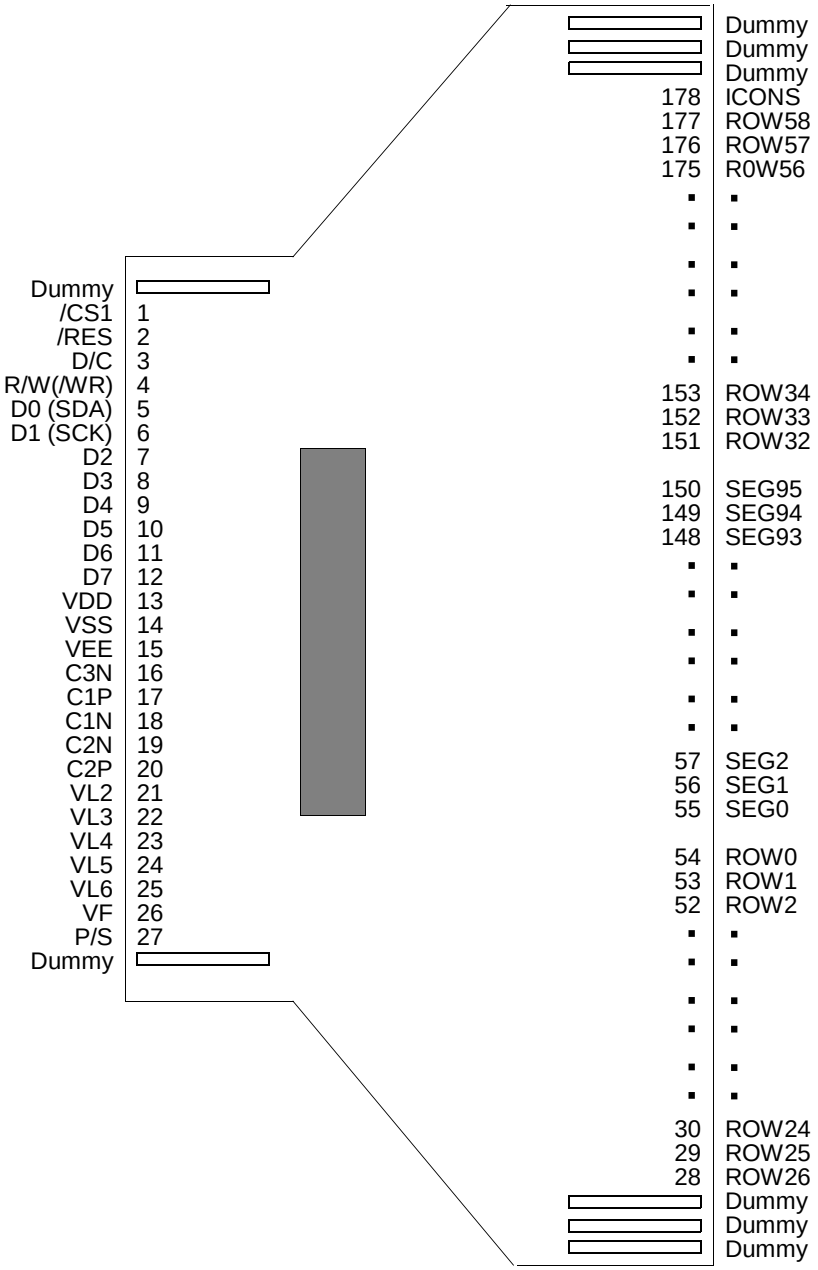
This document contains information on a new product under development. Solomon reserves the right to change or discontinue this product without notice.

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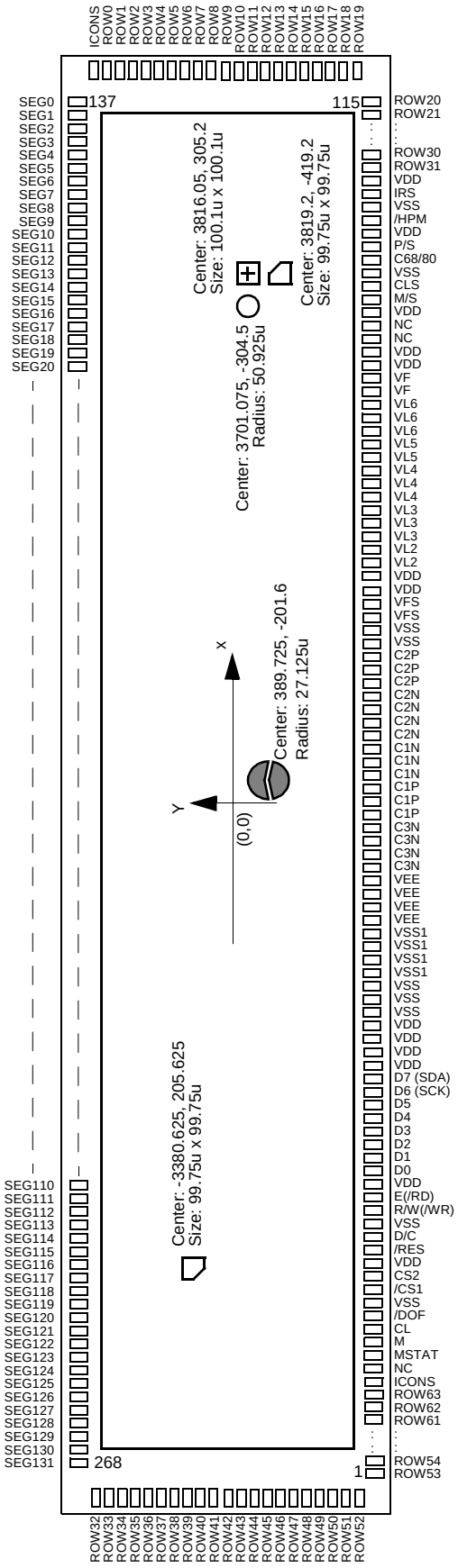
SOLOMON

Block Diagram





SSD1812T Pin Assignment
(Copper View)



SSD1812Z Die Pin Assignment

Gold Bump Alignment Mark
This alignment mark contains gold nump for IC bumping process alignment and IC identifications. No conductive tracks should be laid underneath this mark to avoid short circuit.

Note:
Coordinates and Size of all alignment marks are in unit um and w.r.t. center of the chip.

PIN #1

Die Size: 10.977mm X 1.912mm
Die Thickness: 533 +/-25um
Bump Pitch: 76.2 um [Min]
Bump Height: Nominal 18um

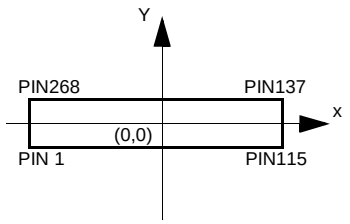
Table 1. ROW pins assignment for COM signals in Programmable Multiplex Ratio
[On power-on-reset, SSD1812 is set to 54 Multiplex]

Die Pad Name	54 Mux Com Signal Output	53 Mux Com Signal Output	52 Mux Com Signal Output	51 Mux Com Signal Output	48 Mux Com Signal Output	47 Mux Com Signal Output	34 Mux Com Signal Output	33 Mux Com Signal Output	32 Mux Com Signal Output
ROW0	COM0	COM0	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW1	COM1	COM1	COM0	COM0	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW2	COM2	COM2	COM1	COM1	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW3	COM3	COM3	COM2	COM2	COM0	COM0	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW4	COM4	COM4	COM3	COM3	COM1	COM1	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW5	COM5	COM5	COM4	COM4	COM2	COM2	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW6	COM6	COM6	COM5	COM5	COM3	COM3	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW7	COM7	COM7	COM6	COM6	COM4	COM4	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW8	COM8	COM8	COM7	COM7	COM5	COM5	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW9	COM9	COM9	COM8	COM8	COM6	COM6	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW10	COM10	COM10	COM9	COM9	COM7	COM7	COM0	COM0	NON-SELECT*
ROW11	COM11	COM11	COM10	COM10	COM8	COM8	COM1	COM1	COM0
ROW12	COM12	COM12	COM11	COM11	COM9	COM9	COM2	COM2	COM1
ROW13	COM13	COM13	COM12	COM12	COM10	COM10	COM3	COM3	COM2
ROW14	COM14	COM14	COM13	COM13	COM11	COM11	COM4	COM4	COM3
ROW15	COM15	COM15	COM14	COM14	COM12	COM12	COM5	COM5	COM4
ROW16	COM16	COM16	COM15	COM15	COM13	COM13	COM6	COM6	COM5
ROW17	COM17	COM17	COM16	COM16	COM14	COM14	COM7	COM7	COM6
ROW18	COM18	COM18	COM17	COM17	COM15	COM15	COM8	COM8	COM7
ROW19	COM19	COM19	COM18	COM18	COM16	COM16	COM9	COM9	COM8
ROW20	COM20	COM20	COM19	COM19	COM17	COM17	COM10	COM10	COM9
ROW21	COM21	COM21	COM20	COM20	COM18	COM18	COM11	COM11	COM10
ROW22	COM22	COM22	COM21	COM21	COM19	COM19	COM12	COM12	COM11
ROW23	COM23	COM23	COM22	COM22	COM20	COM20	COM13	COM13	COM12
ROW24	COM24	COM24	COM23	COM23	COM21	COM21	COM14	COM14	COM13
ROW25	COM25	COM25	COM24	COM24	COM22	COM22	COM15	COM15	COM14
ROW26	COM26	COM26	COM25	COM25	COM23	COM23	COM16	COM16	COM15
ROW27	NC	NC	NC	NC	NC	NC	NC	NC	NC
ROW28	NC	NC	NC	NC	NC	NC	NC	NC	NC
ROW29	NC	NC	NC	NC	NC	NC	NC	NC	NC
ROW30	NC	NC	NC	NC	NC	NC	NC	NC	NC
ROW31	NC	NC	NC	NC	NC	NC	NC	NC	NC
ROW32	COM27	COM27	COM26	COM26	COM24	COM24	COM17	COM17	COM16
ROW33	COM28	COM28	COM27	COM27	COM25	COM25	COM18	COM18	COM17
ROW34	COM29	COM29	COM28	COM28	COM26	COM26	COM19	COM19	COM18
ROW35	COM30	COM30	COM29	COM29	COM27	COM27	COM20	COM20	COM19
ROW36	COM31	COM31	COM30	COM30	COM28	COM28	COM21	COM21	COM20
ROW37	COM32	COM32	COM31	COM31	COM29	COM29	COM22	COM22	COM21
ROW38	COM33	COM33	COM32	COM32	COM30	COM30	COM23	COM23	COM22
ROW39	COM34	COM34	COM33	COM33	COM31	COM31	COM24	COM24	COM23
ROW40	COM35	COM35	COM34	COM34	COM32	COM32	COM25	COM25	COM24
ROW41	COM36	COM36	COM35	COM35	COM33	COM33	COM26	COM26	COM25
ROW42	COM37	COM37	COM36	COM36	COM34	COM34	COM27	COM27	COM26
ROW43	COM38	COM38	COM37	COM37	COM35	COM35	COM28	COM28	COM27
ROW44	COM39	COM39	COM38	COM38	COM36	COM36	COM29	COM29	COM28
ROW45	COM40	COM40	COM39	COM39	COM37	COM37	COM30	COM30	COM29
ROW46	COM41	COM41	COM40	COM40	COM38	COM38	COM31	COM31	COM30
ROW47	COM42	COM42	COM41	COM41	COM39	COM39	COM32	COM32	COM31
ROW48	COM43	COM43	COM42	COM42	COM40	COM40	COM33	NON-SELECT*	NON-SELECT*
ROW49	COM44	COM44	COM43	COM43	COM41	COM41	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW50	COM45	COM45	COM44	COM44	COM42	COM42	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW51	COM46	COM46	COM45	COM45	COM43	COM43	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW52	COM47	COM47	COM46	COM46	COM44	COM44	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW53	COM48	COM48	COM47	COM47	COM45	COM45	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW54	COM49	COM49	COM48	COM48	COM46	COM46	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW55	COM50	COM50	COM49	COM49	COM47	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW56	COM51	COM51	COM50	COM50	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW57	COM52	COM52	COM51	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW58	COM53	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW59	NC	NC	NC	NC	NC	NC	NC	NC	NC
ROW60	NC	NC	NC	NC	NC	NC	NC	NC	NC
ROW61	NC	NC	NC	NC	NC	NC	NC	NC	NC
ROW62	NC	NC	NC	NC	NC	NC	NC	NC	NC
ROW63	NC	NC	NC	NC	NC	NC	NC	NC	NC

Remark:
* The ROW will output a Non-Select COM signal.
* NC = No Connection.

SSD1812Z Die Pad Coordinates

PAD #	NAME	X	Y	PAD #	NAME	X	Y	PAD #	NAME	X	Y
1	ROW53	-4958.45	-751.98	61	C2N	266.70	-771.93	116	ROW19	5285.18	-768.78
2	ROW54	-4882.15	-751.98	62	C2N	355.60	-771.93	117	ROW18	5285.18	-692.48
3	ROW55	-4805.85	-751.98	63	C2N	444.50	-771.93	118	ROW17	5285.18	-616.18
4	ROW56	-4729.55	-751.98	64	C2N	533.40	-771.93	119	ROW16	5285.18	-539.88
5	ROW57	-4653.25	-751.98	65	C2P	622.30	-771.93	120	ROW15	5285.18	-463.58
6	ROW58	-4576.95	-751.98	66	C2P	711.20	-771.93	121	ROW14	5285.18	-387.28
7	ROW59	-4500.65	-751.98	67	C2P	800.10	-771.93	122	ROW13	5285.18	-310.98
8	ROW60	-4424.35	-751.98	68	VSS	889.00	-771.93	123	ROW12	5285.18	-234.68
9	ROW61	-4348.05	-751.98	69	VSS	977.90	-771.93	124	ROW11	5285.18	-158.38
10	ROW62	-4271.75	-751.98	70	VFS	1066.80	-771.93	125	ROW10	5285.18	-82.08
11	ROW63	-4195.45	-751.98	71	VFS	1155.70	-771.93	126	ROW9	5285.18	-5.78
12	ICONS	-4119.15	-751.98	72	VDD	1244.60	-771.93	127	ROW8	5285.18	70.53
13	NC	-4000.50	-771.93	73	VDD	1333.50	-771.93	128	ROW7	5285.18	146.83
14	MSTAT	-3911.60	-771.93	74	VL2	1422.40	-771.93	129	ROW6	5285.18	223.13
15	M	-3822.70	-771.93	75	VL2	1511.30	-771.93	130	ROW5	5285.18	299.43
16	CL	-3733.80	-771.93	76	VL3	1600.20	-771.93	131	ROW4	5285.18	375.73
17	/DOF	-3644.90	-771.93	77	VL3	1689.10	-771.93	132	ROW3	5285.18	452.03
18	VSS	-3556.00	-771.93	78	VL3	1778.00	-771.93	133	ROW2	5285.18	528.33
19	/CS1	-3467.10	-771.93	79	VL4	1866.90	-771.93	134	ROW1	5285.18	604.63
20	CS2	-3378.20	-771.93	80	VL4	1955.80	-771.93	135	ROW0	5285.18	680.93
21	VDD	-3289.30	-771.93	81	VL4	2044.70	-771.93	136	ICONS	5285.18	757.23
22	/RES	-3200.40	-771.93	82	VL5	2133.60	-771.93				
23	D/C	-3111.50	-771.93	83	VL5	2222.50	-771.93				
24	VSS	-3022.60	-771.93	84	VL6	2311.40	-771.93				
25	R/W	-2933.70	-771.93	85	VL6	2400.30	-771.93				
26	E/RD	-2844.80	-771.93	86	VL6	2489.20	-771.93				
27	VDD	-2755.90	-771.93	87	VF	2578.10	-771.93				
28	D 0	-2667.00	-771.93	88	VF	2667.00	-771.93				
29	D 1	-2578.10	-771.93	89	VDD	2755.90	-771.93				
30	D 2	-2489.20	-771.93	90	VDD	2844.80	-771.93				
31	D 3	-2400.30	-771.93	91	NC	2933.70	-771.93				
32	D 4	-2311.40	-771.93	92	NC	3022.60	-771.93				
33	D 5	-2222.50	-771.93	93	VDD	3111.50	-771.93				
34	D 6	-2133.60	-771.93	94	M/S	3200.40	-771.93				
35	D 7	-2044.70	-771.93	95	CLS	3289.30	-771.93				
36	VDD	-1955.80	-771.93	96	VSS	3378.20	-771.93				
37	VDD	-1866.90	-771.93	97	C68/80	3467.10	-771.93				
38	VDD	-1778.00	-771.93	98	P/S	3556.00	-771.93				
39	VDD	-1689.10	-771.93	99	VDD	3644.90	-771.93				
40	VSS	-1600.20	-771.93	100	/HPM	3733.80	-771.93				
41	VSS	-1511.30	-771.93	101	VSS	3822.70	-771.93				
42	VSS	-1422.40	-771.93	102	IRS	3911.60	-771.93				
43	VSS1	-1333.50	-771.93	103	VDD	4000.50	-771.93				
44	VSS1	-1244.60	-771.93	104	ROW31	4119.15	-751.98				
45	VSS1	-1155.70	-771.93	105	ROW30	4195.45	-751.98				
46	VSS1	-1066.80	-771.93	106	ROW29	4271.75	-751.98				
47	VEE	-977.90	-771.93	107	ROW28	4348.05	-751.98				
48	VEE	-889.00	-771.93	108	ROW27	4424.35	-751.98				
49	VEE	-800.10	-771.93	109	ROW26	4500.65	-751.98				
50	VEE	-711.20	-771.93	110	ROW25	4576.95	-751.98				
51	C3N	-622.30	-771.93	111	ROW24	4653.25	-751.98				
52	C3N	-533.40	-771.93	112	ROW23	4729.55	-751.98				
53	C3N	-444.50	-771.93	113	ROW22	4805.85	-751.98				
54	C3N	-355.60	-771.93	114	ROW21	4882.15	-751.98				
55	C1P	-266.70	-771.93	115	ROW20	4958.45	-751.98				
56	C1P	-177.80	-771.93								
57	C1P	-88.90	-771.93								
58	C1N	0.00	-771.93								
59	C1N	88.90	-771.93								
60	C1N	177.80	-771.93								



Die Size: 10.977mm X 1.912mm
Bump Height: 18 +/- 4um (Chip to chip), 18 +/- 2um (Within chip)

Die Size: 10.977mm X 1.912mm
Bump Size:

Pad #	X [um]	Y [um]	Pad #	X [um]	Y [um]	Pad #	X [um]	Y [um]	Pad #	X [um]	Y [um]
1 - 12	43.5	101.6	116 - 136	101.6	43.5	137 - 268	43.5	101.6	269 - 289	101.6	43.5
13 - 103	61.7	61.7	Gold bump size tolerance: +/-1.5um.								
104 - 115	43.5	101.6									

SSD1812Z Die Pad Coordinates

PAD #	NAME	X	Y	PAD #	NAME	X	Y	PAD #	NAME	X	Y
137	SEG0	4997.65	751.98	203	SEG66	-38.15	751.98	269	ROW32	-5285.18	757.23
138	SEG1	4921.35	751.98	204	SEG67	-114.45	751.98	270	ROW33	-5285.18	680.93
139	SEG2	4845.05	751.98	205	SEG68	-190.75	751.98	271	ROW34	-5285.18	604.63
140	SEG3	4768.75	751.98	206	SEG69	-267.05	751.98	272	ROW35	-5285.18	528.33
141	SEG4	4692.45	751.98	207	SEG70	-343.35	751.98	273	ROW36	-5285.18	452.03
142	SEG5	4616.15	751.98	208	SEG71	-419.65	751.98	274	ROW37	-5285.18	375.73
143	SEG6	4539.85	751.98	209	SEG72	-495.95	751.98	275	ROW38	-5285.18	299.43
144	SEG7	4463.55	751.98	210	SEG73	-572.25	751.98	276	ROW39	-5285.18	223.13
145	SEG8	4387.25	751.98	211	SEG74	-648.55	751.98	277	ROW40	-5285.18	146.83
146	SEG9	4310.95	751.98	212	SEG75	-724.85	751.98	278	ROW41	-5285.18	70.53
147	SEG10	4234.65	751.98	213	SEG76	-801.15	751.98	279	ROW42	-5285.18	-5.78
148	SEG11	4158.35	751.98	214	SEG77	-877.45	751.98	280	ROW43	-5285.18	-82.08
149	SEG12	4082.05	751.98	215	SEG78	-953.75	751.98	281	ROW44	-5285.18	-158.38
150	SEG13	4005.75	751.98	216	SEG79	-1030.05	751.98	282	ROW45	-5285.18	-234.68
151	SEG14	3929.45	751.98	217	SEG80	-1106.35	751.98	283	ROW46	-5285.18	-310.98
152	SEG15	3853.15	751.98	218	SEG81	-1182.65	751.98	284	ROW47	-5285.18	-387.28
153	SEG16	3776.85	751.98	219	SEG82	-1258.95	751.98	285	ROW48	-5285.18	-463.58
154	SEG17	3700.55	751.98	220	SEG83	-1335.25	751.98	286	ROW49	-5285.18	-539.88
155	SEG18	3624.25	751.98	221	SEG84	-1411.55	751.98	287	ROW50	-5285.18	-616.18
156	SEG19	3547.95	751.98	222	SEG85	-1487.85	751.98	288	ROW51	-5285.18	-692.48
157	SEG20	3471.65	751.98	223	SEG86	-1564.15	751.98	289	ROW52	-5285.18	-768.78
158	SEG21	3395.35	751.98	224	SEG87	-1640.45	751.98				
159	SEG22	3319.05	751.98	225	SEG88	-1716.75	751.98				
160	SEG23	3242.75	751.98	226	SEG89	-1793.05	751.98				
161	SEG24	3166.45	751.98	227	SEG90	-1869.35	751.98				
162	SEG25	3090.15	751.98	228	SEG91	-1945.65	751.98				
163	SEG26	3013.85	751.98	229	SEG92	-2021.95	751.98				
164	SEG27	2937.55	751.98	230	SEG93	-2098.25	751.98				
165	SEG28	2861.25	751.98	231	SEG94	-2174.55	751.98				
166	SEG29	2784.95	751.98	232	SEG95	-2250.85	751.98				
167	SEG30	2708.65	751.98	233	SEG96	-2327.15	751.98				
168	SEG31	2632.35	751.98	234	SEG97	-2403.45	751.98				
169	SEG32	2556.05	751.98	235	SEG98	-2479.75	751.98				
170	SEG33	2479.75	751.98	236	SEG99	-2556.05	751.98				
171	SEG34	2403.45	751.98	237	SEG100	-2632.35	751.98				
172	SEG35	2327.15	751.98	238	SEG101	-2708.65	751.98				
173	SEG36	2250.85	751.98	239	SEG102	-2784.95	751.98				
174	SEG37	2174.55	751.98	240	SEG103	-2861.25	751.98				
175	SEG38	2098.25	751.98	241	SEG104	-2937.55	751.98				
176	SEG39	2021.95	751.98	242	SEG105	-3013.85	751.98				
177	SEG40	1945.65	751.98	243	SEG106	-3090.15	751.98				
178	SEG41	1869.35	751.98	244	SEG107	-3166.45	751.98				
179	SEG42	1793.05	751.98	245	SEG108	-3242.75	751.98				
180	SEG43	1716.75	751.98	246	SEG109	-3319.05	751.98				
181	SEG44	1640.45	751.98	247	SEG110	-3395.35	751.98				
182	SEG45	1564.15	751.98	248	SEG111	-3471.65	751.98				
183	SEG46	1487.85	751.98	249	SEG112	-3547.95	751.98				
184	SEG47	1411.55	751.98	250	SEG113	-3624.25	751.98				
185	SEG48	1335.25	751.98	251	SEG114	-3700.55	751.98				
186	SEG49	1258.95	751.98	252	SEG115	-3776.85	751.98				
187	SEG50	1182.65	751.98	253	SEG116	-3853.15	751.98				
188	SEG51	1106.35	751.98	254	SEG117	-3929.45	751.98				
189	SEG52	1030.05	751.98	255	SEG118	-4005.75	751.98				
190	SEG53	953.75	751.98	256	SEG119	-4082.05	751.98				
191	SEG54	877.45	751.98	257	SEG120	-4158.35	751.98				
192	SEG55	801.15	751.98	258	SEG121	-4234.65	751.98				
193	SEG56	724.85	751.98	259	SEG122	-4310.95	751.98				
194	SEG57	648.55	751.98	260	SEG123	-4387.25	751.98				
195	SEG58	572.25	751.98	261	SEG124	-4463.55	751.98				
196	SEG59	495.95	751.98	262	SEG125	-4539.85	751.98				
197	SEG60	419.65	751.98	263	SEG126	-4616.15	751.98				
198	SEG61	343.35	751.98	264	SEG127	-4692.45	751.98				
199	SEG62	267.05	751.98	265	SEG128	-4768.75	751.98				
200	SEG63	190.75	751.98	266	SEG129	-4845.05	751.98				
201	SEG64	114.45	751.98	267	SEG130	-4921.35	751.98				
202	SEG65	38.15	751.98	268	SEG131	-4997.65	751.98				

MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, T_A=25°C)

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{EE}		-4.0 to -12.0	V
V_{in}	Input Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-30 to +85	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, V_{DD}=1.8 to 3.5V, T_A=25°C; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	Logic Circuit Supply Voltage Range	Recommend Operating Voltage	2.4	2.7	3.5	V
	Voltage Generator Circuit Supply Voltage Range	Possible Operating Voltage	1.8	-	3.5	
I_{AC}	Access Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, Voltage Generator On, 4X Converter Enabled, Write accessing, T_{cyc} =3.3MHz, Osc. Freq.=31kHz, Display On.	-	300	TBD	µA
I_{DP1}	Display Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, V_{EE} = -8.1V, Voltage Generator Disabled, R/W(WR) Halt, Osc. Freq. = 31kHz, Display On, V_{L6} - V_{DD} = -8.1V.	-	120	TBD	µA
I_{DP2}	Display Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, V_{EE} = -8.1V, Voltage Generator On, 4x DC-DC Converter Enabled, R/W(WR) Halt, Osc. Freq. = 31kHz, Display On, V_{L6} - V_{DD} = -8.1V.	-	150	TBD	µA
I_{SB}	Standby Mode Supply Current Drain (V_{DD} Pins)	V_{DD}=2.7V, LCD Driving Waveform Off, Osc. Freq. = 31kHz, R/W(WR) halt.	-	3.5	10	µA
I_{SLEEP}	Sleep Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, LCD Driving Waveform Off, Oscillator Off, R/W(WR) halt.	-	0.2	5	µA
V_{EE}	LCD Driving Voltage Generator Output (V_{EE} Pin)	Display On, Voltage Generator Enabled, DC/DC Converter Enabled, Osc. Freq.=31KHz, Regulator Enabled, Divider Enabled.	-12.0	-	-1.8	V
V_{LCD}	LCD Driving Voltage Input (V_{EE} Pin)	Voltage Generator Disabled.	-12.0	-	-1.8	V
V_{OH1}	Output High Voltage (D_0-D_7)	I_{out}=100µA	0.9*V_{DD}	-	V_{DD}	V
V_{OL1}	Output Low Voltage (D_0-D_7)	I_{out}=100µA	0	-	0.1*V_{DD}	V
V_{L6}	LCD Driving Voltage Source (V_{L6} Pin)	Regulator Enabled (V_{L6} voltage depends on Int/Ext Contrast Control)	V_{EE}-0.5	-	V_{DD}	V
V_{L6}	LCD Driving Voltage Source (V_{L6} Pin)	Regulator Disable	-	Floating	-	V

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, V_{DD}=1.8 to 3.5V, T_A=25°C; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IH1}	Input high voltage ($\overline{RES}$, D_0-D_7,R/$\overline{W}$($\overline{WR}$), D/$\overline{C}$)		0.8*V_{DD}	-	V_{DD}	V
V_{IL1}	Input Low voltage ($\overline{RES}$, $\overline{CS1}$,CS2, D_0-D_7, R/$\overline{W}$($\overline{WR}$), D/$\overline{C}$, S/$\overline{P}$)		0	-	0.2*V_{DD}	V
V_{L2}	LCD Display Voltage Output	Voltage reference to V_{DD}, Smart Bias Divider	-	1/6*V_{L6}	-	V
V_{L3}	(V_{L2}, V_{L3}, V_{L4}, V_{L5}, V_{L6} Pins)	Enabled, 1:6 bias ratio	-	2/6*V_{L6}	-	V
V_{L4}			-	4/6*V_{L6}	-	V
V_{L5}			-	5/6*V_{L6}	-	V
V_{L6}			-	V_{L6}	-	V
V_{L2}	LCD Display Voltage Output	Voltage reference to V_{DD}, Smart Bias Divider	-	1/8*V_{L6}	-	V
V_{L3}	(V_{L2}, V_{L3}, V_{L4}, V_{L5}, V_{L6} Pins)	Enabled, 1:8 bias ratio	-	2/8*V_{L6}	-	V
V_{L4}			-	6/8*V_{L6}	-	V
V_{L5}			-	7/8*V_{L6}	-	V
V_{L6}			-	V_{L6}	-	V
V_{L2}	LCD Display Voltage Input	Voltage reference to V_{DD}, External Voltage Gener-	V_{L3}	-	V_{DD}	V
V_{L3}	(V_{L2}, V_{L3},V_{L4}, V_{L5}, V_{L6} Pins)	ator, Smart Bias Divider Disabled	V_{L4}	-	V_{L2}	V
V_{L4}			V_{L5}	-	V_{L3}	V
V_{L5}			V_{L6}	-	V_{L4}	V
V_{L6}			-12V	-	V_{L5}	V
I_{OH}	Output High Current Source (D_0-D_7)	V_{out}=V_{DD}-0.4V	50	-	-	µA
I_{OL}	Output Low Current Drain (D_0-D_7)	V_{out}=0.4V	-	-	-50	µA
I_{OZ}	Output Tri-state Current Drain Source (D_0-D_7)		-1	-	1	µA
I_{IL}/I_{IH}	Input Current ($\overline{RES}$, D_0-D_7, R/$\overline{W}$($\overline{WR}$), D/$\overline{C}$, S/$\overline{P}$)		-1	-	1	µA
C_{IN}	Input Capacitance (all logic pins)		-	5	7.5	pF
ΔV_{L6}	Variation of V_{L6} Output (V_{DD} is fixed)	Regulator Enabled, Internal Contrast Control Enabled, Set Contrast Control Register = 0	-	± 3	-	%
	Temperature Coefficient Compensation					
PTC0	Flat Temperature Coefficient [POR]	Voltage Regulator Enabled	0	-0.01	-0.075	%/C
PTC1	Temperature Coefficient 1*	Voltage Regulator Enabled		TBD		%/C
PTC2	Temperature Coefficient 2*	Voltage Regulator Enabled	-0.075	-0.10	-0.15	%/C
PTC3	Temperature Coefficient 3*	Voltage Regulator Enabled		TBD		%/C
PTC4	Temperature Coefficient 4*	Voltage Regulator Enabled	-0.15	-0.18	-0.20	%/C
PTC5	Temperature Coefficient 5*	Voltage Regulator Enabled		TBD		%/C
PTC6	Temperature Coefficient 6*	Voltage Regulator Enabled		TBD		%/C
PTC7	Temperature Coefficient 7*	Voltage Regulator Enabled	-0.20	-0.25		%/C

* The formula for the temperature coefficient is:

$$TC(\%) = \frac{V_{ref} \text{ at } 50°C - V_{ref} \text{ at } 0°C}{50°C - 0°C} \times \frac{1}{V_{ref} \text{ at } 25°C} \times 100\%$$

AC ELECTRICAL CHARACTERISTICS (T_A=25°C, Voltage referenced to V_{SS}, AV_{DD}=DV_{DD}=3V: unless otherwise specified.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display Timing Generator	Internal Oscillator Enabled	27	31	35	kHz
F_{FRM}	Frame Frequency	Display ON, Set 132X 54 Graphic Display Mode	-	$\frac{F_{OSC}}{8*55}$	-	Hz

TABLE 3. Parallel Timing Characteristics (T_A=25°C, V_{DD}=2.7V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	- -	- -	ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

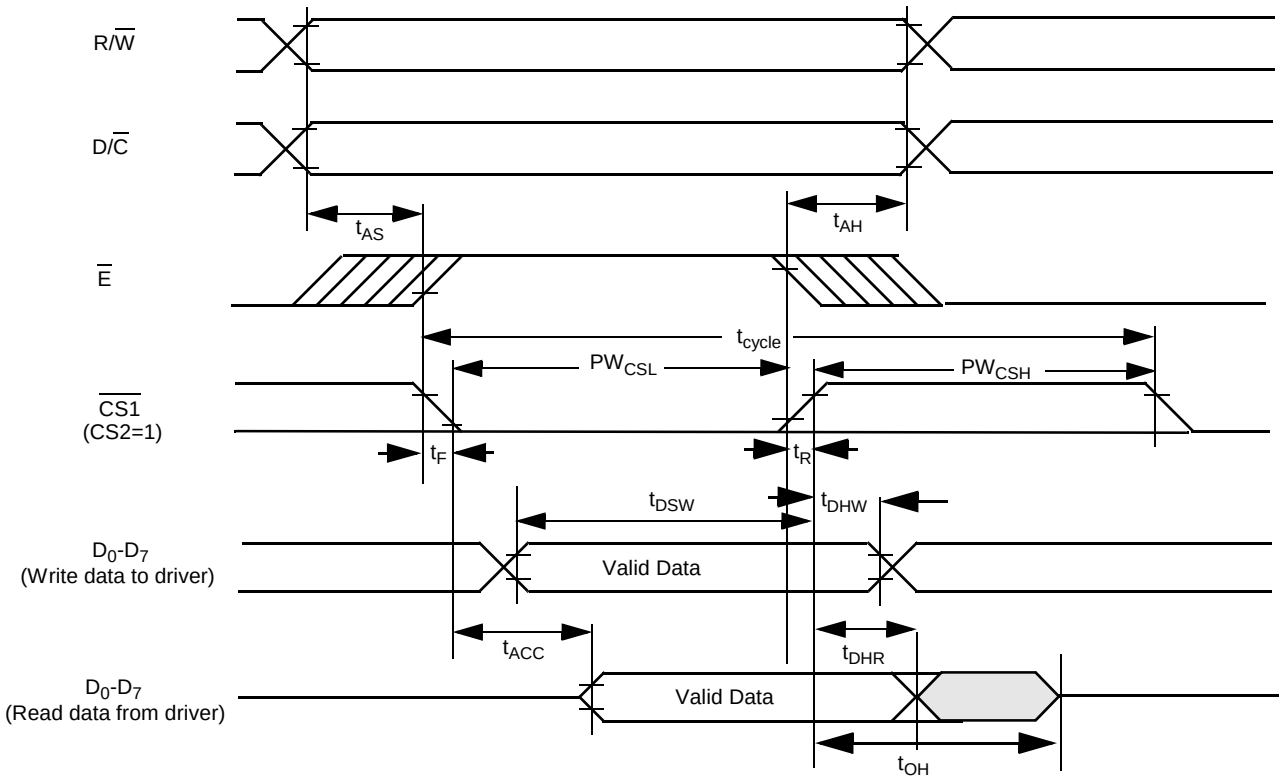


Figure 1. Parallel 6800-series Interface Timing Characteristics

TABLE 4. Parallel Timing Characteristics (T_A=25°C, V_{DD}=2.7V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	20	-	-	ns
t_{DHW}	Write Data Hold Time	40	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	- -	- -	ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

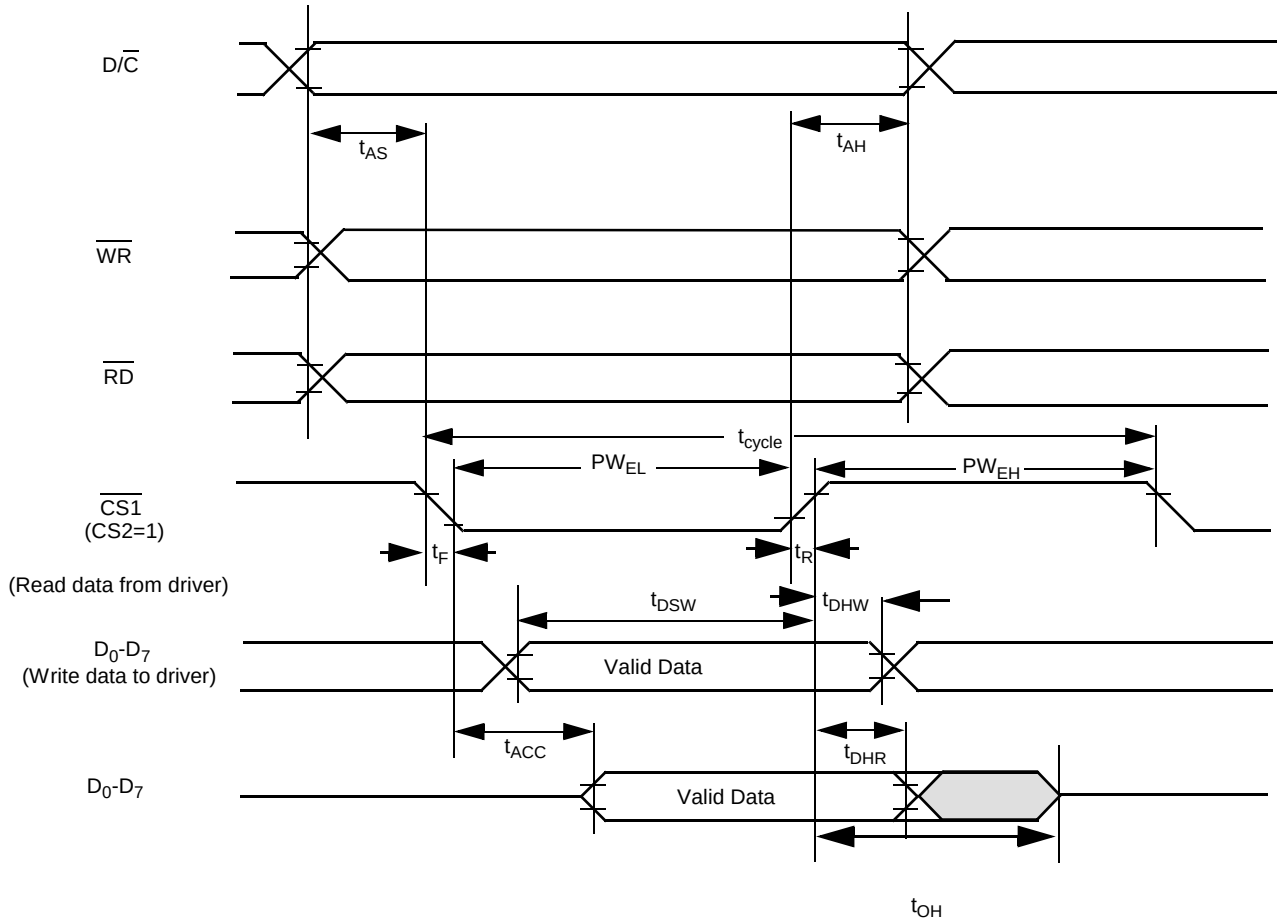


Figure 2. Parallel 8080-series Interface Timing Characteristics

TABLE 5. Serial Timing Characteristics (T_A=25°C, DV_{DD}=2.7V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	400	-	-	ns
t_{AS}	Address Setup Time	250	-	-	ns
t_{AH}	Address Hold Time	250	-	-	ns
t_{CSS}	Chip Select Setup Time	250	-	-	ns
t_{CSH}	Chip Select Hold Time	250	-	-	ns
t_{DSW}	Write Data Setup Time	150	-	-	ns
t_{DHW}	Write Data Hold Time	150	-	-	ns
t_{CLKL}	Clock Low Time	150	-	-	ns
t_{CLKH}	Clock High Time	150	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

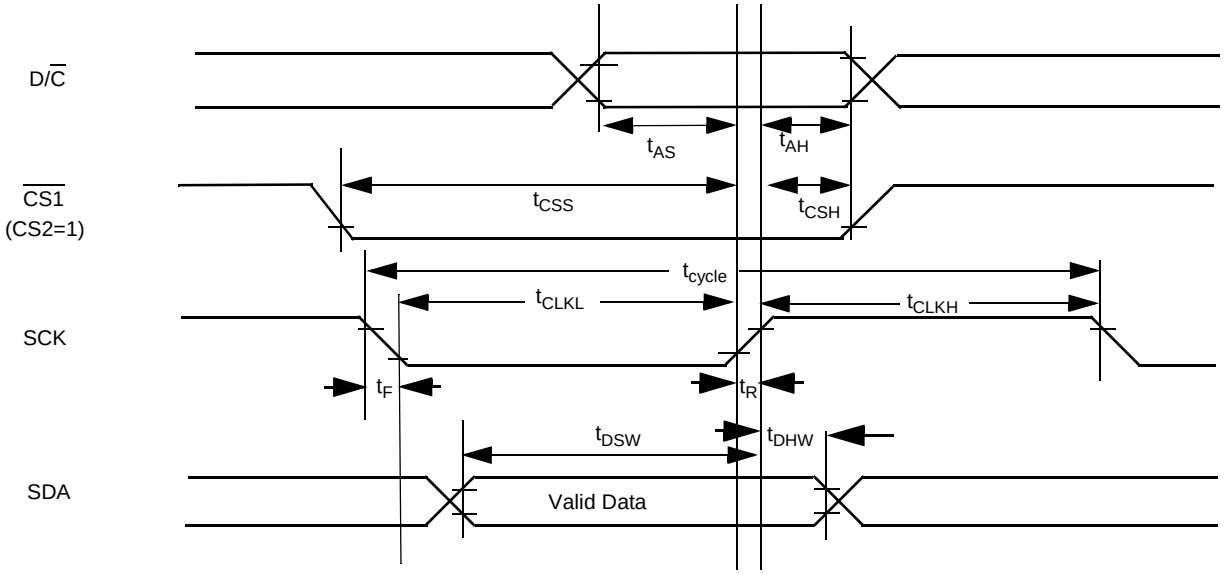


Figure 3. Serial Timing Characteristics

PIN DESCRIPTIONS

M/$\overline{S}$

This pin is master/slave mode selection input. When this pin is pulled high, master mode is selected and CL, M, MSTAT and $\overline{DOF}$ will be output to slave devices. When pulled low, slave mode is selected. CL, M, $\overline{DOF}$ are required to be input from master device while MSTAT is high impedance.

M

This pin is the frame signal input/output. In master mode, the pin supplies frame signal to slave devices while in slave mode, the pin receives frame signal from the master device.

MSTAT

This pin is used together with M in master operation for static drive output. It becomes high impedance in slave mode operation.

CL

This pin is the display clock input/output. In master mode, the pin supplies display clock signal to slave devices while in slave mode, the pin receives display clock signal from the master device.

$\overline{DOF}$

This pin is LCD blanking control input/output. In master mode, the pin supplies on/off signal to slave devices. In slave mode, the pin receives on/off signal from the master device.

CLS

This pin is a internal clock enable input pin. When this pin is high, the internal clock is enabled. The internal clock will be disabled when it is low, an external clock should be input to CL pin.

$\overline{RES}$

This pin is reset signal input. When the pin is low, initialization of the chip is executed.

P/$\overline{S}$

This pin is serial/parallel interface select input. When P/$\overline{S}$ is high, parallel mode is selected and when P/$\overline{S}$ is low, serial mode is selected. In serial mode, only write operation is allowed.

$\overline{CS1}$, CS2

These pin are chip select inputs. The chip is enabled for data operation only when $\overline{CS1}$ is low and CS2 is high.

C68/$\overline{80}$

This pin is microprocessor interface select input. When the pin is high, 6800 series interface is selected and when the pin is low, 8080 series interface is selected.

D_0-D_7

These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D_7 is the serial data input SDA and D_6 is the serial clock input SCK.

D/$\overline{C}$

This pin is control/display data input control flag. When the pin is high, the data on D_0-D_7 is display data. When the pin is low, the data on D_0-D_7 is control data.

R/$\overline{W}$($\overline{WR}$)

This pin is microprocessor interface signal. When interfacing to an 6800-series microprocessor, the signal indicates read mode when high and write mode when low. When interfacing to an 8080-microprocessor, a data write operation is initiated when R/W(WR) is low and the chip is selected.

$\overline{E}$($\overline{RD}$)

This pin is microprocessor interface signal. When interfacing to an 6800-series microprocessor, a data operation is initiated when $\overline{E}$(RD) is high and the chip is selected. When interfacing to an 8080-microprocessor, a data read operation is initiated when $\overline{E}$(RD) is low and the chip is selected.

V_{DD}

Power supply pin.

V_{SS}

Ground.

V_{SS1}

Reference voltage input for internal DC-DC converter. The voltage of generated VEE equals to the multiple factor (2X, 3X or 4X) times the potential different between this pin, **V_{SS1}**, and **V_{DD}**. All generated voltage is referenced to**V_{DD}**.

Note: voltage at this input pin must less than or equal to **V_{SS}**.

V_{EE}

This is the most negative voltage supply pin of the chip. It can be supplied externally or generated by the internal DC-DC converter.

When using internal DC-DC converter as generator, voltage at this pin is for internal reference only. It CANNOT be used for driving external circuitries.

C_{3N}, C_{1P}, C_{1N}, C_{2P} and C_{2N}

When internal DC-DC voltage converter is used, external capacitor(s) is/are connected among these pins.

V_{L6}

This pin is the most negative LCD driving voltage. It can be supplied externally or generated by the internal regulator.

V_F

This pin is an input of the internal voltage regulator. When internal regulator is used to generate V_{L6}, external resistors are connected between V_{DD} and V_F, and V_F and V_{L6}, respectively (see application circuit).

V_{FS}

This pin is an input to provide an external voltage reference for the internal voltage regulator. It is only enabled in External Input chip options.

IRS

This pin is an input pin to enable the internal resistors network for the voltage regulator when IRS is high. When it is low, the external resistors R1/R2 should be connected to VL6 and VF.

$\overline{HPM}$

This pin is an input pin to enable the high power current mode when it is low. The contrast curves in High Power Mode will be different to Normal Mode. Details of the High Power Mode Contrast curve is TBD.

V_{L2}, V_{L3}, V_{L4} and V_{L5} (Voltages referenced to V_{DD})

LCD driving voltages. They can be supplied externally or generated by the internal smart bias divider. They have the following relationship:

$$V_{DD} > V_{L2} > V_{L3} > V_{L4} > V_{L5} > V_{L6}$$

	1:6 bias	1:8 bias
V_{L2}	1/6*V_{L6}	1/8*V_{L6}
V_{L3}	2/6*V_{L6}	2/8*V_{L6}
V_{L4}	4/6*V_{L6}	6/8*V_{L6}
V_{L5}	5/6*V_{L6}	7/8*V_{L6}

ROW0 - ROW63

These pins provide the row driving signal COM0 - COM53 to the LCD panel. See Table.1 about the COM signal mapping in different multiplex ratio N.

ICONS

This pin is the special icons line.

SEG0 - SEG131

These pins provide the LCD column driving signal. Their voltage level is V_{DD} during sleep mode and standby mode.

OPERATION OF LIQUID CRYSTAL DISPLAY DRIVER

Description of Block Diagram Module

Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the D/C pin. If D/C is high, data is written to Graphic Display Data RAM (GDDRAM). If D/C is low, the input at D_0-D_7 is interpreted as a Command and it will be decoded and written to the corresponding command register.

Reset is of the same function as Power ON Reset (POR). Once RES receives a negative reset pulse of about 1us, all internal circuitry will be back to its initial status. Refer to Command Description section for more information.

MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D_0-D_7), R/W(WR), D/C, E(RD), CS1 and CS2. R/W(WR) input High indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. R/W(WR) input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/C input. The E(RD) input serves as data latch signal (clock) when high provided that CS1 and CS2 are low and high respectively. Refer to Figure 1 of parallel timing characteristics for Parallel Interface Timing Diagram of 6800-series microprocessors.

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 4 below.

MPU Parallel 8080-series interface

The parallel interface consists of 8 bi-directional data pins (D_0-D_7), E(RD), R/W(WR), D/C, CS1 and CS2. E(RD) input serves as data read latch signal (clock) when low provided that CS1 and CS2 are low and high respectively. Whether it is display data or status register read is controlled by D/C. R/W(WR) input serves as data write latch signal(clock) when high provided that CS1 and CS2 are low and high respectively. Whether it is display data or command register write is controlled by D/C. Refer to Figure 2 of parallel timing characteristics for Parallel Interface Timing Diagram of 8080-series microprocessor.

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

MPU Serial interface

The serial interface consists of serial clock SCK, serial data SDA, D/C, CS1 and CS2. SDA is shifted into a 8-bit shift register on every rising edge of SCL in the order of D_7, D_6,... D_0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock.

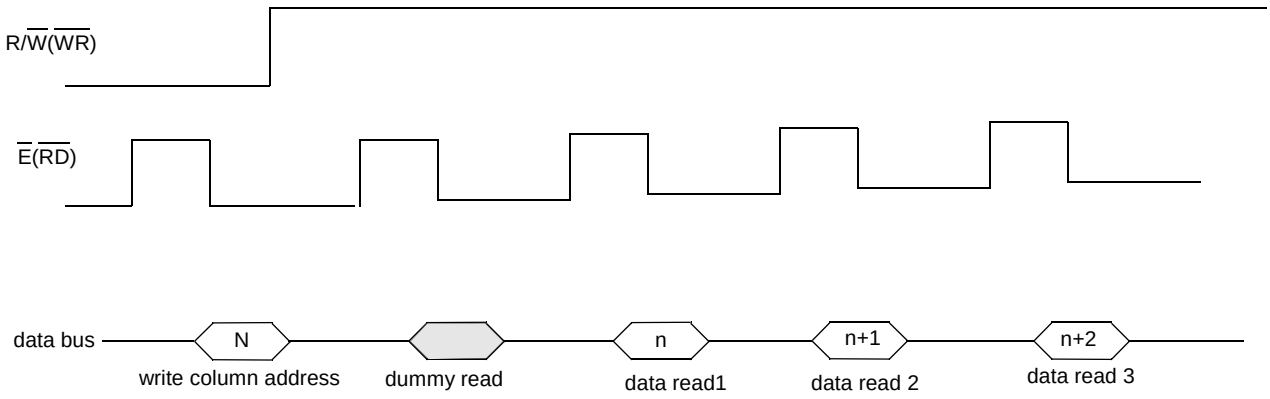
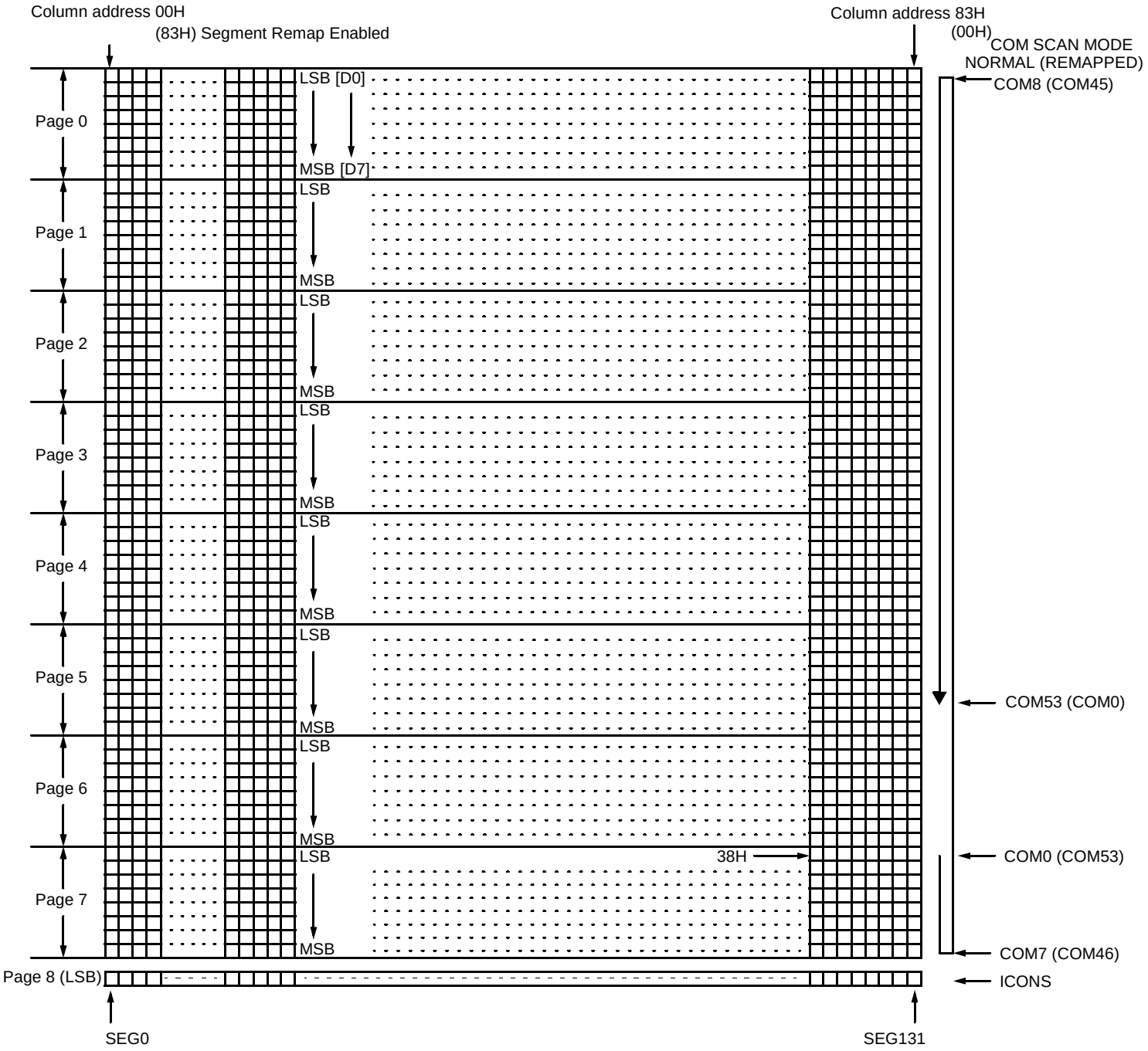


Figure 4: display data read with the insertion of dummy read

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132 x 65= 8580 bits. Figure 5 is a description of the GDDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs are provided. For vertical scrolling of display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display. Figure 5 shows the case in which the display start line register is set at 38H.



Note: The configuration in parentheses represent the non-remapping of Rows and Columns

Figure 5. Graphic Display Data RAM (GDDRAM) Address Map (with display start line value 38H) For 132 X 54 Graphic Display Mode

Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 6). The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

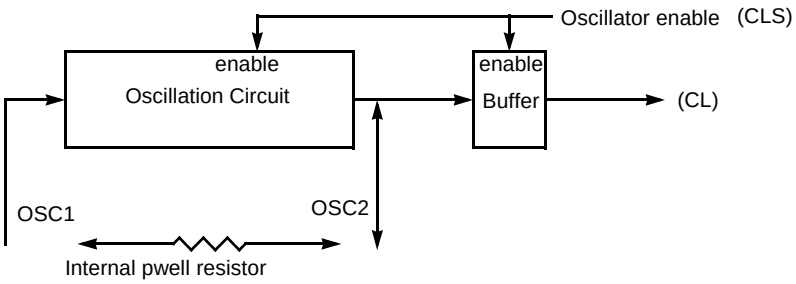


Figure 6. Oscillator Circuitry

LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage needed for display output. It takes a single supply input and generate necessary bias voltages. It consists of:

1. 2X, 3X and 4X DC-DC voltage converter
   Please refer to application notes.

2. Voltage Regulator (Voltages referenced to V_{DD})
   Feedback gain control for initial LCD voltage. External resistors are connected between V_{DD} and V_F, and between V_F and V_{L6}. These resistors are chosen to give the desired V_{L6} according to the following equation:
   $V_{L6} = (1 + R_2/R_1)V_{ref}$
   where Vref is the internally generated reference voltage with a known R_1 and R_2, and V_{ref} can be calculated by a measured V_{L6}. R_1 and R_2 are the resistance values of the resistors between V_{DD} and V_F, and V_F and V_{L6}, respectively.
3. Smart Bias Divider
   Divide the regulator output to give the LCD driving voltages (V_{L2} - V_{L5}). This is a low power consumption circuit which saves most of the display current.
4. Contrast Control (Voltages referenced to V_{DD})
   Software control of 64 voltage levels of LCD voltage.
5. Bias Ratio Selection circuitry
   Software control of 1/6 and 1/8 bias ratio to match the characteristic of LCD panel. In addition, 1/4, 1/5, 1/7 and 1/9 bias ratios are software selectable for any mux application.
6. Self adjust temperature compensation circuitry
   Provide 8 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control. Defaulted temperature coefficient (TC) value is -0.05%/^{o}C.

187 Bit Latch

A register carries the display signal information. In 132 X 55 display mode. Data will be fed to the HV-buffer Cell and level-shifted to the required level.

Level Selector

Level Selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

HV Buffer Cell (Level Shifter)

HV Buffer Cell works as a level shifter which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

Reset Circuit

When $\overline{RES}$ input is low, the chip is initialized with the following status:

1. Display is OFF
2. 132x48 [Not included ICONS line] Display Mode
3. Normal segment and display data column address mapping (SEG0 mapped to address 00H)
4. Read-modify-write mode is OFF
5. Power control register is set at 000B.
6. Shift register data clear in serial interface
7. Bias ratio is set at 1/8
8. Static indicator is OFF
9. Display start line is set at display RAM address 0
10. Column address counter is set at 0
11. Page address is set at 0
12. Normal scan direction of the COM outputs
13. Internal Regulator Resistor Ratio at 4
14. Contrast control register is set at 20H
15. Test mode is OFF
16. Temperature Coefficient is set to PTC0

LCD Panel Driving Waveform

The following is an example of how the Common and Segment drivers may be connected to a LCD panel. The waveforms shown in Figure 7a and 7b illustrate the desired multiplex scheme.

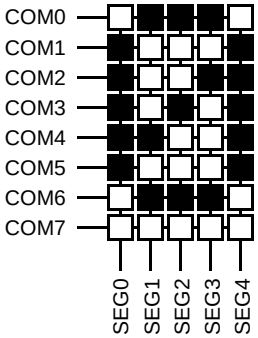
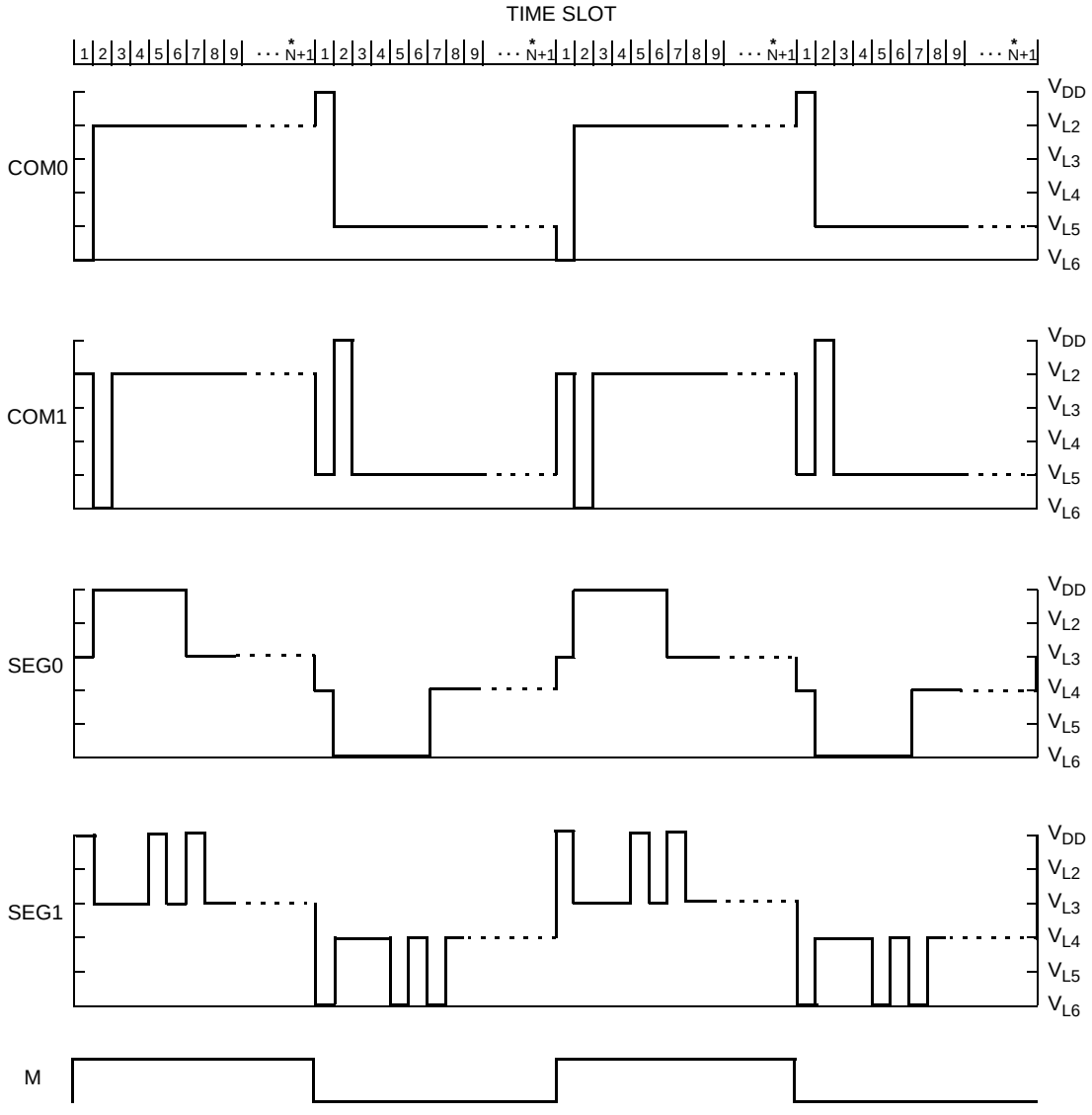


Figure 7a. LCD Display Example "0"



* Note : N is the number of multiplex ratio not included Icon, N is equal to 54 on POR.

Figure 7b. LCD Driving Signal from SSD1812

Command Description

Set Display On/Off

This command alternatively turns the display on and off. When display off is issued with entire display on, power save mode will be entered. See "Set Power Save Mode" for details.

Set Display Start Line

This command is to set **Display Start Line** register to determine starting address of display RAM to be displayed by selecting a value from 0 to 63. With value equals to 0, D0 of Page 0 is mapped to COM0. With value equals to 1, D1 of Page0 is mapped to COM0. The display start line values of 0 to 63 are assigned to Page 0 to 7.

Set Page Address

This command positions the page address to 0 to 8 possible positions in GDDRAM. Refer to figure 5.

Set Higher Column Address

This command specifies the higher nibble of the 8-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU.

Set Lower Column Address

This command specifies the lower nibble of the 8-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU.

Set Segment Re-map

This commands changes the mapping between the display data column address and segment driver. It allows flexibility in layout during LCD module assembly. Refer to figure 5.

Set Normal/Reverse Display

This command sets the display to be either normal/reverse. In normal display, a RAM data of 1 indicates an "ON" pixel while in reverse display, a RAM data of 0 indicates an "ON" pixel. In icon mode, the icon line is not reversed by this command.

Set Entire Display On/Off

This command forces the entire display, including the icon row, to be "ON" regardless of the contents of the display data RAM. This command has priority over normal/reverse display. This command will be used with "Set Display Display ON/OFF" command to form a compound command for entering power save mode. See "Set Power Save Mode".

Set LCD Bias

This command selects a suitable bias ratio (1/6 or 1/8) required for driving the particular LCD panel in use. The POR default for SSD1812 is set to 1/8 bias. For setting 1/4, 1/5, 1/7 and 1/9 bias, an extended compound command should be used.

Set Read-Modify-Write Mode

This command puts the chip in read-modify-write mode in which:

1. the column address is saved before entering the mode
2. the column address is incremented by display data write but not by display data read

Set End of Read-Modify-Write Mode

This command relieves the chip from read-modify-write mode. The column address that is saved before entering read-modify-write mode will be restored.

Software Reset

This command causes some of the internal status of the chip to be initialized:

1. Display is OFF
3. Normal segment and display data column address mapping (SEG0 mapped to address 00H)
4. Read-modify-write mode is OFF
5. Power control register is set at 0
6. Bias ratio is set at 1/8
7. Static indicator is OFF
8. Display start line is set at display RAM address 0
9. Column address counter is set at 0
10. Page address is set at 0
11. Normal scan direction of the COM outputs
12. Internal Regulator Resistor Ratio at 4
13. Contrast control register is set at 20H
14. Test mode is OFF

Set COM Output Scan Direction

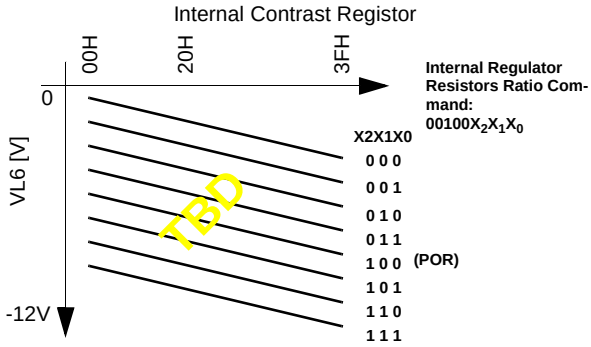
This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly.

Set Power Control Register

This command turns on/off the various power circuits associated with the chip.

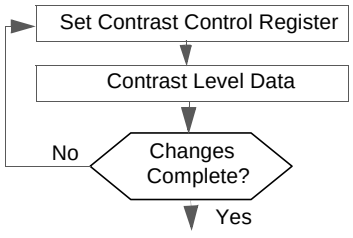
Set Internal Regulator Resistors Ratio

This command is to enable any one of the eight internal resistor sets for different regulator gain when using internal regulator resistor network (IRS pin pulled high). The relationship between the VL6 and the 64 levels of contrast step is TBD.



Set Contrast Control Register

This commands adjusts the contrast of the LCD panel by changing V_{L6} of the LCD drive voltage provided by the On-Chip power circuits. V_{L6} is set with 64 steps (6-bit) contrast control register. It is a compound commands:



Set Indicator On/Off

This command turns on and off the static drive indicators. It also controls whether standby mode or sleep mode will be entered after the power save compound command. See “Set Power Save Mode”.

When the “Set Indicator On” command is sent, the “Indicator Display Mode” must be followed in the next command. The “Set Indicator Off” command is a single byte command and no following command is required.

Set Power Save Mode

To enter Standby or Sleep Mode, it should be done by using a compound command composed of “Set Display ON/OFF” and “Set Entire Display ON/OFF” commands. When “Set Entire Display ON” is issued during display is OFF, either Standby Mode or Sleep Mode will be entered.

The status of the Static Indicator will determine which power save mode is entered. If static indicator is off, the Sleep Mode will be entered:

1. Internal oscillator and LCD power supply circuits are stopped
2. Segment and Common drivers output V_{DD} level
3. The display data and operation mode before sleep are held
4. Internal display RAM can still be accessed

If the static indicator is on, the chip enters Standby Mode which is similar to sleep mode except:

1. the internal oscillator is on
2. the static drive system is on

Note also that if the software reset command is issued during Standby Mode, Sleep Mode will be entered. Both power save modes can be exited by the issue of a new software command or by pulling Low at hardware pin $\overline{RES}$.

NOP

No Operation Command

Set Test Mode

This command force the driver chip into its test mode for internal testing of the chip. Under normal operation, user should NOT use this command.

Status register Read

This command is issued by setting D/$\overline{C}$ Low during a data read (refer to figure 1 and 2 parallel interface waveform). It allows the MCU to monitor the internal status of the chip. No status read is provided for serial mode.

EXTENDED COMMANDS

These commands are used, in addition to basic commands, to trigger the enhanced features, on top of general ones, designed for the chip.

Set Multiplex Ratio

This command switches default 54 multiplex mode to any multiplex mode from 1 to 54. The chip pads ROW0-ROW63 will be switched to corresponding COM signal output, see Table 1.

Set RAM Page Blinking Freq.

This command sets the blinking frequency of blinking page(s) which is set using the “Set RAM Page Blinking” extended command.

Set Bias Ratio

Except the 1/4 bias, all the available bias ratio (1/5, 1/6, 1/7, 1/8, 1/9) could be set using this command. When changing the display multiplex ratio, the bias ratio also need to be adjusted to make display contrast consistent.

Set Temperature Coefficient (TC) Value

This command is to set 1 out of 8 different temperature coefficients in order to match various liquid crystal temperature grades.

Set 1/4 Bias Ratio

This command sets the bias ratio directly to 1/4 bias. This ratio is especially for use in under 12mux display.

In order to restore to other bias ratio, this command must be executed, with LSB=0, before the “Set Multiplex ratio” or “Set LCD Bias” command is sent.

Set Display Offset

This command should be sent ONLY when the multiplex ratio is set less than 54.

When the mulitplex ratio less than 54 is set, the display will be mapped in the middle (y-direction) of the LCD, see Table 1. Use this command could move the display vertically within the 54 commons.

To make the Reduced-Mux Com 0 (Com 0 after reducing the multiplex ratio) towards the Row 0 direction for L lines, the 6-bit data in second command should be given by L.

To move in the other direction by L lines, the 6-bit data should be given by 64-L.

Please note that the display is confined within the un-reduced 54 mux. That is maximum value of L is given by the half of 54 minus the reduced-multiplex ratio. For an odd display mux after reduction, moving away from Row 0 direction will has 1 more step.

Set Smart Icon Mode

This command is used to enter/leave the Smart Icon Mode.

In Smart Icon Mode, Entire display will be turned off except the Icon row.

Set RAM Page Blinking

This command enable the whole page to blink in the frequency set by “Set RAM Page Blinking Freq.” command.

Setting either bit(s) in the data given in the second command will force cooresponding page to blink. LSB of the data points to Page 0 and so on to MSB for Page 7.

COMMAND TABLE

Bit Pattern	Write Command (D/$\overline{C}$=0, R/$\overline{W}$($\overline{WR}$)=0, $\overline{E}$($\overline{RD}$)=1)	Comment
1010111X_0	Set Display On/Off	X_0=0: turns off LCD panel (POR) X_0=1: turns on LCD panel
01$X_5X_4X_3X_2X_1X_0$	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_4X_3X_2X_1X_0$. Display start line register is reset to 000000 during POR.
1011$X_3X_2X_1X_0$	Set Page Address	Set GDDRAM Page Address (0-8) using $X_3X_2X_1X_0$
0001$X_3X_2X_1X_0$	Set Higher Column Address	Set the higher nibble of the colume address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000 during POR.
0000$X_3X_2X_1X_0$	Set Lower Column Address	Set the lower nibble of the colume address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000 during POR.
1010000X_0	Set Segment Re-map	X_0=0: column address 00H is mapped to SEG0 (POR) X_0=1: column address 83H is mapped to SEG0 Refer to Fig. 5 for details.
1010011X_0	Set Normal/Reverse Display	X_0=0: normal display (POR) X_0=1: reverse display
1010010X_0	Set Entire Display On/Off	X_0=0: normal display (POR) X_0=1: entire display on
1010001X_0	Set LCD Bias	X_0=0: 1/8 bias (POR) X_0=1: 1/6 bias For setting bias ratio to 1/4, 1/5, 1/7 or 1/9, see Extended Command Table.
11100000	Set Read-Modify-Write Mode	Read-modify-write mode will be entered in which the column address will not be incremented during display data read
11101110	Set End of Read-Modify-Write Mode	Exit Read-modify-write mode. Column address before entering the mode will be restored
11100010	Software Reset	Initialize the internal status
1100X_3 * * *	Set COM Output Scan Direction	X_3=0: normal mode (POR) X_3=1: remapped mode. COM0 to COM[N-1] becomes COM[N-1] to COM0 in Multiplex ratio is equal to N. See Fig.5 as an example for N equal to 54.
00101$X_2X_1X_0$	Set Power Control Register	X_0=0: turns off the output op-amp buffer (POR) X_0=1: turns on the output op-amp buffer X_1=0: turns off the internal regulator (POR) X_1=1: turns on the internal regulator X_2=0: turns off the internal voltage booster (POR) X_2=1: turns on the internal voltage booster
00100$X_2X_1X_0$	Set Internal Regulator Resistor Ratio	Internal regulator gain increases as $X_2X_1X_0$ increased from 000b to 111b. $X_2X_1X_0$ = 100b (POR)
10000001 * * $X_5X_4X_3X_2X_1X_0$	Set Contrast Control Register	Set Contrast level from 64 contrast steps. Contrast increases as $X_5X_4X_3X_2X_1X_0$ is increased. $X_5X_4X_3X_2X_1X_0$ = 100000b (POR)
1010110X_0 * * * * * * X_1X_0	Set Indicator On/Off Indicator Display Mode, This second byte command is required ONLY when “Set Indicator On” command is sent.	X_0 = 0: indicator off (POR, no need of second command byte) X_0 = 1: indicator on (second command byte required) X_1X_0 = 00: indicator off X_1X_0 = 01: indicator on and blinking at ~1 second interval X_1X_0 = 10: indicator on and blinking at ~1/2 second interval X_1X_0 = 11: indicator on constantly
* * * * * * * *	Set Power Save Mode	Standby or sleep mode will be entered with compound commands
11100011	NOP	Command for No Operation
1111 * * * *	Set Test Mode	Reserved for IC testing. Do NOT use.
11110000	Test Mode Reset	Reserved for IC testing. Do NOT use.

Bit Pattern	Read Command (D/$\overline{C}$=0, R/$\overline{W}$($\overline{WR}$)=1, $\overline{E}$($\overline{RD}$)=0)	Comment
$D_7D_6D_5D_4D_3D_2D_1D_0$ (Data Read Back from the driver)	Status Register Read	D_7=0: indicates an internal operation is completed. D_7=1: indicates an internal operation is in progress. D_6=0: indicates normal segment mapping with column address D_6=1: indicates reverse segment mapping with column address D_5=0: indicates the display is ON D_5=1: indicates the display is OFF D_4=0: initialization is not in progress D_4=1: initialization is in progress after $\overline{RES}$ or software reset $D_3D_2D_1D_0$ = 1010, these 4-bit is fixed to 1010 which could be used to identify as Solomon Systech Device.

Data Read / Write

To read data from the GDDRAM, input High to R/$\overline{W}$($\overline{WR}$) pin and D/$\overline{C}$ pin for 6800-series parallel mode, Low to $\overline{E}$($\overline{RD}$) pin and High to D/$\overline{C}$ pin for 8080-series parallel mode. No data read is provided for serial mode. In normal mode, GDDRAM column address pointer will be increased by one automatically after each data read. However, no automatic increase will be performed in read-modify-write mode. Also, a dummy read is required before the first data read. See Figure 4 in Functional Description.

To write data to the GDDRAM, input Low to R/W(WR) pin and High to D/C pin for 6800-series parallel mode. For serial interface, it will always be in write mode. GDDRAM column address pointer will be increased by one automatically after each data write.

Address Increment Table (Automatic)

D/$\overline{C}$	R/$\overline{W}$($\overline{WR}$)	Comment	Address Increment	Remarks
0	0	Write Command	No	
0	1	Read Status	No	
1	0	Write Data	Yes	
1	1	Read Data	Yes	*1

Address Increment is done automatically after data read write. The column address pointer of GDDRAM*2 is affected.

Remarks: *1. If read data is issued in read-modify-write mode, address increase is not applied.

*2. Column Address will NOT wrap round when overflow.

Commands Required for R/$\overline{W}$($\overline{WR}$) Actions on RAM

R/$\overline{W}$($\overline{WR}$) Actions on RAMs	Commands Required	
Read/Write Data from/to GDDRAM.	Set GDDRAM Page Address	(1011$X_3X_2X_1X_0$)*
	Set GDDRAM Column Address	(0001$X_3X_2X_1X_0$)*
		(0000$X_3X_2X_1X_0$)
	Read/Write Data	($X_7X_6X_5X_4X_3X_2X_1X_0$)
Save/Restore GDDRAM Column Address.	Save GDDRAM Column Address by read-modify-write mode	(11100000)
	Restore GDDRAM Column Address by end of read-modify-write mode	(11101110)

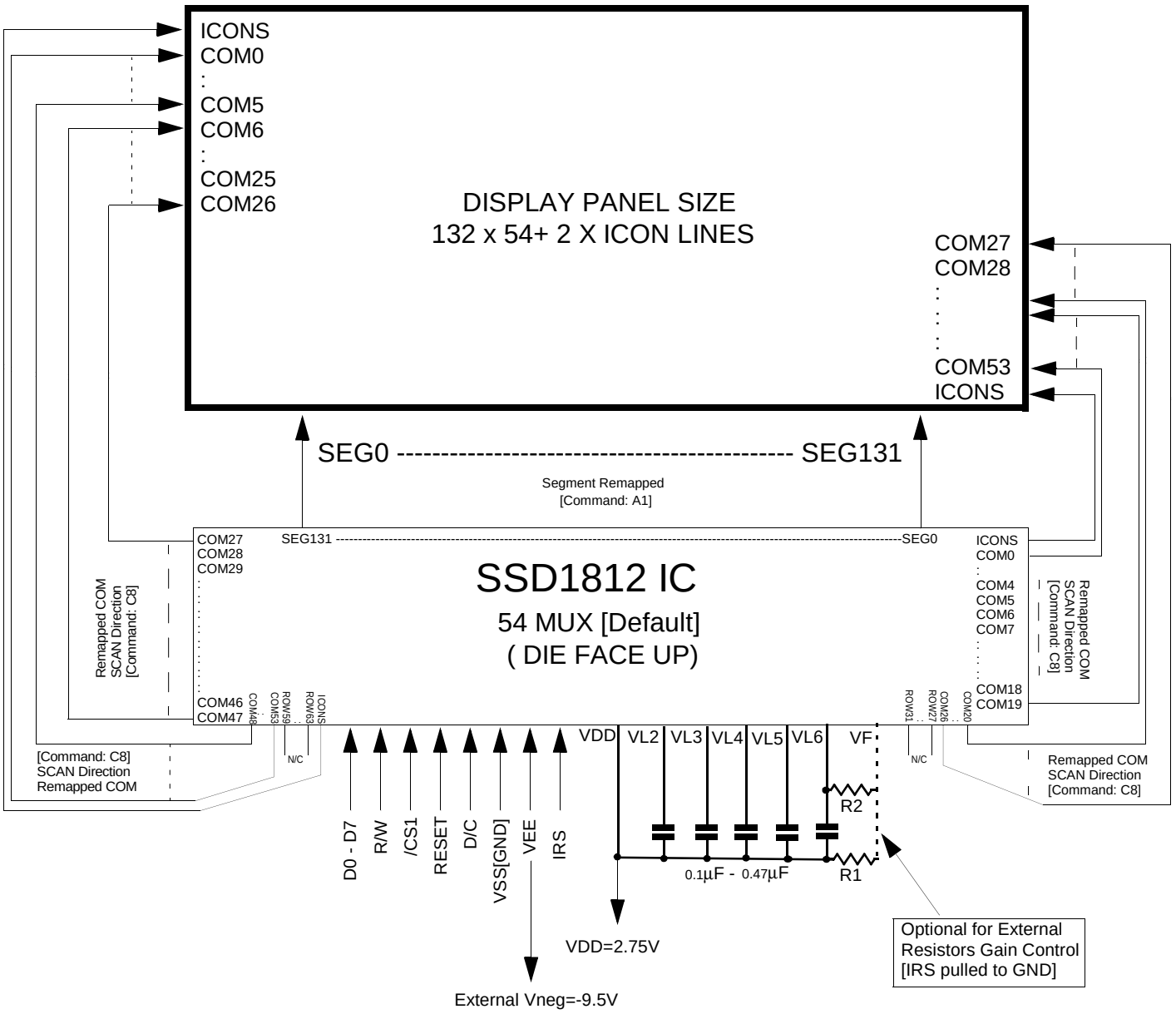
* No need to resend the command again if it is set previously.

The read / write action to the Display Data RAM does not depend on the display mode. This means the user can change the RAM content whether the target RAM content is being displayed or not.

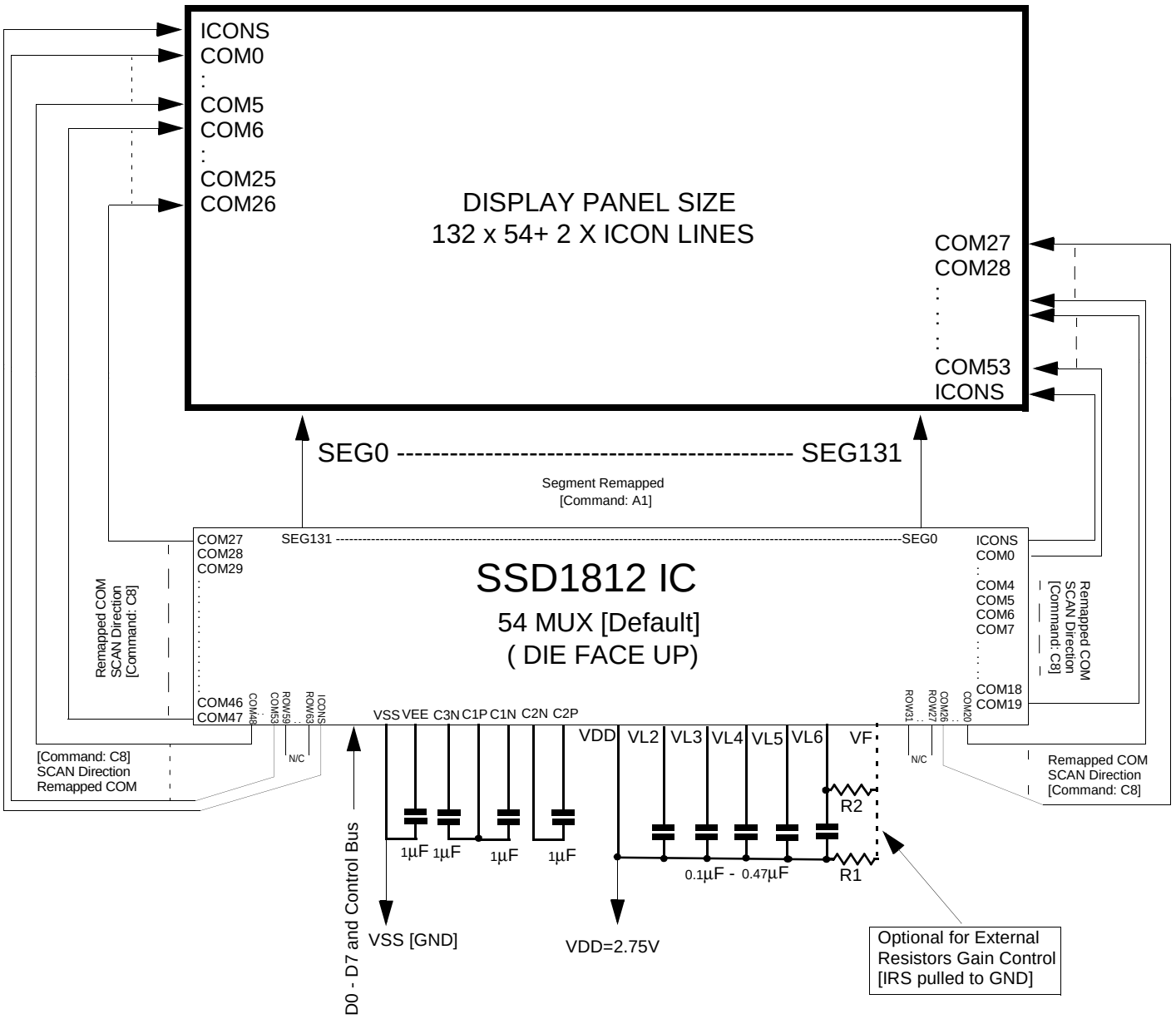
EXTENDED COMMAND TABLE

Bit Pattern	Command	Comment
10101000 $X_7X_6X_5X_4X_3X_2X_1X_0$	$X_5X_4X_3X_2X_1X_0$: Set Multiplex Ratio	To select multiplex ratio N from 2 to 55 [Included Icon Line]. N = $X_5X_4X_3X_2X_1X_0$ + 2, eg. N = 110101b + 2 = 55 (POR)
	X_7X_6 : Set RAM Page Blinking Freq.	X_7X_6 = 00: 1.00sec (POR) X_7X_6 = 01: 0.50sec X_7X_6 = 10: 0.25sec X_7X_6 = 11: always off
10101001 $010X_4X_3X_2X_1X_0$	X_1X_0 : Set Bias Ratio	X_1X_0 = 00: 1/8, 1/6 (POR) X_1X_0 = 01: 1/6, 1/5 X_1X_0 = 10: 1/9, 1/7 X_1X_0 = 11: Prohibited
	$X_4X_3X_2$: Set TC Value	$X_4X_3X_2$ = 000: -0.01%/C (POR) $X_4X_3X_2$ = 001: Reserved $X_4X_3X_2$ = 010: -0.10%/C $X_4X_3X_2$ = 011: Reserved $X_4X_3X_2$ = 100: -0.18%/C $X_4X_3X_2$ = 101: Reserved $X_4X_3X_2$ = 110: Reserved $X_4X_3X_2$ = 111: -0.25%/C
$1010101X_0$	X_0: Set 1/4 Bias Ratio	X_0 = 0: use original setting (POR) X_0 = 1: fixed 1/4 bias
11010010 $X_7X_6X_5X_4X_3X_2X_1X_0$	Set Test Mode	Reserved for IC testing. Do NOT use.
11010011 $00X_5X_4X_3X_2X_1X_0$	$X_5X_4X_3X_2X_1X_0$: Set Display Offset (for mux ratio has been set less than 54 only)	After POR, $X_5X_4X_3X_2X_1X_0$ = 0 After setting mux ratio less than 54, data will be displayed at Center of matrix. See Table 1. To move display towards Row 0 by L, $X_5X_4X_3X_2X_1X_0$ = L To move display away from Row 0 by L, $X_5X_4X_3X_2X_1X_0$ = 64-L Note: max. value of L = (54 - display mux)/2
$1101000X_0$	X_0: Set Smart Icon Mode	X_0 = 0: Normal display mode (POR) X_0 = 1: Smart Icon Mode
11010100 $X_7X_6X_5X_4X_3X_2X_1X_0$	Set Test Mode	Reserved for IC testing. Do NOT use.
11010101 $X_7X_6X_5X_4X_3X_2X_1X_0$	Set RAM Page Blinking	After POR, $X_7X_6X_5X_4X_3X_2X_1X_0$ = 00h Set either bit to “1” will set cooresponding page (0-7) to blink.

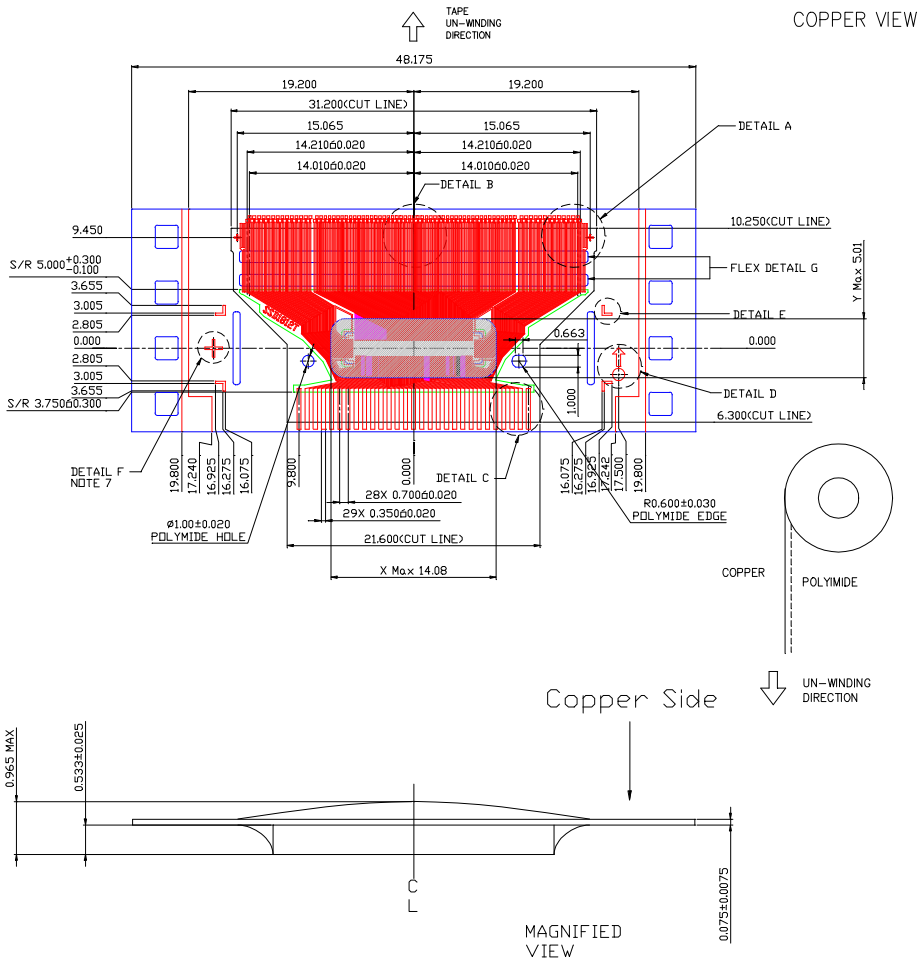
Application Circuit: External VEE with internal regulator and divider mode [Command: 2B] in 54 Mux.



Application Circuit: ALL internal power mode [Command: 2F] in 54 Mux [Default].

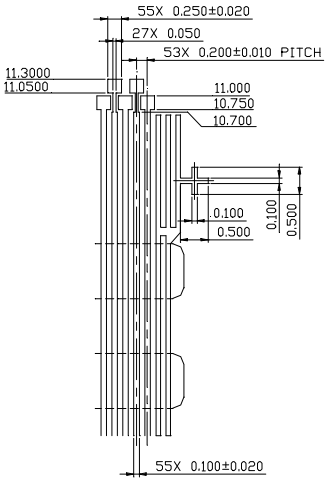


PACKAGE DIMENSIONS
SSD1812T
TAB PACKAGE DIMENSION - 1
(DO NOT SCALE THIS DRAWING)

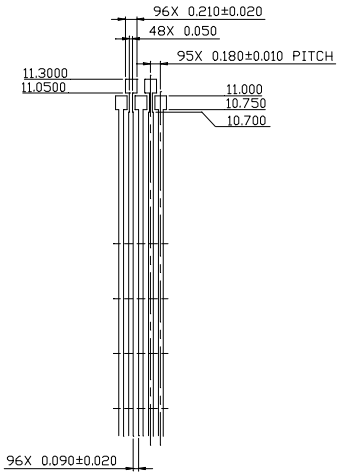


NOTES FOR ALL PAGES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. IF NOT SPECIFIED, SIZE IN MILLIMETER
3. UNSPECIFIED DIMENSION TOLERANCE IS ±0.05
4. BASE MATERIAL: 75 MICRON UPILEX-S
5. COPPER TYPE: 3/4 OZ COPPER (THICKNESS TYP. 25 MICROMETER, MIN 18 MICROMETER)
6. 4 SPROCKET HOLES DEVICE
7. OPTIONAL FEATURE FOR SSL INTERNAL USE ONLY WHICH MAY BE REPLACED BY ø2.0 MM HOLE.

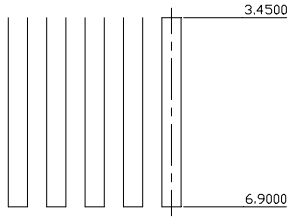
PACKAGE DIMENSIONS
SSD1812T
TAB PACKAGE DIMENSION - 2
(DO NOT SCALE THIS DRAWING)



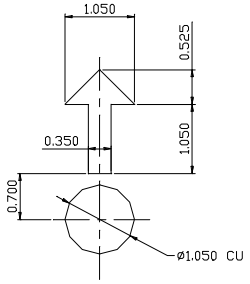
DETAIL A



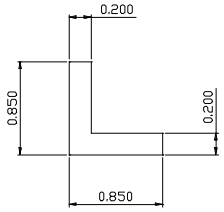
DETAIL B



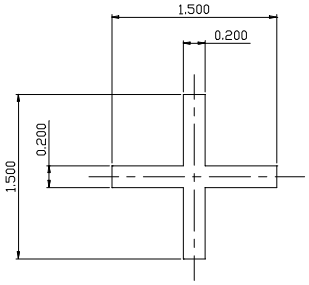
DETAIL C



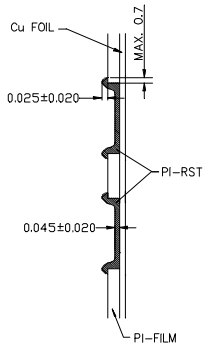
DETAIL D



DETAIL E



DETAIL F



FLEX MATERIAL DETAIL G

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