HMC561

GaAs MMIC x2 ACTIVE FREQUENCY MULTIPLIER, 8 - 21 GHz OUTPUT

Typical Applications

The HMC561 is suitable for:

- Clock Generation Applications: SONET OC-192 & SDH STM-64
- Point-to-Point & VSAT Radios
- Test Instrumentation
- Military & Space

Features

High Output Power: +17 dBm

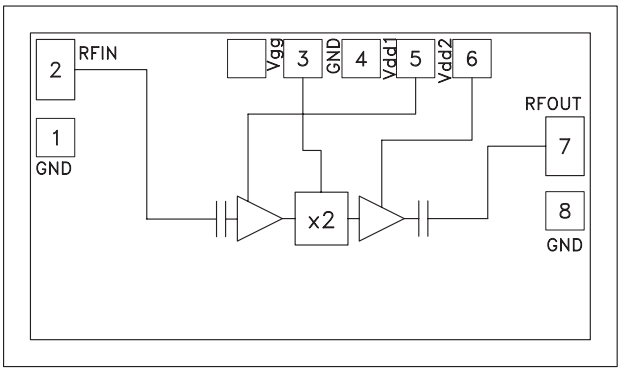
Low Input Power Drive: 0 to +6 dBm

Fo Isolation: 15 dBc @ Fout= 16 GHz

100 KHz SSB Phase Noise: -139 dBc/Hz

Die Size: 1.6 x 0.9 x 0.1 mm

Functional Diagram



General Description

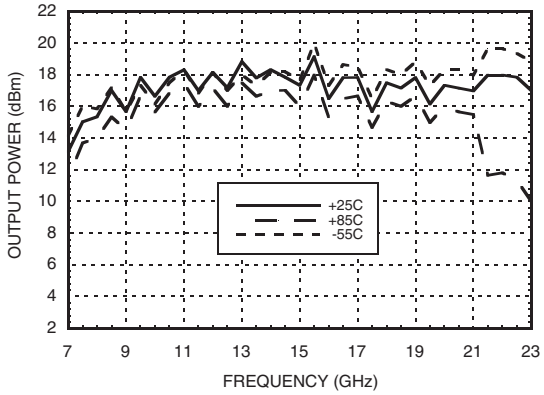
The HMC561 is a x2 active broadband frequency multiplier chip utilizing GaAs PHEMT technology. When driven by a +5 dBm signal, the multiplier provides +17 dBm typical output power from 8 to 21 GHz and the Fo and 3Fo isolations are 15 dBc at 16 GHz. The HMC561 is ideal for use in LO multiplier chains for Pt to Pt & VSAT Radios yielding reduced parts count vs. traditional approaches. The low additive SSB Phase Noise of -139 dBc/Hz at 100 kHz offset helps maintain good system noise performance.

Electrical Specifications, T_A = +25°C, Vdd1= Vdd2= +5V, 5 dBm Drive Level

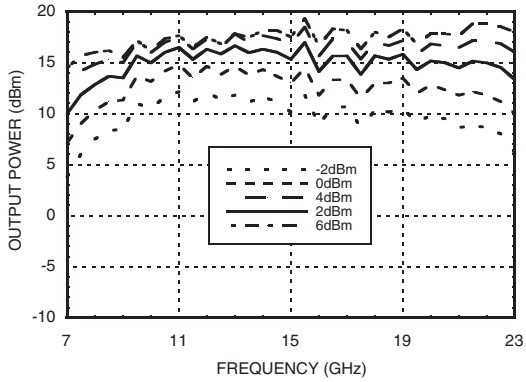
Parameter	Min.	Typ.	Max.	Units
Frequency Range, Input		4 - 10.5		GHz
Frequency Range, Output		8 - 21		GHz
Output Power	14	17		dBm
Fo Isolation (with respect to output level)		15		dBc
3Fo Isolation (with respect to output level)		15		dBc
4Fo Isolation (with respect to output level)		15		dBc
Input Return Loss		15		dB
Output Return Loss		12		dB
SSB Phase Noise (100 kHz Offset)		-139		dBc/Hz
Supply Current (Idd) (Vdd1= Vdd2= +5V, Vgg = -1.7V Typ.)		98	126	mA

Adjust Vgg between -2.0 and -1.2V to achieve Idd1 + Idd2 = 98 mA

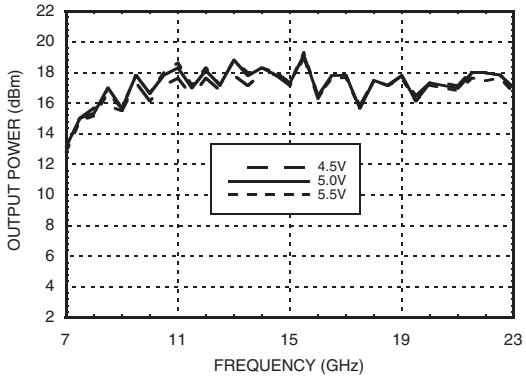
Output Power vs. Temperature @ 5 dBm Drive Level



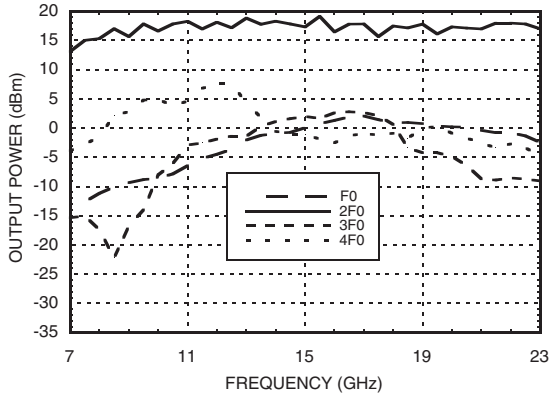
Output Power vs. Drive Level



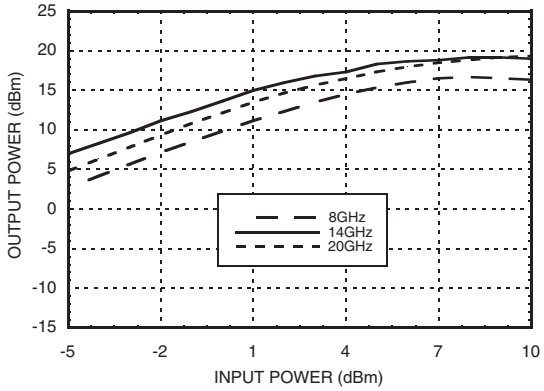
Output Power vs. Supply Voltage @ 5 dBm Drive Level



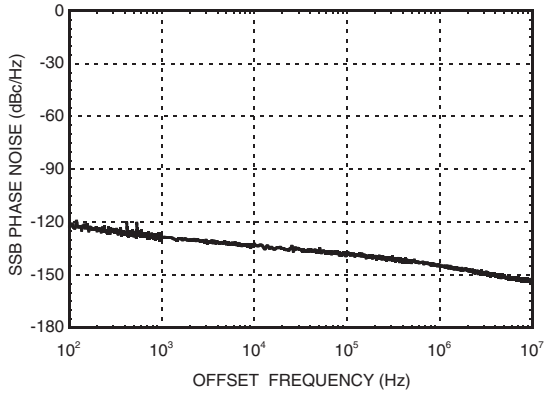
Isolation @ 5 dBm Drive Level



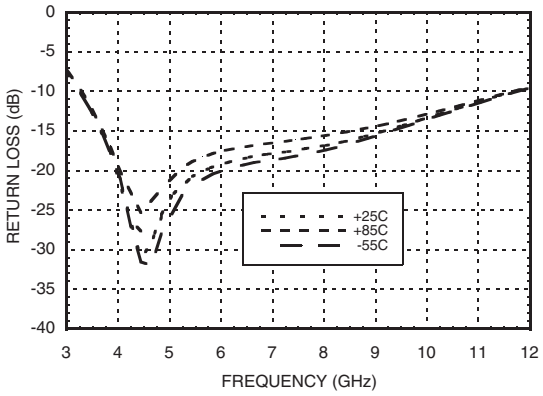
Output Power vs. Input Power



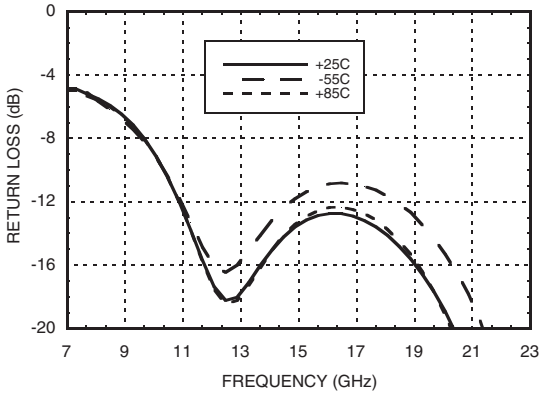
SSB Phase Noise Performance, Fout= 16 GHz, Input Power = +3 dBm



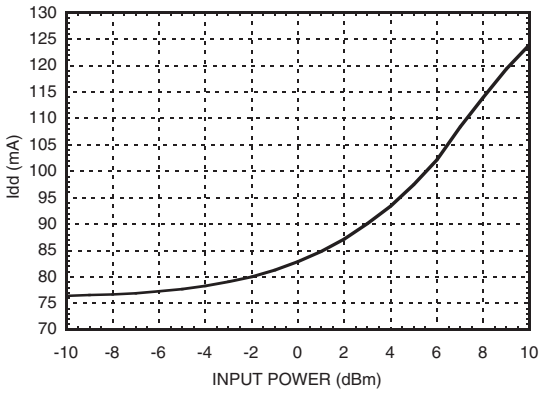
Input Return Loss vs. Temperature



Output Return Loss vs. Temperature



Supply Current vs. Input Power



Absolute Maximum Ratings

RF Input (Vdd1= Vdd2= +5V)	+10 dBm
Supply Voltage (Vdd1, Vdd2)	+5.5 Vdc
Channel Temperature	175 °C
Continuous Pdiss (T= 85 °C) (derate 10.4 mW/°C above 85 °C)	940 mW
Thermal Resistance (channel to ground paddle)	95.9 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

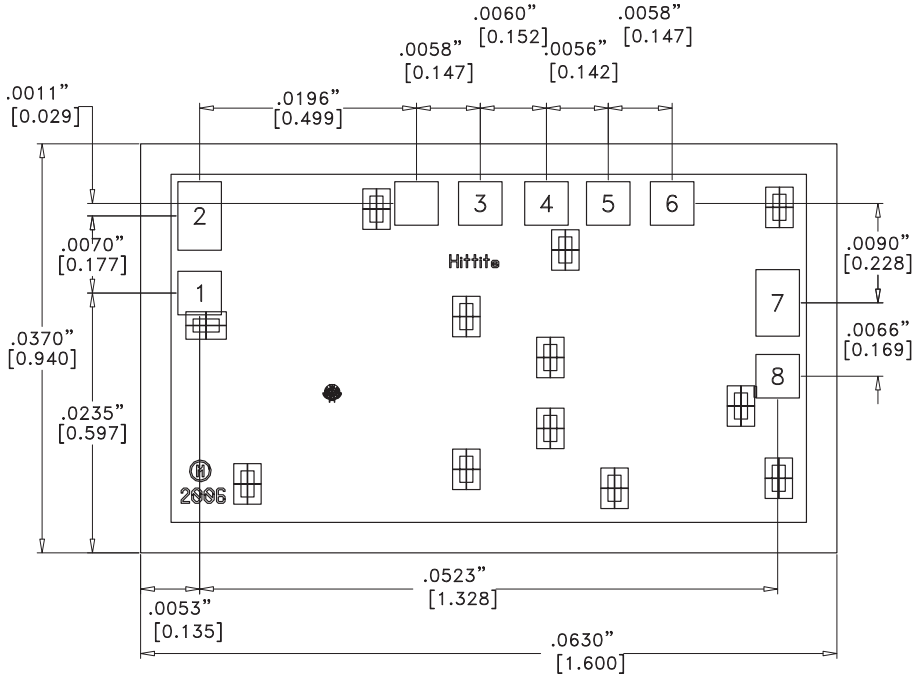
Typical Supply Current vs. Vdd1, Vdd2

Vdd1, Vdd2 (Vdc)	Idd1 + Idd2 (mA)
4.5	97
5.0	98
5.5	99

Note:
Multiplier will operate over full voltage range shown above.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



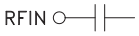
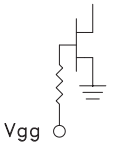
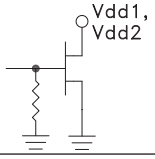
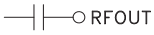
Die Packaging Information [1]

Standard	Alternate [2]
GP-2 (Gel Pack)	—

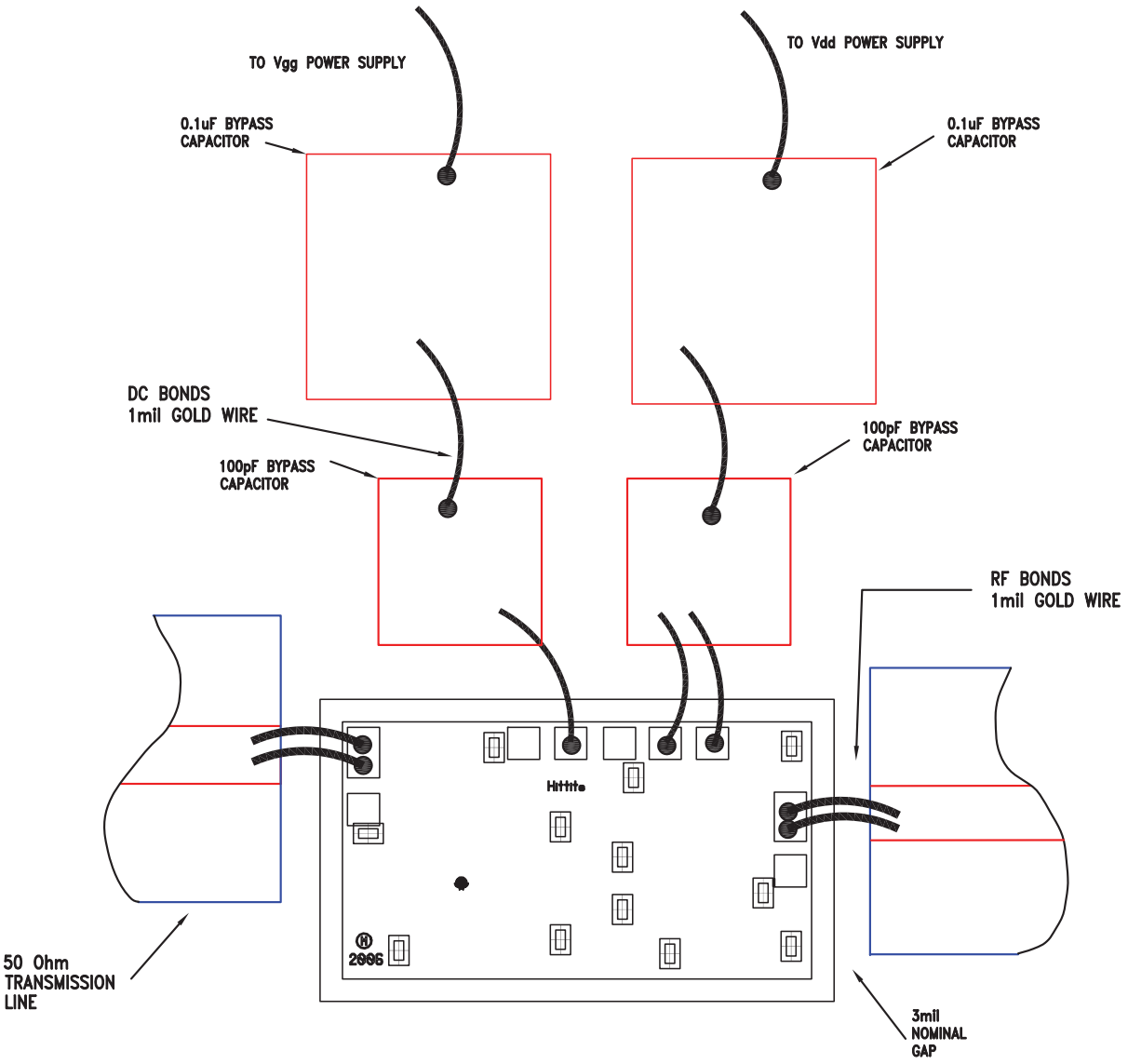
[1] Refer to the "Packaging Information" section for die packaging dimensions.
[2] Reference this suffix only when ordering alternate die packaging.

NOTES:
1. ALL DIMENSIONS ARE IN INCHES [MILLIMETERS].
2. DIE THICKNESS IS .004"
3. TYPICAL BOND PAD IS .004" SQUARE.
4. TYPICAL BOND SPACING IS .006" CENTER TO CENTER.
5. BOND PAD METALIZATION: GOLD
6. BACKSIDE METALIZATION: GOLD
7. BACKSIDE METAL IS GROUND.
8. NO CONNECTION REQUIRED FOR UNLABELED BOND PADS.

Pin Description

Pin Number	Function	Description	Interface Schematic
1, 4, 8	GND	Die bottom must be connected to RF ground.	
2	RFIN	Pin is AC coupled and matched to 50 Ohms.	
3	Vgg	Gate control for multiplier. Adjust to achieve Idd of 98 mA. Please follow "MMIC Amplifier Biasing Procedure" Application note.	
5, 6	Vdd1, Vdd2	Supply voltage 5V ± 0.5V.	
7	RFOUT	Pin is AC coupled and matched to 50 Ohms.	

Assembly Diagram



Mounting & Bonding Techniques for Millimeterwave GaAs MMICs

The die should be attached directly to the ground plane eutectically or with conductive epoxy (see HMC general Handling, Mounting, Bonding Note).

50 Ohm Microstrip transmission lines on 0.127mm (5 mil) thick alumina thin film substrates are recommended for bringing RF to and from the chip (Figure 1). If 0.254mm (10 mil) thick alumina thin film substrates must be used, the die should be raised 0.150mm (6 mils) so that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.102mm (4 mil) thick die to a 0.150mm (6 mil) thick molybdenum heat spreader (moly-tab) which is then attached to the ground plane (Figure 2).

Microstrip substrates should be brought as close to the die as possible in order to minimize ribbon bond length. Typical die-to-substrate spacing is 0.076mm (3 mils). Gold ribbon of 0.075 mm (3 mil) width and minimal length <0.31 mm (<12 mils) is recommended to minimize inductance on RF, LO & IF ports.

An RF bypass capacitor should be used on the Vdd input. A 100 pF single layer capacitor (mounted eutectically or by conductive epoxy) placed no further than 0.762mm (30 Mils) from the chip is recommended.

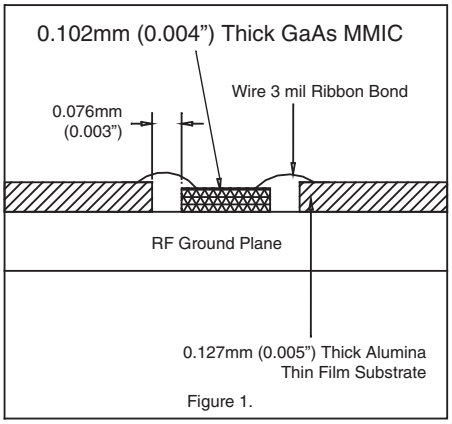


Figure 1.

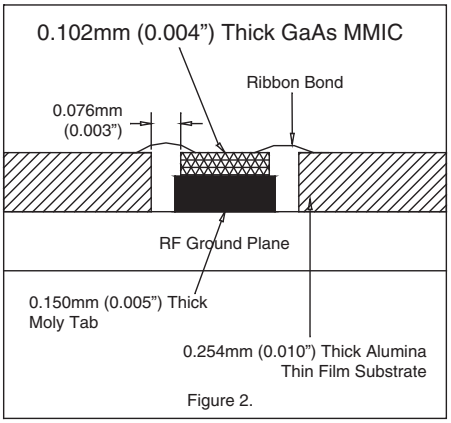


Figure 2.

Handling Precautions

Follow these precautions to avoid permanent damage.

Storage: All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

Storage: All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

Static Sensitivity: Follow ESD precautions to protect against > ± 250V ESD strikes.

Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip may have fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. The mounting surface should be clean and flat.

Eutectic Die Attach: A 80/20 gold tin preform is recommended with a work surface temperature of 255 deg. C and a tool temperature of 265 deg. C. When hot 90/10 nitrogen/hydrogen gas is applied, tool tip temperature should be 290 deg. C. DO NOT expose the chip to a temperature greater than 320 deg. C for more than 20 seconds. No more than 3 seconds of scrubbing should be required for attachment.

Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.

Wire Bonding

Ball or wedge bond with 0.025mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 deg. C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31mm (12 mils).