MA31751

Memory Management & Block Protection Unit

Replaces June 1999 version, DS4083-2.0

DS4083-3.0 January 2000

The MA31751 Memory Management Unit/Block Protect Unit (MMU/BPU) is an optional chip which may be used to expand the capabilities of the MA31750.

User configurable, the MA31751 can perform as an MMU, a BPU or both MMU and BPU, conforming to MIL-STD-1750A and 1750B. MMU mapping and BPU protection for 1M words of memory is provided by the internal memory. Up to 16 MA31751 devices can be used to give 16M words of logical mapped onto 8M words of physical address space with protection in 1750B mode.

The MA31751 is designed to have a simple interface to both the CPU and the system bus with the minimal number of control lines. This reduces board space and simplifies system design.

The MA31751 traps the MMU and BPU XIO commands to program and read the logical to physical mapping and memory access control. This provides simple memory management as defined by the MIL-STD-1750.

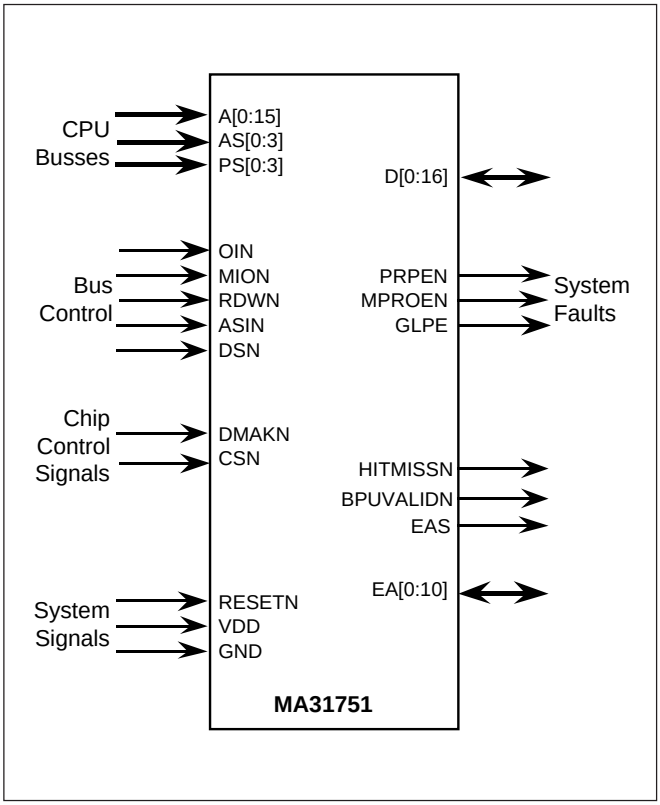


Figure 1: Chip Control Signals

FEATURES

- MIL-STD-1750A/B Compatible
- Radiation Hard CMOS/SOS Technology
- User Configurable as Either a Memory Management Unit (MMU) or a Block Protect Unit (BPU) or Both
- Memory Management Unit Configuration
  - 1 MWord Physical Address Space
  - Access Lock and Key of 4K-Word Blocks
  - Write/Execute Protection of 4K-Word Blocks
- Block Protect Unit Configuration
  - Protection of 1K-Word Blocks
  - Global Memory Write Protection During Initialisation
- Direct Memory Access Support

1.0 DEVICE OPERATION

The MA31751 is an interface device designed to increase the memory addressing capability of the MA31750 CPU. It is user configurable as an MMU and/or a BPU conforming to the MIL-STD-1750A and the proposed MIL-STD-1750B. The MMU provides expanded addressing and full access lock/key protection in both modes, together with write/execute protection on 4K pages.

The BPU allows up to 1M words of memory to be protected in 1K blocks (MIL-STD-1750A). Up to 8M words may be protected by multiple MMU/BPU units (draft MIL-STD-1750B).

In 1750A mode, one MA31751 unit can act as both MMU and BPU for the maximum 1M words of address space. In 1750B mode, up to 8 MA31751 units may be used to provide the maximum BPU functions and up to 16 units for the maximum MMU functions. For any given physical memory location the MMU and BPU function may be split across two MA31751 devices depending on the logical to physical address mapping.

1.1 INITIALISATION

The MA31751 is initialised by the CPU when a system reset occurs. Initially all mappings are set one to one to give a linear 1M word logical to physical mapping. The BPU defaults to no protection on a reset and requires 256 machine cycles (AS pulsing) to set the internal BPU memory. The CPU recognises the presence of the MMU/BPU by the setting of appropriate bits in the configuration register. When the configuration register is read, the MA31751 stores MMU, BPU, parity and 1750 mode information internally. The CPU may change the mapping and access protection when it is in privileged instruction mode using XIO commands 4D00 to 52FF as defined in MIL-STD-1750.

1.2 ADDRESS TRANSLATION AND PROTECTION

The MMU maps system memory into 4K word pages by the mechanism shown in figure 3. A page is a block of physical memory which is uniquely specified by the physical page address, the PPA. A given address within any page is specified by the least significant 12 bits of the CPU address bus. One page register has the physical page address and the access control information relating to one page. There are 512 page registers, organized into 16 sets. The 16 sets are addressed by AS[0:3]. Each set has two groups of page registers, one for operand memory space and one for instruction memory space. These are addressed by OIN. Each group contains 16 page registers accommodating a total of 256 registers for each of operand and instruction memory space.

The MMU also checks for protection violation by comparing the processor state (PS), read from the CPU status word, with the access lock (AL) field in the page register. An additional bit in each page register allows the system to disable writes to operand pages or reads (execution) of instruction pages. If any memory violation occurs, the memory protect output (MPROEN) is asserted low. This typically causes a bus-fault-timeout on the processor which aborts the error cycle.

Figure 2 illustrates the Access Key mapping mechanism. When memory transactions are controlled by the MA31750, the AS[0:3] and PS[0:3] bits necessary to perform the address translation and access protection functions respectively, are obtained from a copy of the processor status word held by the MMU. Modifications to the CPU status word are reflected in the MMU copy.

Figure 4 illustrates the standard way to map the logical CPU addresses, AS[0:3] and PB[0:3] onto the physical extended address bus for both 1750A (a 20-bit physical address) and for 1750B (a 23-bit physical address). Figure 5 shows the various selections to achieve the required memory size and protection.

AL Code	Acceptable Access Key Codes
0	0
1	0,1
2	0,2
3	0,3
4	0,4
5	0,5
6	0,6
7	0,7
8	0,8
9	0,9
A	0,A
B	0,B
C	0,C
D	0,D
E	0,E
F	0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F

Figure 2: Access Lock and Key Mapping

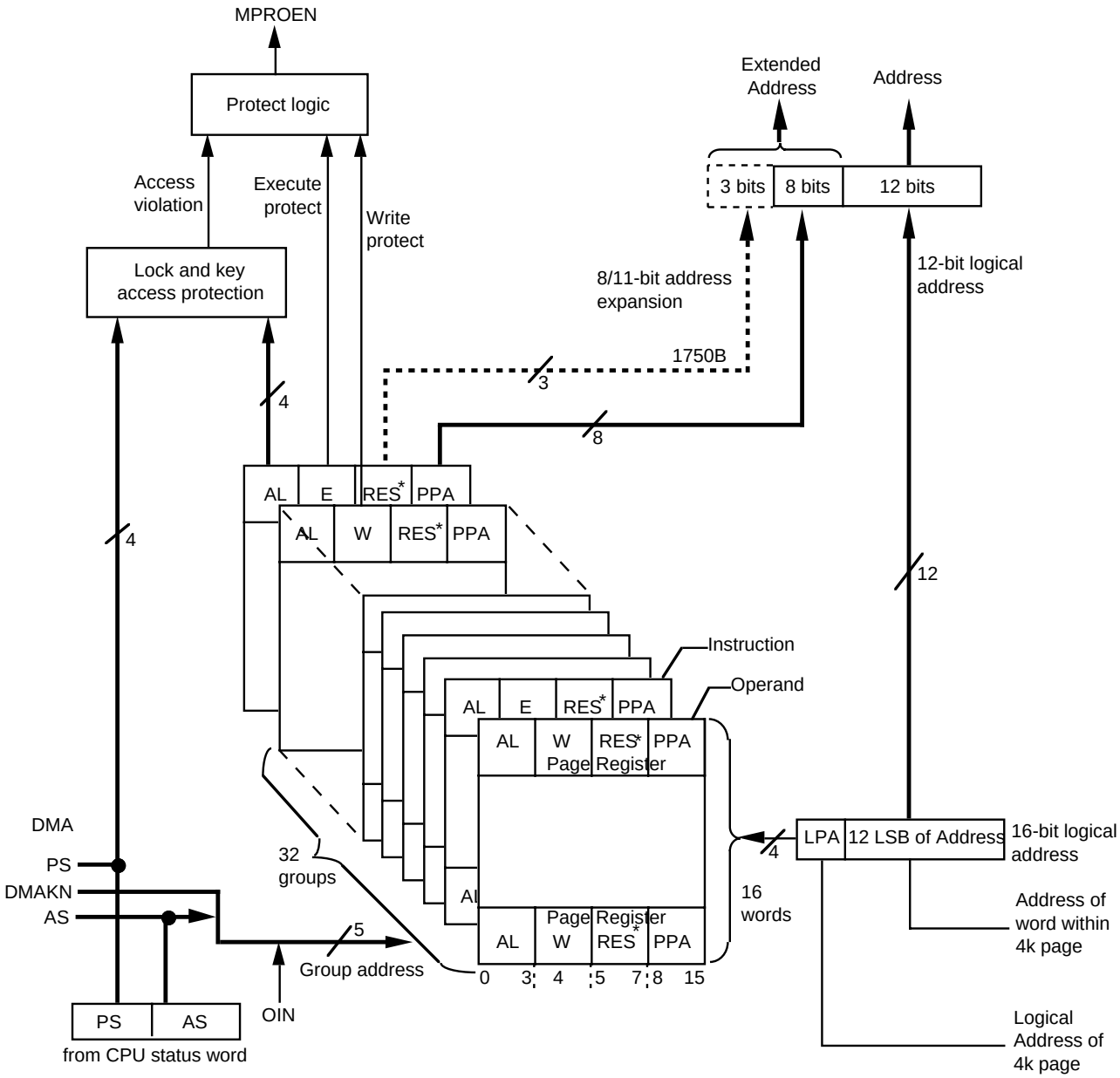
1.3 BLOCK PROTECTION

The presence of a BPU in the system is determined from the CPU configuration word. A BPU present in the system offers protection of the physical memory in 1k blocks. It takes the physcial address from the EA bus hence the BPU protection cannot start until the MMU lookup has completed and EAS rises. If no MMU is present, the physical address is read from the processor address bus. The address selects the relevant 16 bit word from the BPU RAM or cache. Each bit in this word represents the protection on 1k of physical memory. Any attempt to write a protected block results in an access violation error from the BPU.

NOTE: MIL-STD-1750 states that the MSB of the Block Protect Register (BPR) should protect the least significant address block.

1.4 DIRECT MEMORY ACCESS

The MA31751 supports DMA access within the expanded memory space, including translation and protection. When a DMA controller is performing memory transactions, it must provide the AS[0:3] and PS[0:3] signals to the inputs of the MMU for address translation and access protection.



* These 3 bits are reserved in 1750A. In 1750B they are used as extra PPA bits to form the MSB's of the extended address bus.

Figure 3: MMU Memory Mapping Mechanism

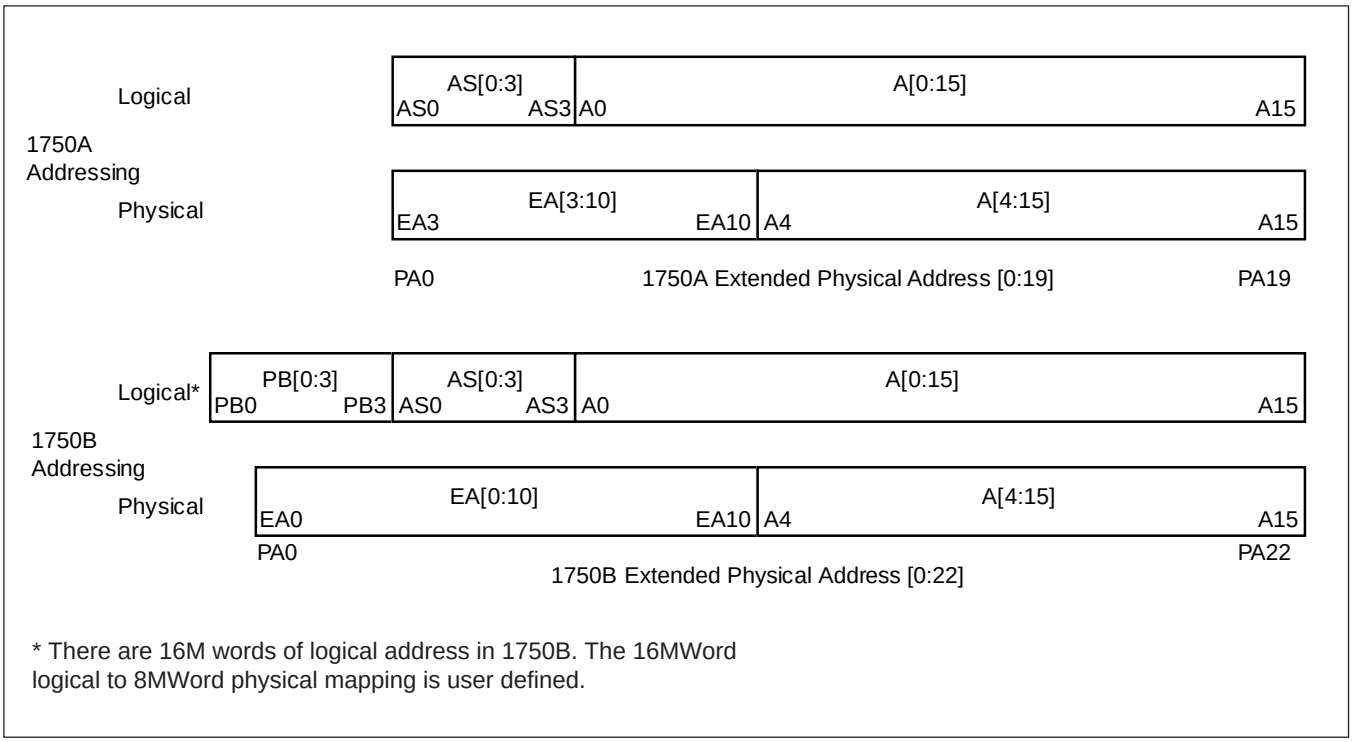


Figure 4: Extended Address Mapping in 1750A/B Mode

Addressable Physical Memory	Addressable Logical Memory	Is BPU Protection Required?	Mode	Number of MMUs	Number of BPUs	Number of MA31751s Required
64KW	64KW	NO	A	0	0	0
1MW	1MW	NO	A	1	0	1
64KW	64KW	YES	A	0	1	1
1MW	1MW	YES	A	1	1	1
64KW	64KW	NO	B	0	0	0
8MW	1MW	NO	B	1	0	1
8MW	2MW	NO	B	2	0	2
8MW	4MW	NO	B	4	0	4
8MW	8MW	NO	B	8	0	8
8MW	16MW	NO	B	16	0	16
64KW	64KW	YES	B	0	1	1
8MW	1MW	YES	B	1	8	8
8MW	2MW	YES	B	2	8	8
8MW	4MW	YES	B	4	8	8
8MW	8MW	YES	B	8	8	8
8MW	16MW	YES	B	16	8	16

Notes: 1. Memory is specified in terms of addressable instruction space.
2. It is assumed that the whole of the physical address space is used in 1750B - if this is not the case the number of MA31751 chips may be reduced.

Figure 5: MA31751 Selection Chart for Varying Memory Requirements

2.0 TIMING CONSIDERATIONS

2.1 MMU TIMINGS

To enable a fast page register look-up time, the MMU has two fast translation cache registers. These hold the address translation information on the 4K memory page which is currently being accessed. When the CPU has control of the system, one cache register is for operand transfers and one for instruction transfers, as these often occur in different pages. The appropriate translation cache register is chosen by the operand/instruction (OIN) signal from the CPU. When a DMA has system control, the caches operate as Read/Write caches, the appropriate cache being selected by the RDWN signal. When either an instruction/read or an operand/write crosses a page boundary, one wait state may be added whilst the translation cache register is updated from internal memory. This system minimises the MMU overhead.

2.2 BPU TIMINGS

A similar caching system is employed in the BPU section of the MA31751 to allow more rapid detection of access violations. If the physical address crosses a 16K block boundary, then one wait state may be added.

Different combinations of cache hits and misses give different access times if the MA31751 is acting as both an MMU and a BPU. If the logical address (from the CPU) gives an MMU cache hit, the physical address is looked-up from the translation cache register (operand or instruction, depending on OIN). If the physical address gives a cache hit, the protection for the block is looked-up in the BPU cache register. This situation (both hits) gives the fastest access time. The access time is a maximum if both logical and physical addresses give cache misses.

3.0 OUTPUTS FROM THE MA31751

3.1 PRPEN

This signal goes active low if a parity error occurs on a memory access, ie. there is a parity error in the MMU page register. There is no parity checking on XIO cycles, (this should be covered by the processor).

3.2 MPROEN

This signal is always low when ASIN is low. On a memory access, with an MMU only present it stays low until the address translation is validated. If the translation is erroneous, it stays low, causing a machine cycle time-out. If a BPU is present with the MMU, an erroneous translation causes the output to stay low. If the translation is correct, MPROEN will still stay low until the BPU check has completed. If there is no block protection set, MPROEN goes high, allowing the cycle to proceed. If the block protection is set, MPROEN stays low and the cycle times out. In a BPU only system, MPROEN indicates whether or not the protection bit is set for the address being accessed.

In a 1750B system with both an MMU and BPU present, MPROEN may glitch between the translation validation and the protection check (as the MMU and BPU functions may be on different devices). In this case, MPROEN should be gated with BPUVALIDN being low before being input to the CPU.

3.3 BPUVALIDN

BPUVALIDN falls to indicate that the output from the BPU is valid. If no BPU is present, BPUVALIDN remains high.

4.0 PIN DESCRIPTIONS

A description of each pin function appears in Figure 6. The acronym is presented first, followed by its function and description. Timing characteristics of each of the functions are shown in section 6.

All CMOS compatible signals are protected by an Electrostatic Discharge (ESD) protection circuit. Throughout this data sheet, active low signals are denoted either by placing a bar over the signal name,or by following the signal name with an “N” suffix, e.g.,DSN.

All unused inputs should be connected to their inactive state and should not be allowed to float.

4.1 SIGNAL DEFINITIONS

Pin Name	Function	Description
SYSTEM BUSSES		
A00-A15	Processor Address Bus	An active-high address bus for addresses and XIO commands. A15 is the LSB.
D00-D16	System Data Bus	Data bus used to transfer data to and from the MMU/BPU. D15 is the LSB and D16 is the parity bit.
EA00-EA10	Extended Address Bus	If the MMU is selected (using CSN) then EA0-EA10 provides the system extended address. EA3-EA10 should be combined with A4-A15 from the processor to give the full 20 bit 1750A system address bus and EA0-EA10 with A4-A15 gives a 23 bit 1750B system address bus. (See Fig 4).During XIO transfers, EA7-10 mimic A0-A3 to present the full processor address to the system. When the MMU is not selected, EA0-EA10 become inputs to allow the BPU to protect the appropriate section of extended memory.
BUS CONTROL		
ASIN	Address Strobe In	The rising edge of this active-high signal generated by the CPU or DMA controller, indicates that a valid address is present on the MA31750.
DSN	Data Strobe	The rising edge of this active-low signal generated by the CPU or DMA controller, indicates that valid data is present on D00-D16 of the MA31750.
EAS	Extended Address Strobe	The rising edge of this active-high signal indicates that a valid and stable extended address is available from the MA31751. This pin becomes an input when no MMU is selected and should be driven from the system address strobe. During XIO cycles, EAS follows ASIN.
MION	Memory / IO Select	This input is used to select between normal operation and command transfer (XIO) mode. A high indicates memory whilst a low indicates IO. This signal is provided by the CPU or the DMA controller.
RDWN	Read / Write Select	This input indicates the direction of data transfer on the data bus. A high level indicates that the processor is reading the bus whilst a low level indicates that the processor is driving the bus. The input is driven by the CPU or the DMA controller.
OIN	Operand / Instruction Select	This input indicates the type of data on the data bus. A high indicates operand data whilst a low indicates the presence of instruction data. The signal is provided by the CPU or the DMA controller.
EXTENDED MEMORY CONTROL		
AS0-AS3	Address State	This bus comes from the DMA controller during DMA accesses. It is used by the MMU as part of the page selection operation. (During CPU operation, this information is read from the MMU's copy of the CPU status word). If no MMU function is required, these inputs should be tied to ground.
PS0-PS3	Processor State	This bus comes from the DMA controller during DMA accesses. It is used by the MMU to provide lock and key protection on page accesses. (During CPU operation, this information is read from the MMU's copy of the CPU status word.) If no MMU function is required, these inputs should be tied to ground.

Figure 6: Pin Description Table

Pin Name	Function	Description
ERROR INDICATION		
MPROEN	Memory Protect Error	The MPROEN output is always asserted low when ASIN is low. On an external memory cycle, MPROEN low at the end of the cycle indicates there has been a protection error in either the MMU or the BPU. A high indicates no error. MPROEN goes high after ASIN rising on XIO cycles.
PRPEN	Page RAM Parity Error	This active-low output is asserted low if a parity error is detected during an MMU/BPU memory transfer.
MISCELLANEOUS		
RESETN	System Reset	Active low device reset input. Should be connected to system reset.
CSN	MMU Chip Select	A low on this input selects the MMU. In a 1750A system, this input may be tied to ground if MMU functions are required, or tied to MION if only BPU functions are required (must be active for XIO cycles when the device may need to respond to an MMU/BPU XIO command.) In 1750B, this input should be derived by decoding the PB[0:3] bus from the CPU. (Note that in 1750B mode, one device is required per implemented page bank.)
BPUVALIDN	BPU enabled and selected	This output becomes active (low) when MPROEN is valid if there is at least one BPU present in the system .
DMAKN	DMA Acknowledge	This active-low input is used to select between the CPU and DMA protection registers within the MA31751, and should be asserted low when the CPU has relinquished control to a DMA in the system. DMAKN active low means that the MMU gets the AS[0:3] and PS[0:3] information from the pins rather than from the internal copy of the CPU Status Word. The signal is driven by the system.
GLPE	Global Protect Enable	This active-high signal goes high in BPU mode following a system reset to indicate that the memory system is globally write-protected. The signal is set low by the XIO MPEN command. GPLE is inactive high when the BPU functions are disabled.
HITMISSN	Cache hit/miss	A high on this output indicates that a memory cycle is a cache hit - a low indicates a cache miss. This output goes low when ASIN is low and rises on memory cycles when a hit has been validated. This output goes high on XIO cycles.
POWER		
VDD	Power Supply	5V DC power supply input.
GND	Ground	0V reference point.

Figure 6: Pin Description Table (continued)

5.0 DC PARAMETERS - ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current through any pin except V_{DD} and GND	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Figure 7: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.1 DC PARAMETERS - NORMAL OPERATING CONDITIONS

			Total dose radiation not exceeding 3x10^5 Rad(si)			
Symbol	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
VDD	Supply voltage	-	4.5	5.0	5.5	V
VIH	Input high voltage	-	80% VDD	-	-	V
VIL	Input low voltage	-	-	-	20% VDD	V
VOH	Output high voltage	IOH=-5mA	VDD-0.5	-	-	V
VOL	Output low voltage	IOL=5mA	-	-	VSS+0.4	V
IIH	Input high current (Note 1)	-	-	-	10	µA
IIL	Input low current (Note 1)	-	-	-	-10	µA
IOZH	I/O tristate high current	-	-	50	-	µA
IOZL	I/O tristate low current	-	-	-50	-	µA
IDDYN	Dynamic supply current	-	-	-	50	mA
IDDS	Static supply current	-	-	0.2	10	mA

VDD=5V±10% over full operating temperature range.
Mil-Std-883, method 5005, subgroups 1, 2, 3
Note 1: Guaranteed but not measured at -55°C

Figure 8: Operating DC Parameters

Subgroup	Definition
1	Static characteristics specified in Figure 8 at +25°C
2	Static characteristics specified in Figure 8 at +125°C
3	Static characteristics specified in Figure 8 at -55°C
7	Functional characteristics specified at +25°C
8A	Functional characteristics specified at +125°C
8B	Functional characteristics specified at -55°C
9	Switching characteristics specified in Figure 10 at +25°C
10	Switching characteristics specified in Figure 10 at +125°C
11	Switching characteristics specified in Figure 10 at -55°C

Figure 9: Definition of Subgroups

6.0 TIMING PARAMETERS

	Parameter	Min	Max	Units
1	DSN falling to data bus active (XIO Read)	-	40	ns
2	DSN falling to data from MMU valid (XIO Read)	-	90	ns
3	Data valid after DSN rising (XIO Read)	10	-	ns
4	Data bus inactive after DSN rising (XIO Read)	-	45	ns
5	Address and control setups to ASIN rising	15	-	ns
6	Address and control hold after ASIN falling	5	-	ns
7	CSN setup to DSN rising (1750B) (XIO)	75	-	ns
8	CSN hold after DSN rising (1750B) (XIO)	0	-	ns
9	Data hold after DSN rising (XIO Write)	10	-	ns
10	Data setup to DSN rising (XIO Write)	5	-	ns
11	ASIN falling to EAS falling	-	30	ns
12	Extended address valid to EAS rising	5	30	ns
13	ASIN rising to EA bus valid (MMU cache hit)	-	40	ns
14	EA bus valid to PRPEN active	5	15	ns
15	ASIN rising to EA bus valid (MMU cache miss)	-	80	ns
16	ASIN rising to MPROEN active (MMU cache hit)	-	60	ns
17	ASIN rising to MPROEN active (MMU cache miss)	-	105	ns
18	ASIN rising to MPROEN active (2 cache hits)	-	60	ns
19	ASIN rising to MPROEN active (1 miss, 1 cache hit)	-	105	ns
20	ASIN rising to MPROEN active (No MMU, BPU miss)	-	50	ns
21	ASIN rising to MPROEN active (MMU and BPU miss)	-	185	ns
22	MPROEN setup to BPUVALIDN falling	5	-	ns
23	ASIN rising to GLPE falling	-	-	ns
24	RESETN falling to GLPE/MPROEN/PRPEN rising	-	-	ns
25	MPROEN valid after ASIN falling	5	-	ns
26	ASIN rising to EAS rising (XIO Cycles)	-	15	ns
27	DMAKN setup to ASIN rising	10	-	ns
28	DMAKN hold after ASIN falling	0	-	ns
29	PS[0:3] to MPROEN valid	5	40	ns
30	PRPEN hold after ASIN falling	10	-	ns

Mil-Std-883, method 5005, subgroups 9, 10 and 11

Figure 10: Timing Parameters

7.0 TIMING DIAGRAMS

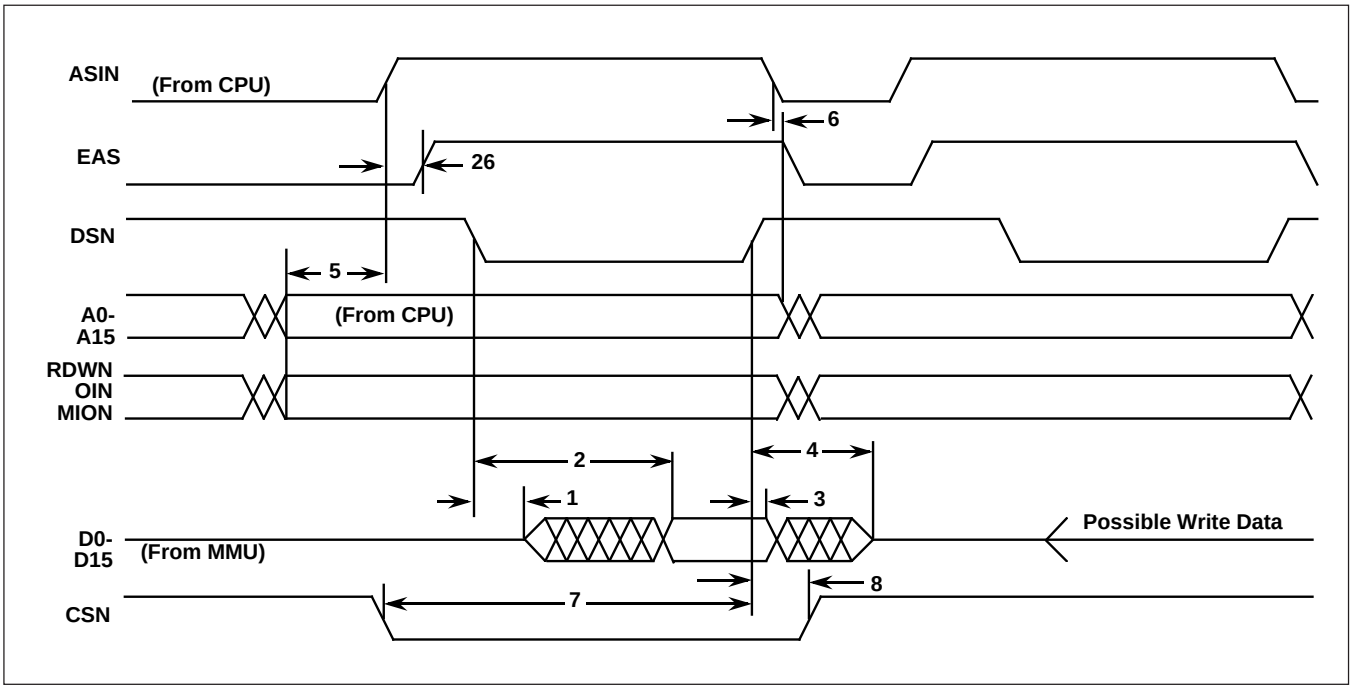


Figure 11: MA31750 XIO Read of MMU

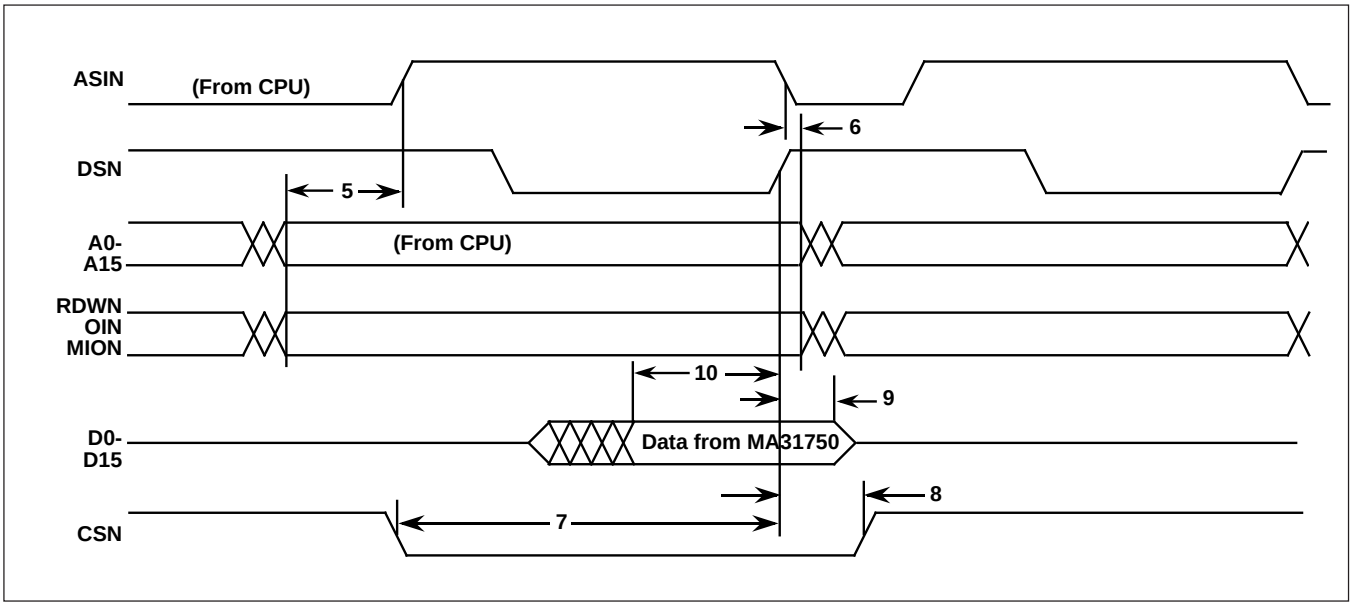


Figure 12: MA31750 XIO Write to MMU

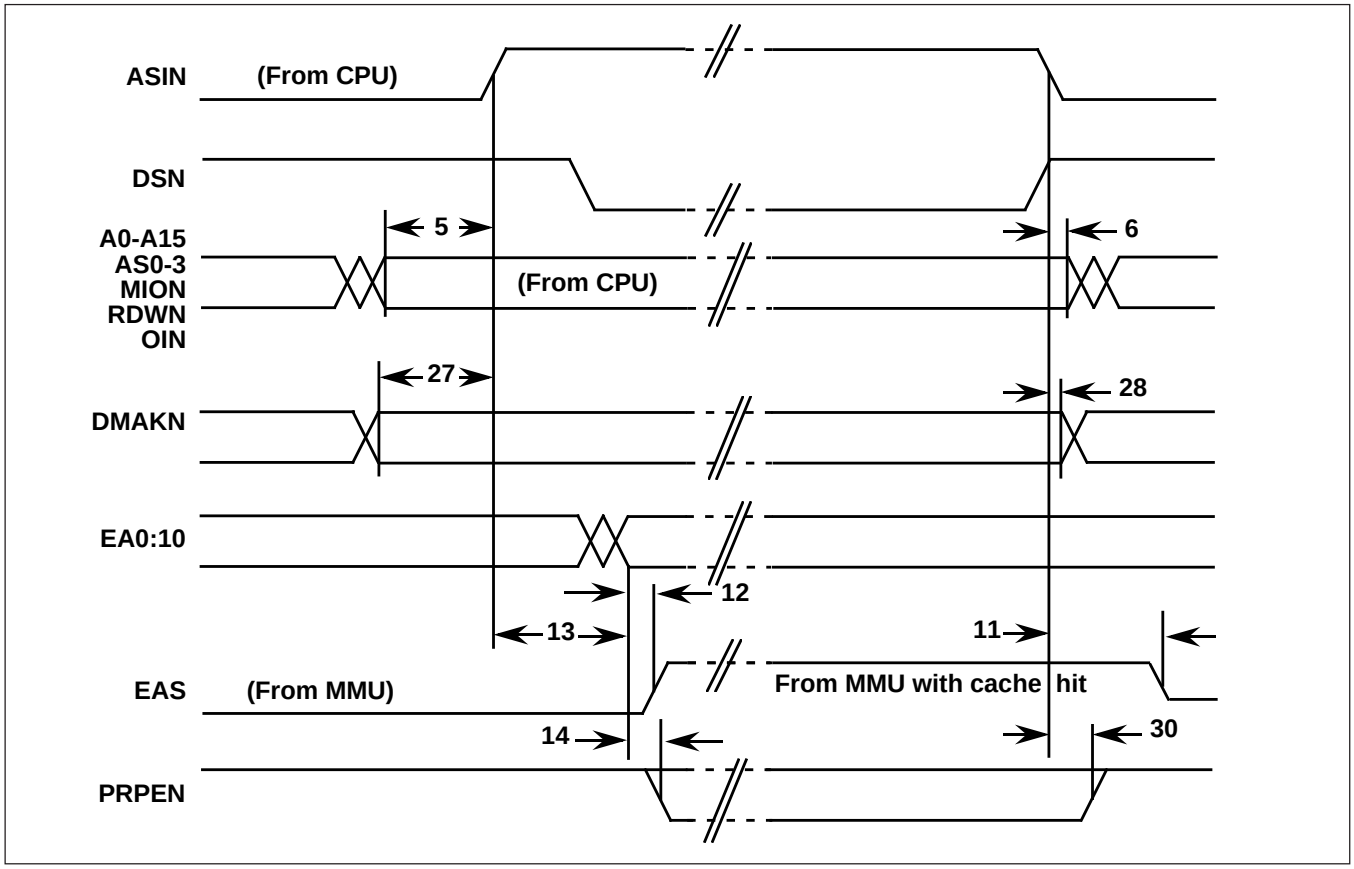


Figure 13: MMU Address Translation (Cache Hit)

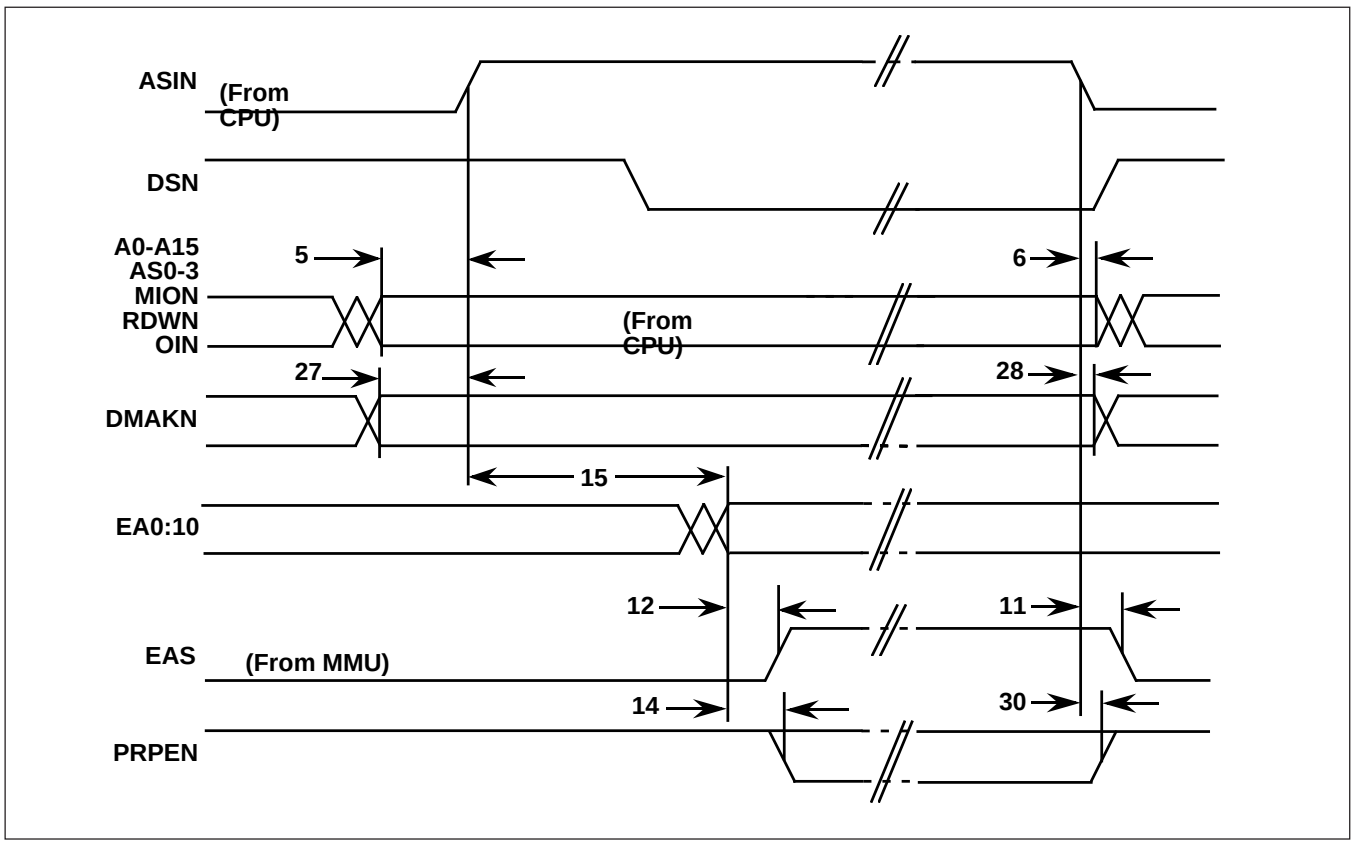


Figure 14: MMU Address Translation (Cache Miss)

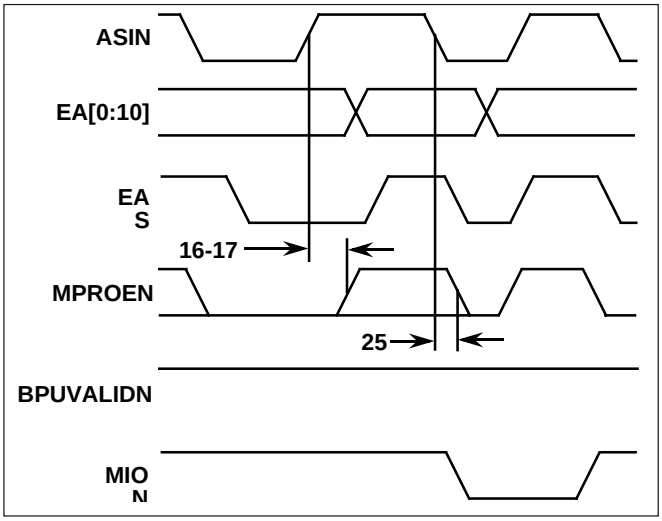


Figure 15: MMU Timing With No BPU

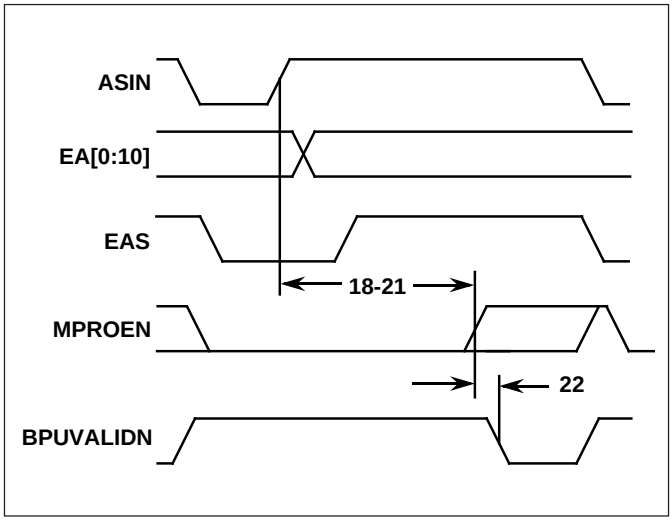


Figure 16: MMU and BPU Timings

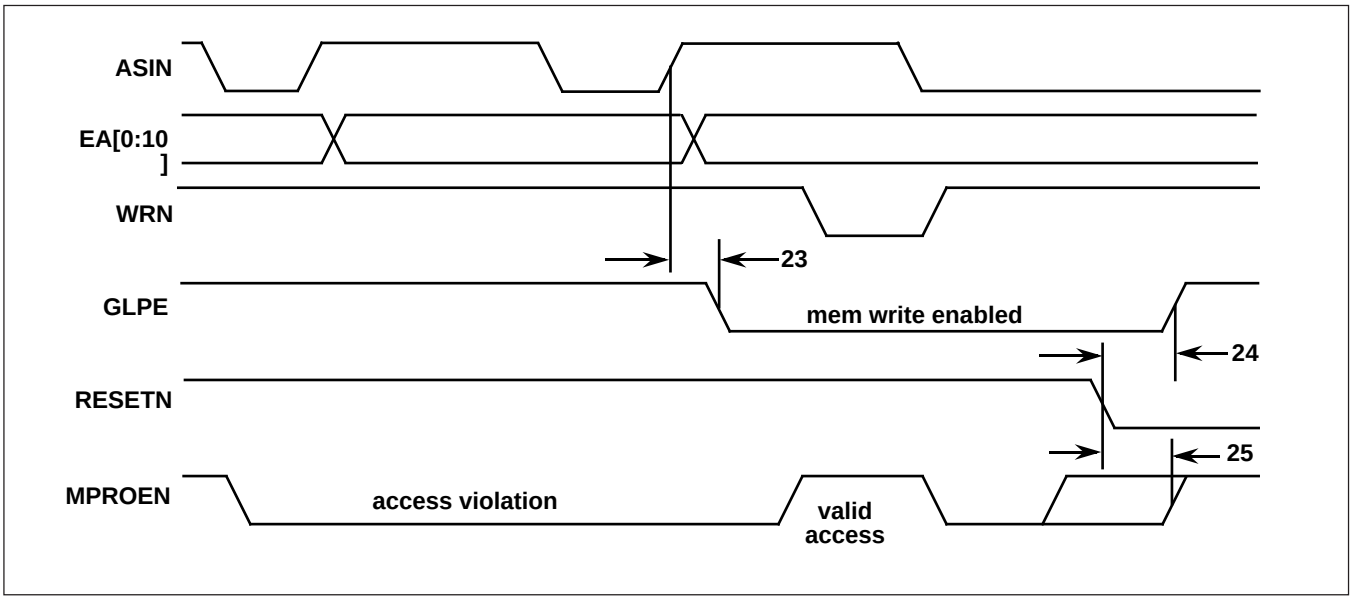


Figure 17: Reset and Enable Timings

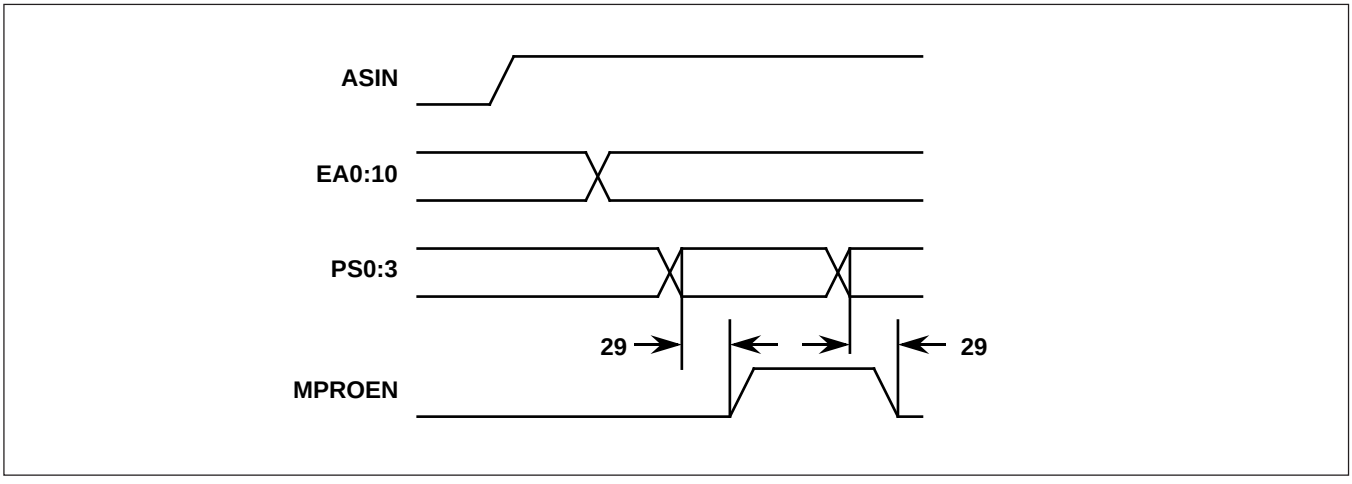


Figure 18: Processor State Timings

8.0 PACKAGING INFORMATION

8.1 FLATPACK PINOUT

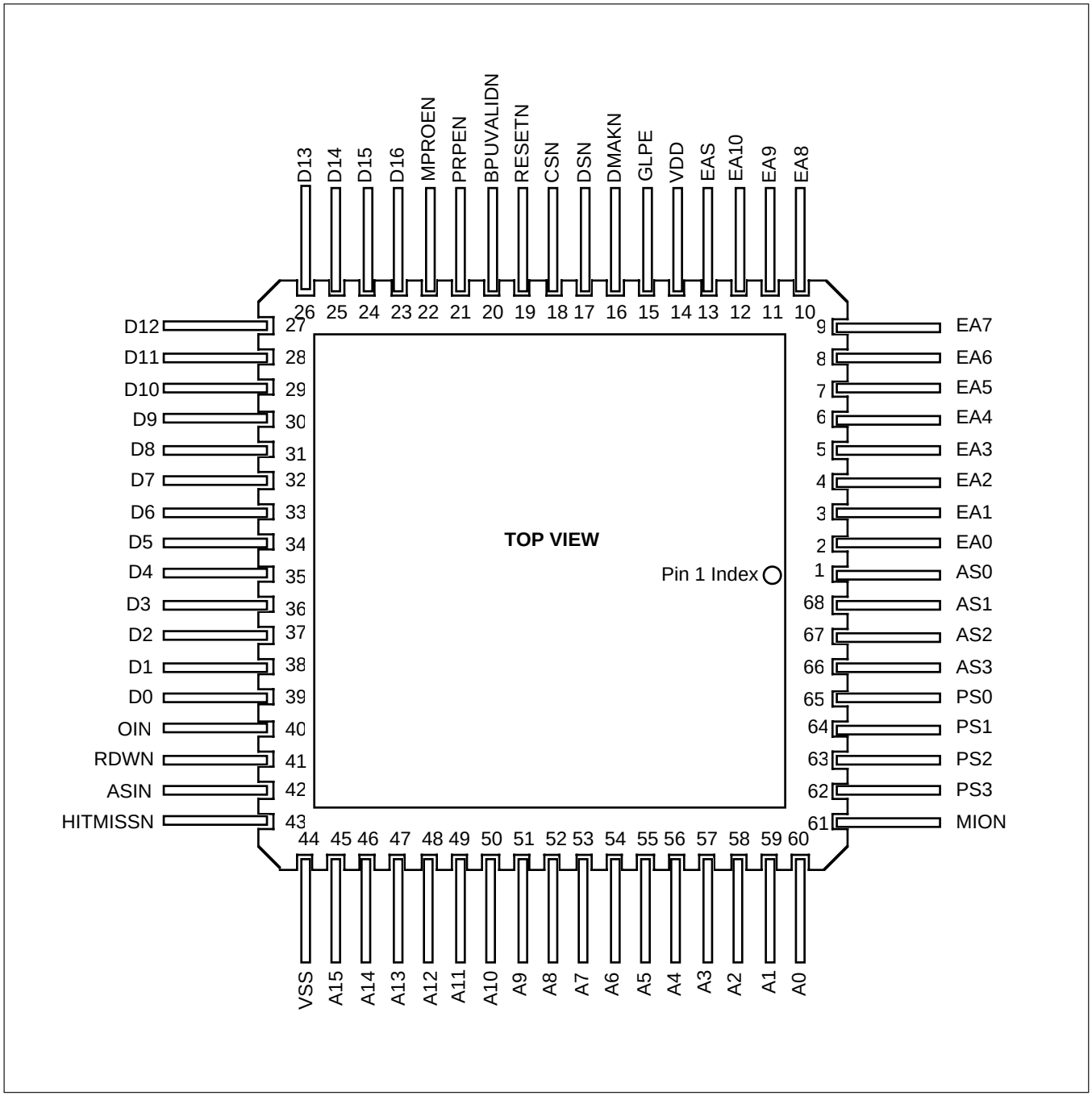


Figure 19: 68 Pin Lead Flatpack - Package Style F

8.2 FLATPACK DIMENSIONAL DRAWING

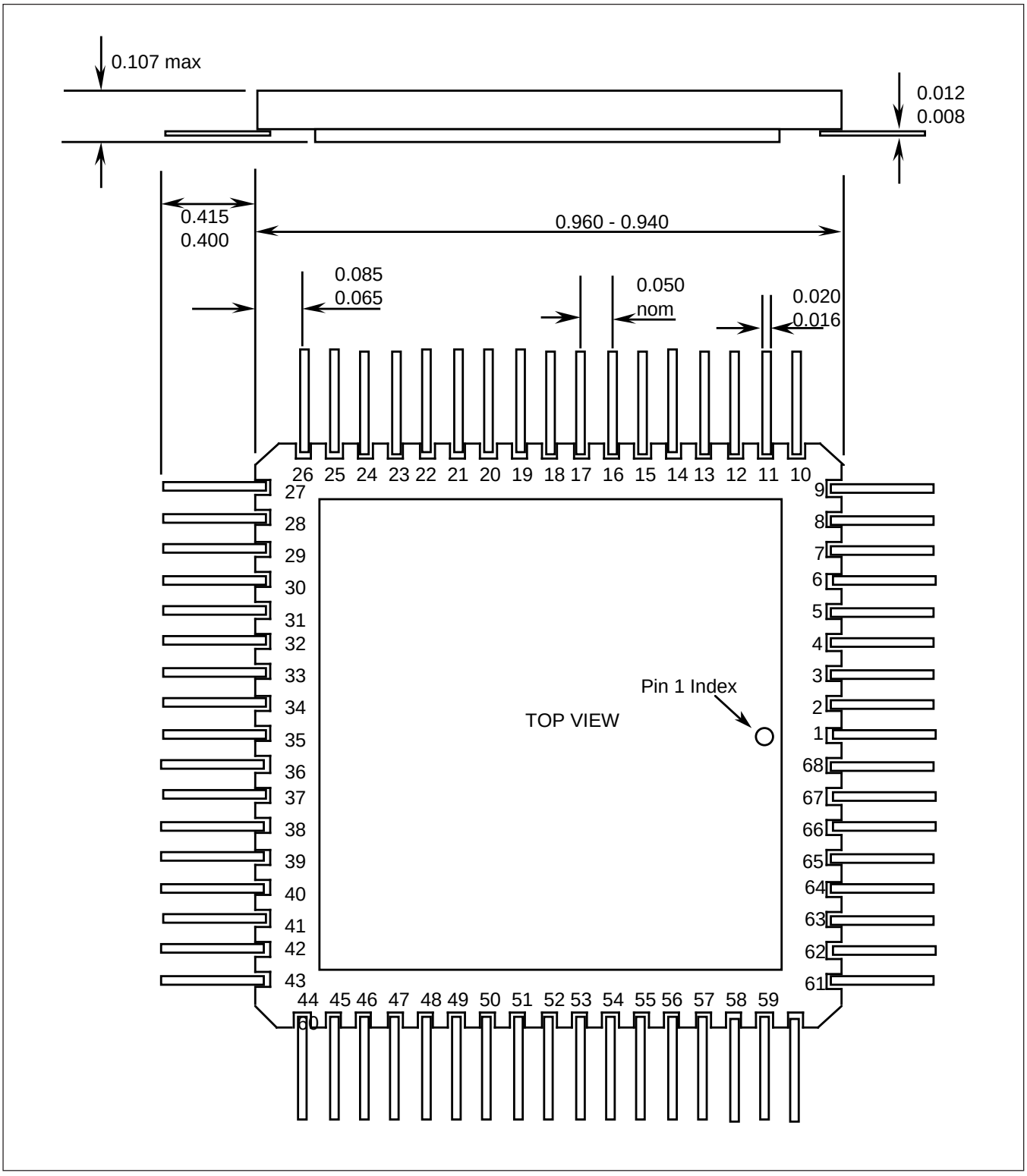
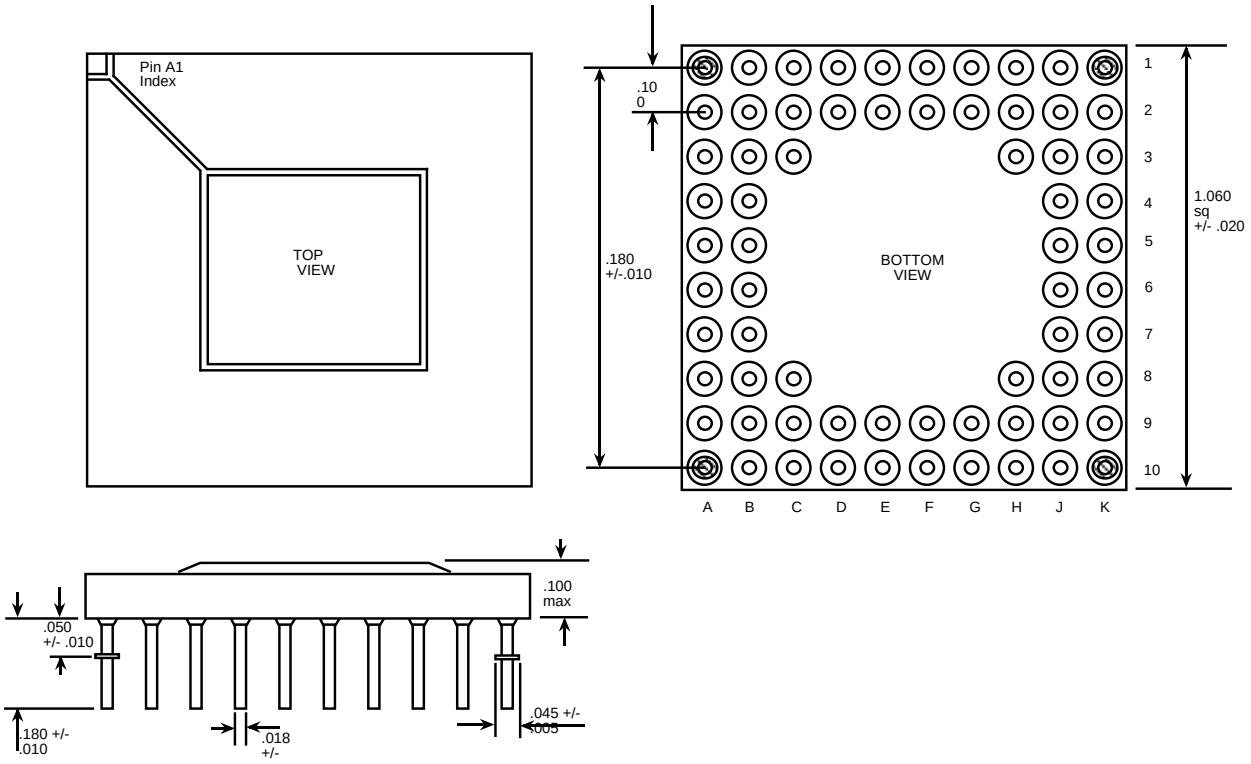


Figure 20: Dimensional Drawing of 68 Pin Lead Flatpack - Package Style F

8.3 PGA PINOUT AND DIMENSIONED DRAWING



Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	PS3	C1	PS0	G9	D7	K3	VDD
A2	A2	C2	PS2	G10	D6	K4	DMAKN
A3	A4	C3	MION	H1	EA3	K5	CSN
A4	A5	C8	GND	H2	EA6	K6	RESETN
A5	A7	C9	ASIN	H3	EA8	K7	PRPEN
A6	A8	C10	D0	H8	D12	K8	MPROEN
A7	A10	D1	AS2	H9	D10	K9	D15
A8	A12	D2	AS3	H10	D8	K10	D11
A9	A13	D9	OIN	J1	EA5		
A10	A15	D10	D1	J2	EA7		
B1	PS1	E1	AS0	J3	EA10		
B2	A0	E2	AS1	J4	GLPE		
B3	A1	E9	D2	J5	DSN		
B4	A3	E10	D3	J6	BPUVALIDN		
B5	A6	F1	EA0	J7	D16		
B6	A9	F2	EA1	J8	D14		
B7	A11	F9	D5	J9	D13		
B8	A14	F10	D4	J10	D9		
B9	HITMISSN	G1	EA2	K1	EA9		
B10	RDWN	G2	EA4	K2	EAS		

Figure 21: PGA Pinout and Dimensioned Drawing

9.0 RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Dynex Semiconductor can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{11}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

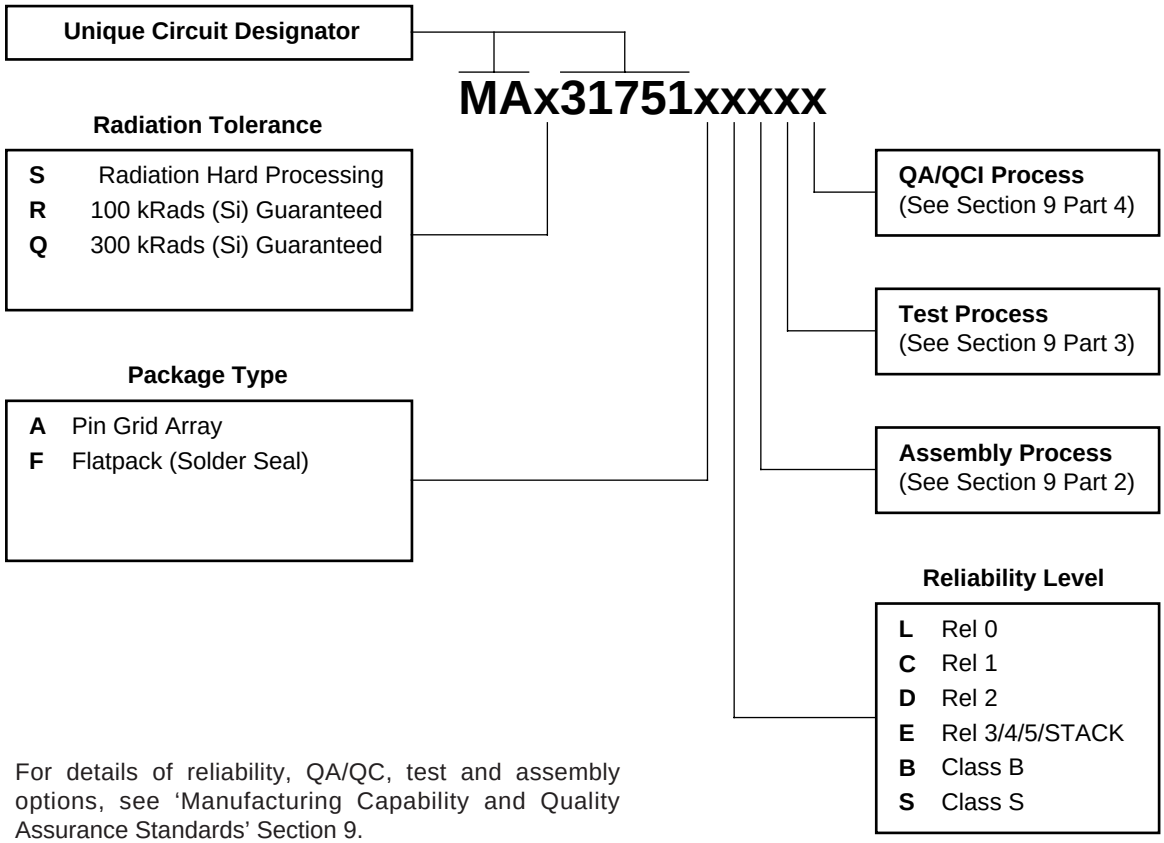
* Other total dose radiation levels available on request
** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 22: Radiation Hardness Parameters

10.0 OTHER INFORMATION

Reference: MA31751 Application Note 5 - Detailed Device Description.

11.0 ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

http://www.dynexsemi.com

e-mail: power_solutions@dynexsemi.com

HEADQUARTERS OPERATIONS
DYNEX SEMICONDUCTOR LTD
Doddington Road, Lincoln.
Lincolnshire. LN6 3LF. United Kingdom.
Tel: 00-44-(0)1522-500500
Fax: 00-44-(0)1522-500550

DYNEX POWER INC.
Unit 7 - 58 Antares Drive,
Nepean, Ontario, Canada K2E 7W6.
Tel: 613.723.7035
Fax: 613.723.1518
Toll Free: 1.888.33.DYNEX (39639)

CUSTOMER SERVICE CENTRES
France, Benelux, Italy and Spain Tel: +33 (0)1 69 18 90 00. Fax: +33 (0)1 64 46 54 50
North America Tel: 011-800-5554-5554. Fax: 011-800-5444-5444
UK, Germany, Scandinavia & Rest Of World Tel: +44 (0)1522 500500. Fax: +44 (0)1522 500020

SALES OFFICES
France, Benelux, Italy and Spain Tel: +33 (0)1 69 18 90 00. Fax: +33 (0)1 64 46 54 50
Germany Tel: 07351 827723
North America Tel: (613) 723-7035. Fax: (613) 723-1518. Toll Free: 1.888.33.DYNEX (39639) /
Tel: (831) 440-1988. Fax: (831) 440-1989 / Tel: (949) 733-3005. Fax: (949) 733-2986.
UK, Germany, Scandinavia & Rest Of World Tel: +44 (0)1522 500500. Fax: +44 (0)1522 500020
These offices are supported by Representatives and Distributors in many countries world-wide.
© Dynex Semiconductor 2000 Publication No. DS4083-3 Issue No. 3.0 January 2000
TECHNICAL DOCUMENTATION – NOT FOR RESALE. PRINTED IN UNITED KINGDOM

Datasheet Annotations:

Dynex Semiconductor annotate datasheets in the top right hard corner of the front page, to indicate product status. The annotations are as follows:-

Target Information: This is the most tentative form of information and represents a very preliminary specification. No actual design work on the product has been started.

Preliminary Information: The product is in design and development. The datasheet represents the product as it is understood but details may change.

Advance Information: The product design is complete and final characterisation for volume production is well in hand.

This publication is issued to provide information only which (unless agreed by the Company in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. The Company reserves the right to alter without prior notice the specification, design or price of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to the Company's conditions of sale, which are available on request.

All brand names and product names used in this publication are trademarks, registered trademarks or trade names of their respective owners.