Low-Voltage, 0.8-Ω r_{ON}, Dual SPST Analog Switch

FEATURES

- Low Voltage Operation (1.6 V to 3.6 V)
- Low On-Resistance - $r_{DS(on)}$: 0.8 Ω @ 2.7 V
- High Current Handling Capacity: 150-mA Continuous
- Off-Isolation: –56 dB @ 1 MHz
- Fast Switching: 25 ns t_{ON}
- Low Charge Injection—Q_{INJ}: 5.8 pC
- Low Power Consumption: < 1 μW
- ESD Protection > 2,000 V

BENEFITS

- High Accuracy
- High Bandwidth
- TTL and Low Voltage Logic Compatibility
- Low Power Consumption
- Reduced PCB Space (SOT23-8 and MSOP-8)

APPLICATIONS

- Mixed Signal Routing
- Portable and Battery Operated Systems
- Low Voltage Data Acquisition
- Modems
- PCMCIA Cards

DESCRIPTION

The DG2741/2742/2743 are low voltage, single supply, dual SPST analog switches. Designed for high performance switching of analog signals, the DG2741/2742/2743 provide low on-resistance (0.8 Ω @ +2.7 V), fast speed (t_{ON}, t_{OFF} @ 35 ns and 33 ns) and the ability to handle signals over the entire analog voltage range.

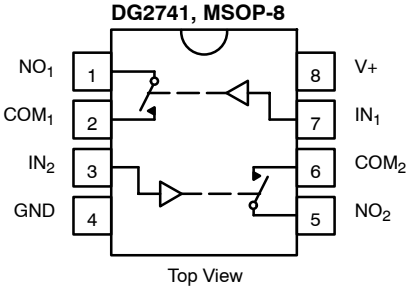
When operated on a +3-V supply, control pins are compatible with 1.8-V digital logic. Additionally,on-resistance flatness and matching (0.18 Ω and 0.08 Ω, respectively) offer high accuracy between channels.

The DG2741 contains two normally open (NO) switches, the DG2742 contains two normally closed (NC) switches, and the DG2743 contains one normally open and one normally closed switch. Break-before-make is guaranteed.

Built on Vishay Siliconix's low voltage submicron CMOS process, the DG2741/2742/2743 were designed to offer solutions that extend beyond audio/video functions, to providing the performance required for today's demanding mixed-signal switching in portable applications.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION—DG2741

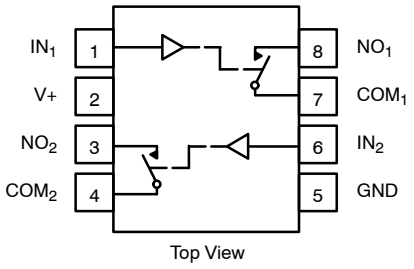
DG2741, MSOP-8



Top View

Device Marking: 2741

DG2741. SOT23-8



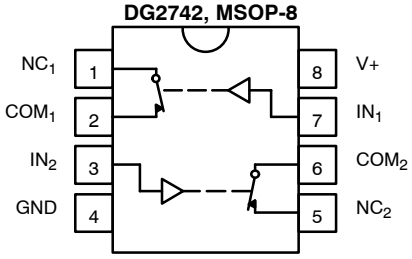
Top View

Device Marking: F3

TRUTH TABLE - DG2741	
Logic	**Switch**
0	Off
1	On

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION—DG2742/DG2743

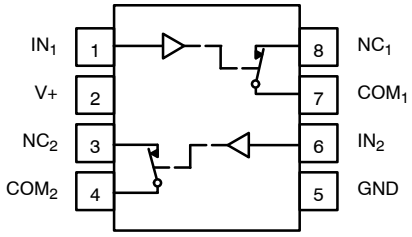
DG2742, MSOP-8



Top View

Device Marking: 2742

DG2742. SOT23-8

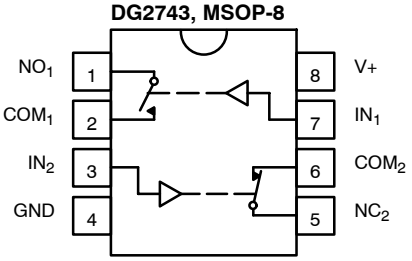


Top View

Device Marking: F4

TRUTH TABLE - DG2742	
Logic	**Switch**
0	On
1	Off

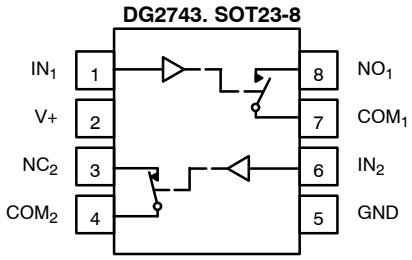
DG2743, MSOP-8



Top View

Device Marking: 2743

DG2743. SOT23-8



Top View

Device Marking: F5

TRUTH TABLE - DG2743		
Logic	**Switch-1**	**Switch-2**
0	Off	On
1	On	Off

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
-40 to 85°C	MSOP-8	DG2741DQ–T1
		DG2742DQ–T1
		DG2743DQ–T1
	SOT23-8	DG2741DS–T1
		DG2742DS–T1
		DG2743DS–T1

ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+ ..... -0.3 to +4 V

IN, COM, NC, NO[a] ..... -0.3 to (V+ + 0.3 V)

Continuous Current (NO, NC and COM Pins) ..... ±200 mA

Peak Current ..... ±300 mA

(Pulsed at 1 ms, 10% duty cycle)

ESD per Method 3015.7 ..... >2 kV

Storage Temperature (D Suffix) ..... -65 to 150°C

Power Dissipation (Packages)[c]

6-Pin SC-70[c] ..... 250 mW

Notes:

a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC Board.

c. Derate 3.1 mW/°C above 70°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V+ = 1.8 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 1.8 V, ±10%, V_{IN} = 0.4 or 1.0 V[e]	Temp[a]	Limits −40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 1.8 V, V_{COM} = 0.9 V, I_{NO}, I_{NC} = 10 mA	Room Full[d]		0.9	2.5 4.0	Ω
r_{ON} Flatness[d]	r_{ON} Flatness	V+ = 1.8 V, V_{COM} = 0 to V+, I_{NO}, I_{NC} = 10 mA	Room		0.25		Ω
r_{ON} Match[d]	Δr_{ON}	V+ = 1.8 V, V_{COM} = 0 to V+, I_{NO}, I_{NC} = 10 mA	Room		0.05		Ω
Switch Off Leakage Current[f]	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 1.8 V, V_{NO}, V_{NC} = 0.2 V/2.0 V, V_{COM} = 1.5 V/0.3 V	Room Full[d]	−1 −10		1 10	nA
	$I_{COM(off)}$	V+ = 1.8 V, V_{NO}, V_{NC} = 0.2 V/2.0 V, V_{COM} = 1.5 V/0.3 V	Room Full[d]	−1 −10		1 10	nA
Channel-On Leakage Current[f]	$I_{COM(on)}$	V+ = 1.8 V, V_{NO}, V_{NC} = V_{COM} = 0.3 V/1.5 V	Room Full[d]	−1 −10		1 10	nA
Digital Control							
Input High Voltage	V_{INH}		Full	1.0			V
Input Low Voltage	V_{INL}		Full			0.4	V
Input Capacitance[d]	C_{in}		Full		5.5		pF
Input Current[f]	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	−1		1	µA
Dynamic Characteristics							
Turn-On Time[d]	t_{ON}	V_{NO} or V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF Figures 1 and 2	Room Full[d]		33	45 50	ns
Turn-Off Time[d]	t_{OFF}	V_{NO} or V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF Figures 1 and 2	Room Full[d]		27	40 45	ns
Break-Before-Make Time[d]	t_d	V_{NO} or V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF Figures 1 and 2	Room	3			ns
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω, Figure 3	Room		20		pC
Off-Isolation[d]	OIRR	R_L = 1 kΩ, C_L = 5 pF, f = 1 MHz	Room		55		dB
Crosstalk[d]	X_{TALK}	R_L = 1 kΩ, C_L = 5 pF, f = 1 MHz	Room		91		dB
NO, NC Off Capacitance[d]	$C_{NO(off)}$, $C_{NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		88		pF
Channel-On Capacitance[d]	C_{ON}	V_{IN} = 0 or V+, f = 1 MHz	Room		105		pF

SPECIFICATIONS (V+ = 3.0 V)

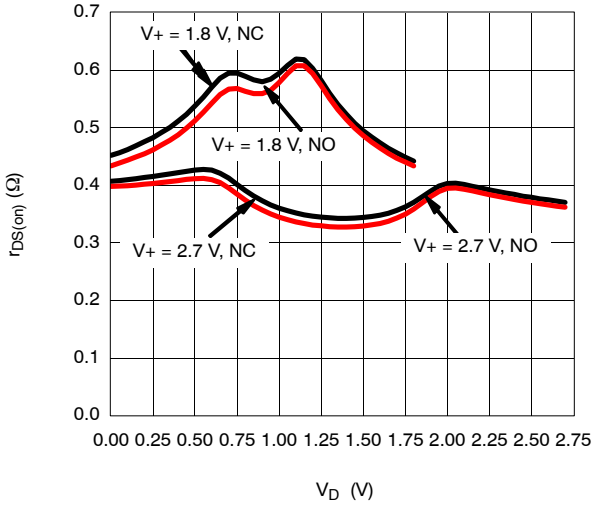
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, V_{IN} = 0.5 or 1.4 V[e]	Temp[a]	Limits −40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V, I_{NO} I_{NC} = 100 mA	Room Full		0.4	0.8 0.9	Ω
r_{ON} Flatness	r_{ON} Flatness	V+ = 2.7 V, V_{COM} = 1.5, 2 V, I_{NO}, I_{NC} = 100 mA	Room		0.08	0.18	
r_{ON} MatchFlat	Δr_{ON}		Room		0.05	0.08	
Switch Off Leakage Current	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 3.3 V V_{NO}, V_{NC} = 0.3 V/3 V, V_{COM} = 3 V/0.3 V	Room Full	−1 −10		1 10	nA
	$I_{COM(off)}$		Room Full	−1 −10		1 10	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 0.3 V/3 V	Room Full	−1 −10		1 10	
Digital Control							
Input High Voltage	V_{INH}		Full	1.4			V
Input Low Voltage	V_{INL}		Full			0.5	
Input Capacitance[d]	C_{in}		Full		5.5		pF
Input Current[f]	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	−1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF V+ = 2.7 V, Figure 1 and 2	Room Full		20	30 35	ns
Turn-Off Time	t_{OFF}		Room Full		18	28 33	
Break-Before-Make Time	t_d		Room	1			
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω, Figure 3	Room		5.8		pC
Off-Isolation[d]	OIRR	R_L = 1 kΩ, C_L = 5 pF, f = 1 MHz	Room		−56		dB
Crosstalk[d]	X_{TALK}		Room		−89		
NO, NC Off Capacitance[d]	$C_{NO(off)}$, $C_{NC(off)}$	V+ = 3.6 V, V_{IN} = 0 or V+, f = 1 MHz	Room		81		pF
Channel-On Capacitance[d]	C_{ON}		Room		103		
Power Supply							
Power Supply Range	V+			1.5		3.6	V
Power Supply Current	I+	V+ = 3.6 V, V_{IN} = 0 or V+			0.01	1.0	µA

Notes:

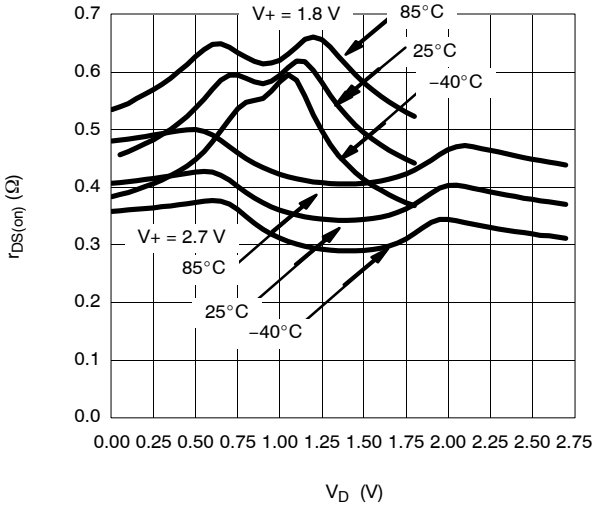
a. Room = 25°C, Full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 3-V leakage testing, not production tested.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

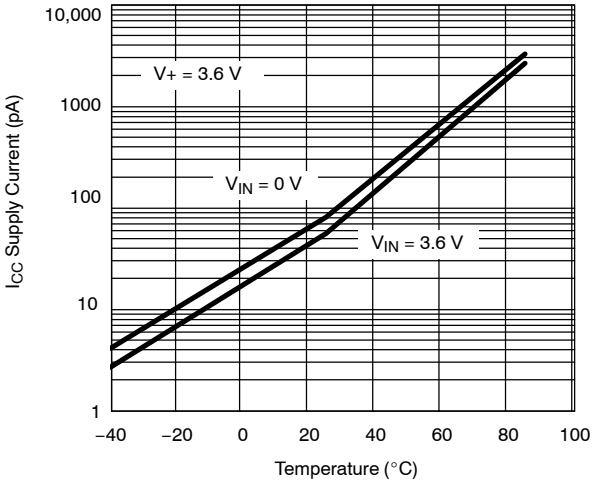
$r_{DS(on)}$ vs. V_{COM} vs. 1 V_{CC}



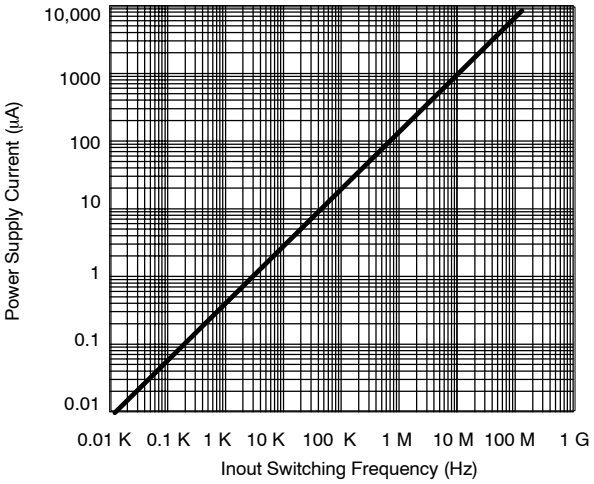
$r_{DS(on)}$ vs. V_D, V_{CC} and Temperature



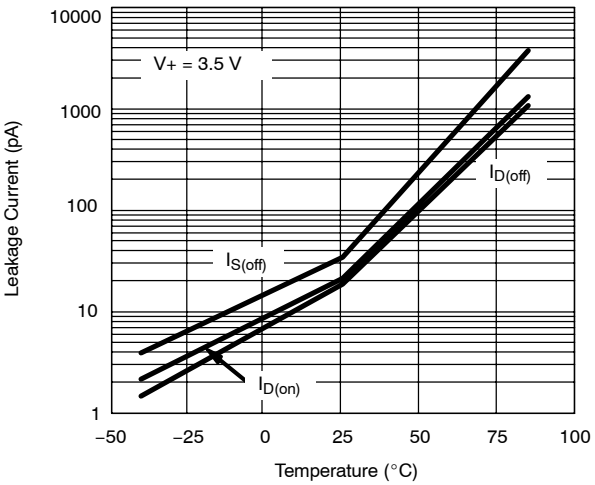
Supply Current vs. Temperature



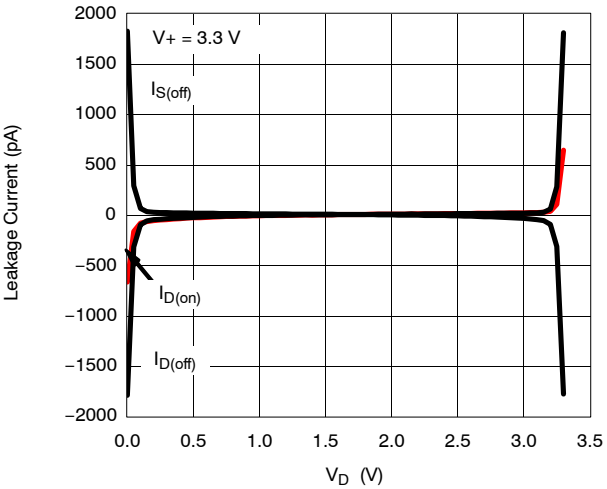
Switching Frequency vs. Supply Current



Leakage Current vs. Temperature

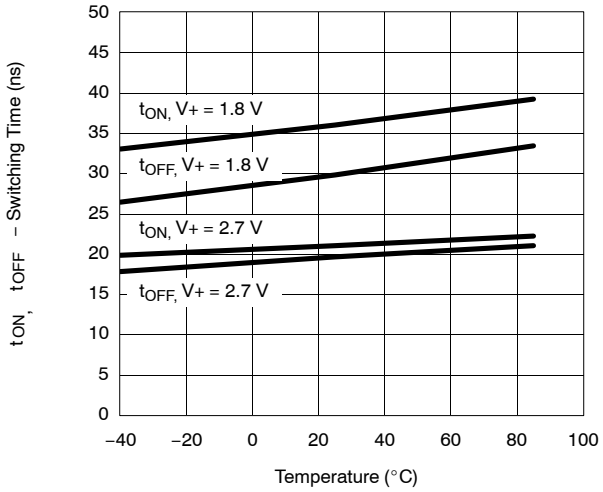


Leakage Current vs. Analog Voltage

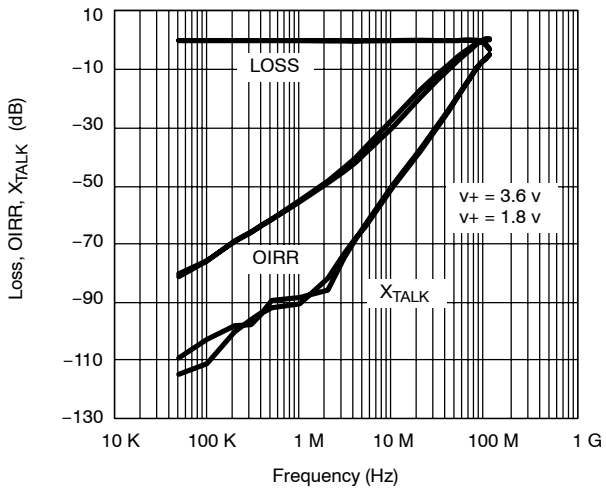


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

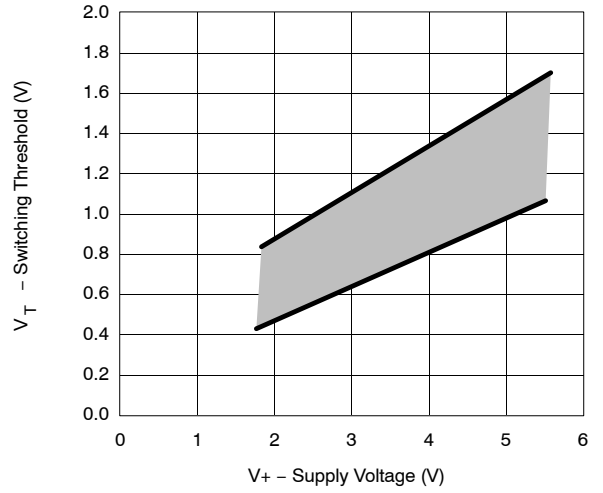
Switching Time vs. V_{CC} and Temperature



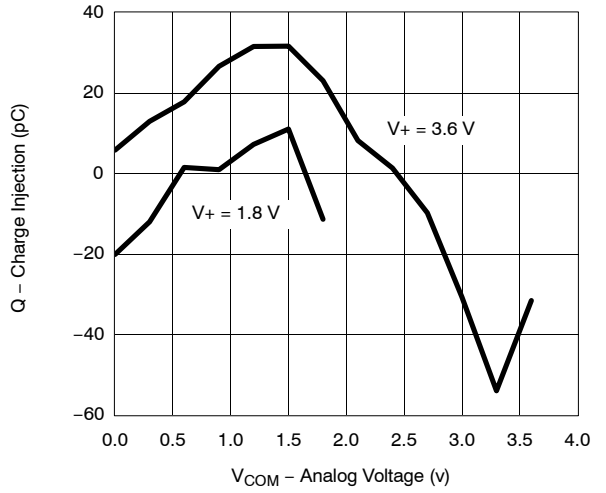
Insertion Loss, Off-Isolation, Crosstalk vs. Frequency



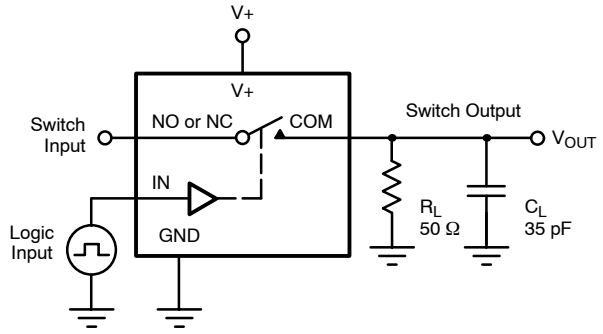
Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage

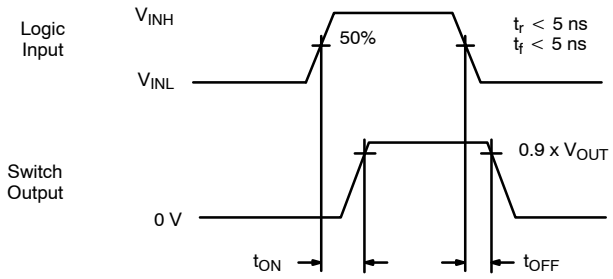


TEST CIRCUITS



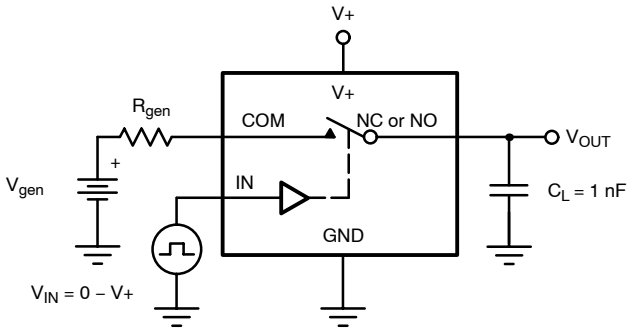
C_L (includes fixture and stray capacitance)

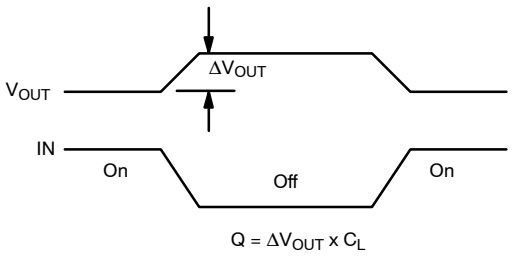
$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

FIGURE 1. Switching Time

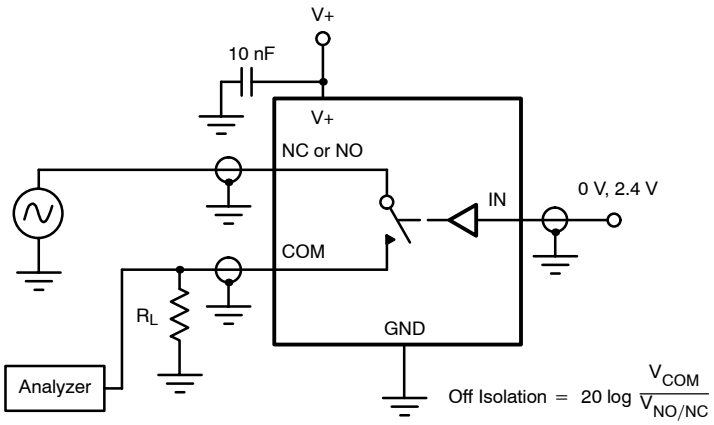




$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 2. Charge Injection



$$\text{Off Isolation} = 20 \log \frac{V_{COM}}{V_{NO/NC}}$$

FIGURE 3. Off-Isolation

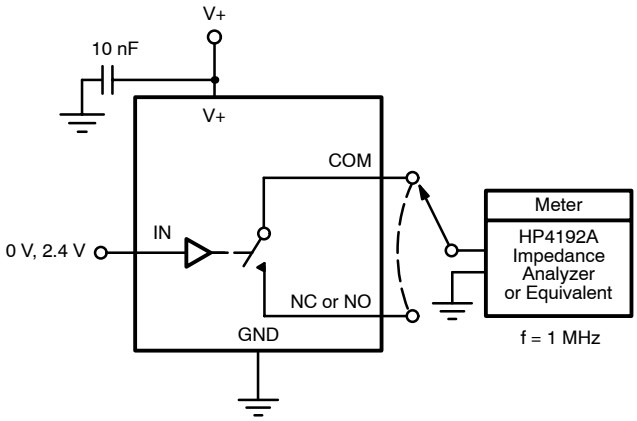


FIGURE 4. Channel Off/On Capacitance