SL2150F

Front End Power Splitter with AGC

Data Sheet

DS5535 Issue 2.1 April 2002

Features

- Single chip quadruple power splitter (primary channel, secondary channel, OOB channel and loop through)
- Wide dynamic range on all channels
- Independent AGC facility incorporated into all
- channel paths
- CSO, CTB, CXM all better than -62dBc for +3dBmV agc attack point
- Full ESD protection. (Normal ESD handling procedures should be observed)

Applications

- Multi-tuner cable set top box and cable modem applications
- Data communications systems
- Terrestrial TV tuner loop though

Ordering Information

SL2150F/KG/LH2S (tubes)

SL2150F/KG/LH2T (tape and reel)

Description

The SL2150F is a wide dynamic range single chip power splitter for cable set top box multi-tuner applications.

The device offers four buffered outputs from a single input.

All signal paths contain an independently controllable AGC facility.

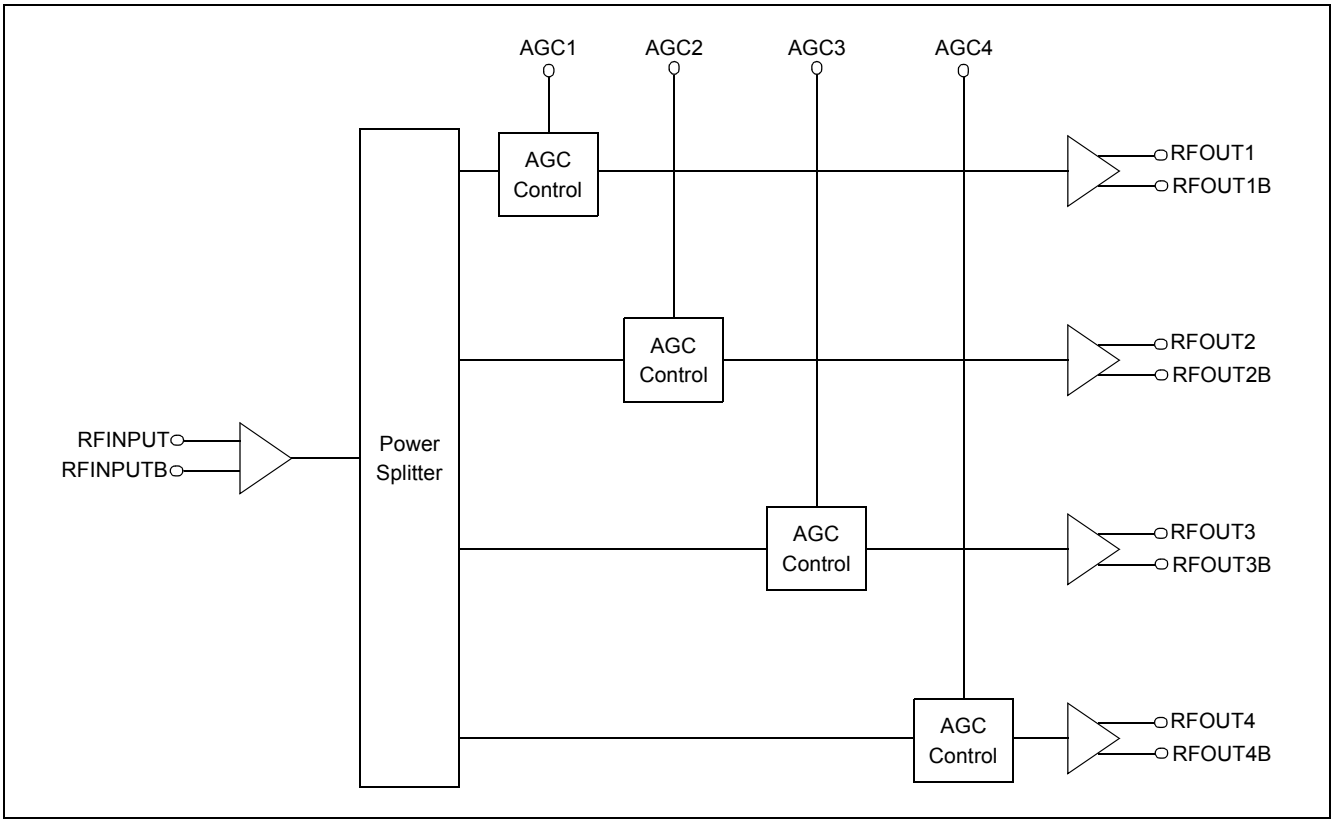


Figure 1 - SL2150F Block Diagram

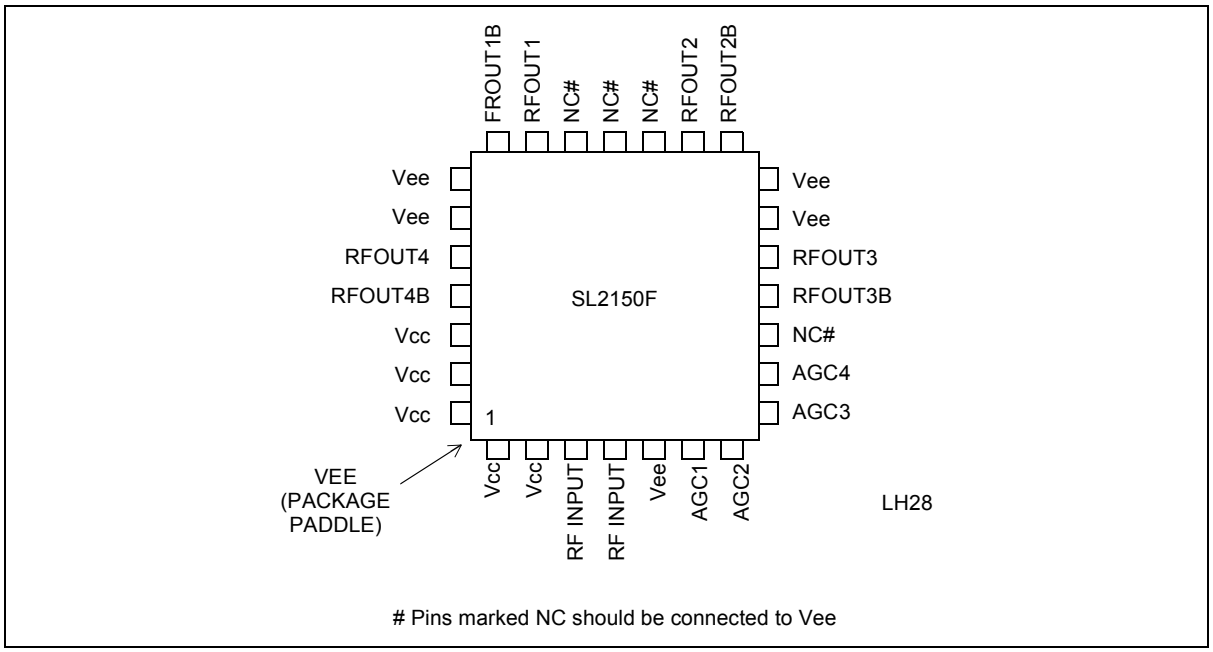


Figure 2 - Pin Allocation

1.0 Quick Reference Data

NB all data applies with differential termination and single ended source both of 75Ω.

Characteristics		Units
RF input operating range	50-860	MHz
Conversion gain, with external load as in Figure 12 maximum minimum	 5.5 -25	 dB dB
Input NF, all signal paths at maximum conversion gain	7	dB
IPIP3, all paths	127	dBµV
IPIP2, all paths	151	dBµV
CTB*	-66	dBc
CSO*	-64	dBc
CXM*	-66	dBc
Input impedance	75	Ω
Input VSWR	8	dB
Output impedance differential, all loops (requires external load for example as in Figure 12)	440	Ω
Input to output isolation (all loops)	30	dB
Output to output isolation (all loops)	25	dB

Table 1 - Quick Reference Data

*132 channel matrix at +15 dBmV per channel, 75 Ω source impedance, all paths, max gain.

2.0 Functional Description

The SL2150F is a broadband wide dynamic range power splitter with AGC and is optimized for application in multi tuner cable set top box applications. It also has application in any system where a wide dynamic range broadband power splitter is required.

The pin assignment is contained in Figure 2 and the block diagram in Figure 1. The port internal peripheral circuits are contained in Figure 15 - "Port Peripheral Circuitry".

In normal application the RF input is interfaced to the device input. The input preamplifier is designed for low noise figure, within the operating region of 50 to 860 MHz and for high intermodulation distortion intercept so offering good signal to noise plus composite distortion spurious performance when loaded with a multi carrier system. The preamplifier when combined with the input network shown in Figure 3 - "RF Input Matching Network" provides an impedance match to a 75Ω source. The typical impedance is shown in Figure 4 - "Typical Single-Ended RF Input Impedance with Input Match".

The input NF and input referred two-tone intermodulation test condition spectrum are shown in Figure 5 - "Input NF at 25 deg C" and Figure 6 - "Two Tone Intermodulation Test Condition Spectrum, Input Referred" respectively.

The output of the preamplifier is then power split to four independently controlled AGC stages.

Each AGC stage provides for a minimum of 30 dB of gain control across the input frequency range. The typical AGC characteristic and NF versus gain setting are contained in Figure 7 - "Typical AGC versus Control Voltage Characteristic" and Figure 8 - "Typical Variation in NF versus Gain Setting" respectively.

The input referred third order intercept point is independent of gain setting.

Finally, each of the AGC stages drive an output buffer of nominal differential output impedance of 440Ω, which provides a nominal 5.5 dB of conversion gain when terminated into a differential 75Ω load.

In application it is important to avoid saturation of the output stage, therefore it is recommended that the output standing current be sunk to Vcc through an inductor. A resistive pull up can also be used as shown in Figure 14 - "Example Application Driving 200 Ohm Load with Resistive Pull Up", however the resistor values should not exceed 38 ohm single ended.

If an inductive current sink is used the maximum available gain from the device is circa 20 dB. This gain can be reduced by application of an external load between the differential output ports. The gain can be approximately calculated from the following formula:

GAIN = 20*log ((Parallel combination of 440 ohm and external load between ports) / 44 ohm) + 2dB

For example, when driving a 200 ohm load as in Figure 13 - "Example Application Driving 200 Ohm Load with Inductive Pull Up", the gain equals

Gain = 20 *log ((440 * 200)/(440+200)/44) +2dB
= 12dB.

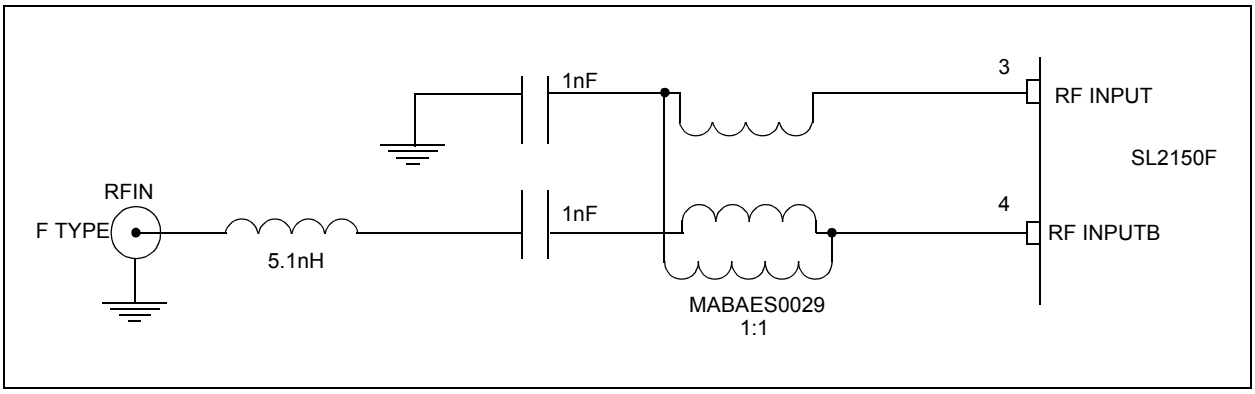


Figure 3 - RF Input Matching Network

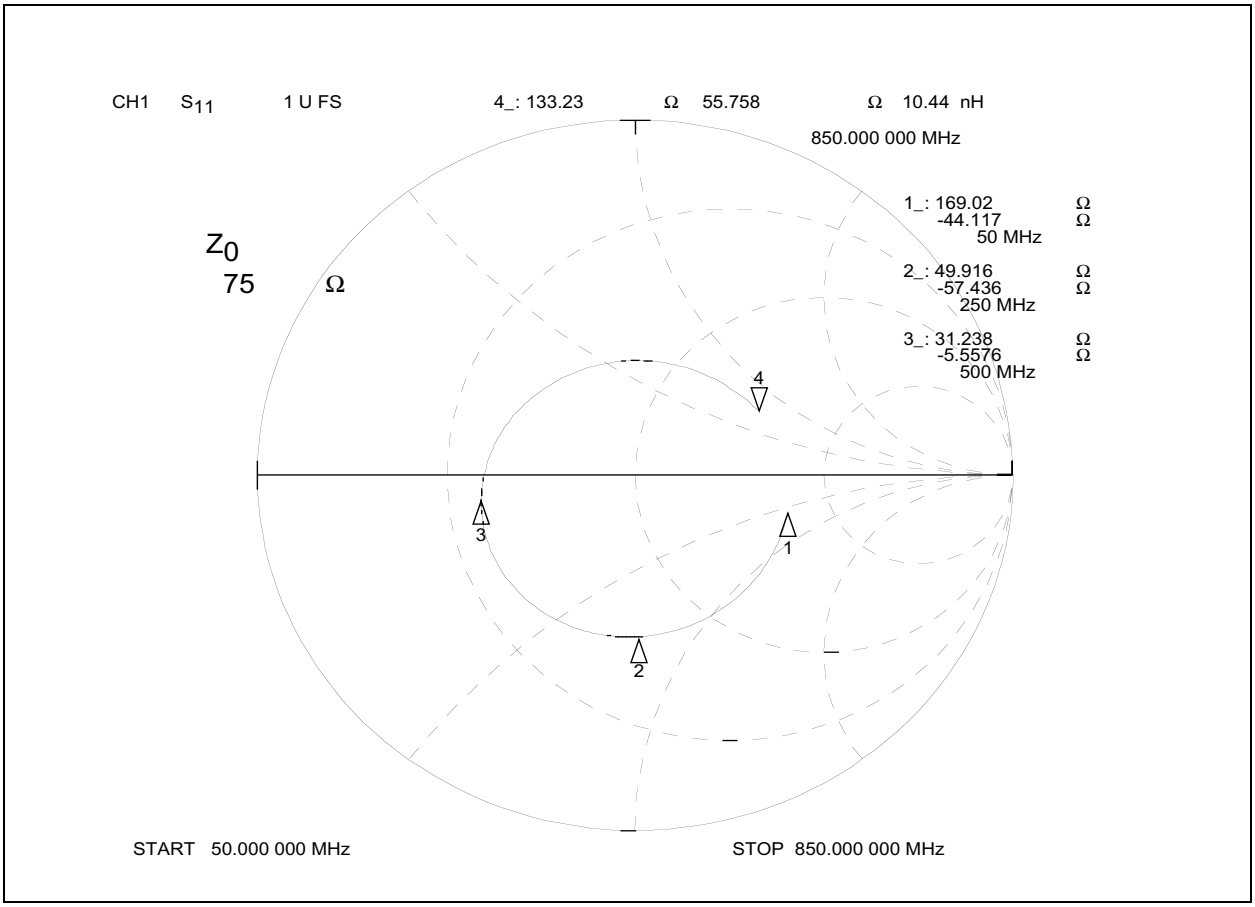


Figure 4 - Typical Single-Ended RF Input Impedance with Input Match

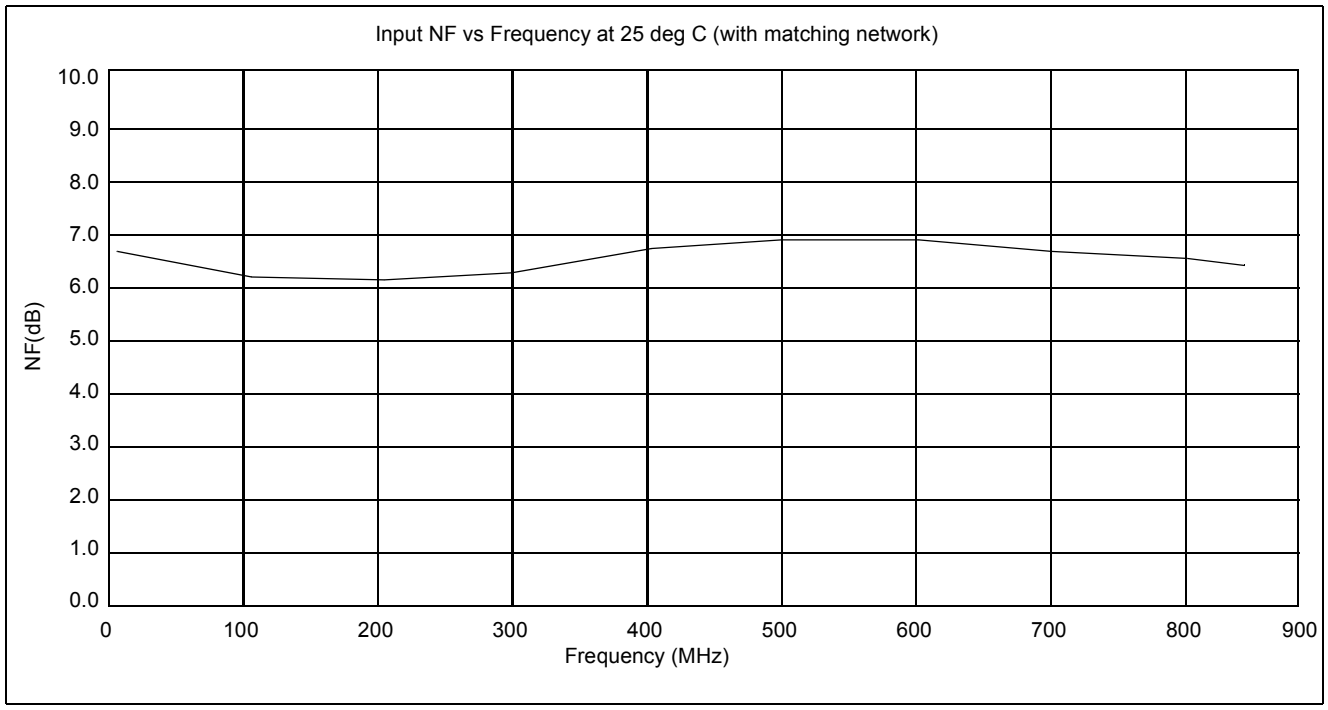


Figure 5 - Input NF at 25 deg C

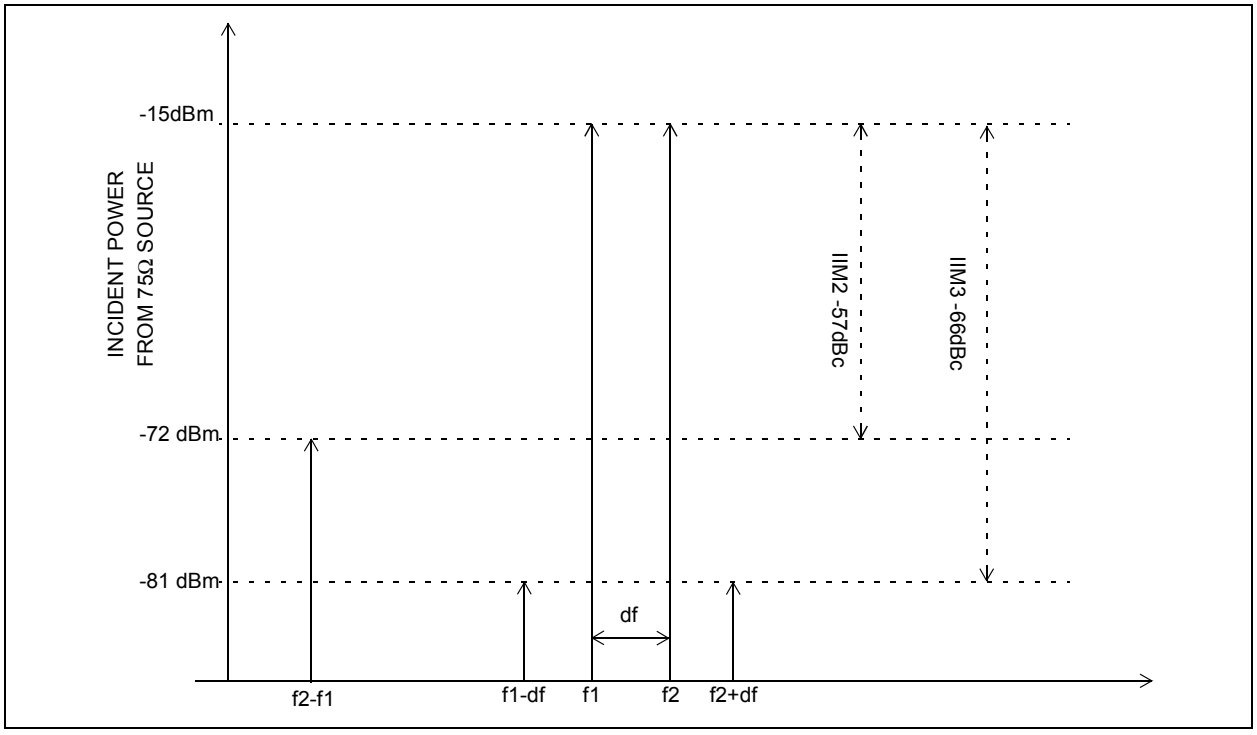


Figure 6 - Two Tone Intermodulation Test Condition Spectrum, Input Referred

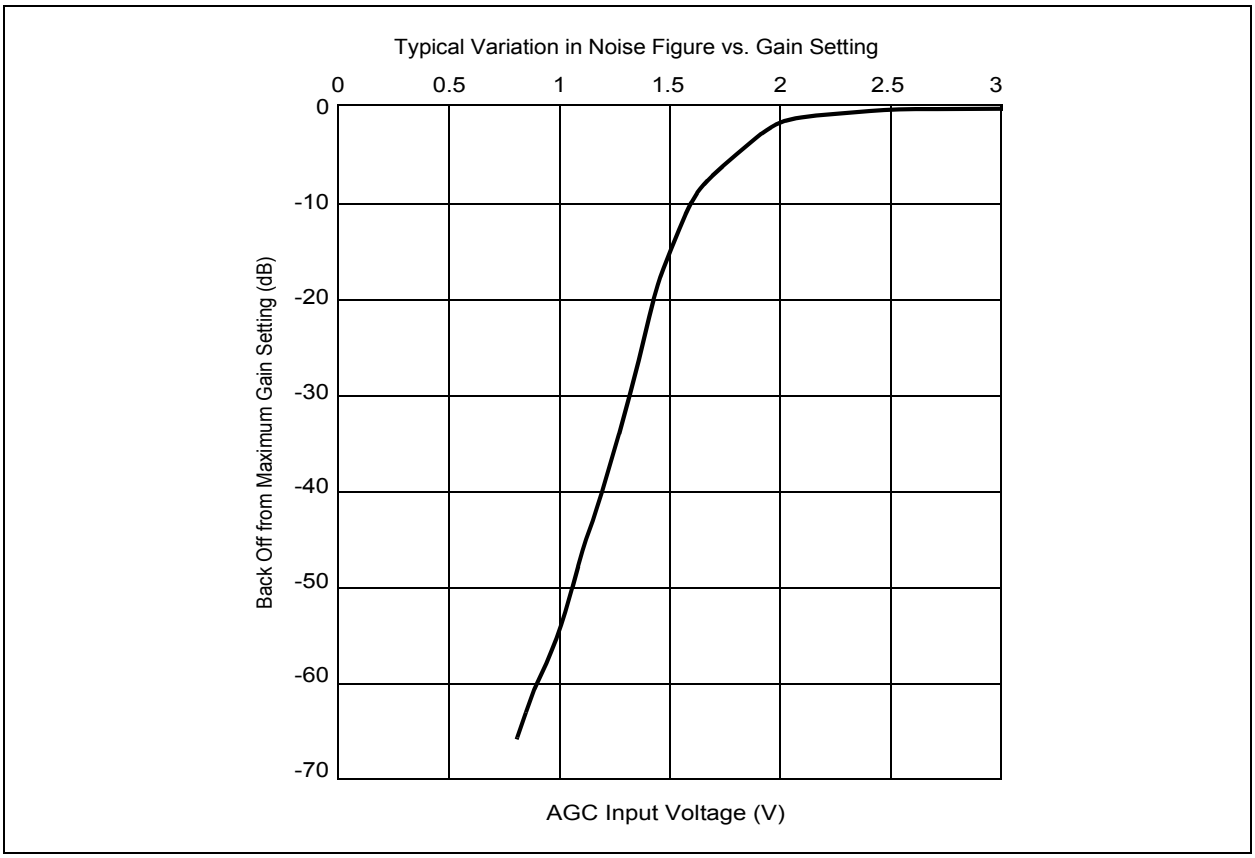


Figure 7 - Typical AGC versus Control Voltage Characteristic

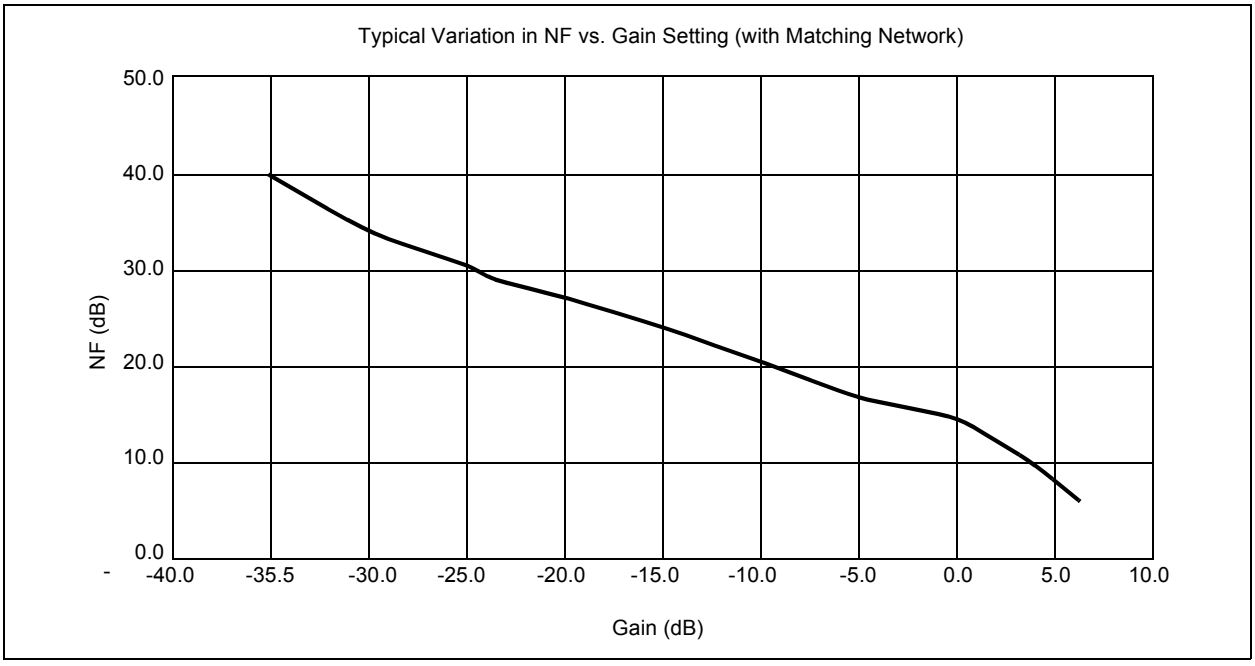


Figure 8 - Typical Variation in NF versus Gain Setting

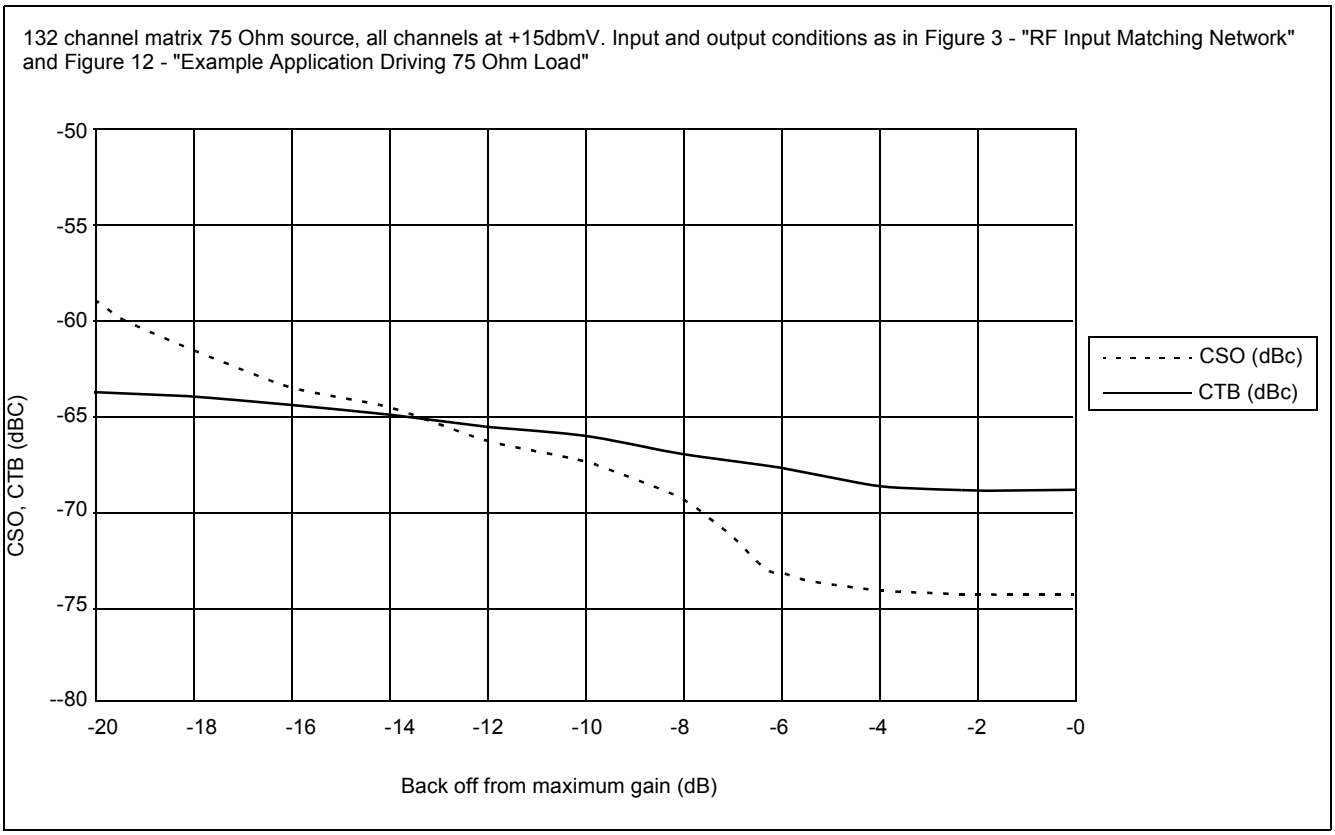


Figure 9 - Typical Variation in CSO and CTB versus Back Off from Maximum Gain

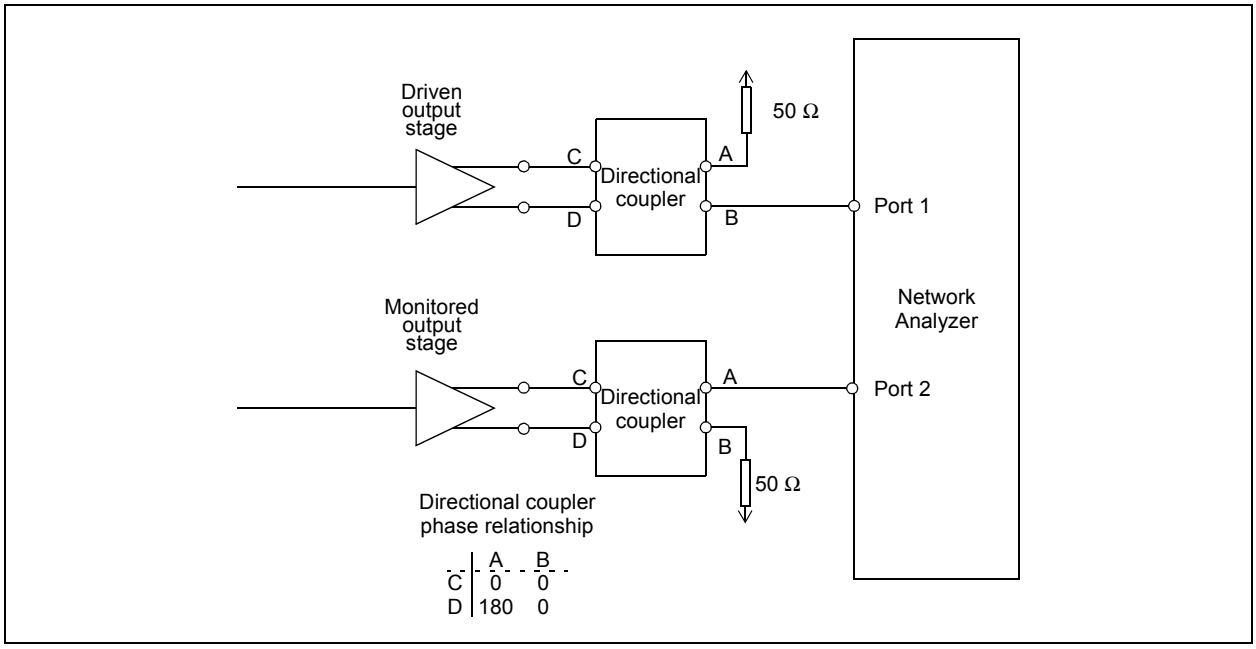


Figure 10 - Test Condition for Output Crosstalk

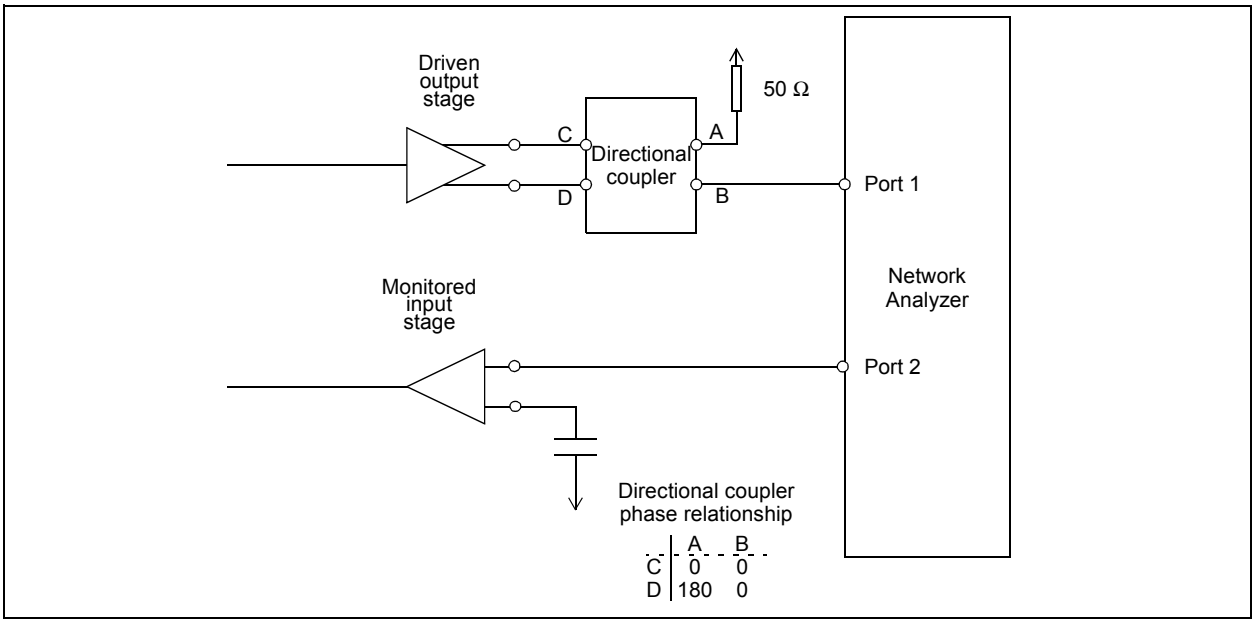


Figure 11 - Test Condition for Output to Input Crosstalk

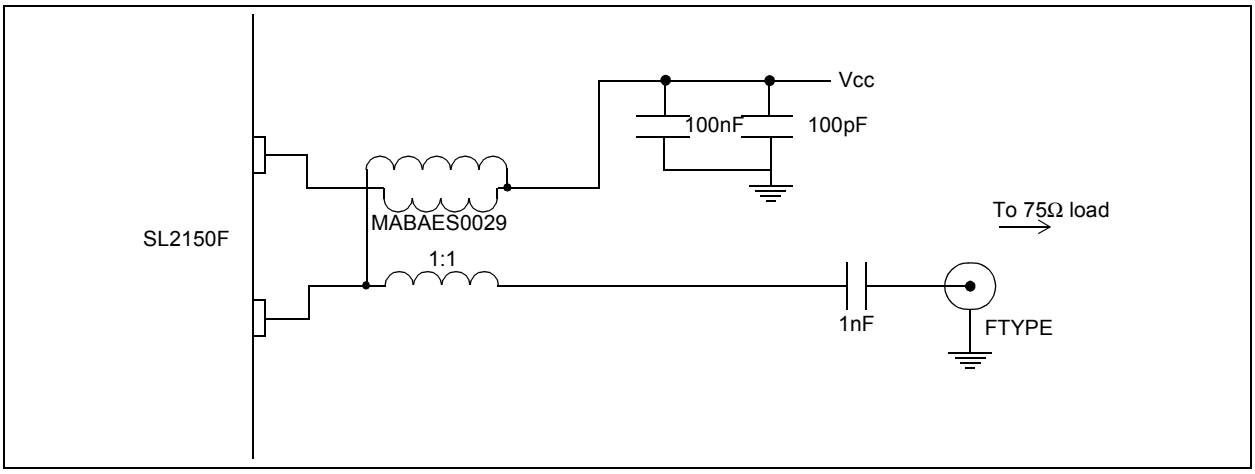


Figure 12 - Example Application Driving 75 Ohm Load

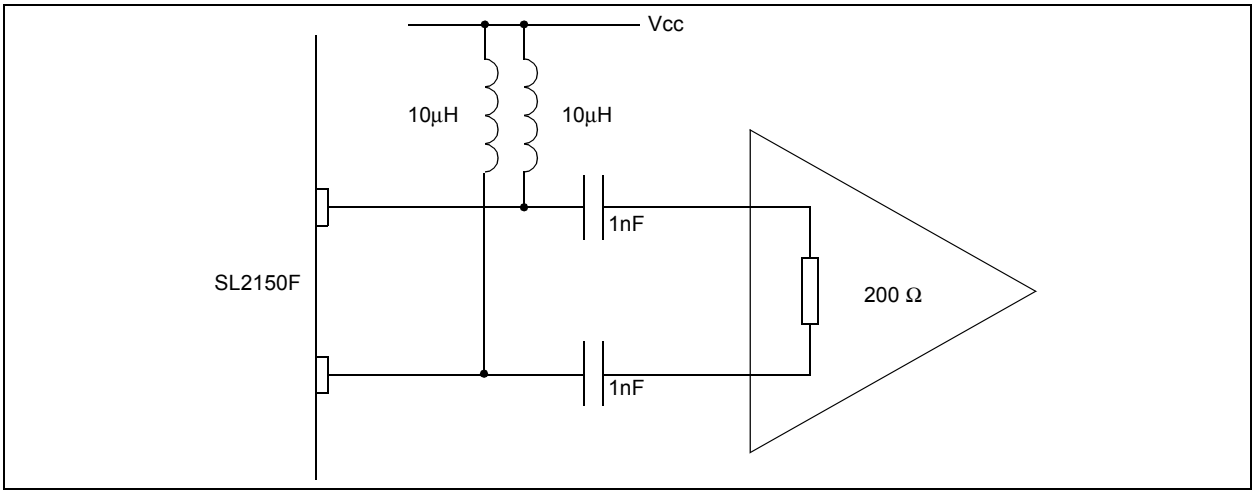


Figure 13 - Example Application Driving 200 Ohm Load with Inductive Pull Up

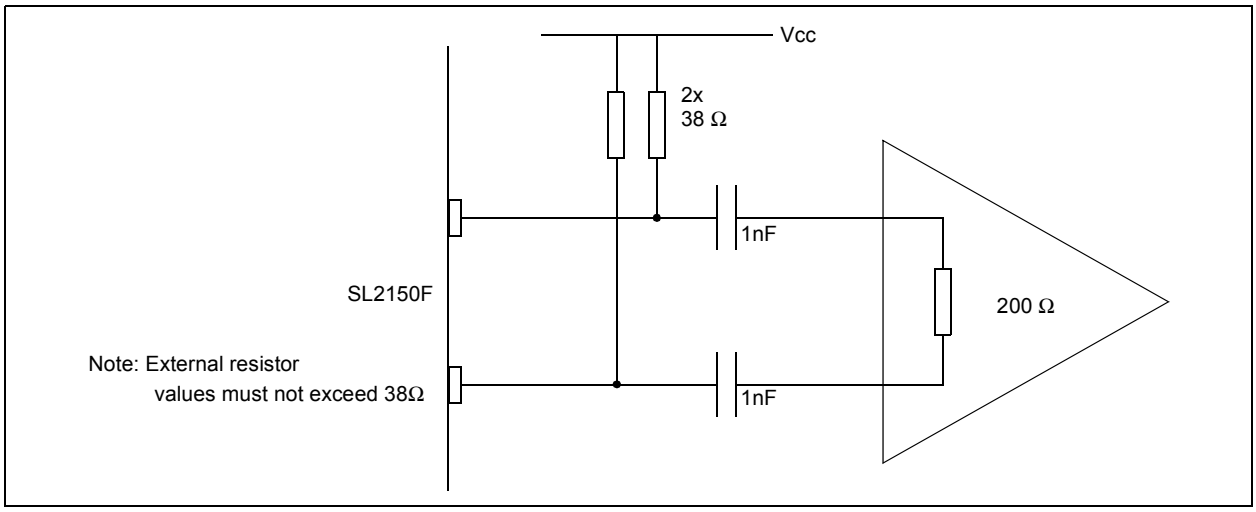


Figure 14 - Example Application Driving 200 Ohm Load with Resistive Pull Up

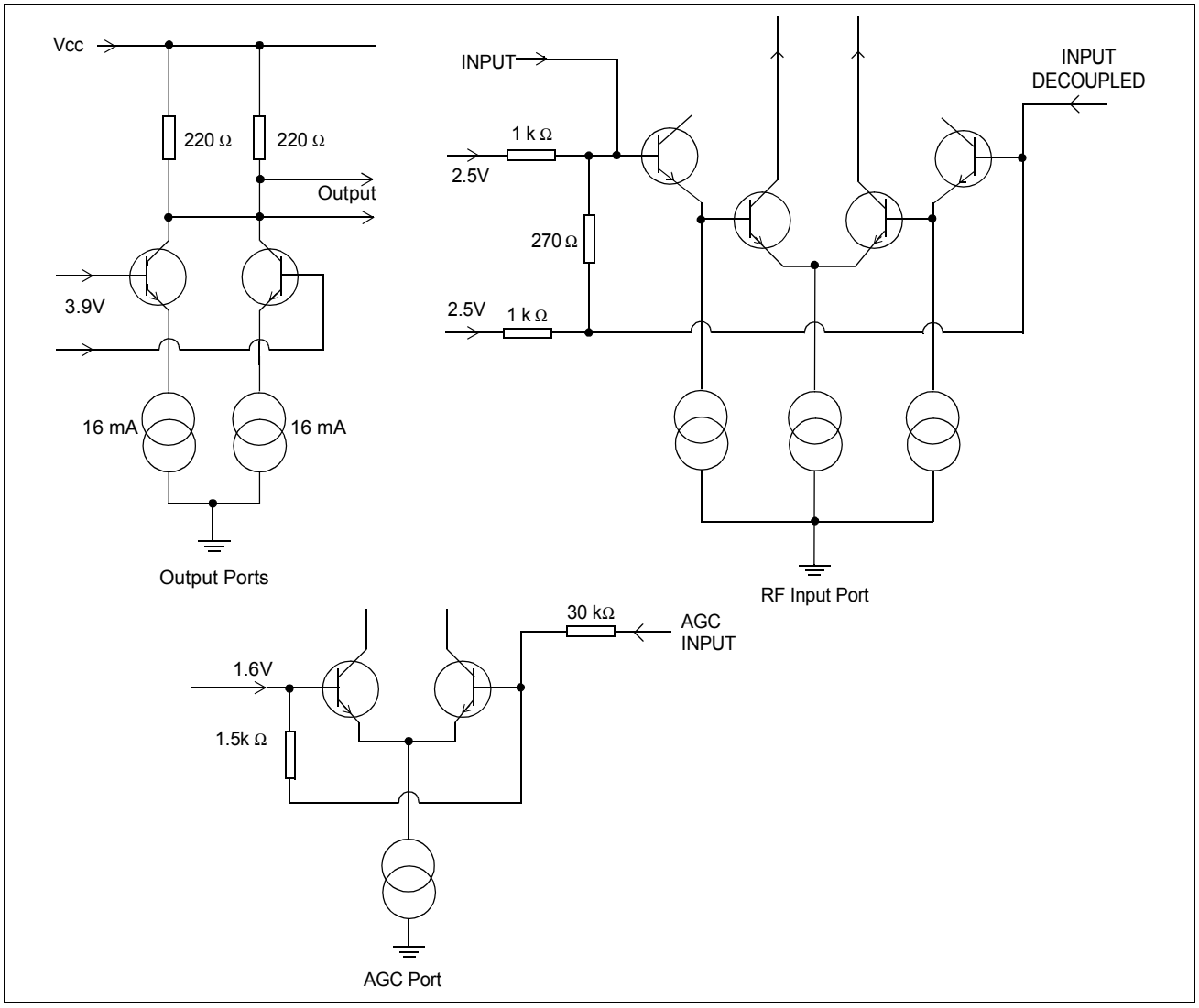


Figure 15 - Port Peripheral Circuitry

3.0 Electrical Characteristics

Test conditions (unless otherwise stated)

T amb = -40^{o} to 85^{o} C, Vee=0V, Vcc=5V+-5%.

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Electrical Characteristics

Characteristic	pin	min	typ	max	units	Conditions
Supply current			190	228	mA	
Input frequency range		50		860	MHz	
Input impedance	3, 4		75		Ω	See Figure 4
Input return loss			8		dB	
Input Noise Figure				8	dB	Tamb=27^{0}C, see Figure 8 All loops at maximum conversion gain
Variation in NF with gain adjust				-1	dB/dB	See Figure 4
Gain maximum minimum minimum		4	5.5 -65	7 -25	dB dB dB	Power gain from 75 Ω single ended source to differential 75 Ω load. Vagcip=3.0V Vagcip=0.5V Vagcip=Vee AGC monotonic from Vee to Vcc. Refer to Functional description section for information on calculating maximum gain with other load conditions
Input referred IP2		42			dBm	Assuming ideal power match. See note 2 and Figure 6.
Input referred IP3		18			dBm	Assuming ideal power match. See note 2 and Figure 6.
Input referred IM2				-57 -37	dBc dBc	See note 2 and Figure 6. See note 3 and Figure 6.

Electrical Characteristics (continued)

Characteristic	pin	min	typ	max	units	Conditions
Input referred IM3				-66 -46	dBc dBc	See note 2 and Figure 6. See note 3 and Figure 6. All gain settings
CSO				-62	dBc	See note 4 and Figure 9.
CTB				-64	dBc	See note 4.
CXM				-64	dBc	See note 4.
Input P1dB			+4.5		dBm	All gain settings, with load as in Figure 12 - "Example Application Driving 75 Ohm Load"
Gain variation within channel			0.25		dB	Channel bandwidth 8 MHz within operating frequency range, all loops, all gain settings
Output impedance	11,12, 15,16 20,21 24,25		440		Ω	Differential
Output port DC standing current	11,12, 15,16 20,21 24,25			25	mA	Standing current that any external load has to sustain.
AGC input leakage current	6,7 8,9	-150		150	µA	Vagcip =Vee to Vcc, all control inputs.
Crosstalk between all loop outputs				-25	dB	All gain settings, measured differential output to differential output, driven ports in phase and monitored ports out of phase, see Figure 10 - "Test Condition for Output Crosstalk".
Crosstalk between outputs and RF input				-30	dB	All gain settings, measured differential output to single ended input, driven ports in phase, see Figure 11 - "Test Condition for Output to Input Crosstalk"

Note 1: All power levels are referred to 75Ω and 0 dBm = 109 dBµV.
Note 2: Any two tones within RF operating range at -15 dBm, from single-ended 75 ohm source into differential 75Ω load as in Figure 12 - "Example Application Driving 75 Ohm Load", gain setting between maximum and -15dB backoff.
Note 3: Any two tones within RF operating range at -5 dBm, from single-ended 75 ohm source into differential 75Ω load as in Figure 12 - "Example Application Driving 75 Ohm Load".
Note 4: Load as in Figure 12 - "Example Application Driving 75 Ohm Load" and Figure 13 - "Example Application Driving 200 Ohm Load with Inductive Pull Up", max gain, 132 channel matrix, 75 ohm source with all channels at +15 dBmV, assuming power match.

Absolute Maximum Ratings All voltages are referred to Vee at 0V

Characteristic	min	max	units	Conditions
Supply voltage	-0.3	6	V	
RF input voltage		8	dBm	Differential
All I/O port DC offsets	-0.3	Vcc+0.3	V	
Storage temperature	-55	150	^{o}C	
Junction temperature		125	^{o}C	Power applied
Package thermal resistance, chip to ambient		35	^{o}C/W	Paddle to be soldered to ground plane
Power consumption at 5.25V		1200	mW	
ESD protection	1.5		kV	Mil-std 883B method 3015 cat1

4.0 SL2150F Demonstration Board

The SL2150F demonstration board is designed to allow testing of device functionality as a stand alone power splitter. It allows for testing of the AGC function and independent testing of all channels.

The SL2150F is designed to interface differentially into a silicon tuner such as the SL2101 with simple inductive or resistive pull-ups. However, to facilitate testing the differential, output is converted to a single ended signal through a balun. The differential conversion is necessary for achieving second order performance.

All outputs require a DC return path to Vcc to prevent output saturation. This can be provided by the balun, inductive pull up or resistive pull up. In the case of a resistive pull up, the maximum load value is 38 Ω.

The balun also provides the DC bias to the outputs; all outputs have to be DC 'shorted' to Vcc to prevent saturation of the output stages.

All input and output terminations are 75 Ω.

The board schematic and layout are contained in Figure 19 - "Test Board Schematic" and Figure 20 - "Test Board Layout" respectively.

Operation note

The supply voltage must be connected and enabled before any AGC voltage is applied unless the AGC supplies are current limited to <1 mA or else permanent damage may occur through the ESD structures on the device.

4.1 Pin Connections

All references are with the board oriented as in bottom view on Figure 1 - "SL2150F Block Diagram". Pin 1 of the header is defined as the left-hand pin.

4.2 Power Supply

A single 5V supply is required. Power is supplied through the two-pin header PL1, located top right hand corner.

Pin	Function
1	Vcc
2	Vee

4.3 RF Input

The RF input F type, SK1, is located on the right hand side of the board.

4.4 RF Outputs

Output 1 is the upper of the two F type connectors, SK3, located on the left-hand side.

Output 2 is the lower of the two F type connector, SK4, located on the left-hand side.

Output 3 is the F type connector, SK5, located at the bottom of the board

Output 4 is the F type connector, SK2, located at the top of the board.

4.5 AGC Control

All AGCs are connected through the 5-pin header, PL2, located in the bottom right hand corner. See note on connection of supplies in the power supply section.

Pin allocation is as follows:

Pin	Function
1	Vagc1
2	Vagc 2
3	Vagc 3
4	Vagc 4
5	Vee

AGC control voltage is Vee to 3V for minimum to maximum gain setting.

4.6 Test Procedure

4.6.1 CSO

CSO is tested using an RDL matrix generator set to deliver all channels from 55.25 MHz to 859.25 MHz at 15 dBmV per carrier.

Each output is tested independently over maximum gain setting through 15 dB of gain reduction.

The output intermodulation is monitored on a spectrum analyzer with video bandwidth of 1 kHz and resolution bandwidth of 10 kHz. To avoid intermodulation in the test set up the output channel is filtered through a narrow band filter and then amplified to compensate for insertion loss. The higher of all CSO beats is recorded.

Under gain reduction the amplitude is normalized to channel 2 output at the required AGC onset

4.6.2 CTB

CTB is tested using an RDL matrix generator set to deliver all channels from 55.25 MHz to 859.25 MHz at 15 dBmV per carrier.

Each output is tested independently over maximum gain setting through 15 dB of gain reduction.

The output intermodulation is monitored on a spectrum analyzer with video bandwidth of 1 kHz and resolution bandwidth of 10 kHz. To minimize intermodulation in the test set up the output channel is filtered through a narrow band filter and then amplified to compensate for insertion loss.

CTB is measured with N+-1 also disabled since these channels were found to produce intermodulation in the filter and the post amplifier.

Under gain reduction the amplitude is normalized to channel 2 output at the required AGC onset.

4.6.3 CXM

CTB is tested using an RDL matrix generator set to deliver all channels from 55.25 MHz to 859.25 MHz at 15 dBmV per carrier with 100% modulation at line rate.

Each output is tested independently over maximum gain setting through 15 dB of gain reduction.

To minimize crossmodulation in the test set up the output channel is filtered through a narrow band filter and then amplified to compensate for insertion loss. The amplifier output is then demodulated on a first spectrum analyzer set to linear mode with maximum resolution and video bandwidth. The video out of the first spectrum analyzer, which will be the demodulated AM on the carrier, is connected to a second spectrum analyzer centred on line rate frequency with video averaging enabled. The cross modulation can then be monitored on the second spectrum analyzer.

The CXM is measured with modulation disabled on N+-1 since these channels were found to produce crossmodulation in the filter and the post amplifier.

Under gain reduction the amplitude is normalized to channel 2 output at the required AGC onset.

4.6.4 Gain

Gain is measured using a network analyzer with 50/75 Ω pads to ensure correct source and load impedance.

4.6.5 AGC

Output amplitude at a given channel is measured on a spectrum analyzer with all AGC settings from 0V to Vcc.

4.6.6 S11

S11 is measured at the test board RF input F type connector, using a network analyzer calibrated to 75Ω F type connector.

4.6.7 S22

S22 is not measured since the device is not designed to be impedance matched on its output. Rather the output load is used as the terminating impedance for the device.

4.6.8 NF

NF is measured using a NF meter with a 50/75Ω pad on the input.

4.7 Typical performance characteristics

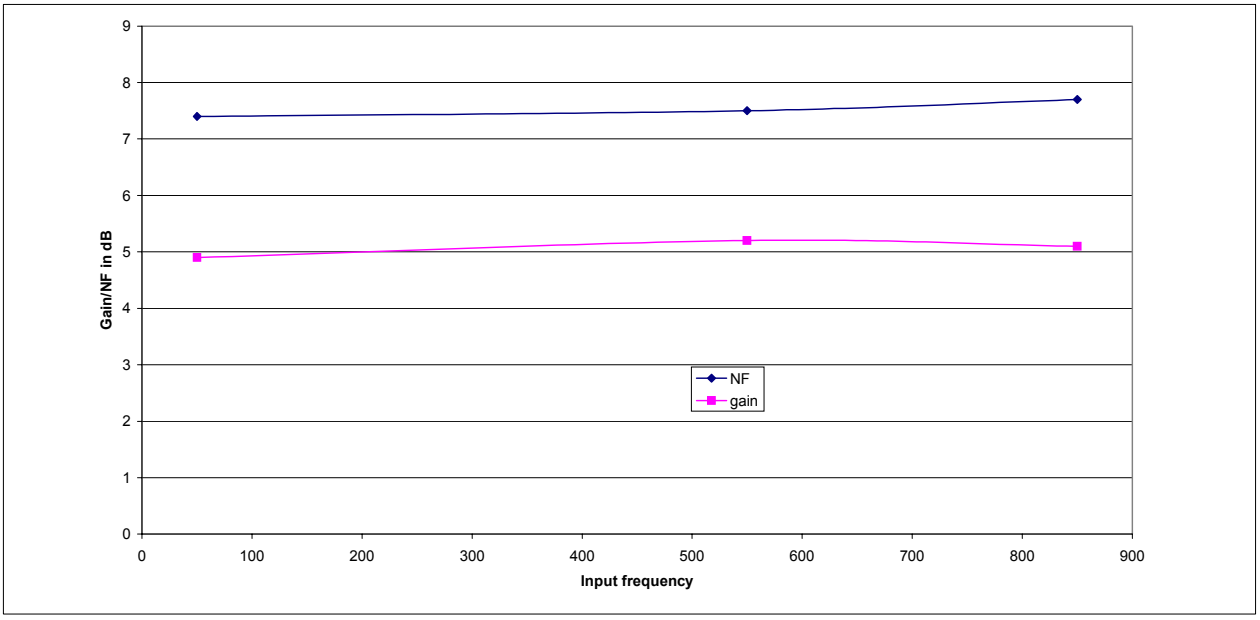


Figure 16 - SL2150F NF and Gain at Maximum Gain Setting

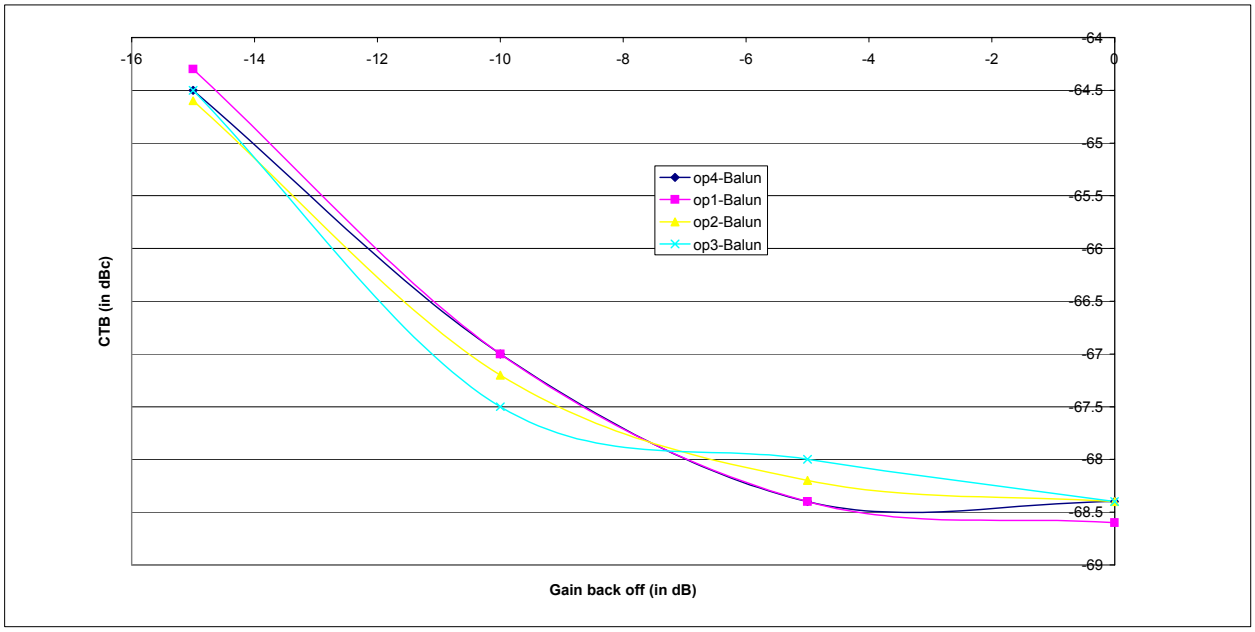


Figure 17 - SL2150F CTB at 505.25 MHz Measured with 15dBmV per Carrier

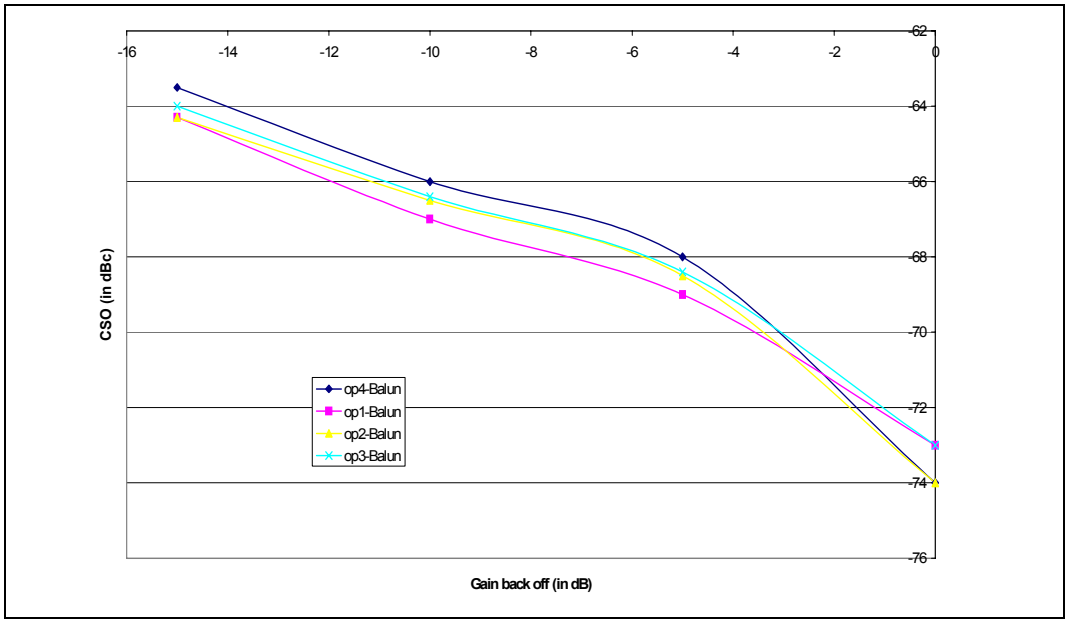


Figure 18 - SL2150F CSO at 859.25 MHz Measured with 15 dBmV per Carrier

4.8 Evaluation Board

Figure 19 - "Test Board Schematic" and Figure 20 - "Test Board Layout" show schematic and PCB layout for a 4 layer evaluation board.

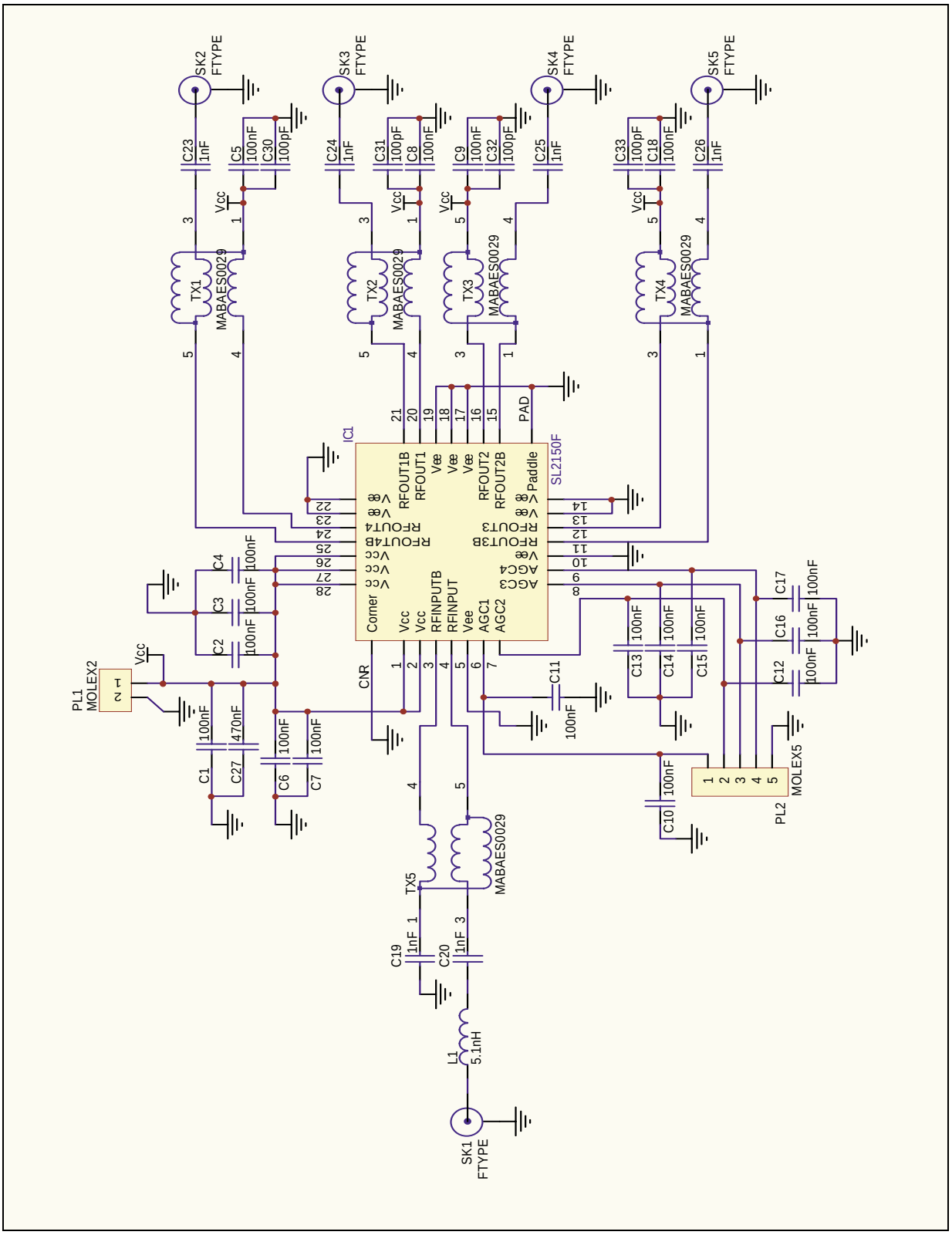


Figure 19 - Test Board Schematic

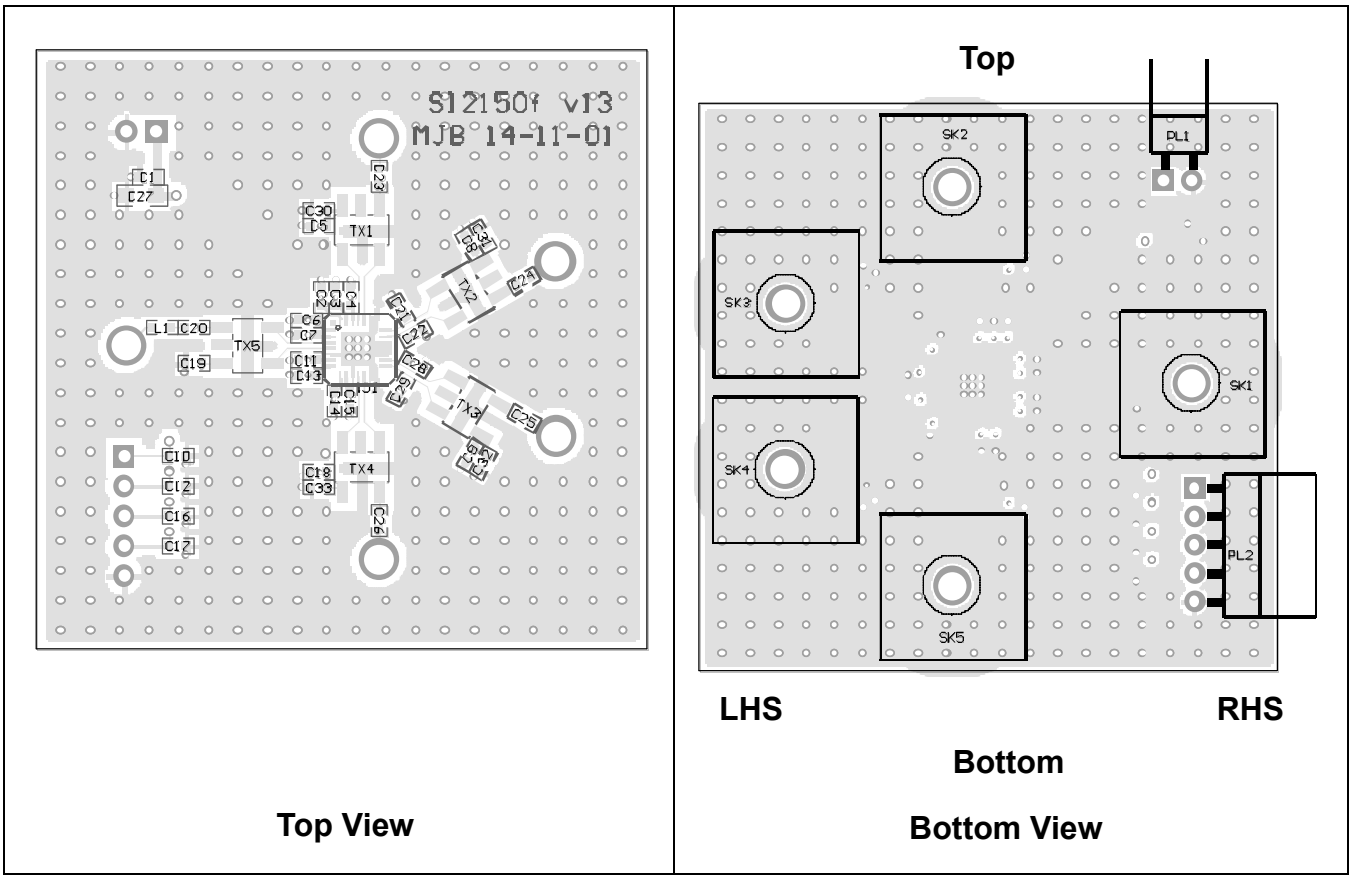
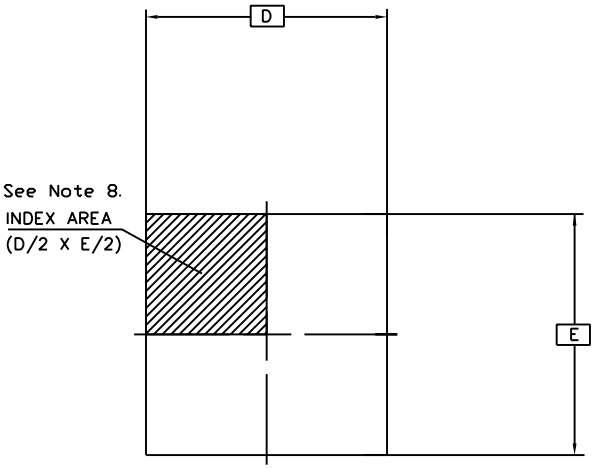
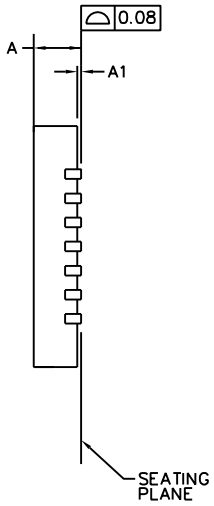
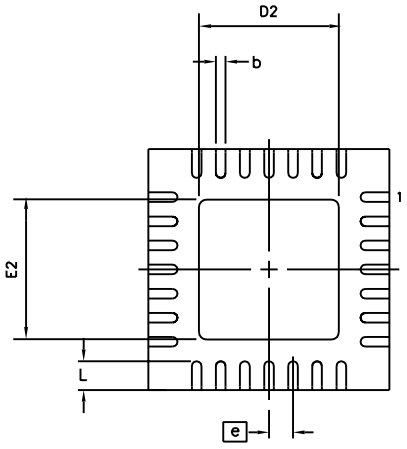


Figure 20 - Test Board Layout



TOP VIEW





BOTTOM VIEW

SYMBOL	COMMON DIMENSIONS	
	MIN.	MAX.
A	–	1.00
A1	0.00	0.05
b	0.18	0.30
D	5.00 BSC	
D2	3.00	3.25
E	5.00 BSC	
E2	3.00	3.25
N	28	
Nd	7	
Ne	7	
e	0.50 BSC	
L	0.35	0.75

Conforms to JEDEC MO-220 VHHD-1 iss A

NOTES:
1. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd & Ne ARE THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. ALL DIMENSIONS ARE IN MILLIMETERS.
5. LEAD COUNT IS 28 .
6. PACKAGE WARPAGE MAX 0.08mm.
7. NOT TO SCALE.
8. TERMINAL #1 IDENTIFIER MUST BE LOCATED WITHIN THE ZONE INDICATED AND MAY BE EITHER A MOULD OR MARKED FEATURE.

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