TIMESTREAM® PRODUCT FAMILY

VSC9180

VITESSE

VSC9180 Arapahee - 2.5G SONET/SDH Backplane Transceiver

FEATURES:

Parallel to Serial Transmit

- Receives 16 or 4-Bit Parallel LVDS/LVPECL Inputs Operating at 155MHz or 622MHz into Internal FIFO using Source Synchronous Timing
- 16-Bit 155MHz Bus or 4-Bit 622MHz Bus is Bit Multiplexed to Serial 2.5GHz Output
- Retimes Four Serial STS-12/STM-4 Inputs and Deskews up to +/- 3 Bytes of Skew using the A1/A2 Boundaries
- Byte Interleaves Four Serial STS-12/STM-4 Inputs to Create an STS-48 like Signal
- Clear Channel Non-SONET/SDH Capability and Support for Both SONET/SDH and G.709 OTU1 Frames

Serial to Parallel Receive

- Dual 2.5Gb/s Frequency Synchronous Serial CML Inputs with Onboard Clock and Data Recovery
- Onboard Frame Alignment of Received Signals and Large Internal FIFO for Tolerance of up to +/-75ns of Serial Backplane Skew
- Realignment of Incoming Signals Allows Hitless Selection of Incoming Channel for Maintenance Purposes, and Prevents Downstream Devices from Having to Reframe in a Failure Condition
- Hardware Based Switch Over within Receipt of Two or Four Errored Frame Boundaries
- Loss of Signal, Loss of Alignment, and Loss of Frame Alarm Indication
- Received Frame Pointer Output
- Programmable BER Threshold Monitors Based on B1 Parity Monitoring of Both Serial Inputs
- Returns 16 or 4-Bit Parallel LVDS Bit De-multiplexed Outputs Operating at 155MHz or 622MHz with Recovered Bus Clock (Non Interleave Mode)
- Returns Quad STS-12/STM-4 Outputs Operating at 622 Mb/s (Interleave Mode)
- Clear Channel Non-SONET/SDH Capability and Support for Both SONET/SDH and G.709 OTU1 Frames

Special Features

- 4-Bit or 16-Bit Parallel Bus Loopback with Output Bus Clock
- Parallel Loopback also Allows Quad STS-12/STM-4 Retime, Realign, and Loopback Output
- Serial Loopback with Hitless Input Selection and Realignment
- Onboard Discrete CMU and CRU to Accommodate Non-synchronous TX/RX Applications

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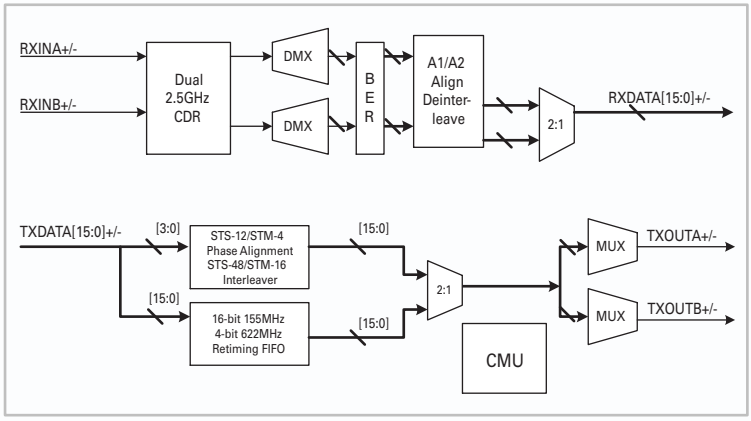
GENERAL DESCRIPTION:

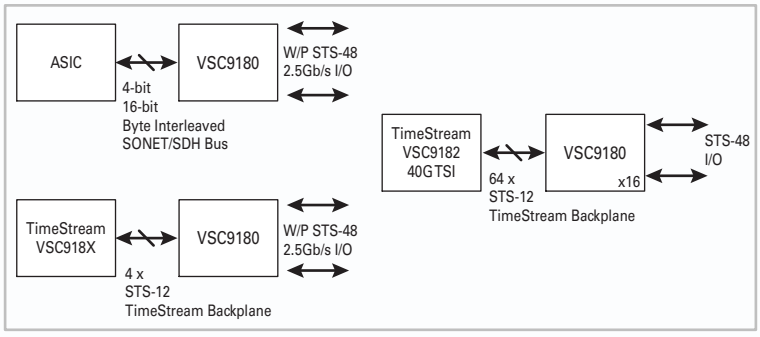
The VSC9180 is a multi-rate SONET/SDH transceiver with support for working and protection hitless backplane 1+1 protection. It is designed to serialize four STS-12/STM-4 signals, or byte interleaved SONET/SDH data from 4-bit 622MHz or 16-bit 155MHz parallel buses onto redundant 2.5Gb/s serial backplane outputs. It also receives two synchronous and serial STS-48/STM-16 signals, recovers the clock, deskews them and then allows hitless selection between the two. Selection criteria can be derived from BER monitoring, in-frame status or signal integrity monitoring. The selected signal is deserialized to a 4-bit 622MHz bus, a 16-bit 155MHz bus or quad STS-12's operating at 622Mb/s.

The VSC9180 can serialize a 4-bit or 16-bit byte interleaved STS-48/STM-16 bus to working and protection 2.5Gb/s I/O (Non Interleave mode). Alternatively it can recover four serial STS-12 backplane signals, re-align them, and interleave them to form a serial STS-48 signal (Interleave mode). Interleave mode allows the VSC9180 to be used to add 2.5Gb/s backplane connectivity to the VSC9182 40G STS-1 TSI switch, or act as a transponder between existing serial STS-48/STM-16 signals to serial STS-12/STM-4 backplane architectures. TOH transparency is preserved and B1 parity is intelligently recalculated for compatibility with the backplane BER monitoring of adjacent devices.

VSC9180 BLOCK DIAGRAM:



VSC9180 ARCHITECTURES:



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