

**W83176R-735**

**W83176G-735**

**Winbond 3 DIMM DDR ZERO  
DELAY BUFFER**

Date: Mar/31/2006    Revision: 1.1

# W83176R-735/W83176G-735



## 3 DIMM DDR ZERO DELAY BUFFER FOR SIS CHIPSET

### W83176R-735/W83176G-735 Data Sheet Revision History

	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1	n.a.			n.a.	All of the versions before 0.50 are for internal use.
2	3.7	12/18/03	0.5	n.a.	Correction IC version, add register default value and correction some description and default value
3		05/03/04	1.0	1.0	Update to web
4		03/31/06	1.1	1.1	Add lead-free part number W83176G-735
5					
6					
7					
8					
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10					

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## 3 DIMM DDR ZERO DELAY BUFFER FOR SIS CHIPSET

### Table of Contents-

1.	GENERAL DESCRIPTION .....	1
2.	PRODUCT FEATURES .....	1
3.	PIN CONFIGURATION .....	1
3.1	Block diagram .....	2
4.	PIN DESCRIPTION.....	3
4.1	Clock Outputs .....	3
4.2	Power Pins.....	3
5.	REGISTER 0 ~ REGISTER 4 RESERVED.....	4
5.1	Register 5 : Output Control ( 1 = Active, 0 = Inactive ) (Default =FFH).....	4
5.2	Register 6 : Output Control ( 1 = Active, 0 = Inactive ) (Default =FFH).....	4
6.	ACCESS INTERFACE .....	5
6.1	Block Write protocol.....	5
6.2	Block Read protocol.....	5
6.3	Byte Write protocol .....	5
6.4	Byte Read protocol .....	5
7.	SPECIFICATIONS .....	6
7.1	ABSOLUTE MAXIMUM RATINGS .....	6
7.2	AC CHARACTERISTICS .....	6
7.3	DC CHARACTERISTICS.....	7
8.	ORDERING INFORMATION .....	8
9.	HOW TO READ THE TOP MARKING.....	8
10.	PACKAGE DRAWING AND DIMENSIONS.....	9

# W83176R-735/W83176G-735



## 3 DIMM DDR ZERO DELAY BUFFER FOR SIS CHIPSET

### 1. GENERAL DESCRIPTION

The W83176R-735 is a 2.5V Zero-delay D.D.R. Clock buffer designed for SiS system. W83176R-735 can support 3 D.D.R. DRAM DIMMs.

The W83176R-735 provides I<sup>2</sup>C serial bus interface to program the registers to enable or disable each clock outputs. The W83176R-735 accepts a reference clock as its input and runs on 2.5V supply.

### 2. PRODUCT FEATURES

- Zero-delay clock outputs
- Feedback pins for synchronous
- Supports up to 3 D.D.R. DIMMs
- One pairs of additional outputs for feedback
- Low Skew outputs (< 100ps)
- Supports 400MHz D.D.R. SDRAM
- I<sup>2</sup>C 2-Wire serial interface and supports Byte or Block Date RW
- 48-pin SSOP package

### 3. PIN CONFIGURATION

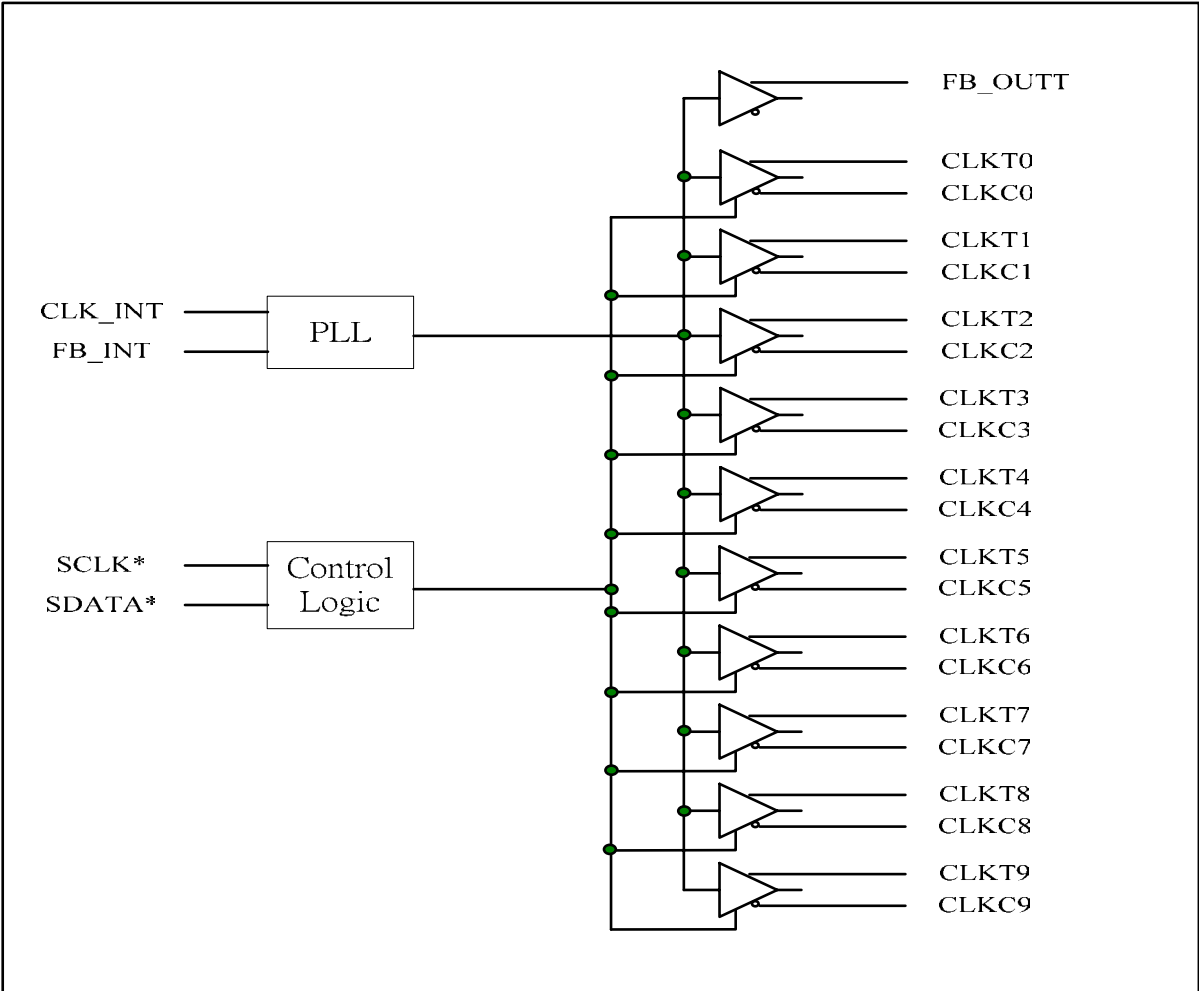
G N D	1	4 8	G N D
C L K C 0	2	4 7	C L K C 5
C L K T 0	3	4 6	C L K T 5
V D D	4	4 5	V D D
C L K T 1	5	4 4	C L K T 6
C L K C 1	6	4 3	C L K C 6
G N D	7	4 2	G N D
G N D	8	4 1	G N D
C L K C 2	9	4 0	C L K C 7
C L K T 2	1 0	3 9	C L K T 7
V D D	1 1	3 8	V D D
* S C L K	1 2	3 7	S D A T A *
C L K _ I N T	1 3	3 6	N / C
N / C	1 4	3 5	F B _ I N T
V D D	1 5	3 4	V D D
A V D D	1 6	3 3	F B _ O U T T
A G N D	1 7	3 2	N C
G N D	1 8	3 1	G N D
C L K C 3	1 9	3 0	C L K C 8
C L K T 3	2 0	2 9	C L K T 8
V D D	2 1	2 8	V D D
C L K T 4	2 2	2 7	C L K T 9
C L K C 4	2 3	2 6	C L K C 9
G N D	2 4	2 5	G N D

\*: Internal pull-up resistor 120K to VDD



3 DIMM DDR ZERO DELAY BUFFER FOR SIS CHIPSET

3.1 Block diagram





## 3 DIMM DDR ZERO DELAY BUFFER FOR SIS CHIPSET

### 4. PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

\*- Internal 120kΩ pull-up

#### 4.1 Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CLKC[9:0]	26,30,40,43,47,23,19,9,6,2	OUT	Complementary Clocks of differential pair outputs
CLKT[9:0]	27,29,39,44,46,22,20,10,5,3	OUT	True Clocks of differential pair outputs
SDATA *	37	I/O	Serial data of I <sup>2</sup> C 2-wire control interface Internal pull-up resistor 120K to Vdd
SCLK *	12	IN	Serial clock of I <sup>2</sup> C 2-wire control interface Internal pull-up resistor 120K to Vdd
CLK_INT	13	IN	True reference clock input, 3.3V tolerant input
NC	14, 32,36	NONE	Not connected
FB_OUTT	33	OUT	True Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT.
FB_INT	35	IN	True Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error.

#### 4.2 Power Pins

SYMBOL	PIN	FUNCTION
GND	1,7,8,18,24,25,31,41,42,48	Ground
VDD	4,11,15,21,28,34,38,45	Power Supply 2.5V
AVDD	16	Analog power supply, 2.5V
AGND	17	Analog ground



### 3 DIMM DDR ZERO DELAY BUFFER FOR SIS CHIPSET

#### 5. REGISTER 0 ~ REGISTER 4 RESERVED

##### 5.1 Register 5 : Output Control ( 1 = Active, 0 = Inactive ) (Default =FFH)

BIT	@POWERUP	PIN	DESCRIPTION
7	1	2,3	CLKC0,CLKT0 output control
6	1	6,5	CLKC1,CLKT1 output control
5	1	9,10	CLKC2,CLKT2 output control
4	1	19,20	CLKC3,CLKT3 output control
3	1	23,22	CLKC4,CLKT4 output control
2	1	26,27	CLKC9,CLKT9 output control
1	1	-	Reserved
0	1	-	Reserved

##### 5.2 Register 6 : Output Control ( 1 = Active, 0 = Inactive ) (Default =FFH)

BIT	@POWERUP	PIN	DESCRIPTION
7	1	-	Reserved
6	1	-	Reserved
5	1	-	Reserved
4	1	30,29	CLKC8,CLKT8 output control
3	1	40,39	CLKC7,CLKT7 output control
2	1	43,44	CLKC6,CLKT6 output control
1	1	47,46	CLKC5,CLKT5 output control
0	1	-	Reserved



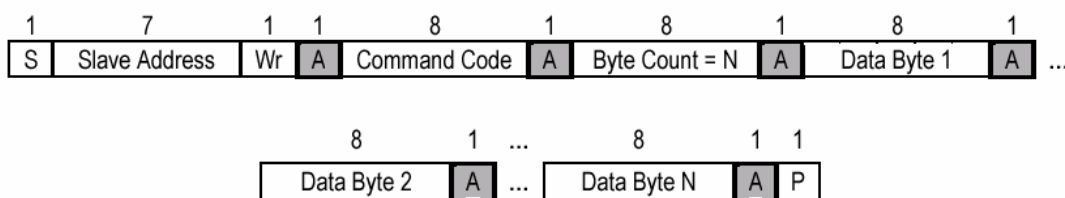
## 3 DIMM DDR ZERO DELAY BUFFER FOR SIS CHIPSET

### 6. ACCESS INTERFACE

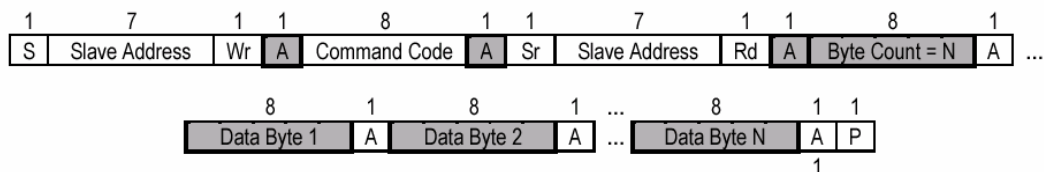
The W83176R-735 provides I<sup>2</sup>C Serial Bus for microprocessor to read/write internal registers. In the W83176R-735 is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I<sup>2</sup>C write address is defined at **0xD4**. The I<sup>2</sup>C read address is defined at **0xD5**.

#### Block Read and Block Write Protocol

##### 6.1 Block Write protocol

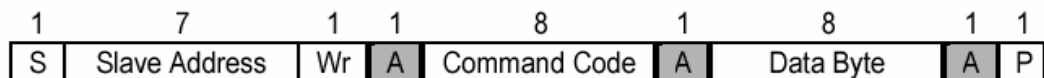


##### 6.2 Block Read protocol

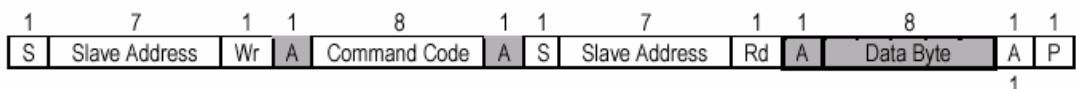


## In block mode, the command code must filled 00H

##### 6.3 Byte Write protocol



##### 6.4 Byte Read protocol







### 3 DIMM DDR ZERO DELAY BUFFER FOR SIS CHIPSET

## 7. SPECIFICATIONS

### 7.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD).

SYMBOL	PARAMETER	RATING
VDD , AVDD	Voltage on any pin with respect to GND	- 0.5 V to + 3.6 V
T <sub>STG</sub>	Storage Temperature	- 65°C to + 150°C
T <sub>B</sub>	Ambient Temperature	- 55°C to + 125°C
T <sub>A</sub>	Operating Temperature	0°C to + 70°C

### 7.2 AC CHARACTERISTICS

VDD = AVDD = 2.5V ( 5 % , TA = 0(C to +70(C, Test load = 10 pF						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Operating clock frequency	FIN	100		200	MHz	
Input Clock Duty Cycle	Dtin	40		60	%	
Dynamic Supply Current	I <sub>dd</sub>			300	mA	Fin=100 to 200Mhz
Cycle to Cycle Jitter	C-Cjitter			200	ps	Fout=100 to 200Mhz
Output to Output Skew	Tskew			100	ps	Fout=100 to 200Mhz
Output clock Rise time	T <sub>or</sub>	650		950	ps	Fout=100 to 200Mhz
Output clock Fall time	T <sub>of</sub>	650		950	ps	Fout=100 to 200Mhz
Output clock Duty Cycle	D <sub>tot</sub>	45		55	%	Fout=100 to 200Mhz
Output differential-pair crossing voltag	V <sub>oc</sub>	(V <sub>dd</sub> /2)-0.2	V <sub>dd</sub> /2	(V <sub>dd</sub> /2)+0.2	V	Fout=100 to 200Mhz



## 3 DIMM DDR ZERO DELAY BUFFER FOR SIS CHIPSET

### 7.3 DC CHARACTERISTICS

V <sub>dd</sub> = AV <sub>DD</sub> = 2.5V ( 5 % , TA = 0(C to +70(C						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
SDATA, SCLK Input Low Voltage	SV <sub>IL</sub>			1.0	V <sub>dc</sub>	
SDATA, SCLK Input High Voltage	SV <sub>IH</sub>	2.2			V <sub>dc</sub>	
CLKIN, FBIN Input Voltage Low	V <sub>IL</sub>			0.4	V <sub>dc</sub>	Fin=100 to 200Mhz
CLKIN, FBIN Input Voltage High	V <sub>IH</sub>	2.1			V <sub>dc</sub>	Fin=100 to 200Mhz
Input Pin Capacitance	C <sub>IN</sub>			5	pF	
Output Pin Capacitance	C <sub>OUT</sub>			6	pF	
Input Pin Inductance	L <sub>IN</sub>			7	nH	

# W83176R-735/W83176G-735

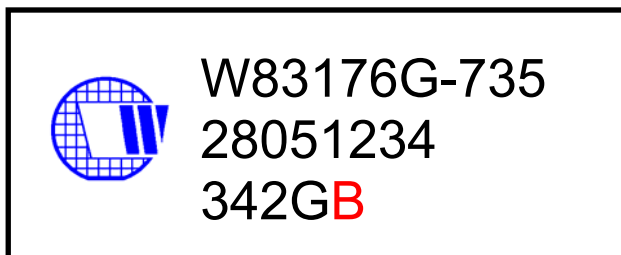
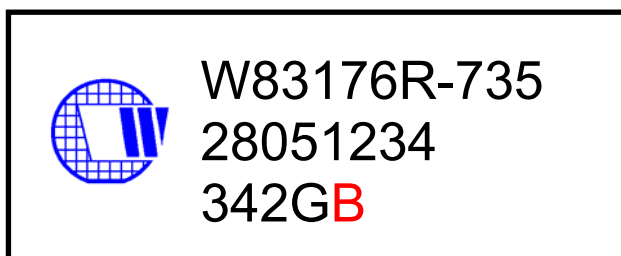


## 3 DIMM DDR ZERO DELAY BUFFER FOR SIS CHIPSET

### 8. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83176R-735	48 PIN SSOP	Commercial, 0°C to +70°C
W83176G-735	48 PIN SSOP (Pb-free package)	Commercial, 0°C to +70°C

### 9. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83176R-735/W83176G-735.

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

**8051234**: wafer production series lot number

3rd line: Tracking code 342 G B

**342**: packages made in '2003, week 42

**G**: assembly house ID; O means OSE, G means GR

**B**: IC revision

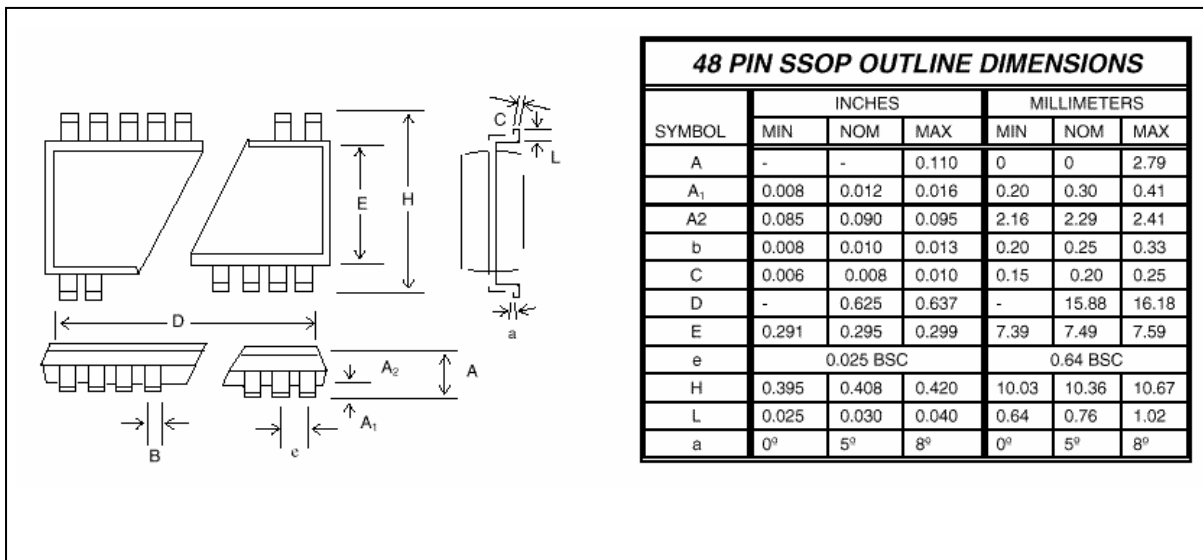
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### 10. PACKAGE DRAWING AND DIMENSIONS



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#### Headquarters

No. 4, Creation Rd. III,  
Science-Based Industrial Park,  
Hsinchu, Taiwan  
TEL: 886-3-5770066  
FAX: 886-3-5665577  
<http://www.winbond.com.tw/>

#### Taipei Office

9F, No.480, Rueiguang Rd.,  
Neihu District, Taipei, 114,  
Taiwan, R.O.C.  
TEL: 886-2-8177-7168  
FAX: 886-2-8751-3579

#### Winbond Electronics Corporation America

2727 North First Street, San Jose,  
CA 95134, U.S.A.  
TEL: 1-408-9436666  
FAX: 1-408-5441798

#### Winbond Electronics Corporation Japan

7F Daini-ueno BLDG, 3-7-18  
Shinyokohama Kohoku-ku,  
Yokohama, 222-0033  
TEL: 81-45-4781881  
FAX: 81-45-4781800

#### Winbond Electronics (Shanghai) Ltd.

27F, 2299 Yan An W. Rd. Shanghai,  
200336 China  
TEL: 86-21-62365999  
FAX: 86-21-62365998

#### Winbond Electronics (H.K.) Ltd.

Unit 9-15, 22F, Millennium City,  
No. 378 Kwun Tong Rd.,  
Kowloon, Hong Kong  
TEL: 852-27513100  
FAX: 852-27552064

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