14-Bit, 1300 MSPS, JESD204B, Analog-to-Digital Converter

Data Sheet **AD9697**

FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
  - Lane rates up to 16 Gbps
- Total power dissipation: 1.00 W at 1300 MSPS
- SNR: 65.6 dBFS at 172.3 MHz (1.59 V p-p analog input full scale)
- SFDR: 78 dBFS at 172.3 MHz (1.59 V p-p analog input full scale)
- Noise density
  - −153.9 dBFS/Hz (1.59 V p-p analog input full scale)
  - −155.6 dBFS/Hz (2.04 V p-p analog input full scale)
- 0.95 V, 1.8 V, and 2.5 V supply operation
- No missing codes
- Internal ADC voltage reference
- Flexible differential input voltage range
  - 1.36 V p-p to 2.04 V p-p (1.59 V p-p typical)
- 2 GHz usable analog input full power bandwidth
- Amplitude detect bits for efficient AGC implementation
- 4 integrated digital downconverters
  - 48-bit NCO
  - Programmable decimation rates
- Differential clock input
- SPI control
  - Integer clock divide by 2 and divide by 4
  - Flexible JESD204B lane configurations
- On-chip dithering to improve small signal linearity

APPLICATIONS

- Communications
- Diversity multiband, multimode digital receivers
  - 3G/4G, TD-SCDMA, W-CDMA, GSM, LTE
- General-purpose software radios
- Ultrawideband satellite receiver
- Instrumentation
  - Oscilloscopes
  - Spectrum analyzers
  - Network analyzers
  - Integrated RF test solutions
- Radars
- Electronic support measures, electronic counter measures, and electronic counter to counter measures
- High speed data acquisition systems
- DOCSIS 3.0 CMTS upstream receive paths
- Hybrid fiber coaxial digital reverse path receivers
- Wideband digital predistortion

FUNCTIONAL BLOCK DIAGRAM

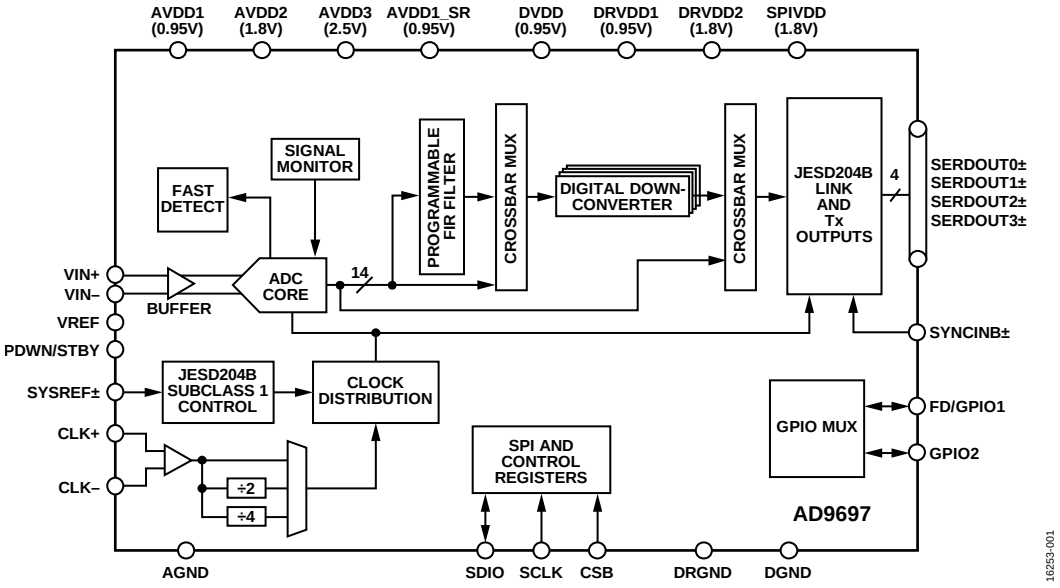


Figure 1.

Rev. 0 Document Feedback

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REVISION HISTORY

3/2018—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9697 is a single, 14-bit, 1300 MSPS analog-to-digital converter (ADC). The device has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. This product is designed to support communications applications capable of direct sampling wide bandwidth analog signals of up to 2 GHz. The −3 dB bandwidth of the ADC input is 2 GHz. The AD9697 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. The ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. The analog input and clock signals are differential inputs. The ADC data outputs are internally connected to four digital downconverters (DDCs) through a crossbar mux. Each DDC consists of multiple signal processing stages: a 48-bit frequency translator (numerically controlled oscillator (NCO)), and decimation filters. The NCO has the option to select up to 16 preset bands over the general-purpose input/output (GPIO) pins, or to use a coherent fast frequency hopping mechanism for band selection. Operation of the AD9697 between the DDC modes is selectable via serial port interface (SPI)-programmable profiles.

In addition to the DDC blocks, the AD9697 has several functions that simplify the automatic gain control (AGC) function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect control bits in Register 0x0245 of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input. In addition to the fast detect outputs, the AD9697 also offers signal monitoring capability. The signal monitoring block provides additional information about the signal being digitized by the ADC.

The user can configure the Subclasss 1 JESD204B-based high speed serialized output using either one lane, two lanes, or four lanes, depending on the DDC configuration and the acceptable lane rate of the receiving logic device. Multidevice synchronization is supported through the SYSREF± and SYNCINB± input pins.

The AD9697 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 3-wire SPI and or PDWN/STBY pin.

The AD9697 is available in a Pb-free, 64-lead LFCSP and is specified over the −40°C to +105°C junction temperature (T_J) range. This product may be protected by one or more U.S. or international patents.

Note that, throughout this data sheet, a multifunction pin, FD/GPIO1, is referred to either by the entire pin name or by a single function of the pin, for example, FD, when only that function is relevant.

PRODUCT HIGHLIGHTS

1. Low power consumption.
2. JESD204B lane rate support up to 16 Gbps.
3. Wide, full power bandwidth supports intermediate frequency (IF) sampling of signals up to 2 GHz.
4. Buffered inputs ease filter design and implementation.
5. Four integrated wideband decimation filters and NCO blocks supporting multiband receivers.
6. Programmable fast overrange detection.
7. On-chip temperature diode for system thermal management.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 0.95 V, AVDD1_SR = 0.95 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.95 V, DRVDD1 = 0.95 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, clock divider = 2, default input full scale, 0.5 V internal reference, analog input (A_{IN}) = −1.0 dBFS, default SPI settings, sample rate = 1300 MSPS, and DCS on, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating T_J range of −40°C to +105°C. Typical specifications represent performance at and T_J = 37°C (T_A = 25°C).

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION	14			Bits
ACCURACY				
No Missing Codes		Guaranteed		
Offset Error[1]		5		Codes
Offset Matching	−0.48	0	+0.48	% FSR
Gain Error	−2.9	±1	+2.9	% FSR
Gain Matching	−2.64	±0.18	+2.64	% FSR
Differential Nonlinearity (DNL)	−0.7		0.8	LSB
Integral Nonlinearity (INL)	−7	±1	5	LSB
TEMPERATURE DRIFT				
Offset Error		±9		ppm/°C
Gain Error		69		ppm/°C
INTERNAL VOLTAGE REFERENCE				
Voltage		0.5		V
INPUT-REFERRED NOISE		3.8		LSB rms
ANALOG INPUTS				
Differential Input Voltage Range	1.36	1.59	2.04	V p-p
Common-Mode Voltage (V_{CM})		1.41		V
Differential Input Resistance		200		Ω
Differential Input Capacitance		1.75		pF
Analog Full Power Bandwidth		2		GHz
POWER SUPPLY				
AVDD1	0.93	0.95	0.98	V
AVDD2	1.71	1.8	1.89	V
AVDD3	2.44	2.5	2.56	V
AVDD1_SR	0.93	0.95	0.98	V
DVDD	0.93	0.95	0.98	V
DRVDD1	0.93	0.95	0.98	V
DRVDD2	1.71	1.8	1.89	V
SPIVDD[2]	1.71	1.8	1.89	V
I_{AVDD1}		177	250	mA
I_{AVDD2}		267	306	mA
I_{AVDD3}		29	33	mA
I_{AVDD1_SR}		15	27	mA
I_{DVDD}		121	302	mA
I_{DRVDD1}[3]		124	204	mA
I_{DRVDD2}		21	25	mA
I_{SPIVDD}		2	5	mA
POWER CONSUMPTION				
Total Power Dissipation (Including Output Drivers)[4]		1.00	1.39	W
Power-Down Dissipation		716		mW
Standby[5]		200		mW

[1] DC offset calibration on (Register 0x0701, Bit 7 = 1 and Register 0x073B, Bit 7 = 0).
[2] The voltage level on the SPIVDD rail and on the DRVDD2 rail must be the same.
[3] All lanes running. Power dissipation on DRVDD changes with lane rate and number of lanes used.
[4] Default mode. No DDCs used.
[5] Can be controlled by SPI.

AC SPECIFICATIONS

AVDD1 = 0.95 V, AVDD1_SR = 0.95 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.95 V, DRVDD1 = 0.95 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, clock divider = 2, default input full scale, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, sample rate = 1300 MSPS, DCS on, and buffer current settings specified in Table 10, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating T_J range of −40°C to +105°C. Typical specifications represent performance at T_J = 37°C (T_A = 25°C).

Table 2.

	Analog Input Full Scale = 1.36 V p-p			Analog Input Full Scale = 1.59 V p-p			Analog Input Full Scale = 2.04 V p-p			
Parameter[1]	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
ANALOG INPUT FULL SCALE		1.36			1.59			2.04		V p-p
NOISE DENSITY[2]		−152.6			−153.9			−155.6		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)										
f_{IN} = 10.3 MHz		64.4			65.7			67.5		dBFS
f_{IN} = 172.3 MHz		64.4		64.5	65.6			67.5		dBFS
f_{IN} = 340 MHz		64.3			65.6			67.3		dBFS
f_{IN} = 750 MHz		64.0			65.2			66.6		dBFS
f_{IN} = 1000 MHz		63.8			64.9			66.1		dBFS
f_{IN} = 1400 MHz		63.2			64.2			65.2		dBFS
f_{IN} = 1700 MHz		62.7			63.6			64.5		dBFS
f_{IN} = 1980 MHz		62.3			63.0			63.9		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)										
f_{IN} = 10.3 MHz		64.3			65.4			66.1		dBFS
f_{IN} = 172.3 MHz		64.3		64.3	65.4			66.2		dBFS
f_{IN} = 340 MHz		64.2			65.3			65.7		dBFS
f_{IN} = 750 MHz		63.9			65.0			65.5		dBFS
f_{IN} = 1000 MHz		63.6			64.7			65.7		dBFS
f_{IN} = 1400 MHz		63.1			63.8			62.9		dBFS
f_{IN} = 1700 MHz		62.6			63.4			64.2		dBFS
f_{IN} = 1980 MHz		62.1			62.8			61.8		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)										
f_{IN} = 10.3 MHz		10.3			10.5			10.6		Bits
f_{IN} = 172.3 MHz		10.3		10.3	10.5			10.7		Bits
f_{IN} = 340 MHz		10.3			10.5			10.6		Bits
f_{IN} = 750 MHz		10.3			10.5			10.5		Bits
f_{IN} = 1000 MHz		10.2			10.4			10.6		dBFS
f_{IN} = 1400 MHz		10.1			10.3			10.1		dBFS
f_{IN} = 1700 MHz		10.1			10.2			10.3		dBFS
f_{IN} = 1980 MHz		10.0			10.1			9.9		dBFS
SPURIOUS FREE DYNAMIC RANGE (SFDR)										
f_{IN} = 10.3 MHz		81			79			73		dBFS
f_{IN} = 172.3MHz		81		74	78			72		dBFS
f_{IN} = 340 MHz		80			77			71		dBFS
f_{IN} = 750 MHz		83			80			72		dBFS
f_{IN} = 1000 MHz		82			81			79		dBFS
f_{IN} = 1400 MHz		80			76			67		dBFS
f_{IN} = 1700 MHz		80			80			78		dBFS
f_{IN} = 1980 MHz		81			79			68		dBFS

Parameter[1]	Analog Input Full Scale = 1.36 V p-p			Analog Input Full Scale = 1.59 V p-p			Analog Input Full Scale = 2.04 V p-p			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
WORST OTHER, EXCLUDING SECOND OR THIRD HARMONIC										
f_{IN} = 10.3 MHz		−96			−94			−101		dBFS
f_{IN} = 172.3 MHz		−95			−96	−85		−95		dBFS
f_{IN} = 340 MHz		−98			−99			−98		dBFS
f_{IN} = 750 MHz		−95			−95			−92		dBFS
f_{IN} = 1000 MHz		−96			−93			−91		dBFS
f_{IN} = 1400 MHz		−90			−89			−86		dBFS
f_{IN} = 1700 MHz		−91			−90			−84		dBFS
f_{IN} = 1980 MHz		−90			−90			−77		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD), AIN1 AND AIN2 = −7.0 dBFS										
f_{IN1} = 170.8 MHz, f_{IN2} = 173.8 MHz		−84			−84			−83		dBFS
f_{IN1} = 343.5 MHz, f_{IN2} = 346.5 MHz		−83			−82			−81		dBFS
ANALOG INPUT BANDWIDTH, FULL POWER[3]		2			2			2		GHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and details on how these tests were completed.
[2] Noise density is measured at a low analog input frequency (10 MHz).
[3] Full power bandwidth is the bandwidth of operation to achieve proper ADC performance.

DIGITAL SPECIFICATIONS

AVDD1 = 0.95 V, AVDD1_SR = 0.95 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.95 V, DRVDD1 = 0.95 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, clock divider = 2, default input full scale, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, sample rate = 1300 MSPS, and DCS on, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating T_J range of −40°C to +105°C. Typical specifications represent performance at and T_J = 37°C (T_A = 25°C).

Table 3.

Parameter	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	400	800	1600	mV p-p
Input Common-Mode Voltage		0.65		V
Input Resistance (Differential)		32		kΩ
Input Capacitance (Differential)			0.9	pF
SYSREF INPUTS (SYSREF+, SYSREF−)				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage		0.65	2	V
Input Resistance (Differential)		18		kΩ
Input Capacitance (Differential)		1		pF
LOGIC INPUTS (SDIO, SCLK, CSB, PDWN/STBY, FD/GPIO1, GPIO2)				
Logic Compliance		CMOS		
Logic 1 Voltage	0.75 × SPIVDD			V
Logic 0 Voltage	0		0.35 × SPIVDD	V
Input Resistance		30		kΩ
LOGIC OUTPUT (SDIO, FD)				
Logic Compliance		CMOS		
Logic 1 Voltage (I_{OH} = 4 mA)	SPIVDD − 0.45			V
Logic 0 Voltage (I_{OL} = 4 mA)	0		0.45	V

Parameter	Min	Typ	Max	Unit
SYNCIN INPUTS (SYNCINB−, SYNCINB+)				
Logic Compliance		LVDS/LVPECL/CMOS		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage		0.65	2	V
Input Resistance (Differential)		18		kΩ
Input Capacitance (Single-Ended per Pin)		1		pF
DIGITAL OUTPUTS (SERDOUTx±, x = 0 TO 3)				
Logic Compliance		SST		
Differential Output Voltage	360	520	770	mV p-p
Differential Termination Impedance	80	100	1200	Ω

SWITCHING SPECIFICATIONS

AVDD1 = 0.95 V, AVDD1_SR = 0.95 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.95 V, DRVDD1 = 0.95 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, clock divider = 2, default input full scale, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, sample rate = 1300 MSPS, and DCS on, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating T_J range of −40°C to +105°C. Typical specifications represent performance at and T_J = 37°C (T_A = 25°C).

Table 4.

Parameter	Min	Typ	Max	Unit
CLOCK				
Clock Rate (at CLK+/CLK− Pins)	0.24		1.40	GHz
Maximum Sample Rate[1]	1400			MSPS
Minimum Sample Rate[2]	240			MSPS
Clock Pulse Width[3]				
High	156.25			ps
Low	156.25			ps
OUTPUT PARAMETERS				
Unit Interval (UI)[4]	62.5	76.9		ps
Rise Time (t_R) (20% to 80% into 100 Ω Load)		28		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)		28		ps
Phase-Locked Loop (PLL) Lock Time		5		ms
Data Rate per Channel (NRZ)[5]	1.6875	13	16	Gbps
LATENCY[6]				
Pipeline Latency		75		Clock cycles
Fast Detect Latency		26		Clock cycles
Wake-Up Time[7]				
Standby		400		µs
Power-Down		15		ms
APERTURE				
Aperture Delay (t_A)		192		ps
Aperture Uncertainty (Jitter, t_J)		43		fs rms
Out of Range Recovery Time		1		Clock cycles

[1] The maximum sample rate is the clock rate after the divider.
[2] The minimum sample rate operates at 240 MSPS. See SPI Register 0x011A to reduce the threshold of the clock detect circuit.
[3] Clock duty stabilizer (DCS) on. See SPI Register 0x011C and Register 0x011E to enable DCS.
[4] Baud rate = 1/UI. A subset of this range can be supported.
[5] Default L = 4. This number can change based on the sample rate and decimation ratio.
[6] No DDCs used. L = 4, M = 2, and F = 1.
[7] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLK+ TO SYSREF+ TIMING REQUIREMENTS	See Figure 3				
t_{SU_SR}	Device clock to SYSREF+ setup time		−70		ps
t_{H_SR}	Device clock to SYSREF+ hold time		120		ps
SPI TIMING REQUIREMENTS	See Figure 4				
t_{DS}	Setup time between the data and the rising edge of SCLK	4			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK must be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK must be in a logic low state	10			ns
t_{ACCESS}	Maximum time delay between falling edge of SCLK and output data valid for a read operation		6	10	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the CSB rising edge (not shown in Figure 4)	10			ns

Timing Diagrams

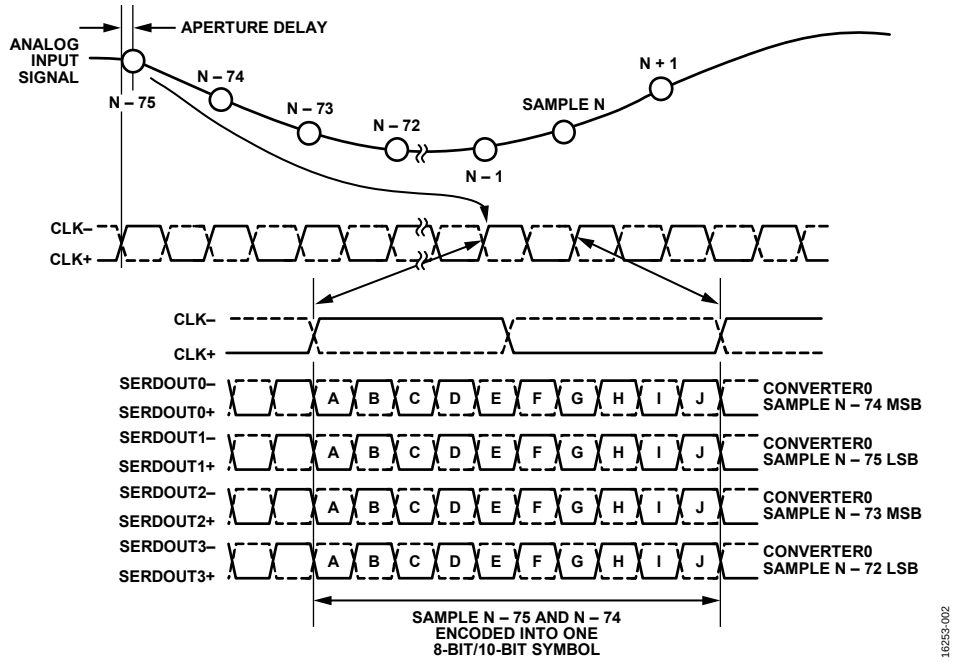


Figure 2. Data Output Timing Diagram

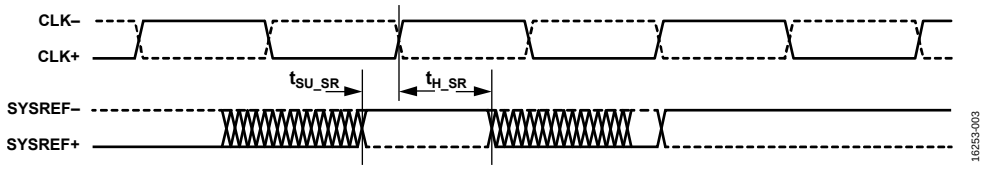


Figure 3. SYSREF± Setup and Hold Timing Diagram

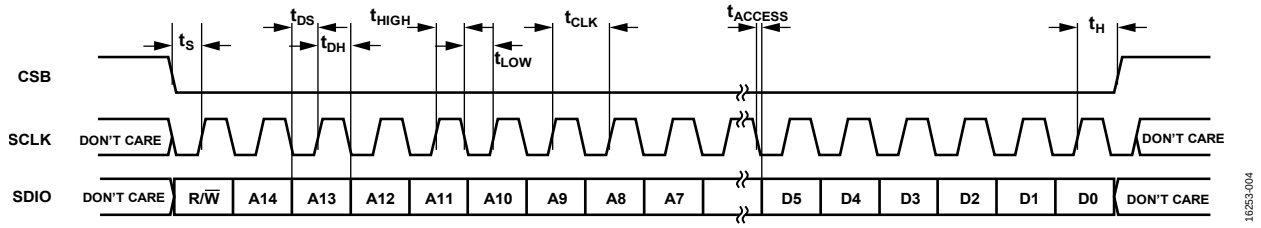


Figure 4. SPI Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.05 V
AVDD1_SR to AGND	1.05 V
AVDD2 to AGND	2.00 V
AVDD3 to AGND	2.70 V
DVDD to DGND	1.05 V
DRVDD1 to DRGND	1.05 V
DRVDD2 to DRGND	2.00 V
SPIVDD to DGND	2.00 V
AGND to DRGND	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
DGND to DRGND	−0.3 V to +0.3 V
VIN± to AGND	AGND − 0.3 V to AVDD3 + 0.3 V
CLK± to AGND	AGND − 0.3 V to AVDD1 + 0.3 V
SCLK, SDIO, CSB to DGND	DGND − 0.3 V to SPIVDD + 0.3 V
PDWN/STBY to DGND	DGND − 0.3 V to SPIVDD + 0.3 V
SYSREF± to AGND	2.5 V
SYNCINB± to DRGND	2.5 V
Junction Temperature Range (T_J)	−40°C to +125°C
Storage Temperature Range, Ambient (T_A)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Typical θ_{JA}, θ_{JB}, and θ_{JC} are specified vs. the number of printed circuit board (PCB) layers in different airflow velocities (in m/sec). Airflow increases heat dissipation effectively reducing θ_{JA} and θ_{JB}. In addition, metal in direct contact with the package leads and exposed pad from metal traces, through holes, ground, and power planes, reduces θ_{JA}. Thermal performance for actual applications requires careful inspection of the conditions in an application. The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 6.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1,2]	θ_{JC_BOT}[1,3]	θ_{JC_TOP}[1,3]	θ_{JB}[1,4]	θ_{JT}[1,2]	Unit
CP-64-17	0	22.5	1.7	7.6	4.3	0.2	°C/W
	1.0	17.9					°C/W
	2.5	16.8					°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

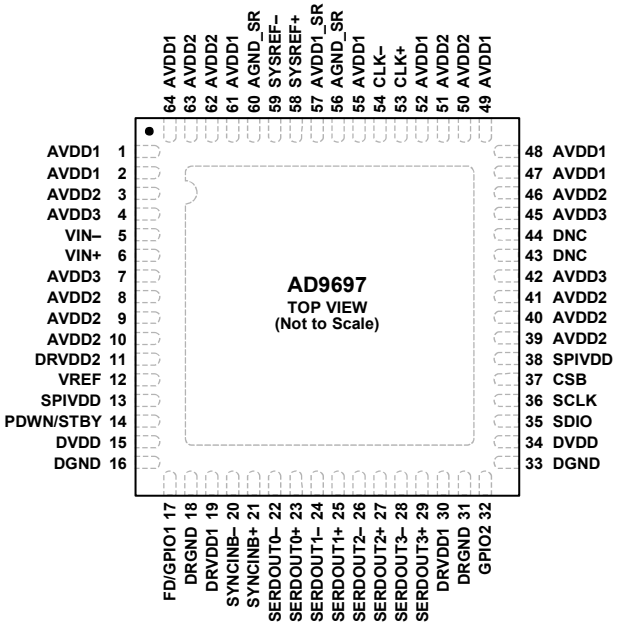


Figure 5. Pin Configuration (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 2, 47 to 49, 52, 55, 61, 64	AVDD1	Power supply	Analog Power Supply (0.95 V Nominal).
3, 8 to 10, 39 to 41, 46, 50, 51, 62, 63	AVDD2	Power supply	Analog Power Supply (1.8 V Nominal).
4, 7, 42, 45	AVDD3	Power supply	Analog Power Supply (2.5 V Nominal).
5, 6	VIN–, VIN+	Analog input	ADC Analog Input Complement/True.
11	DRVDD2	Power supply	Digital Driver Power Supply (1.8 V Nominal).
12	VREF	Input/output	Reference Voltage Input (0.50 V)/Do Not Connect. This pin is configurable through the SPI as a no connect pin or as an input. Do not connect this pin if using the internal reference. This pin requires a 0.50 V reference voltage input if using an external voltage reference source.
13, 38	SPIVDD	Power supply	Digital Power Supply for SPI (1.8 V Nominal).
14	PDWN/STBY	Digital control input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down (PDWN) or standby (STBY).
15, 34	DVDD	Power supply	Digital Power Supply (0.95 V Nominal).
16, 33	DGND	Ground power supply	Digital Control Ground Supply. These pins connect to the digital ground plane.
17	FD/GPIO1	CMOS output	Fast Detect Output (FD). General-purpose input/output (GPIO) pin (GPIO1).
18, 31	DRGND	Ground power supply	Digital Driver Ground Supply. These pins connect to the digital driver ground plane.
19, 30	DRVDD1	Power supply	Digital Driver Power Supply (0.95 V Nominal).
20	SYNCINB–	Digital input	Active Low JESD204B LVDS/CMOS Sync Input True.
21	SYNCINB+	Digital input	Active Low JESD204B LVDS Sync Input Complement.
22, 23	SERDOUT0–, SERDOUT0+	Data output	Lane 0 Output Data Complement/True.
24, 25	SERDOUT1–, SERDOUT1+	Data output	Lane 1 Output Data Complement/True.
26, 27	SERDOUT2– SERDOUT2+	Data output	Lane 2 Output Data Complement/True.

Pin No.	Mnemonic	Type	Description
28, 29	SERDOUT3−, SERDOUT3+	Data output	Lane 3 Output Data Complement/True.
32	GPIO2	CMOS output	General-Purpose Input/Output (GPIO) Pin (GPIO2).
35	SDIO	Digital control input/output	SPI Serial Data Input/Output.
36	SCLK	Digital control input	SPI Serial Clock.
37	CSB	Digital control input	SPI Chip Select (Active Low).
43, 44	DNC	DNC	Do Not Connect. Do not connect to these pins.
53, 54	CLK+, CLK−	Analog input	Clock Input True/Complement.
56, 60	AGND_SR	Ground power supply	Ground Reference for SYSREF±.
57	AVDD1_SR	Power supply	Analog Power Supply for SYSREF± (0.95 V Nominal).
58, 59	SYSREF+, SYSREF−	Digital input	Active High JESD204B LVDS System Reference Input Complement/True.
	EPAD	Ground power supply	Analog Ground. Connect the exposed pad to the analog ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 0.95 V, AVDD1_SR = 0.95 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.95 V, DRVDD1 = 0.95 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, clock divider = 2, default input full scale, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, sample rate = 1300 MSPS, DCS on, buffer current setting specified in Table 10, and dc offset calibration enabled, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating T_J range of −40°C to +105°C. Typical specifications represent performance at T_J = 37°C (T_A = 25°C).

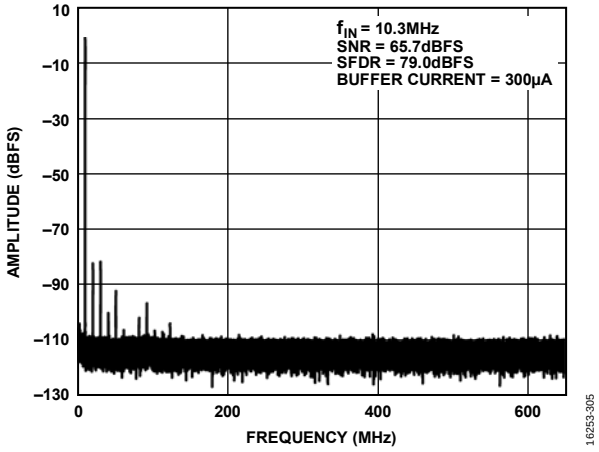


Figure 6. Single-Tone FFT with Analog Input Frequency (f_{IN}) = 10.3 MHz

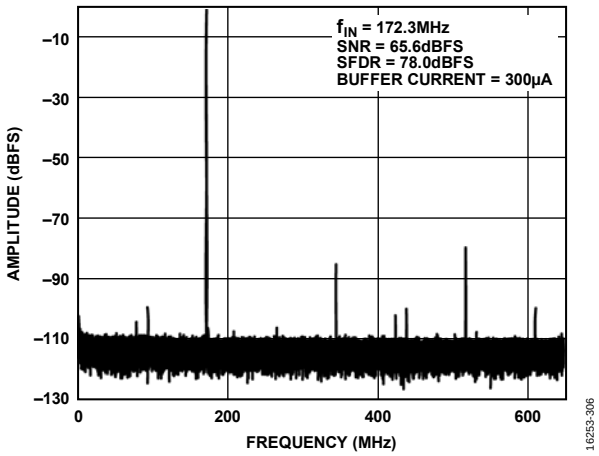


Figure 7. Single-Tone FFT with f_{IN} = 172.3 MHz

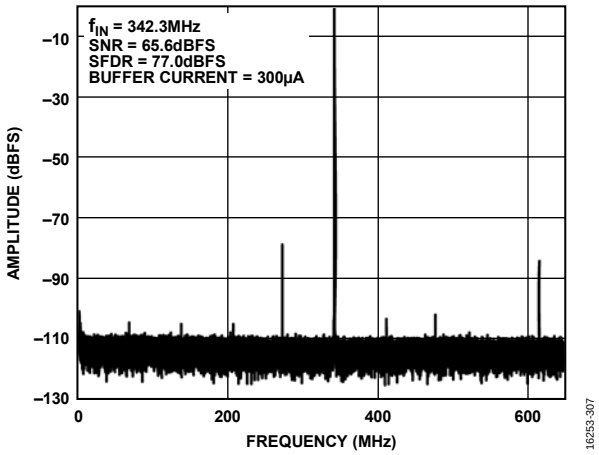


Figure 8. Single-Tone FFT with f_{IN} = 342.3 MHz

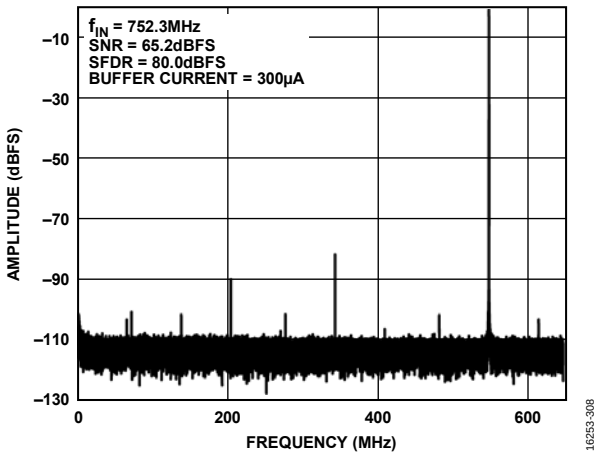


Figure 9. Single-Tone FFT with f_{IN} = 752.3 MHz

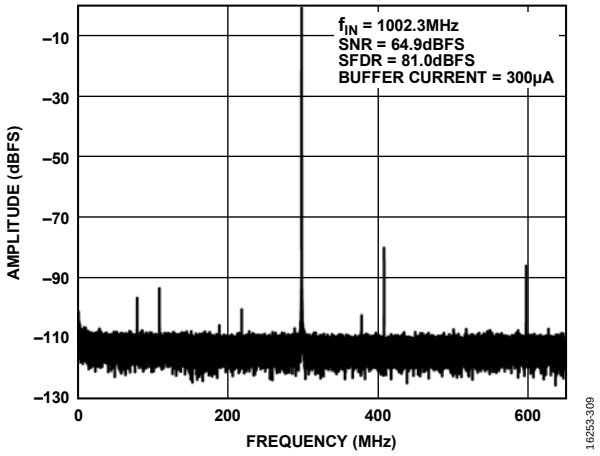


Figure 10. Single-Tone FFT with f_{IN} = 1002.3 MHz

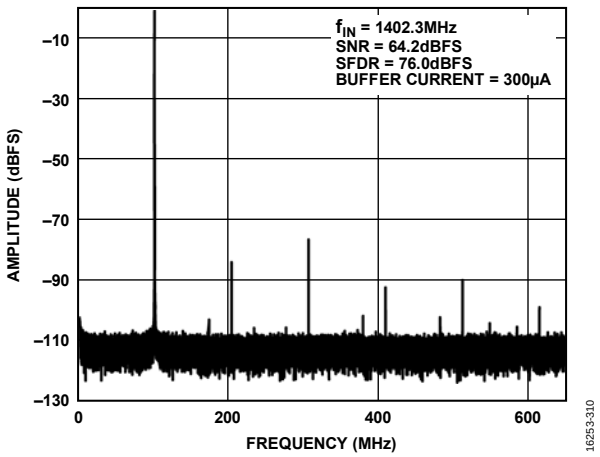


Figure 11. Single-Tone FFT with f_{IN} = 1402.3 MHz

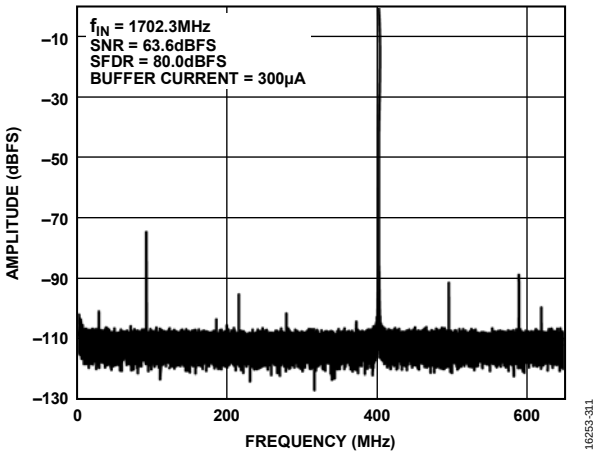


Figure 12. Single-Tone FFT with f_{IN} = 1702.3 MHz

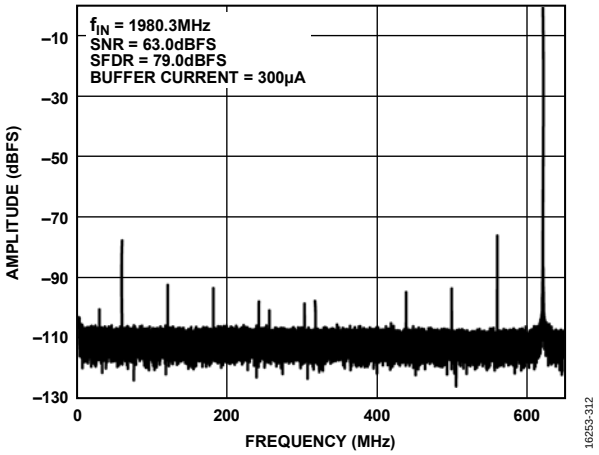


Figure 13. Single-Tone FFT with f_{IN} = 1980.3 MHz

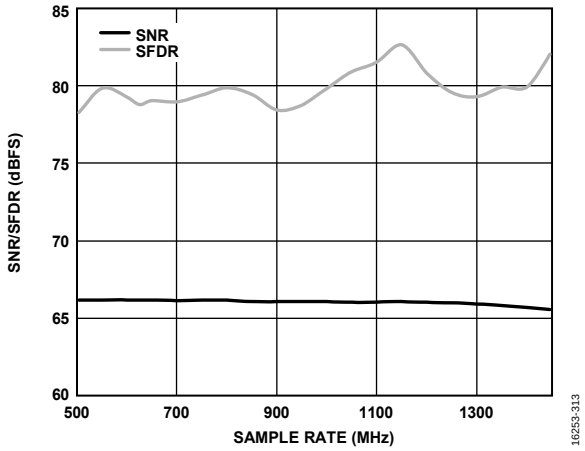


Figure 14. SNR/SFDR vs. Sample Rate, f_{IN} = 172.3 MHz

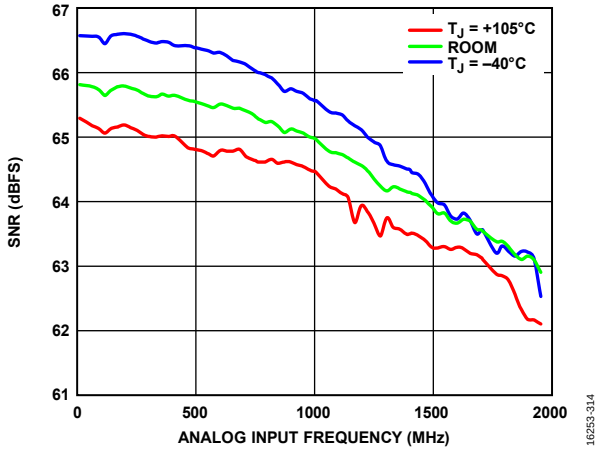


Figure 15. SNR vs. Analog Input Frequency at Minimum, Room, and Maximum Temperatures

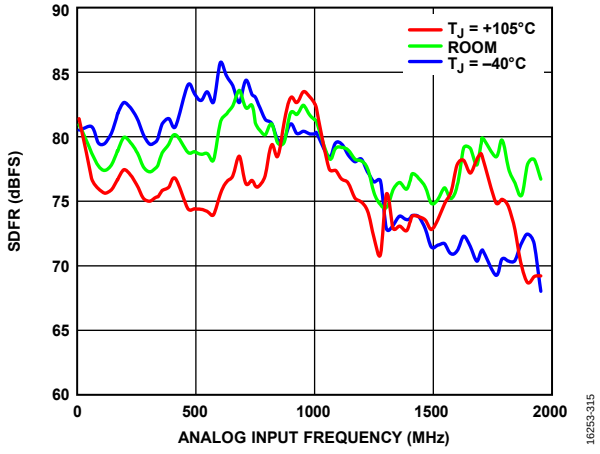


Figure 16. SFDR vs. Analog Input Frequency at Minimum, Room, and Maximum Temperatures

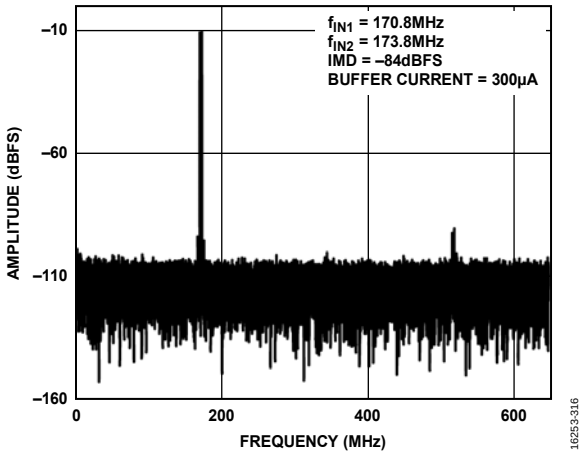


Figure 17. Two-Tone FFT; f_{IN1} = 170.8 MHz, f_{IN2} = 173.8 MHz

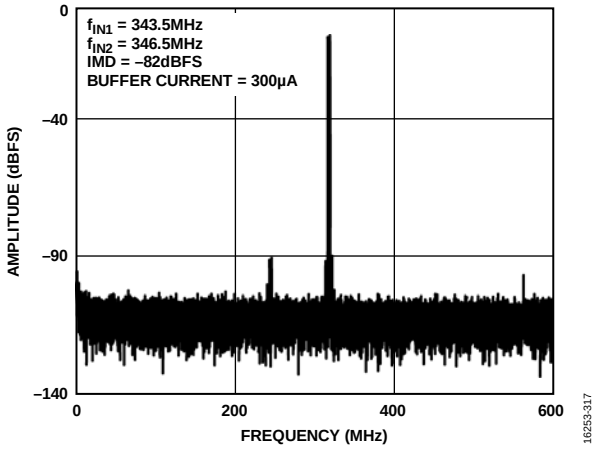


Figure 18. Two-Tone FFT; f_{IN1} = 343.5 MHz, f_{IN2} = 346.5 MHz

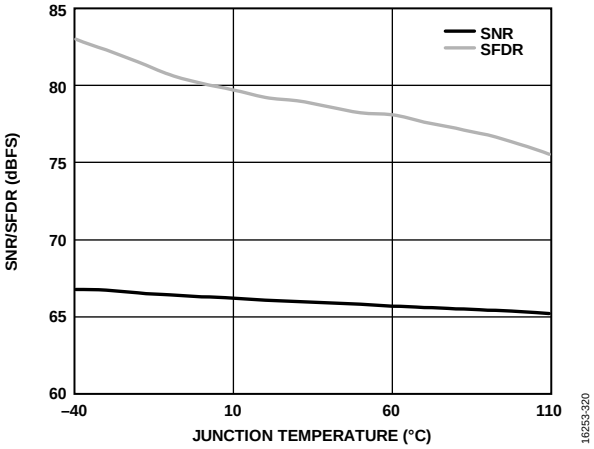


Figure 21. SNR/SFDR vs. Junction Temperature, f_{IN} = 172.3 MHz

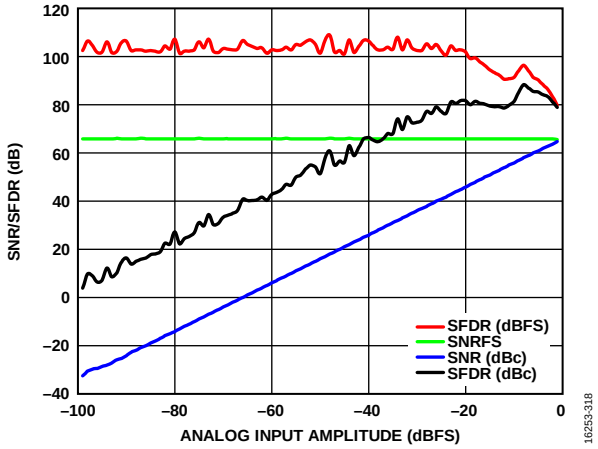


Figure 19. SNR/SFDR vs. Analog Input Amplitude, f_{IN} = 172.3 MHz

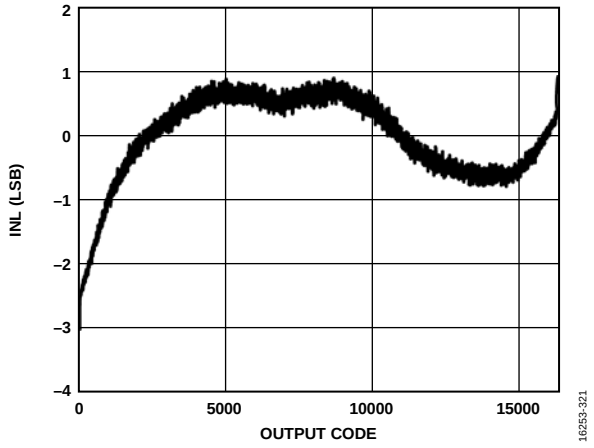


Figure 22. INL, f_{IN} = 10.3 MHz

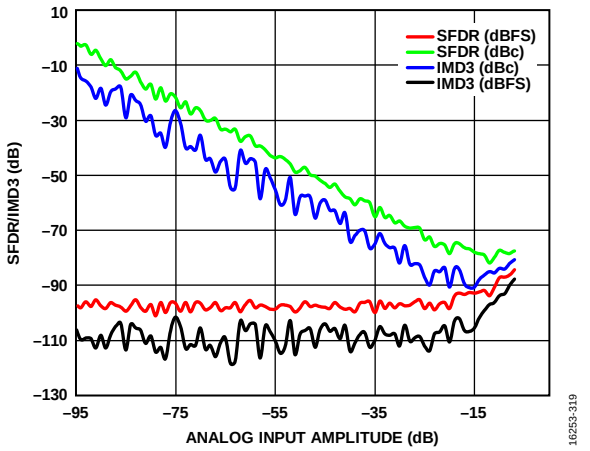


Figure 20. SFDR/IMD3 vs. Analog Input Amplitude, f_{IN} = 172.3 MHz

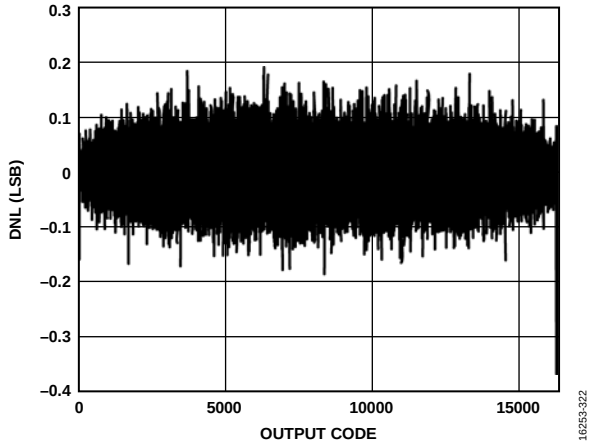


Figure 23. DNL, f_{IN} = 10.3 MHz

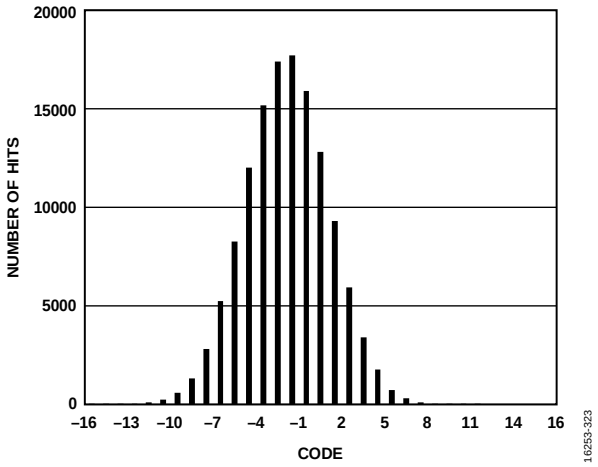


Figure 24. Input Referred Noise Histogram

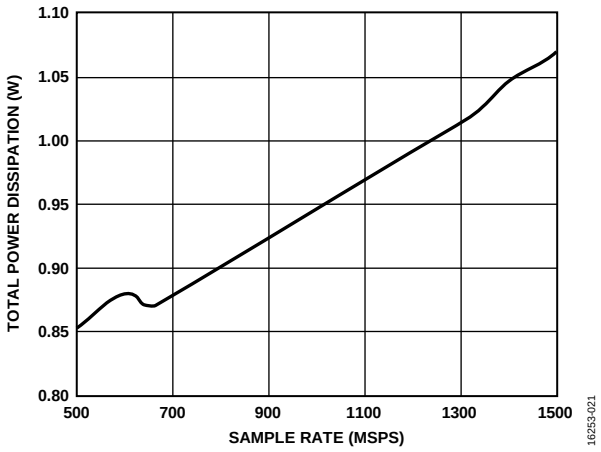


Figure 27. Total Power Dissipation vs. Sample Rate (f_S)

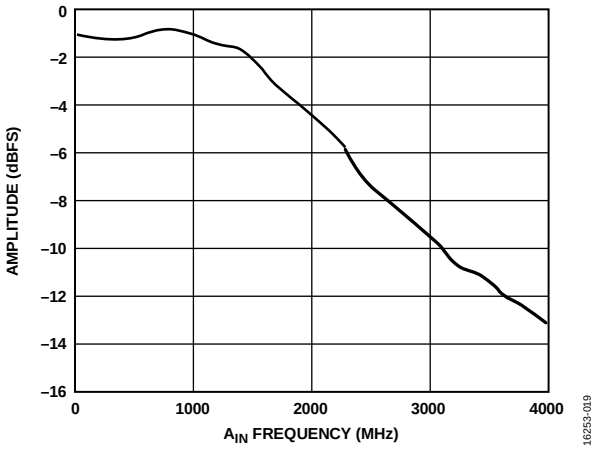


Figure 25. Full Power Bandwidth

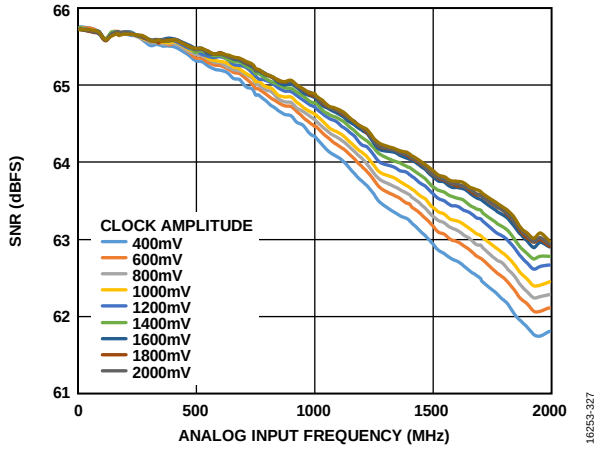


Figure 28. SNR vs. Analog Input Frequency at Different Clock Amplitudes

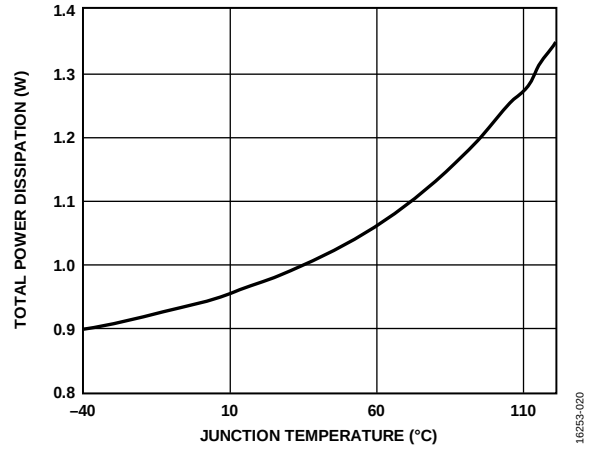


Figure 26. Total Power Dissipation vs. Junction Temperature

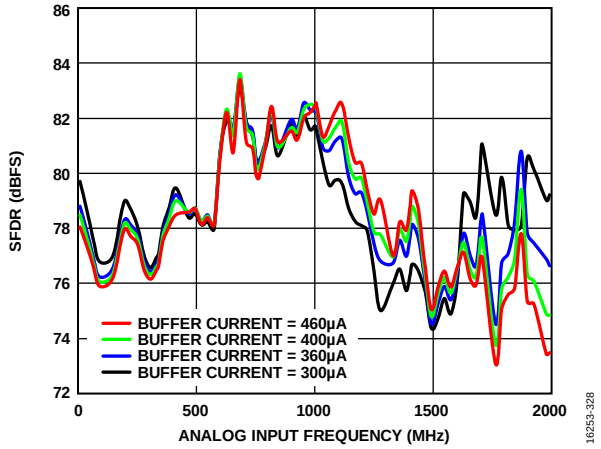


Figure 29. SFDR vs. Analog Input Frequency with Different Buffer Current Settings

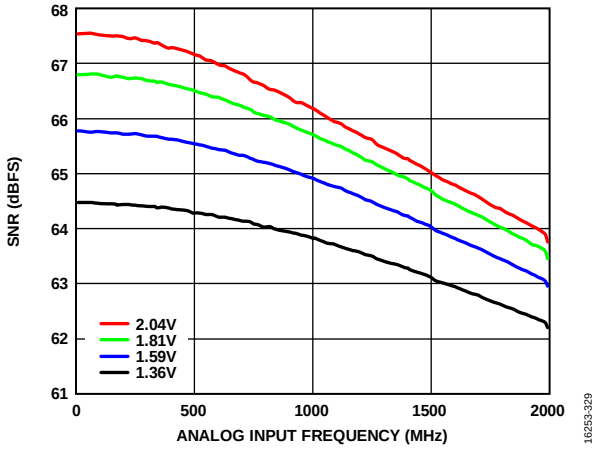


Figure 30. SNR vs. Analog Input Frequency with Different Analog Input Full-Scale Values

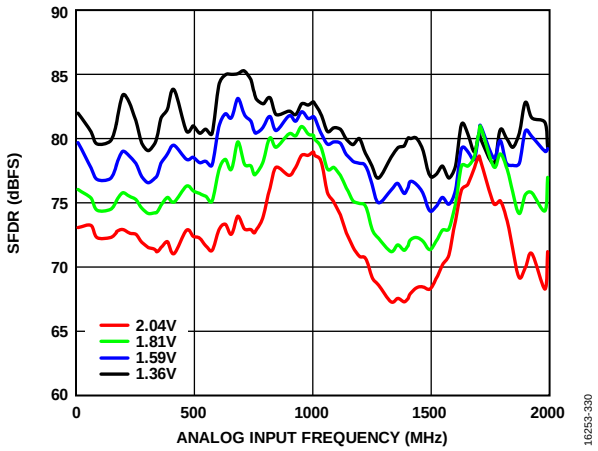


Figure 31. SFDR vs. Analog Input Frequency with Different Analog Input Full-Scale Values

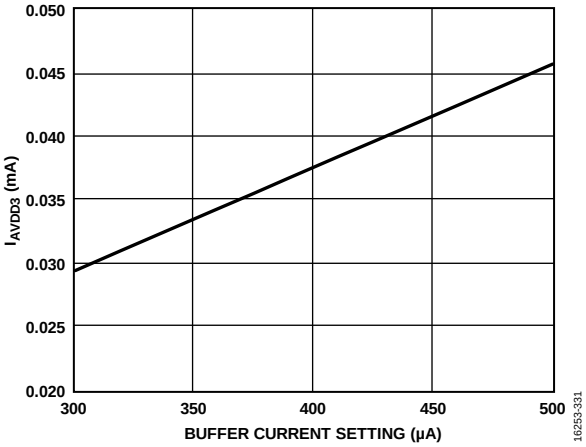


Figure 32. I_{AVDD3} vs. Buffer Current Setting (Buffer Control 1 Setting in Register 0x1A4C)

EQUIVALENT CIRCUITS

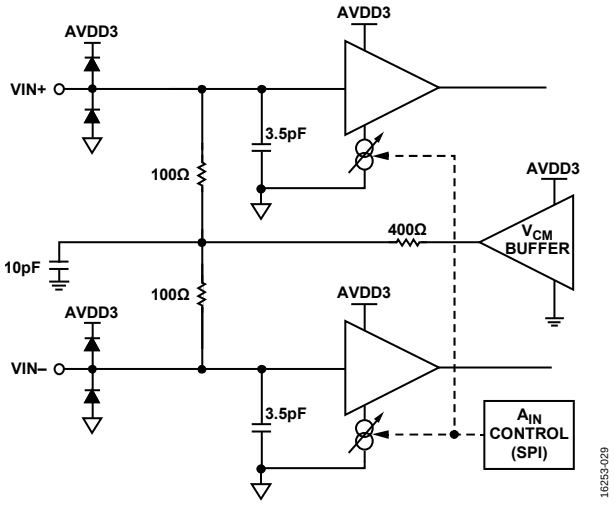


Figure 33. Analog Inputs

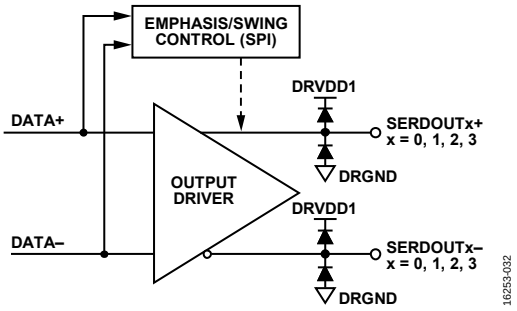


Figure 36. Digital Outputs (DATA+ and DATA– Refer to Internal Signals)

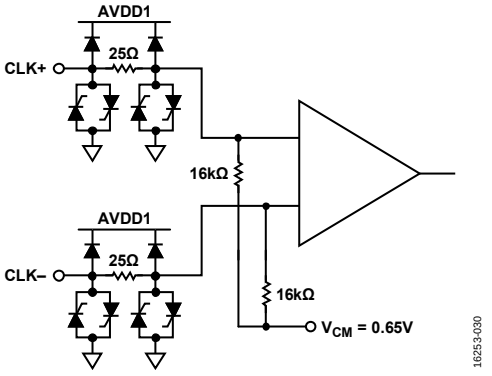


Figure 34. Clock Inputs

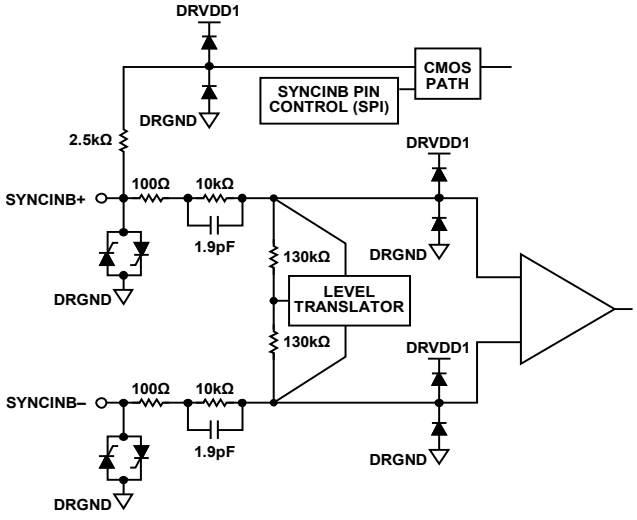


Figure 37. SYNCINB± Inputs

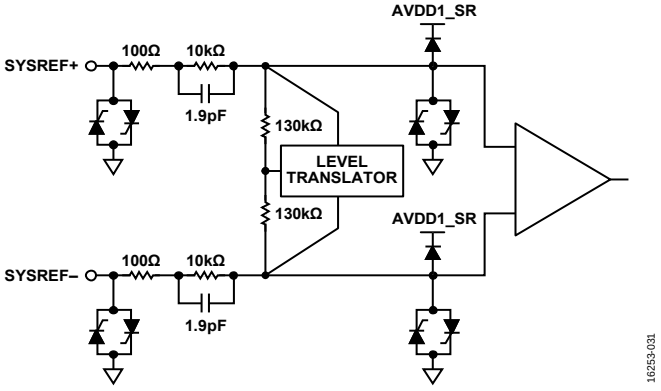


Figure 35. SYSREF± Inputs

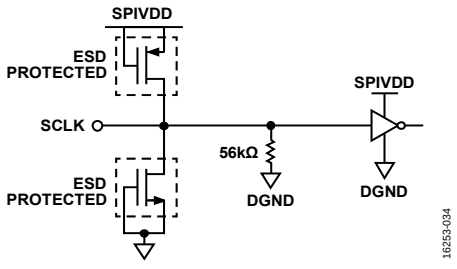


Figure 38. SCLK Input

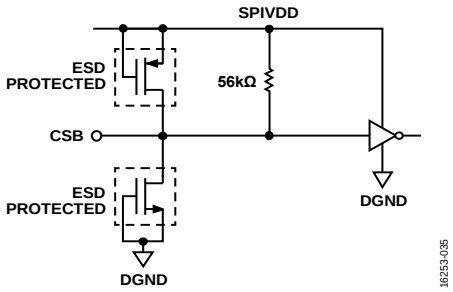


Figure 39. CSB Input

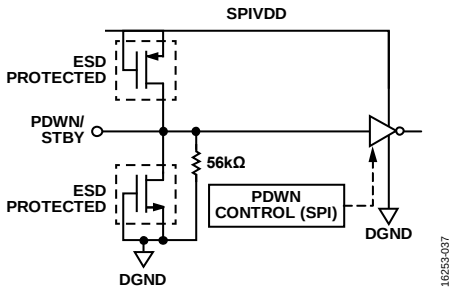


Figure 41. PDWN/STBY Input

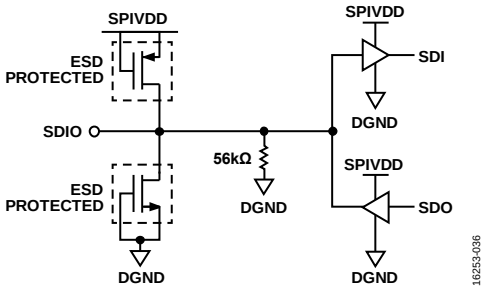


Figure 40. SDIO Input

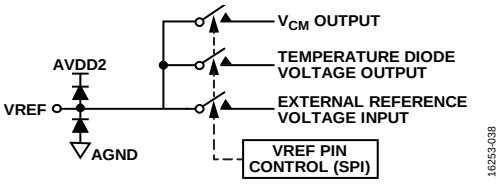


Figure 42. VREF Input/Output

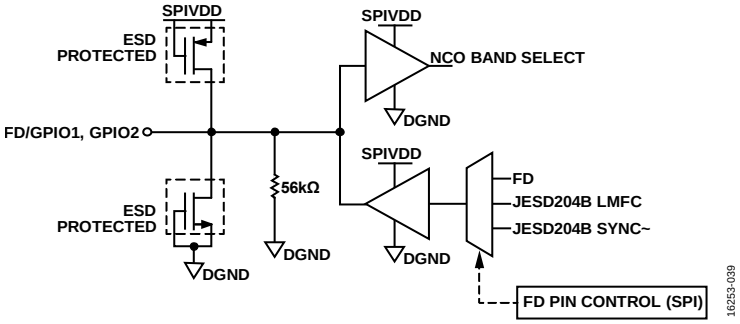


Figure 43. FD/GPIO1, GPIO2 Input

THEORY OF OPERATION

The AD9697 has a single analog input channel and up to four JESD204B output lane pairs. The ADC samples wide bandwidth analog signals of up to 2 GHz. The actual −3 dB roll-off of the analog inputs is 2 GHz. The AD9697 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. The ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

The AD9697 has several functions that simplify the AGC function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

The Subclass 1 JESD204B-based high speed, serialized output data lanes can be configured in one-lane (L = 1), two-lane (L = 2), and four-lane (L = 4) configurations, depending on the sample rate and the decimation ratio. Multiple device synchronization is supported through the SYSREF± and SYNCINB± input pins. The SYSREF± pin in the AD9697 can also be used as a timestamp of data as it passes through the ADC and out of the JESD204B interface.

ADC ARCHITECTURE

The architecture of the AD9697 consists of an input buffered pipelined ADC. The input buffer provides a termination impedance to the analog input signal. This termination impedance is set to 200 Ω. The equivalent circuit diagram of the analog input termination is shown in Figure 33. The input buffer is optimized for high linearity, low noise, and low power across a wide bandwidth.

The input buffer provides a linear high input impedance (for ease of drive) and reduces kickback from the ADC. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample; at the same time, the remaining stages operate with the preceding samples. Sampling occurs on the rising edge of the clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9697 is a differential buffer. The internal common-mode voltage of the buffer is 1.41 V. The clock signal alternately switches the input circuit between sample mode and hold mode.

Either a differential capacitor or two single-ended capacitors (or a combination of both) can be placed on the inputs to provide a matching passive network. These capacitors ultimately create a low-pass filter that limits unwanted broadband noise. For more information, refer to the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005). In general, the precise front-end network component values depend on the application.

Figure 44 shows the differential input return loss curve for the analog inputs across a frequency range of 1 MHz to 10 GHz. The reference impedance is 100 Ω.

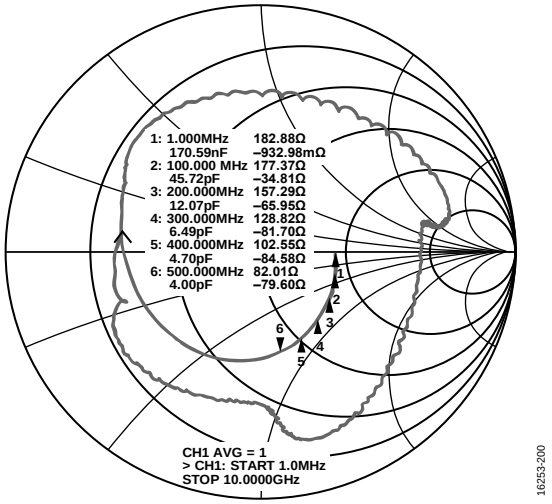


Figure 44. Different Input Return Loss

For best dynamic performance, the source impedances driving VIN+ and VIN− must be matched such that any common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates a differential reference that defines the span of the ADC core.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. For the AD9697, the available span is programmable through the SPI port from 1.36 V p-p to 2.04 V p-p differential, with 1.59 V p-p differential being the default.

Differential Input Configurations

There are several ways to drive the AD9697, either actively or passively. Optimum performance is achieved by driving the analog input differentially.

For applications where SNR and SFDR are key parameters, differential transformer coupling is the recommended input configuration (see Figure 45 and Table 9) because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9697.

For low to midrange frequencies, a double balun or double transformer network (see Figure 45 and Table 9) is recommended for optimum performance of the AD9697. For higher frequencies in the second or third Nyquist zones, it is recommended to remove some of the front-end passive components to ensure wideband operation (see Table 9).

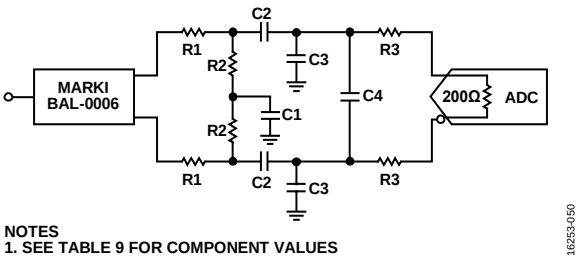


Figure 45. Differential Transformer-Coupled Configuration for the AD9697

Table 9. Differential Transformer-Coupled Input Configuration Component Values

Speed Grade	Frequency Range	Transformer	R1	R2	R3	C1	C2	C3	C4
AD9697-1300	<2 GHz	BAL-0006/BAL-0006SMG	25 Ω	25 Ω	10 Ω	0.1 µF	0.1 µF	DNI[1]	DNI[1]

[1] DNI means do not insert.

Input Common Mode

The analog inputs of the AD9697 are internally biased to the common mode, as shown in Figure 47.

For dc-coupled applications, the recommended operation procedure is to export the common-mode voltage to the VREF pin using the SPI writes listed in this section. The common-mode voltage must be set by the exported value to ensure proper ADC operation. Disconnect the internal common-mode buffer from the analog input using Register 0x1908.

When performing SPI writes for dc coupling operation, use the following register settings, in order:

1. Set Register 0x1908, Bit 2 to 1 to disconnect the internal common-mode buffer from the analog input.
2. Set Register 0x18A6 to 0x00 to turn off the voltage reference.
3. Set Register 0x18E6 to 0x00 to turn off the temperature diode export.
4. Set Register 0x18E3, Bit 6 to 0x01 to turn on the V_{CM} export.
5. Set Register 0x18E3, Bits[5:0] to the buffer current setting (copy the buffer current setting from Register 0x1A4C and Register 0x1A4D to improve the accuracy of the common-mode export).

Figure 46 shows the block diagram representation of a dc-coupled application.

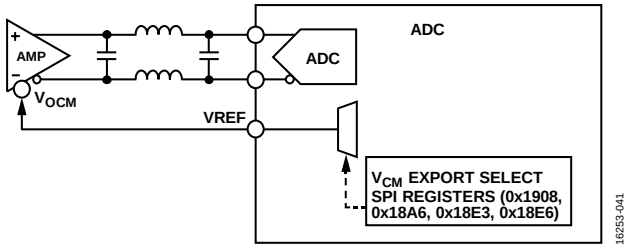


Figure 46. DC-Coupled Application Using the AD9697

Analog Input Buffer Controls and SFDR Optimization

The AD9697 input buffer offers flexible controls for the analog inputs, such as, buffer current and input full-scale adjustment. All the available controls are shown in Figure 47.

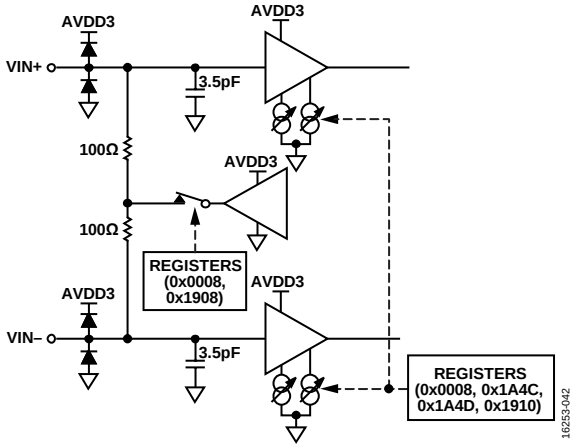


Figure 47. Analog Input Controls

Using Register 0x1A4C and Register 0x1A4D, the buffer behavior can be adjusted to optimize the SFDR over various input frequencies and bandwidths of interest. Use Register 0x1910 to change the internal reference voltage. Changing the internal reference voltage results in a change in the input full-scale voltage.

When the input buffer current in Register 0x1A4C and Register 0x1A4D is set, the amount of current required by the AVDD3 supply changes. This relationship is shown in Figure 48. For a complete list of buffer current settings, see Table 10.

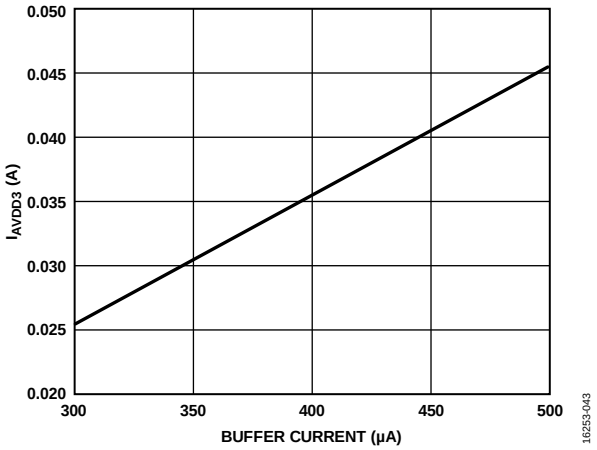


Figure 48. AVDD3 Current (I_{AVDD3}) vs. Buffer Current (Buffer Control 1 Setting in Register 0x1A4C and Buffer Control 2 Setting in Register 0x1A4D)

Table 10 shows the recommended values for the buffer current for various Nyquist zones.

Absolute Maximum Input Swing

The absolute maximum input swing allowed at the inputs of the AD9697 is 5.6 V p-p differential. Signals operating near or at this level can cause permanent damage to the ADC.

Dither

The AD9697 has internal on-chip dither circuitry that improves the ADC linearity and SFDR, particularly at smaller signal levels. A known but random amount of white noise is injected into the input of theAD9697. This dither improves the small signal linearity within the ADC transfer function and is precisely subtracted out digitally. The dither is turned on by default and does not reduce the ADC input dynamic range. The data sheet specifications and limits are obtained with the dither turned on.

The dither is on by default. It is not recommended to turn it off.

Table 10. SFDR Optimization for Input Frequencies

Speed Grade	Frequency	Register 0x1A4C and Register 0x1A4D	Register 0x1B03	Register 0x1B08	Register 0x1B10
AD9697-1300	All A_{IN} frequencies	300 µA	0x02	0xC1	0x00

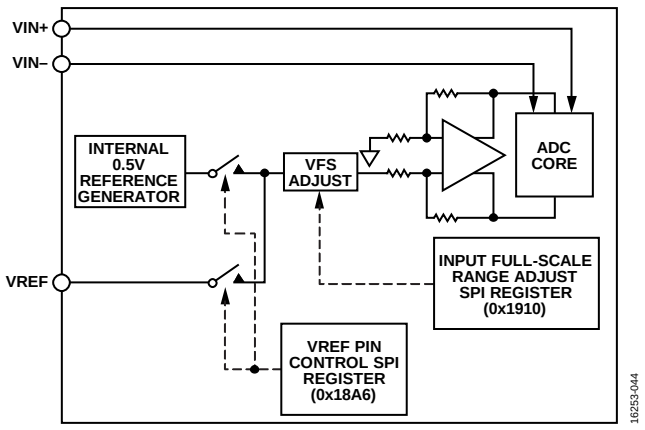


Figure 49. Internal Reference Configuration and Controls

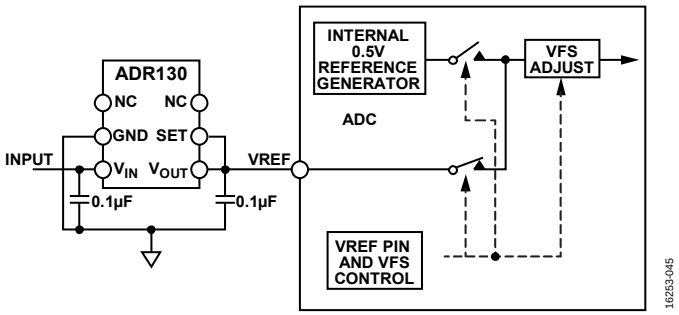


Figure 50. External Reference Using the ADR130

VOLTAGE REFERENCE

A stable and accurate 0.5 V voltage reference is built into the AD9697. This internal 0.5 V reference sets the full-scale input range of the ADC. The full-scale input range can be adjusted via the ADC input full-scale control register (Register 0x1910). For more information on adjusting the input swing, see Table 44. Figure 49 shows the block diagram of the internal 0.5 V reference controls.

The SPI Register 0x18A6 enables the user to either use this internal 0.5 V reference or to provide an external 0.5 V reference. When using an external voltage reference, provide a 0.5 V reference. The full-scale adjustment is made using the SPI, irrespective of the reference voltage. For more information on adjusting the full-scale level of the AD9697, refer to the Memory Map section.

The SPI writes required to use the external voltage reference, in order, are as follows:

1. Set Register 0x18E3 to 0x00 to turn off the V_{CM} export.
2. Set Register 0x18E6 to 0x00 to turn off the temperature diode export.
3. Set Register 0x18A6 to 0x01 to turn on the external voltage reference.

The use of an external reference may be necessary, in some applications, to enhance the gain accuracy of the ADC or to improve thermal drift characteristics. Figure 51 shows the typical drift characteristics of the internal 0.5 V reference.

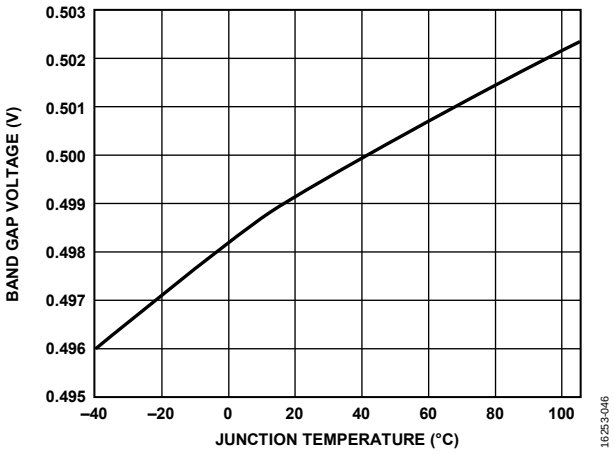


Figure 51. Typical V_{REF} Drift

The external reference must be a stable 0.5 V reference. The ADR130 is a sufficient option for providing the 0.5 V reference. Figure 50 shows how the ADR130 can be used to provide the external 0.5 V reference to the AD9697. The dashed lines show unused blocks within the AD9697 while using the ADR130 to provide the external reference.

DC OFFSET CALIBRATION

The AD9697 contains a digital filter to remove the dc offset from the output of the ADC. For ac-coupled applications, this filter can be enabled by setting Register 0x0701, Bit 7 to 0x1 and setting Register 0x73B, Bit 7 to 0x0. The filter computes the average dc signal and it is digitally subtracted from the ADC output. As a result, the dc offset is improved to better than 70 dBFS at the output. Because the filter does not distinguish between the source of dc signals, this feature can be used when the signal content at dc is not of interest. The filter corrects dc up to ±512 codes and saturates beyond that.

CLOCK INPUT CONSIDERATIONS

For optimum performance, drive the AD9697 sample clock inputs (CLK+ and CLK–) with a differential signal. This signal is typically ac-coupled to the CLK+ and CLK– pins via a transformer or clock drivers. These pins are biased internally and require no additional biasing.

Figure 52 shows a preferred method for clocking the AD9697. The low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer.

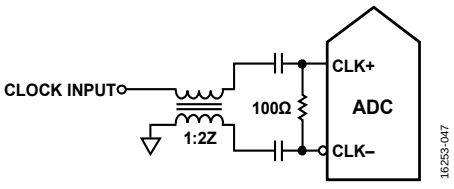


Figure 52. Transformer Coupled Differential Clock

Another option is to ac couple a differential CML or LVPECL signal to the sample clock input pins, as shown in Figure 53 and Figure 54.

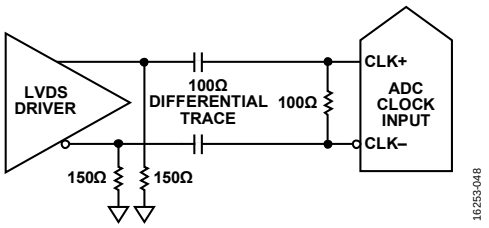


Figure 53. Differential LVPECL Sample Clock

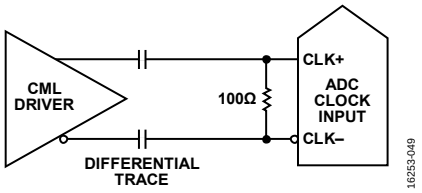


Figure 54. Differential CML Sample Clock

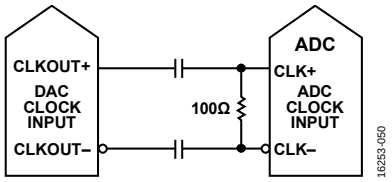


Figure 55. Clock Output Clocking the AD9697

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. The AD9697 contains an internal clock divider and a duty cycle stabilizer comprised of Duty Cycle Stabilizer 1 (DCS1) and Duty Cycle Stabilizer 2 (DCS2).

In applications where the clock duty cycle cannot be guaranteed to be 50%, a higher multiple frequency clock along with the usage of the clock divider is recommended.

When it is not possible to provide a higher frequency clock, it is recommended to turn on DCSx using Register 0x011C and Register 0x011E. Figure 56 shows the different controls to the AD9697 clock inputs. The output of the divider offers a 50% duty cycle, high slew rate (fast edge) clock signal to the internal ADC.

In the AD9697 1300 MSPS speed grade, the DCS is enabled by default. It is recommended to keep DCS on irrespective of clock divide ratio in the AD9697.

See the Memory Map section for more details on using this feature.

Input Clock Divider

The AD9697 contains an input clock divider with the ability to divide the input clock by 1, 2, or 4. Select the divider ratios using Register 0x0108 (see Figure 56).

The maximum frequency at the CLK± inputs is 1.28 GHz, which is the limit of the divider. In applications where the clock input is a multiple of the sample clock, take care to program the appropriate divider ratio into the clock divider before applying the clock signal; this ensures that the current transients during device startup are controlled.

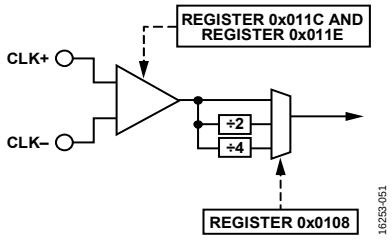


Figure 56. Clock Divider Circuit

The AD9697 clock divider can be synchronized using the external SYSREF± input. A valid SYSREF± signal causes the clock divider to reset to a programmable state. This synchronization feature allows multiple devices to have their clock dividers aligned to guarantee simultaneous input sampling. See the Memory Map Registers section for more information.

Input Clock Divider ½ Period Delay Adjust

The input clock divider inside the AD9697 provides phase delay in increments of ½ the input clock cycle. Register 0x0109 can be programmed to enable this delay. Changing this register does not affect the stability of the JESD204B link.

Clock Fine Delay and Superfine Delay Adjust

Adjust the AD9697 sampling edge instant by writing to Register 0x0110, Register 0x0111, and Register 0x0112. Bits[2:0] of Register 0x0110 enable the selection of the fine delay, or the fine delay with superfine delay. The fine delay allows the user to delay the clock edges with 16 step or 192 step delay options. The superfine delay is an unsigned control to adjust the clock delay in superfine steps of 0.25 ps each.

Register 0x0112, Bits[7:0] offer the user the option to delay the clock in 192 delay steps. Register 0x0111, Bits[7:0] offer the user the option to delay the clock in 128 superfine steps. To use the superfine delay option, set the clock delay control in Register 0x0110, Bits[2:0] to 0x2 or 0x6.

Figure 57 shows the controls available to the clock dividers within AD9697. It is recommended to apply the same delay settings to the digital delay circuits as are applied to the analog delay circuits to maintain sample accuracy through the pipe.

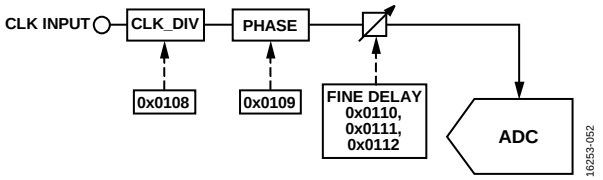


Figure 57. Clock Divider Phase and Delay Controls

The clock delay adjustment takes effect immediately when it is enabled via SPI writes. Enabling the clock fine delay adjust in Register 0x0110 causes a datapath reset. However, the contents of Register 0x0111 and Register 0x0112 can be changed without affecting the stability of the JESD204B link.

Clock Coupling Considerations

The AD9697 has many different domains within the analog supply that control various aspects of the data conversion. The clock domain is supplied by Pin 49 and Pin 64 on the analog supply (AVDD1). To minimize coupling between the clock supply domain and the other analog domains, it is recommended to add a supply Q factor reduction circuitry (de-Q) for Pin 49 and Pin 64, as shown in Figure 58.

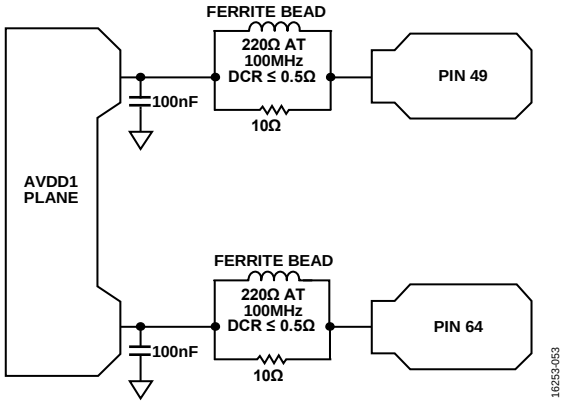


Figure 58. De-Q Network Recommendation for the Clock Domain Supply

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. Calculate the degradation in SNR at a given input frequency (f_{IN}) due only to aperture jitter (t_J) by

$$SNR_{JITTER} = -20 \times \log_{10}(2 \times \pi \times f_{IN} \times t_J)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications.

IF undersampling applications are particularly sensitive to jitter (see Figure 59).

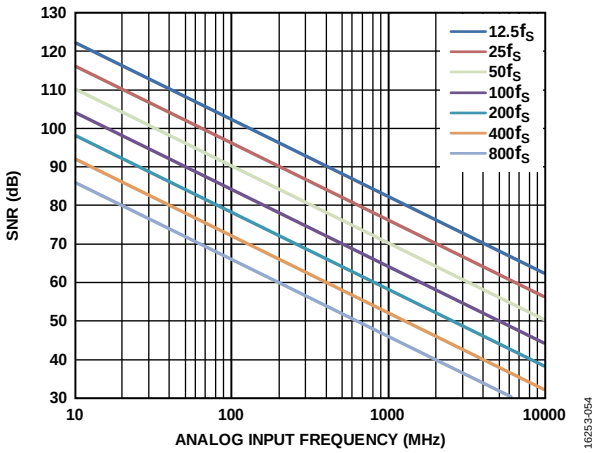


Figure 59. Ideal SNR vs. Analog Input Frequency for Various Jitter

Treat the clock input as an analog signal when aperture jitter may affect the dynamic range of the AD9697. Separate power supplies for clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. If the clock is generated from another type of source (by gating, dividing, or other methods), retime the clock by the original clock at the last step. Refer to the AN-501 Application Note and the AN-756 Application Note for more in depth information about jitter performance as it relates to ADCs.

Figure 60 shows the estimated SNR for the AD9697 across input frequency for different clock induced jitter values. Estimate the SNR by using the following equation:

$$SNR\ (\text{dBFS}) = -10\log_{10}\left(10^{\left(\frac{-SNR_{ADC}}{10}\right)} + 10^{\left(\frac{-SNR_{JITTER}}{10}\right)}\right)$$

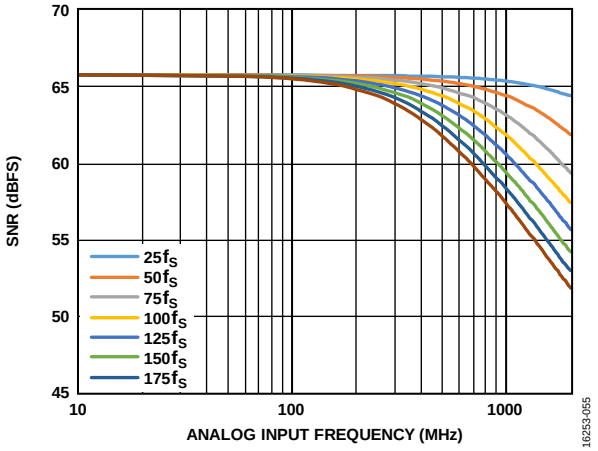


Figure 60. Estimated SNR Degradation for the AD9697 vs. Analog Input Frequency and RMS Jitter

POWER-DOWN/STANDBY MODE

The AD9697 has a PDWN/STBY pin that configure the device in power-down or standby mode. The default operation is PDWN. The PDWN/STBY pin is a logic high pin. When in power-down mode, the JESD204B link is disrupted. The power-down option can also be set via Register 0x003F and Register 0x0040.

In standby mode, the JESD204B link is not disrupted and transmits zeros for all converter samples. Change this transmission using Register 0x0571, Bit 7 to select /K/ characters.

TEMPERATURE DIODE

The AD9697 contains diode-based temperature sensors. The diodes output voltages commensurate to the temperature of the silicon.

There are two diodes on the die, but the results established using the temperature diode at the central location of the die can be regarded as representative of the entire die. Figure 61 shows the locations of the diodes in the AD9697 with voltages that can be output to the VREF pin. In each location, there is a pair of diodes, one of which is 20× the size of the other. It is recommended to use both diodes to obtain an accurate estimate of the die temperature. For more information, see the AN-1432 Application Note, *Practical Thermal Modeling and Measurements in High Power ICs*.

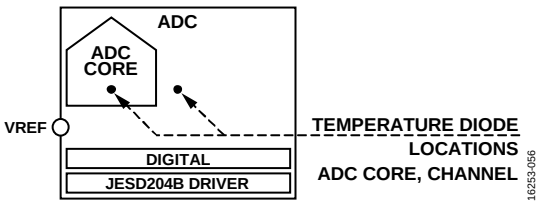


Figure 61. Temperature Diode Locations in the Die

The temperature diode voltages can be exported to the VREF pin using the SPI. Use Register 0x18E6 to enable or disable diodes. It is important to note that other voltages may be exported to the VREF pin at the same time, which can result in undefined behavior. To ensure a proper readout, switch off all other voltage exporting circuits as described in this section.

The SPI writes required to export the temperature diode are as follows (see the Memory Map section for more information):

1. Set Register 0x18E3 to 0x00 to turn off V_{CM} export.
2. Set Register 0x18A6 to 0x00 to turn off voltage reference export.
3. Set Register 0x18E6 to 0x01 to turn on voltage export of the central 1× temperature diode. The typical voltage response of the temperature diode is shown in Figure 62. Although this voltage represents the die temperature, it is recommended to take measurements from a pair of diodes for improved accuracy. The following step explains how to enable the 20× diode.
4. Set Register 0x18E6 to 0x02 to turn on the second temperature diode of the pair, which is 20× the size of the first. For the method using two diodes simultaneously to achieve a more accurate result, see the AN-1432 Application Note, *Practical Thermal Modeling and Measurements in High Power ICs*.

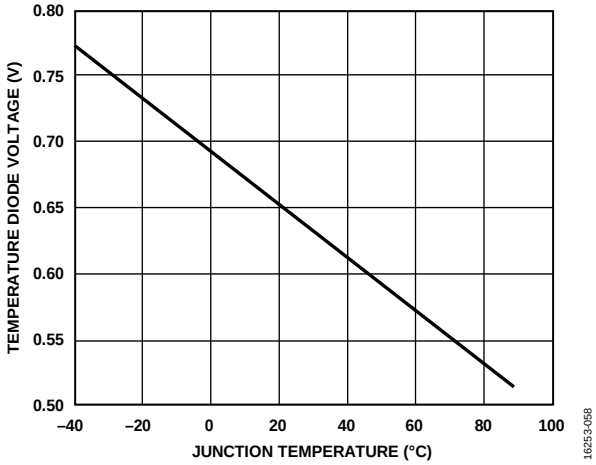


Figure 62. Typical Voltage Response of the 1× Temperature Diode

The relationship between the measured delta voltage (ΔV) and the junction temperature in degrees Celsius (°C) is shown in Figure 63.

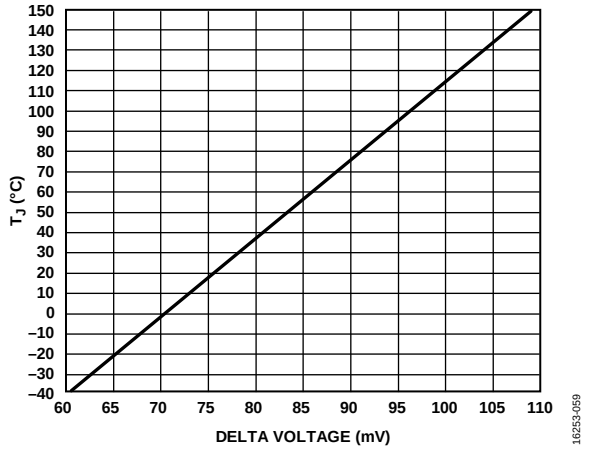


Figure 63. Junction Temperature (T_J) vs. Delta Voltage (ΔV)

ADC OVERRANGE AND FAST DETECT

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to be clipped. The standard overrange bit in the JESD204B outputs provides information on the state of the analog input that is of limited usefulness. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip actually occurs. In addition, because input signals can have significant slew rates, the latency of this function is of major concern. Highly pipelined converters can have significant latency. The AD9697 contains fast detect circuitry to monitor the threshold and assert the FD pin.

ADC OVERRANGE

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange indicator can be embedded within the JESD204B link as a control bit (when CSB > 0). The latency of this overrange indicator matches the sample latency.

The AD9697 also records any overrange condition in any of the eight virtual converters. For more information on the virtual converters, refer to Figure 65. The overrange status of each virtual converter is registered as a sticky bit in Register 0x0563. The contents of Register 0x0563 can be cleared using Register 0x0562, by toggling the bits corresponding to the virtual converter to set and reset position.

FAST THRESHOLD DETECTION (FD)

The fast detect bit is immediately set whenever the absolute value of the input signal exceeds the programmable upper threshold level. The FD bit is only cleared when the absolute value of the input signal drops below the lower threshold level for greater than the programmable dwell time. This feature provides hysteresis and prevents the FD bit from excessively toggling.

The operation of the upper threshold and lower threshold registers, along with the dwell time registers, is shown in Figure 64.

The FD indicator is asserted if the input magnitude exceeds the value programmed in the fast detect upper threshold registers, located at Register 0x0247 and Register 0x0248. The selected threshold register is compared with the signal magnitude at the output of the ADC. The fast upper threshold detection has a latency of 28 clock cycles (maximum). The approximate upper threshold magnitude is defined by

$$\textit{Upper Threshold Magnitude}\ (\text{dBFS}) = 20 \log (\textit{Threshold Magnitude}/2^{13})$$

The FD indicators are not cleared until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold registers, located at Register 0x0249 and Register 0x024A. The fast detect lower threshold register is a 13-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC pipeline latency, but is accurate in terms of converter resolution. The lower threshold magnitude is defined by

$$\textit{Lower Threshold Magnitude}\ (\text{dBFS}) = 20 \log (\textit{Threshold Magnitude}/2^{13})$$

For example, to set an upper threshold of −6 dBFS, write 0xFFF to Register 0x0247 and Register 0x0248. To set a lower threshold of −10 dBFS, write 0xA1D to Register 0x0249 and Register 0x024A.

The dwell time can be programmed from 1 to 65,535 sample clock cycles by placing the desired value in the fast detect dwell time registers, located at Register 0x024B and Register 0x024C. See the Memory Map section (Register 0x0040, and Register 0x0245 to Register 0x024C in Table 44) for more details.

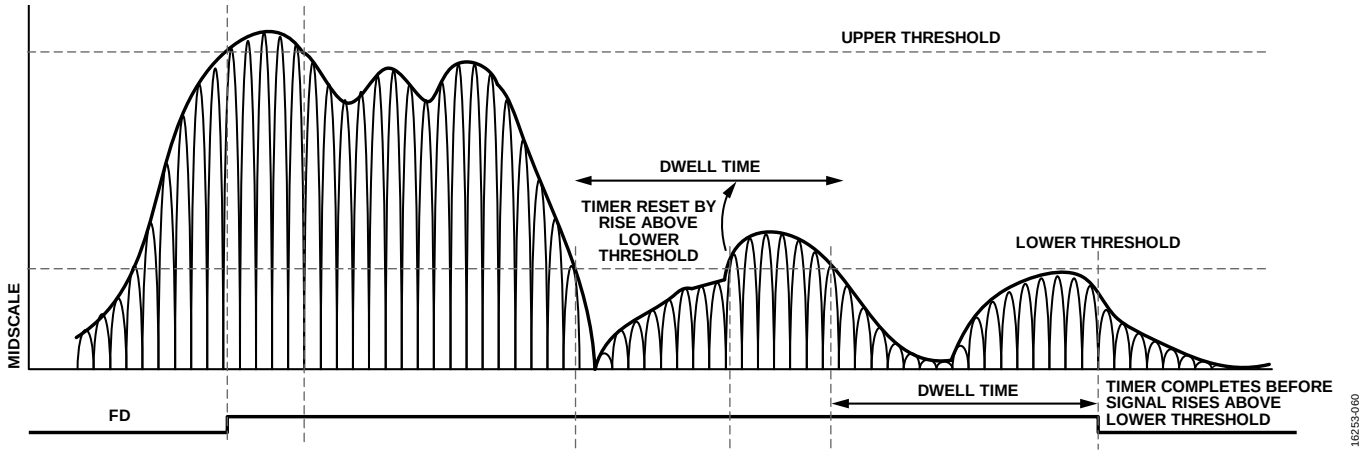


Figure 64. Threshold Settings for FD Signal

ADC APPLICATION MODES AND JESD204B Tx CONVERTER MAPPING

The AD9697 contains a configurable signal path that allows different features to be enabled for different applications. These features are controlled using the chip application mode register, Register 0x0200. The chip operating mode is controlled by Bits[3:0] in this register, and the chip Q ignore is controlled by Bit 5.

The AD9697 contains the following modes:

- Full bandwidth mode: 14-bit ADC core running at the full sample rate.
- DDC mode: up to four digital downconverter (DDC) channels.

After the chip application mode is selected, the output decimation ratio is set using the chip decimation ratio in Register 0x0201, Bits[3:0]. The output sample rate = ADC sample rate/the chip decimation ratio.

To support the different application layer modes, the AD9697 treats each sample stream (real, I, or Q) as originating from separate virtual converters.

Table 11 shows the number of virtual converters required and the transport layer mapping. Figure 65 shows the virtual converters and their relationship to the DDC outputs when complex outputs are used.

Each DDC channel outputs either two sample streams (I/Q) for the complex data components (real + imaginary), or one sample stream for real (I) data. The AD9697 can be configured to use up to eight virtual converters, depending on the DDC configuration.

The I/Q samples are always mapped in pairs with the I samples mapped to the first virtual converter and the Q samples mapped to the second virtual converter. With this transport layer mapping, the number of virtual converters are the same whether a single real converter is used along with a digital downconverter block producing I/Q outputs, or whether an analog downconversion is used with two real converters producing I/Q outputs.

Figure 66 shows a block diagram of the two scenarios described for I/Q transport layer mapping.

Table 11. Virtual Converter Mapping

No. of Virtual Converters Supported	Chip Operating Mode (Reg. 0x0200, Bits[3:0])	Chip Q Ignore (0x0200, Bit 5)	Virtual Converter Mapping							
			0	1	2	3	4	5	6	7
1	Full bandwidth mode (0x0)	Real or complex (0x0)	ADC samples	Unused	Unused	Unused	Unused	Unused	Unused	Unused
1	One DDC mode (0x1)	Real (I only) (0x1)	DDC 0 I samples	Unused	Unused	Unused	Unused	Unused	Unused	Unused
2	One DDC mode (0x1)	Complex (I/Q) (0x0)	DDC 0 I samples	DDC 0 Q samples	Unused	Unused	Unused	Unused	Unused	Unused
2	Two DDC mode (0x2)	Real (I only) (0x1)	DDC 0 I samples	DDC 1 I samples	Unused	Unused	Unused	Unused	Unused	Unused
4	Two DDC mode (0x2)	Complex (I/Q) (0x0)	DDC 0 I samples	DDC 0 Q samples	DDC 1 I samples	DDC 1 Q samples	Unused	Unused	Unused	Unused
4	Four DDC mode (0x3)	Real (I only) (0x1)	DDC 0 I samples	DDC 1 I samples	DDC 2 I samples	DDC 3 I samples	Unused	Unused	Unused	Unused
8	Four DDC mode (0x3)	Complex (I/Q) (0x0)	DDC 0 I samples	DDC 0 Q samples	DDC 1 I samples	DDC 1 Q samples	DDC 2 I samples	DDC 2 Q samples	DDC 3 I samples	DDC 3 Q samples

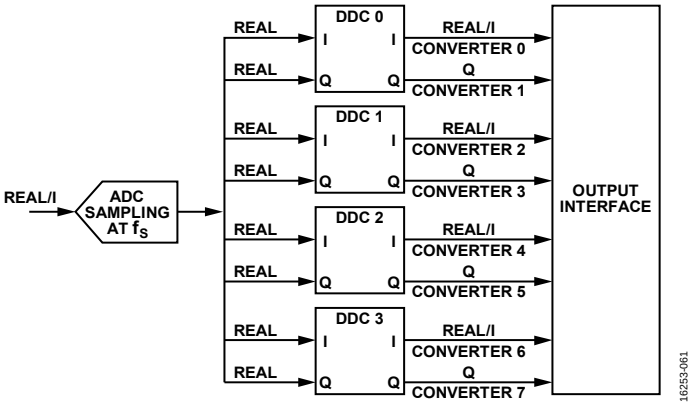


Figure 65. DDCs and Virtual Converter Mapping

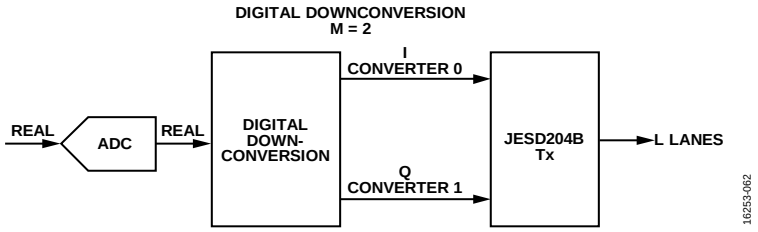


Figure 66. I/Q Transport Layer Mapping

PROGRAMMABLE FINITE IMPULSE RESPONSE (FIR) FILTERS

SUPPORTED MODES

The AD9697 supports the following modes of operation (the asterisk symbol (*) denotes convolution):

- Real 48-tap filter (see Figure 67)
  - DOUT[n] = DIN[n] × XY[n]
- Real 96-tap filter (see Figure 68)
  - DOUT[n] = DIN[n] × XY[n]
- Real set of two cascaded 24-tap filters (see Figure 69)
  - DOUT[n] = DIN[n] × X[n] × Y[n]

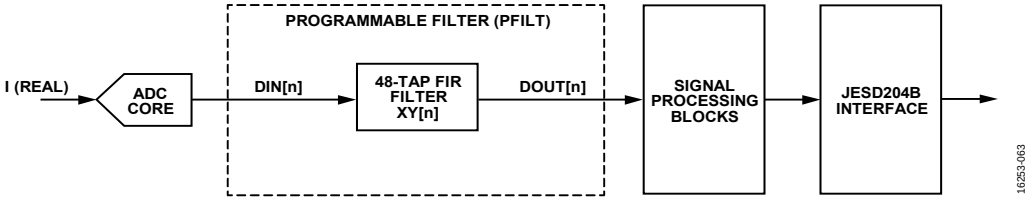


Figure 67. Real 48-Tap Filter Configuration

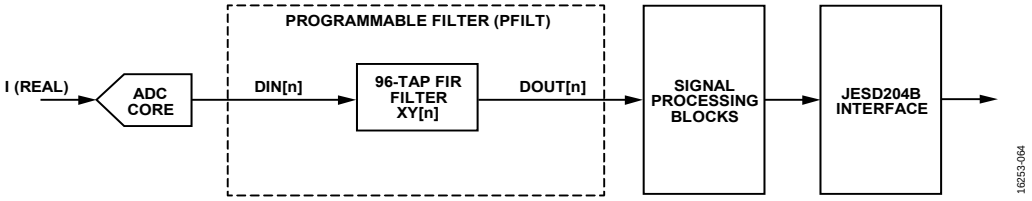


Figure 68. Real 96-Tap Filter Configuration

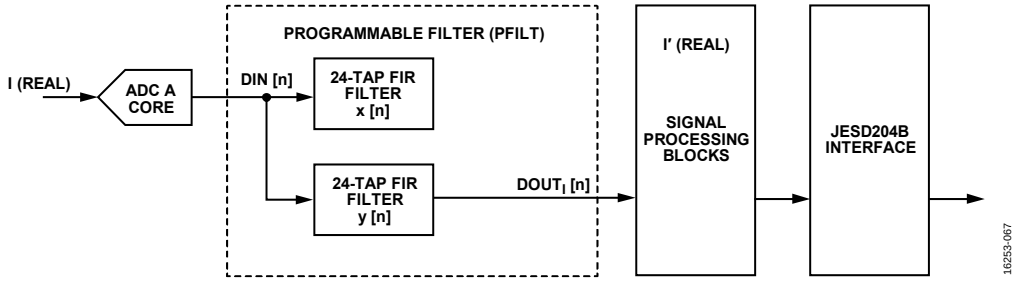


Figure 69. Real, Two Cascaded, 24-Tap Filter Configuration

PROGRAMMING INSTRUCTIONS

Use the following procedure to set up the programmable FIR filter:

1. Enable the sample clock to the device.
2. Configure the mode registers as follows:
   a. Set the I path mode (I mode) and gain in Register 0x0DF8 and Register 0x0DF9 (see Table 12 and Table 13). Only I Mode is available. Q Mode is not available on single-channel devices.
3. Wait at least 5 µs to allow the programmable filter to power up.
4. Program the I path coefficients to the internal shadow registers as follows:
   a. Program the XI coefficients in Register 0x0E00 to Register 0x0E2F (see Table 14).
   b. Program the YI coefficients in Register 0x0F00 to Register 0x0F2F (see Table 14).
   c. Program the tapped delay in Register 0x0F30 (note that this step is optional).
5. Set the chip transfer bit using either of the following methods (note that setting the chip transfer bit applies the programmed shadow coefficients to the filter):
   a. Via the register map by setting the chip transfer bit (Register 0x000F = 0x01).
   b. Via a GPIO pin, as follows:
      i. Configure one of the GPIO pin as the chip transfer bit in Register 0x0040 to Register 0x0042.
      ii. Toggle the GPIO pin to initiate the chip transfer (the rising edge is triggered).
6. When the I path mode register changes in Register 0x0DF8, all coefficients must be reprogrammed.

Table 12. Register 0x0DF8 Definition

Bits	Description
[7:3]	Reserved
[2:0]	Filter mode (I mode or Q mode) 000: filters bypassed 001: real 24-tap filter (X only) 010: real 48-tap filter (X and Y together) 100: real set of two cascaded 24-tap filters (X then Y cascaded) 111: real 96-tap filter (X and Y together)

Table 13. Register 0x0DF9 Definition

Bits	Description
7	Reserved
[6:4]	Y filter gain 110: −12 dB loss 111: −6 dB loss 000: 0 dB gain 001: 6 dB gain 010: 12 dB gain
3	Reserved
[2:0]	X filter gain 110: −12 dB loss 111: −6 dB loss 000: 0 dB gain 001: 6 dB gain 010: 12 dB gain

Table 14 shows the coefficient tables in Register 0x0E00 to Register 0x0F30. All coefficients are Q1.15 format (sign bit + 15 fractional bits).

Table 14. I Coefficient Table (Device Selection = 0x1)[1]

Addr.	Single 24-Tap Filter (I Mode [2:0] = 0x1)	Single 48-Tap Filter (I Mode [2:0] = 0x2)	Two Cascaded 24-Tap Filters (I Mode [2:0] = 0x4)	Single 96-Tap Filter (I Mode[2:0] = 0x7)
0x0E00	XI C0 [7:0]	XI C0 [7:0]	XI C0 [7:0]	XI C0 [7:0]
0x0E01	XI C0 [15:8]	XI C0 [15:8]	XI C0 [15:8]	XI C0 [15:8]
0x0E02	XI C1 [7:0]	XI C1 [7:0]	XI C1 [7:0]	XI C1 [7:0]
0x0E03	XI C1 [15:8]	XI C1 [15:8]	XI C1 [15:8]	XI C1 [15:8]
…	…	…	…	…
0x0E2E	XI C23 [7:0]	XI C23 [7:0]	XI C23 [7:0]	XI C23 [7:0]
0x0E2F	XI C23 [15:0]	XI C23 [15:0]	XI C23 [15:0]	XI C23 [15:0]
0x0F00	Unused	YI C24 [7:0]	YI C0 [7:0]	YI C24 [7:0]
0x0F01	Unused	YI C24 [15:8]	YI C0 [15:8]	YI C24 [15:8]
0x0F02	Unused	YI C25 [7:0]	YI C1 [7:0]	YI C25 [7:0]
0x0F03	Unused	YI C25 [15:8]	YI C1 [15:8]	YI C25 [15:8]
…	…	…	…	…
0x0F2E	Unused	YI C47 [7:0]	YI C23 [7:0]	YI C47 [7:0]
0x0F2F	Unused	YI C47 [15:0]	YI C23 [15:0]	YI C47 [15:0]
0x0F30	Unused	Unused	Unused	Unused

[1] XI Cn means I Path X Coefficient n, and YI Cn means I Path Y Coefficient n.

DIGITAL DOWNCONVERTER (DDC)

The AD9697 includes four digital downconverters (DDC 0 to DDC 3) that provide filtering and reduce the output data rate. This digital processing section includes an NCO, multiple decimating FIR filters, a gain stage, and a complex to real conversion stage. Each of these processing blocks has control lines that allow it to be independently enabled and disabled to provide the desired processing function. The digital downconverter can be configured to output either real data or complex output data.

The DDCs output a 16-bit stream. To enable this operation, the converter number of bits, N, is set to a default value of 16, even though the analog core only outputs 14 bits. In full bandwidth operation, the ADC outputs are the 14-bit word followed by two zeros, unless the tail bits are enabled.

DDC I/Q OUTPUT SELECTION

Each DDC channel has two output ports that can be paired to support both real and complex outputs. For real output signals, only the DDC Output Port I is used (the DDC Output Port Q is invalid). For complex I/Q output signals, both DDC Output Port I and DDC Output Port Q are used.

The I/Q outputs to each DDC channel are controlled by the DDC complex to real enable bit, Bit 3, in the DDC control registers (Register 0x0310, Register 0x0330, Register 0x0350 and Register 0x0370).

The chip Q ignore bit in the chip mode register (Register 0x0200, Bit 5) controls the chip output muxing of all the DDC channels. When all DDC channels use real outputs, set this bit high to ignore all DDC Q output ports. When any of the DDC channels are set to use complex I/Q outputs, the user must clear this bit to use both DDC Output Port I and DDC Output Port Q. For more information, see Figure 86.

DDC GENERAL DESCRIPTION

The four DDC blocks extract a portion of the full digital spectrum captured by the ADC(s). They are intended for IF sampling or oversampled baseband radios requiring wide bandwidth input signals.

Each DDC block contains the following signal processing stages:

- Frequency translation stage (optional)
- Filtering stage
- Gain stage (optional)
- Complex to real conversion stage (optional)

Frequency Translation Stage (Optional)

This stage consists of a phase coherent NCO and quadrature mixers that can be used for frequency translation of both real or complex input signals. The phase coherent NCO allows an infinite number of frequency hops that are all referenced back to a single synchronization event. It also includes 16 shadow registers for fast switching applications. This stage shifts a portion of the available digital spectrum down to baseband.

Filtering Stage

After shifting down to baseband, this stage decimates the frequency spectrum using multiple low pass finite impulse response (FIR) filters for rate conversion. The decimation process lowers the output data rate, which in turn reduces the output interface rate.

Gain Stage (Optional)

Due to losses associated with mixing a real input signal down to baseband, this stage compensates by adding an additional 0 dB or 6 dB of gain.

Complex to Real Conversion Stage (Optional)

When real outputs are necessary, this stage converts the complex outputs back to real by performing an $f_S/4$ mixing operation plus a filter to remove the complex component of the signal.

Figure 70 shows the detailed block diagram of the DDCs implemented in the AD9697.

Figure 71 shows an example usage of one of the four DDC channels with a real input signal and four half-band filters (HB4 + HB3 + HB2 + HB1) used. It shows both complex (decimate by 16) and real (decimate by 8) output options.

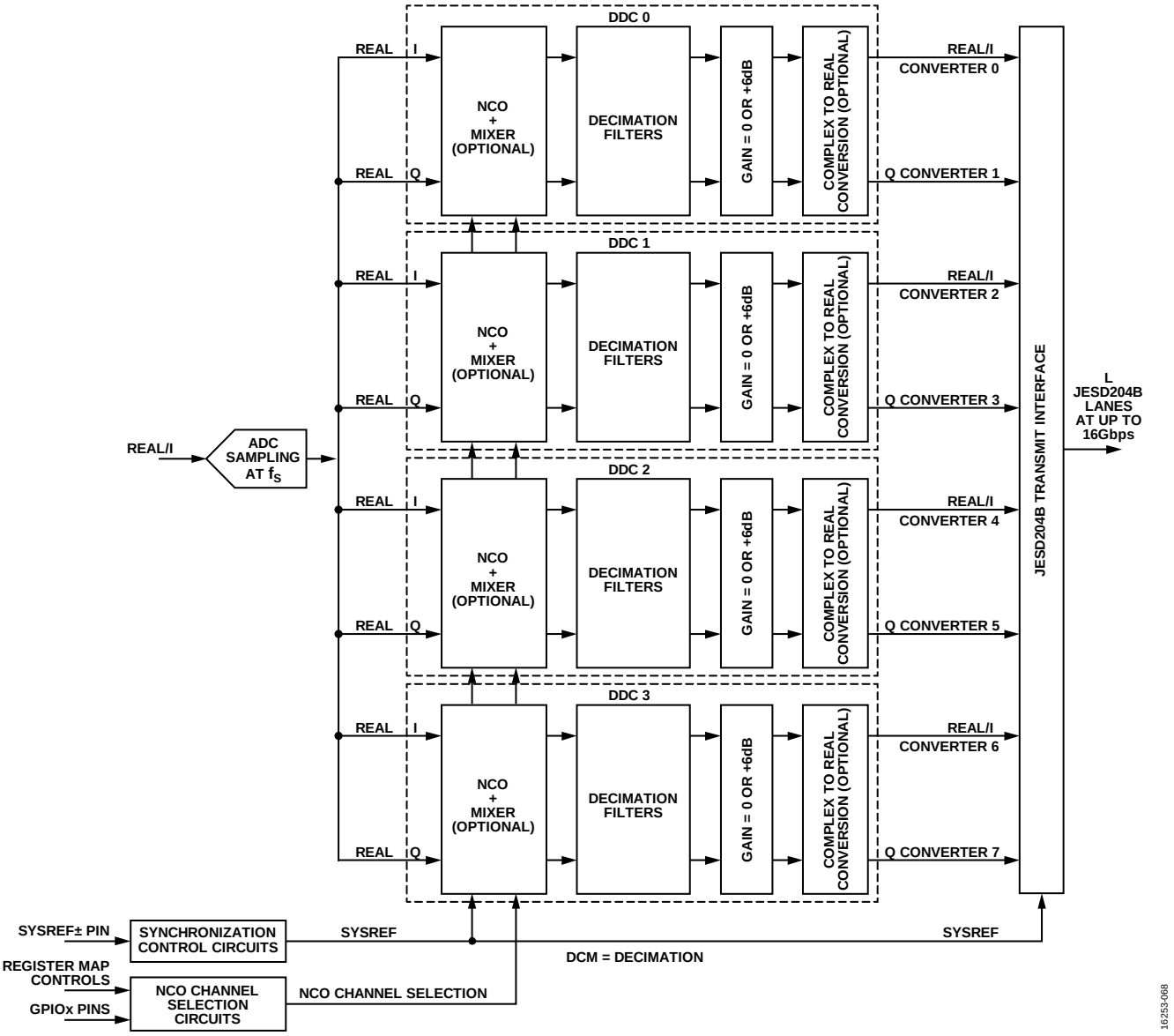


Figure 70. DDC Detailed Block Diagram

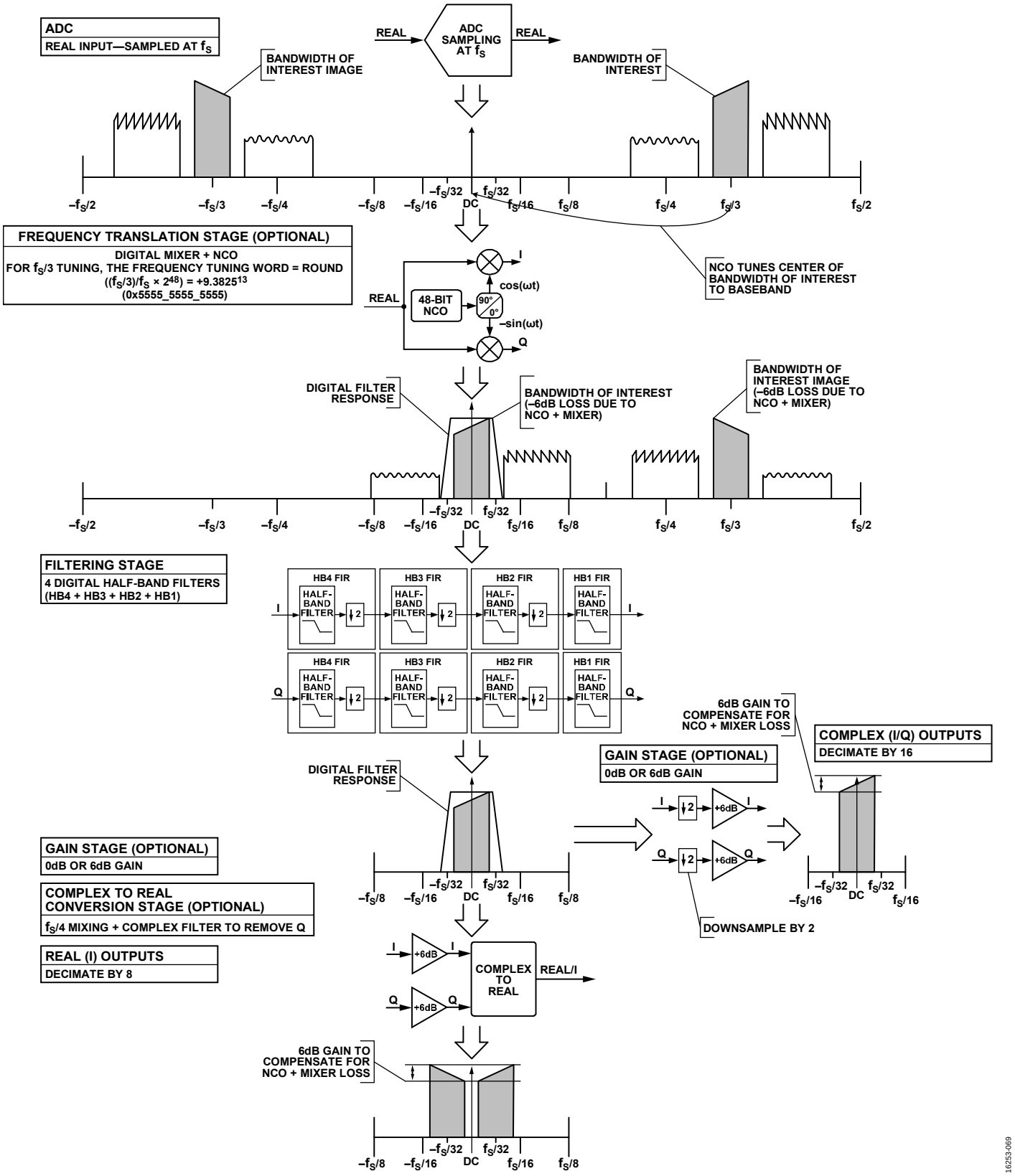


Figure 71. DDC Theory of Operation Example (Real Input)

DDC FREQUENCY TRANSLATION

DDC Frequency Translation General Description

Frequency translation is accomplished by using a 48-bit complex NCO with a digital quadrature mixer. This stage translates either a real or complex input signal from an IF to a baseband complex digital output (carrier frequency = 0 Hz).

The frequency translation stage of each DDC can be controlled individually and supports four different IF modes using Bits[5:4] of the DDC control registers (Register 0x0310, Register 0x0330, Register 0x0350, and Register 0x0370). These IF modes are as follows:

- Variable IF mode
- 0 Hz IF or zero IF (ZIF) mode
- $f_S/4$ Hz IF mode
- Test mode

Variable IF Mode

NCO and mixers are enabled. NCO output frequency can be used to digitally tune the IF frequency.

0 Hz IF (ZIF) Mode

The mixers are bypassed, and the NCO is disabled.

$f_S/4$ Hz IF Mode

The mixers and the NCO are enabled in special downmixing by $f_S/4$ mode to save power.

Test Mode

Input samples are forced to 0.999 to positive full scale. The NCO is enabled. This test mode allows the NCOs to directly drive the decimation filters.

Figure 72 shows an example of the frequency translation stage for real inputs.

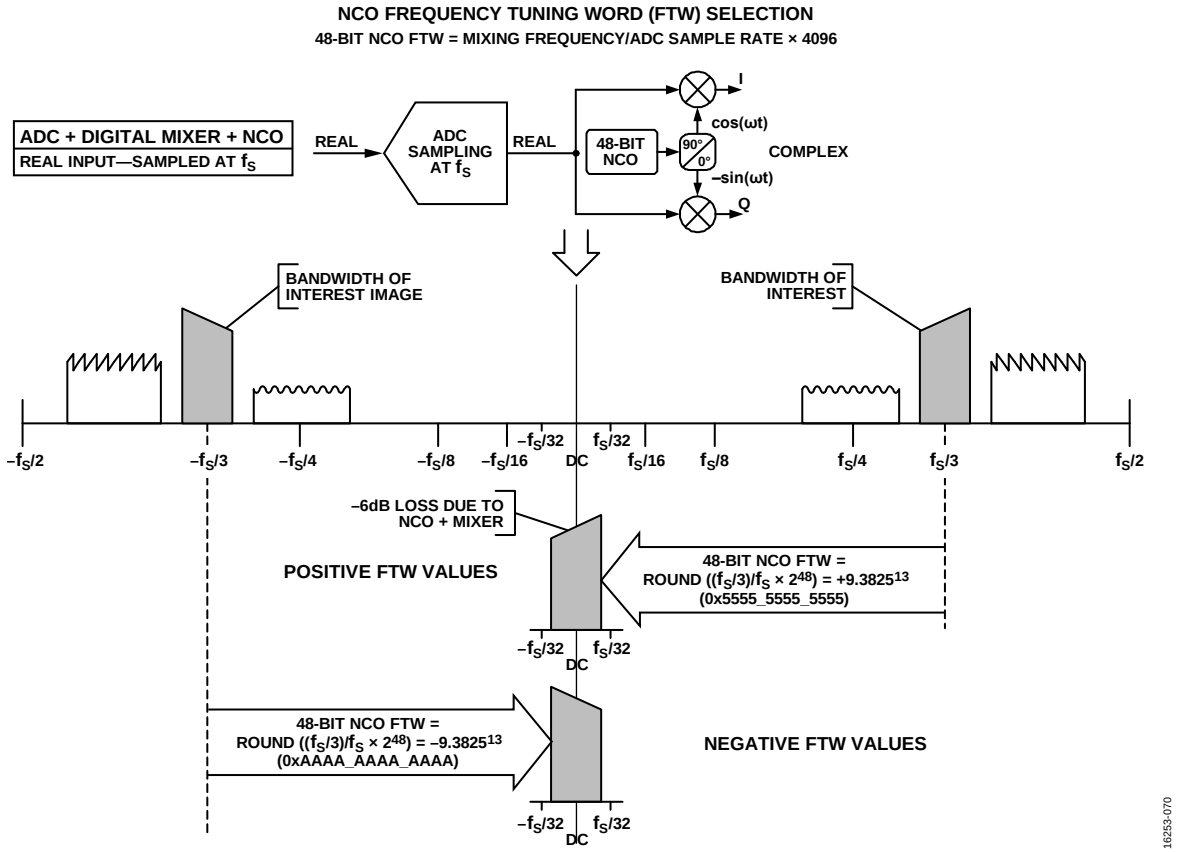


Figure 72. DDC NCO Frequency Tuning Word Selection—Real Inputs

DDC NCO Description

Each DDC contains one NCO. Each NCO enables the frequency translation process by creating a complex exponential frequency ($e^{-j\omega ct}$), which can be mixed with the input spectrum to translate the desired frequency band of interest to dc, where it can be filtered by the subsequent low-pass filter blocks to prevent aliasing.

When placed in variable IF mode, the NCO supports two different additional modes.

DDC NCO Programmable Modulus Mode

This mode supports >48-bit frequency tuning accuracy for applications that require exact rational (M/N) frequency synthesis at a single carrier frequency. In this mode, the NCO is set up by providing the following:

- 48-bit frequency tuning word (FTW)
- 48-bit Modulus A word (MAW)
- 48-bit Modulus B word (MBW)
- 48-bit phase offset word (POW)

DDC NCO Coherent Mode

This mode allows an infinite number of frequency hops where the phase is referenced to a single synchronization event at Time 0. This mode is useful when phase coherency must be maintained when switching between different frequency bands. In this mode, the user can switch to any tuning frequency without the need to reset the NCO. Although only one FTW is required, the NCO contains 16 shadow registers for fast-switching applications. Selection of the shadow registers is controlled by the CMOS GPIO pins or through the register map of the SPI. In this mode, the NCO can be set up by providing the following:

- Up to sixteen 48-bit FTWs.
- Up to sixteen 48-bit POWs.
- The 48-bit MAW must be set to zero in coherent mode.

Figure 73 shows a block diagram of one NCO and its connection to the rest of the design. The coherent phase accumulator block contains the logic that allows an infinite number of frequency hops.

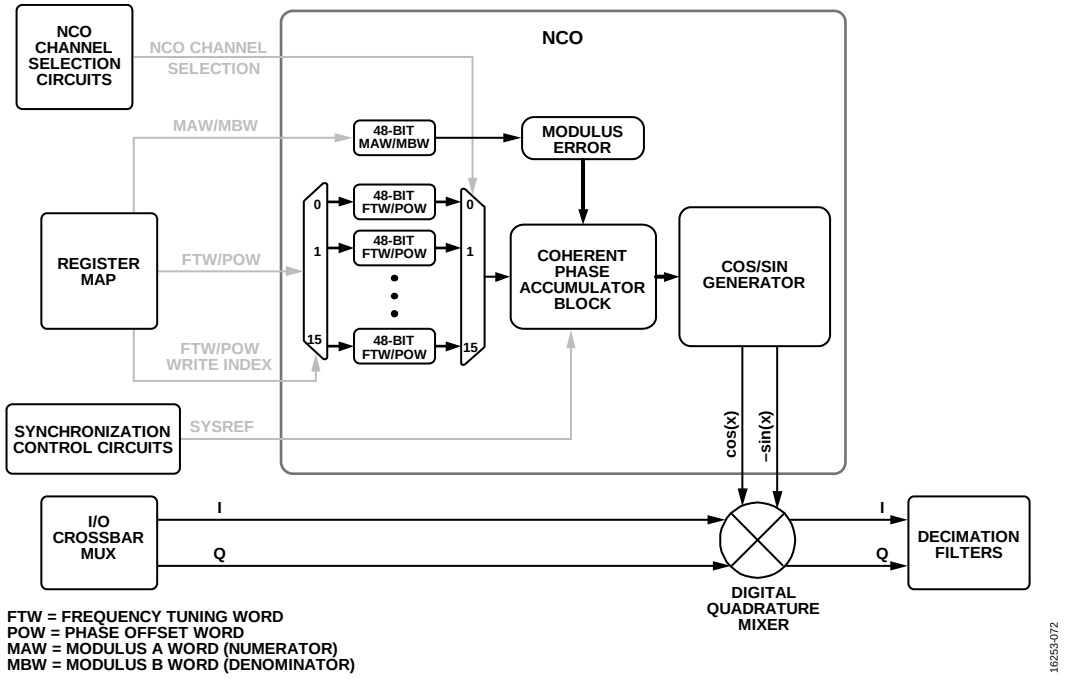


Figure 73. NCO + Mixer Block Diagram

NCO FTW/POW/MAW/MAB Description

The NCO frequency value is determined by the following settings:

- 48-bit twos complement number entered in the FTW
- 48-bit unsigned number entered in the MAW
- 48-bit unsigned number entered in the MBW

Frequencies between $-f_S/2$ and $+f_S/2$ ($f_S/2$ excluded) are represented using the following values:

- FTW = 0x8000_0000_0000 and MAW = 0x0000_0000_0000 represents a frequency of $-f_S/2$.
- FTW = 0x0000_0000_0000 and MAW = 0x0000_0000_0000 represents dc (frequency is 0 Hz).
- FTW = 0x7FFF_FFFF_FFFF and MAW = 0x0000_0000_0000 represents a frequency of $+f_S/2$.

NCO FTW/POW/MAW/MAB Programmable Modulus Mode

For programmable modulus mode, the MAW must be set to a nonzero value (not equal to 0x0000_0000_0000). This mode is only needed when frequency accuracy of >48 bits is required. One example of a rational frequency synthesis requirement that requires >48 bits of accuracy is a carrier frequency of 1/3 the sample rate. When frequency accuracy of ≤48 bits is required, coherent mode must be used (see the NCO FTW/POW/MAW/MAB Coherent Mode section).

In programmable modulus mode, the FTW, MAW, and MBW must satisfy the following four equations (for a detailed description of the programmable modulus feature, see the DDS architecture described in the AN-953 Application Note):

$$\frac{mod(f_C, f_S)}{f_S} = \frac{M}{N} = \frac{FTW + \frac{MAW}{MBW}}{2^{48}} \quad (1)$$

$$FTW = floor\left(2^{48}\frac{mod(f_C, f_S)}{f_S}\right) \quad (2)$$

$$MAW = \text{mod}(2^{48} \times M, N) \quad (3)$$

$$MBW = N \quad (4)$$

where:
f_C is the desired carrier frequency.
f_S is the ADC sampling frequency.
M is the integer representing the rational numerator of the frequency ratio.
N is the integer representing the rational denominator of the frequency ratio.
FTW is the 48-bit twos complement number representing the NCO FTW.
MAW is the 48-bit unsigned number representing the NCO MAW (must be $<2^{47}$).
MBW is the 48-bit unsigned number representing the NCO MBW.
mod(x) is a remainder function. For example mod(110,100) = 10 and for negative numbers, mod(−32,10)= −2.
floor(x) is defined as the largest integer less than or equal to x. For example, floor(3.6) = 3.

Equation 1 to Equation 4 apply to the aliasing of signals in the digital domain (that is, aliasing introduced when digitizing analog signals).

M and N are integers reduced to their lowest terms. MAW and MBW are integers reduced to their lowest terms. When MAW is set to zero, the programmable modulus logic is automatically disabled.

For example, if the ADC sampling frequency (f_S) is 1300 MSPS and the carrier frequency (f_C) is 417.8 MHz, then,

$$\frac{\text{mod}(417.8,1300)}{1300} = \frac{M}{N} = \frac{2089}{6250}$$

$$FTW = floor\left(2^{48}\frac{\text{mod}(2417.8,1300)}{1300}\right)$$

= 0x5590_C0AD_03D9

MAW = mod($2^{48} \times 2089$, 6250) = 0x0000_0000_1117

MBW = 0x0000_0000_186A

The actual carrier frequency can be calculated based on the following equation:

$$f_{C_ACTUAL} = \frac{FTW + \frac{MAW}{MBW} \times f_S}{2^{48}}$$

For the previous example, the actual carrier frequency (f_{C_ACTUAL}) is

$$f_{C_ACTUAL} = \frac{\text{0x5590_C0AD_03D9} + \frac{\text{0x0000_0000_1117}}{\text{0x0000_0000_186A}}}{2^{48}} \times$$

1300 MHz = 417.8MHz

A 48-bit POW is available for each NCO to create a known phase relationship between multiple chips or individual DDC channels inside the chip.

While in programmable modulus mode, the FTW and POW registers can be updated at any time while still maintaining deterministic phase results in the NCO. However, the following procedure must be followed to update the MAW and/or MBW registers to ensure proper operation of the NCO:

1. Write to the MAW and MBW registers for all the DDCs.
2. Synchronize the NCOs either through the DDC soft reset bit accessible through the SPI or through the assertion of the SYSREF± pin (see the Memory Map section).

NCO FTW/POW/MAW/MAB Coherent Mode

For coherent mode, the NCO MAW must be set to zero (0x0000_0000_0000). In this mode, the NCO FTW can be calculated by the following equation:

$$FTW = \text{round}(2^{48} \frac{\text{mod}(f_C, f_S)}{f_S}) \quad (5)$$

where:
FTW is the 48-bit twos complement number representing the NCO FTW.
f_S is the ADC sampling frequency.
f_C is the desired carrier frequency.
mod() is a remainder function. For example mod(110,100) = 10 and for negative numbers, mod(−32,10) = −2.
round() is a rounding function. For example round(3.6) = 4 and for negative numbers, round(−3.4)= −3.

Note that Equation 5 applies to the aliasing of signals in the digital domain (that is, aliasing introduced when digitizing analog signals). The MAW must be set to zero to use coherent mode. When MAW is zero, the programmable modulus logic is automatically disabled.

For example, if the ADC sampling frequency (f_S) is 1300 MSPS and the carrier frequency (f_C) is 417.3333 MHz, then,

$$NCO_FTW = \text{round}\left(2^{48} \frac{\text{mod}(417.33331300}{1300}\right) =$$

0x5578_49CE_E73F

The actual carrier frequency can be calculated based on the following equation:

$$f_{C_ACTUAL} = (FTW \times f_S)/2^{48}$$

For the previous example, the actual carrier frequency (f_{C_ACTUAL}) is

$$f_{C_ACTUAL} = (0x5578_49CE_E73F \times 1300)/2^{48} = 417.33 \text{ MHz}$$

A 48-bit POW is available for each NCO to create a known phase relationship between multiple chips or individual DDC channels inside the chip.

While in coherent mode, the FTW and POW registers can be updated at any time while still maintaining deterministic phase results in the NCO.

NCO Channel Selection

When configured in coherent mode, only one FTW is required in the NCO. In this mode, the user can switch to any tuning frequency without the need to reset the NCO by writing to the FTW directly. However, for fast switching applications, where either all FTWs are known beforehand or it is possible to queue up the next set of FTWs, the NCO contains 16 additional shadow registers (see Figure 74). These shadow registers are hereafter referred to as the NCO channels.

Figure 74 shows a simplified block diagram of the NCO channel selection block.

Only one NCO channel is active at a time, and NCO channel selection is controlled either by the CMOS GPIO pins or through the register map.

Each NCO channel selector supports three different modes, as described in the following sections.

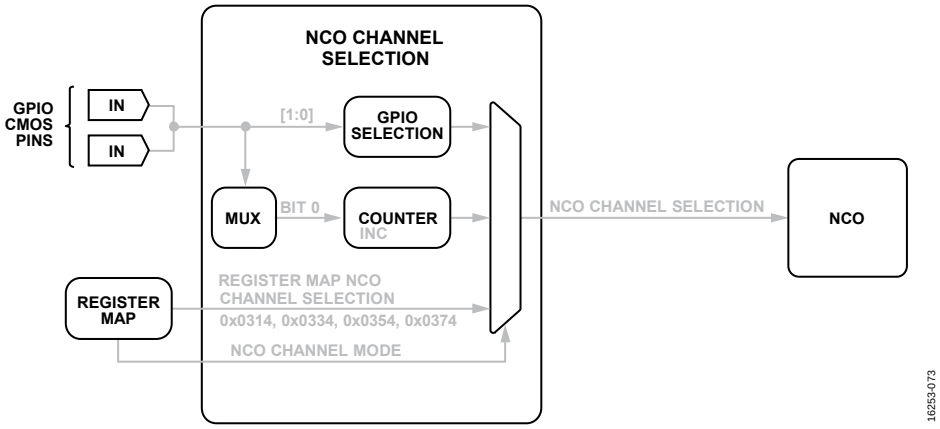


Figure 74. NCO Channel Selection Block

GPIO Level Control Mode

The GPIOx pins determine the exact NCO channel selected.

The following procedure must be followed to use GPIO level control for NCO channel selection:

3. Configure one or more GPIOx pins as NCO channel selection inputs. GPIOx pins not configured as NCO channel selection are internally tied low.
   a. To use GPIO1, write Bits[2:0] in Register 0x0040 to 0x6 and Bits[3:0] in Register 0x0041 to 0x0.
   b. To use GPIO2, write Bits[5:3] in Register 0x0040 to 0x6 and Bits [7:4] in Register 0x0041 to 0x0.
4. Configure the NCO channel selector in GPIO level control mode by setting Bits[7:4] in the NCO control registers (Register 0x0314, Register 0x0334, Register 0x0354, and Register 0x0374) to 0x1 through 0x6, depending on the desired GPIO pin ordering.
5. Select the desired NCO channel through the GPIOx pins.

GPIO Edge Control Mode

Low to high transition on the GPIOx pin determines the exact NCO channel selected. The internal channel selection counter is reset by either SYSREF± or the DDC soft reset.

The following procedure must be followed to use GPIO edge control for NCO channel selection:

6. Configure one or more GPIOx pins as NCO channel selection inputs.
   a. To use GPIO1, write Bits[2:0] in Register 0x0040 to 0x6 and Bits[3:0] in Register 0x0041 to 0x0.
   b. To use GPIO2, write Bits[5:3] in Register 0x0040 to 0x6 and Bits[7:4] in Register 0x0041 to 0x0.
7. Configure the NCO channel selector in GPIO edge control mode by setting Bits[7:4] in the NCO control registers (Register 0x0314, Register 0x0334, Register 0x0354, and Register 0x0374) to 0x8 through 0xB, depending on the desired GPIOx pin.
8. Configure the wrap point for the NCO channel selection by setting Bits[3:0] in the NCO control registers (Register 0x0314, Register 0x0334, Register 0x0354, and Register 0x0374). A value of 4 causes the channel selection to wrap at Channel 4 (0, 1, 2, 3, 4, 0, 1, 2, 3, 4, and so on).
9. Transition the selected GPIOx pin from low to high to increment the NCO channel selection.

Register Map Mode

NCO channel selection is controlled directly through the register map.

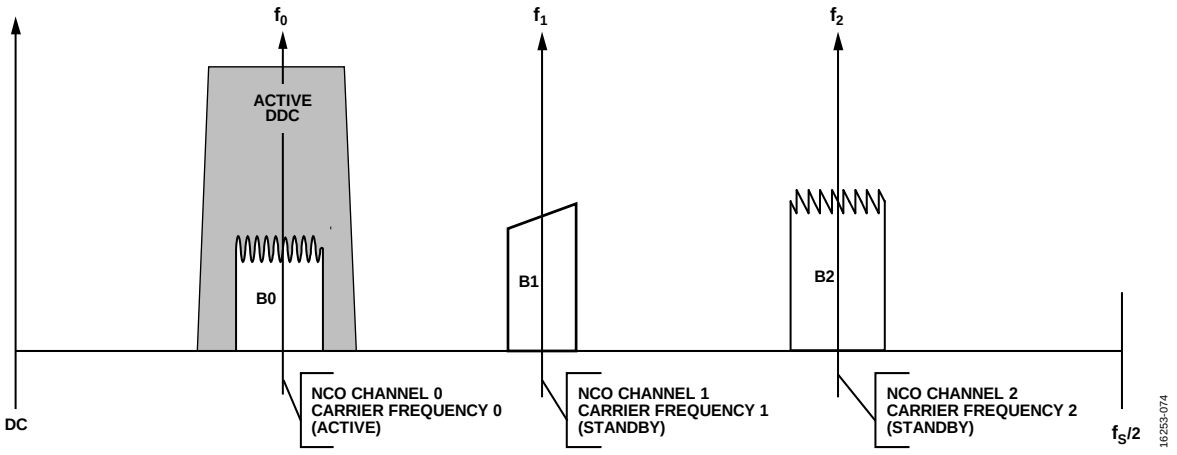


Figure 75. NCO Coherent Mode with Three NCO Channels (B0 Selected)

Figure 75 shows an example use case for coherent mode utilizing three NCO channels. In this example, NCO Channel 0 is actively downconverting bandwidth 0 (B0) while NCO Channel 1 and Channel 2 are in standby and tuned to Bandwidth 1 and Bandwidth 2 (B1 and B2), respectively.

The phase coherent NCO switching feature allows an infinite number of frequency hops that are all phase coherent. The initial phase of the NCO is established at time t0 from SYSREF± synchronization. Switching the NCO FTW does not affect the phase. With this feature, only one FTW is required; however, the user may want to use all 16 channels to queue up the next hop.

After SYSREF± synchronization at start-up, all NCOs across multiple chips are inherently synchronized.

Setting Up the Multichannel NCO Feature

The first step to configure the multichannel NCO is to program the FTWs. The AD9697 memory map has a FTW index register for each DDC. This index determines which NCO channel receives the FTW from the register map. The following sequence describes the method for programming the FTWs.

1. Write the FTW index register with the desired DDC channel.
2. Write the FTW with the desired value. This value is applied to the NCO channel index mentioned in Step 1.
3. Repeat Step 1 and Step 2 for other NCO channels.

After setting the FTWs, the user must then select an active NCO channel. This selection can be done either through the SPI registers or through the external GPIOx pins. The following sequence describes the method for selecting the active NCO channel using SPI.

1. Set the NCO channel selection mode (Bits[7:4]) in Register 0x0314, Register 0x0334, Register 0x0354, and Register 0x0374 to 0x0 to enable SPI selection.
2. Choose the active NCO channel (Bits[3:0]) in Register 0x0314, Register 0x0334, Register 0x0354, and Register 0x0374.

The following sequence describes the method for selecting the active NCO channel using GPIOx CMOS pins.

1. Set NCO channel selection mode (Bits[7:4]) in Register 0x0314, Register 0x0334, Register 0x0354, and Register 0x0374 to a nonzero value to enable GPIOx pin selection.
2. Configure the GPIOx pins as NCO channel selection inputs by writing to Register 0x0040, Register 0x0041, and Register 0x0042.
3. NCO switching is done by externally controlling the GPIOx CMOS pins.

NCO Synchronization

Each NCO contains a separate phase accumulator word (PAW). The initial reset value of each PAW is set to zero and increments every clock cycle. The instantaneous phase of the NCO is calculated using the PAW, FTW, MAW, MBW, and POW. Due to this architecture, the FTW and POW registers can be updated at any time while still maintaining deterministic phase results in the PAW of the NCO.

Two methods can be used to synchronize multiple PAWs within the chip:

- Using the SPI. Use the DDC soft reset bit in the DDC synchronization control register (Register 0x0300, Bit 4) to reset all the PAWs in the chip. This reset is accomplished by setting the DDC soft reset bit high, and then setting this bit low. Note that this method can only be used to synchronize DDC channels within the same chip.
- Using the SYSREF± pin. When the SYSREF± pin is enabled in the SYSREF± control registers (Register 0x0120 and Register 0x0121), and the DDC synchronization is enabled in the DDC synchronization control register (Register 0x0300, Bits[1:0]), any subsequent SYSREF± event resets all the PAWs in the chip. Note that this method can be used to synchronize DDC channels within the same chip or DDC channels within separate chips.

NCO Multichip Synchronization

In some applications, it is necessary to synchronize all the NCOs and local multiframe clocks (LMFCs) within multiple devices in a system. For applications requiring multiple NCO tuning frequencies in the system, a designer likely needs to generate a single SYSREF± pulse at all devices simultaneously. For many systems, generating or receiving a single-shot SYSREF± pulse at all devices is challenging because of the following factors:

- Enabling or disabling the SYSREF± pulse is often an asynchronous event.
- Not all clock generation chips support this feature.

For these reasons, the AD9697 contains a synchronization triggering mechanism that allows the following:

- Multichip synchronization of all NCOs and LMFCs at system startup.
- Multichip synchronization of all NCOs after applying new tuning frequencies during normal operation.

The synchronization triggering mechanism uses a master/slave arrangement, as shown in Figure 76.

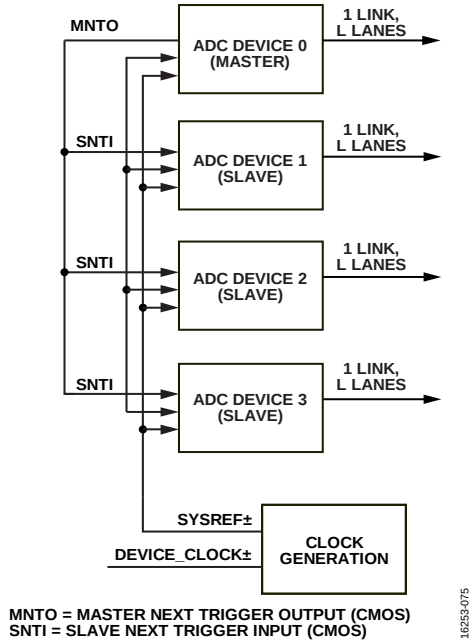


Figure 76. System Using Master/Slave Synchronization Triggering

Each device has an internal next synchronization trigger enable (NSTE) signal that controls whether the next SYSREF± signal causes a synchronization event. Slave ADC devices must source their NSTE from an external slave next trigger input (SNTI) pin. Master devices can either use an external master next trigger output (MNTO) pin (default setting), or use an external SNTI pin.

See Table 44 (Register 0x0041 and Register 0x0042) to configure the FD/GPIOx pins for this operation.

NCO Multichip Synchronization at Startup

Figure 77 shows a timing diagram along with the required sequence of events for NCO multichip synchronization using triggering and SYSREF± at startup. Using this startup sequence synchronizes all the NCOs and LMFCs in the system at once.

NCO Multichip Synchronization During Normal Operation

See the NCO Multichip Synchronization section.

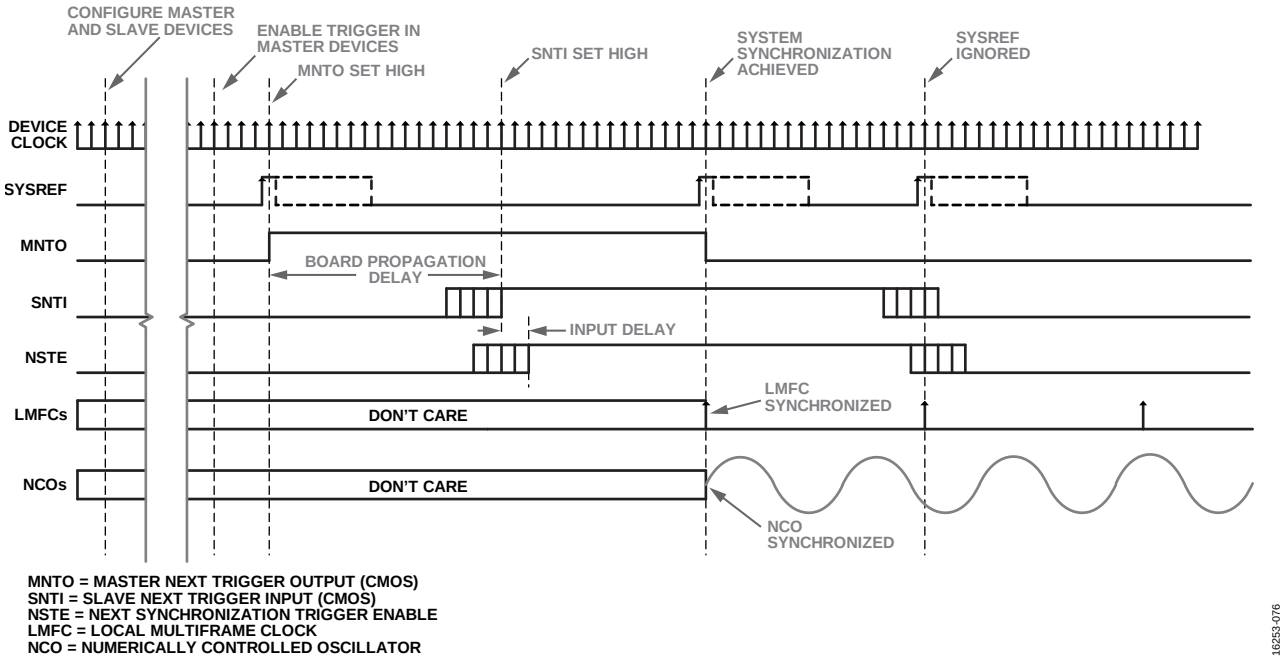


Figure 77. NCO Multichip Synchronization at Startup (Using Triggering and SYSREF±)

DDC Mixer Description

When not bypassed (Register 0x0200 ≠ 0x00), the digital quadrature mixer performs a similar operation to an analog quadrature mixer. It performs the downconversion of the input signal by using the NCO frequency as a local oscillator. Because the input of the DDC is a real signal, a real mixer operation (with two multipliers) is performed.

DDC NCO + Mixer Loss and SFDR

When mixing a real input signal down to baseband, −6 dB of loss is introduced in the signal due to filtering of the negative image. An additional −0.05 dB of loss is introduced by the NCO. The total loss of a real input signal mixed down to baseband is −6.05 dB. For this reason, it is recommended that the user compensate for this loss by enabling the 6 dB of gain in the gain stage of the DDC to recenter the dynamic range of the signal within the full scale of the output bits (see the DDC Gain Stage section for more information).

The worst case spurious signal from the NCO is greater than 102 dBc SFDR for all output frequencies.

DDC DECIMATION FILTERS

After the frequency translation stage, there are multiple decimation filter stages used to reduce the output data rate. After the carrier of interest is tuned down to dc (carrier frequency = 0 Hz), these filters efficiently lower the sample rate, while providing sufficient alias rejection from unwanted adjacent carriers around the bandwidth of interest.

Figure 78 shows a simplified block diagram of the decimation filter stage, and Table 15 describes the filter characteristics of the different FIR filter blocks.

Table 16 and Table 17 show the different filter configurations selectable by including different filters. In all cases, the DDC filtering stage provides 80% of the available output bandwidth, <±0.005 dB of pass-band ripple, and >100 dB of stop band alias rejection.

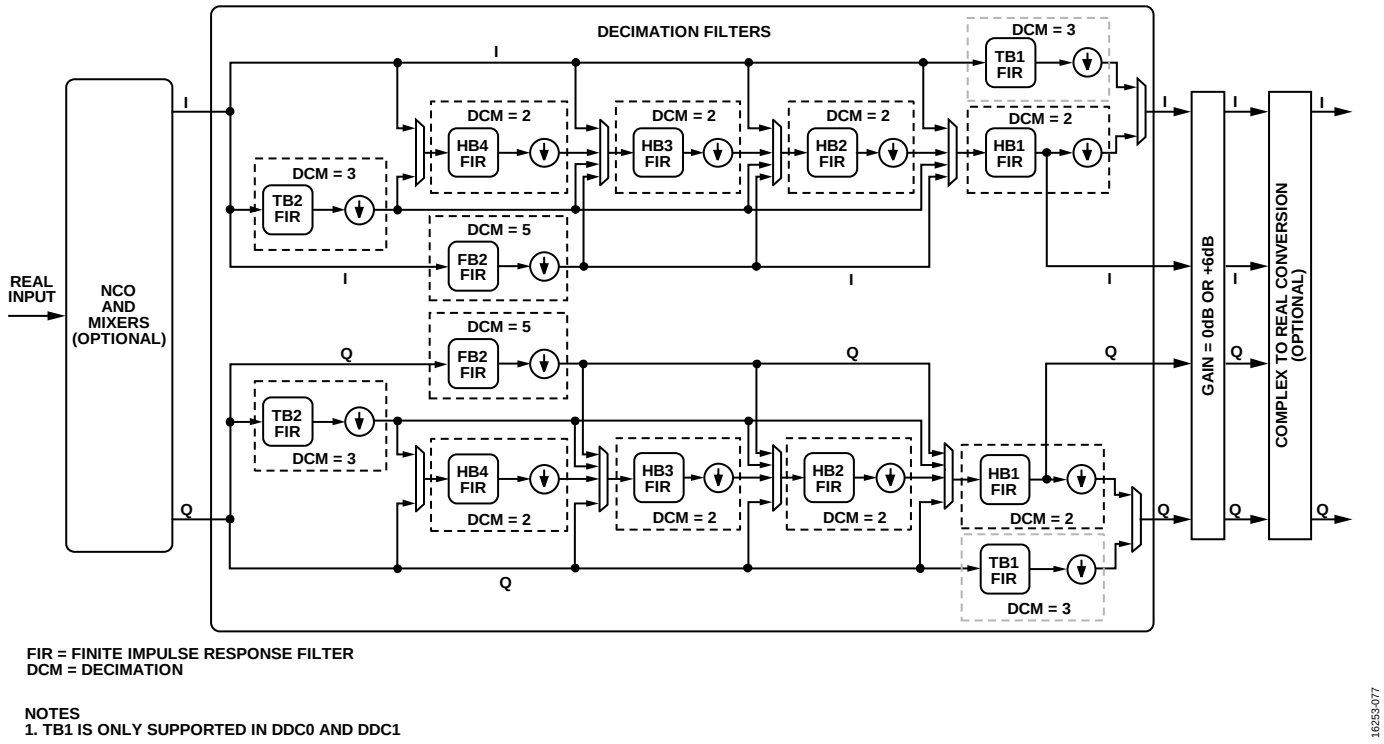


Figure 78. DDC Decimation Filter Block Diagram

Table 15. DDC Decimation Filter Characteristics

Filter Name	Filter Type	Decimation Ratio	Pass Band (rad/sec)	Stop Band (rad/sec)	Pass-Band Ripple (dB)	Stop-Band Attenuation (dB)
HB4	FIR low-pass	2	$0.1 \times \pi/2$	$1.9 \times \pi/2$	<±0.001	>100
HB3	FIR low-pass	2	$0.2 \times \pi/2$	$1.8 \times \pi/2$	<±0.001	>100
HB2	FIR low-pass	2	$0.4 \times \pi/2$	$1.6 \times \pi/2$	<±0.001	>100
HB1	FIR low-pass	2	$0.8 \times \pi/2$	$1.2 \times \pi/2$	<±0.001	>100
TB2	FIR low-pass	3	$0.4 \times \pi/3$	$1.6 \times \pi/3$	<±0.002	>100
TB1[1]	FIR low-pass	3	$0.8 \times \pi/3$	$1.2 \times \pi/3$	<±0.005	>100
FB2	FIR low-pass	5	$0.4 \times \pi/5$	$1.6 \times \pi/5$	<±0.001	>100

[1] TB1 is only supported in DDC 0 and DDC 1.

Table 16. DDC Filter Configurations[1]

ADC Sample Rate	DDC Filter Configuration	Real (I) Output		Complex (I/Q) Outputs		Alias Protected Bandwidth	Ideal SNR Improvement (dB)[2]
		Decimation Ratio	Sample Rate	Decimation Ratio	Sample Rate		
f_S	HB1	1	f_S	2	$f_S/2$ (I) + $f_S/2$ (Q)	$f_S/2 \times 80\%$	1
f_S	TB1[3]	N/A	N/A	3	f $f_S/3$ (I) + $f_S/3$ (Q)	$f_S/3 \times 80\%$	2.7
f_S	HB2 + HB1	2	$f_S/2$	4	$f_S/4$ (I) + $f_S/4$ (Q)	$f_S/4 \times 80\%$	4
f_S	TB2 + HB1	3	$f_S/3$	6	$f_S/6$ (I) + $f_S/6$ (Q)	$f_S/6 \times 80\%$	5.7
f_S	HB3 + HB2 + HB1	4	$f_S/4$	8	$f_S/8$ (I) + $f_S/8$ (Q)	$f_S/8 \times 80\%$	7
f_S	FB2 + HB1	5	$f_S/5$	10	$f_S/10$ (I) + $f_S/10$ (Q)	$f_S/10 \times 80\%$	8
f_S	TB2 + HB2 + HB1	6	$f_S/6$	12	$f_S/12$ (I) + $f_S/12$ (Q)	$f_S/12 \times 80\%$	8.8
f_S	FB2 + TB1[3]	N/A	N/A	15	$f_S/15$ (I) + $f_S/15$ (Q)	$f_S/15 \times 80\%$	9.7
f_S	HB4 + HB3 + HB2 + HB1	8	$f_S/8$	16	$f_S/16$ (I) + $f_S/16$ (Q)	$f_S/16 \times 80\%$	10
f_S	FB2 + HB2 + HB1	10	$f_S/10$	20	$f_S/20$ (I) + $f_S/20$ (Q)	$f_S/20 \times 80\%$	11
f_S	TB2 + HB3 + HB2 + HB1	12	$f_S/12$	24	$f_S/24$ (I) + $f_S/24$ (Q)	$f_S/24 \times 80\%$	11.8
f_S	HB2 + FB2 + TB1[3]	N/A	N/A	30	$f_S/30$ (I) + $f_S/30$ (Q)	$f_S/30 \times 80\%$	12.7
f_S	FB2 + HB3 + HB2 + HB1	20	$f_S/20$	40	$f_S/40$ (I) + $f_S/40$ (Q)	$f_S/40 \times 80\%$	14
f_S	TB2 + HB4 + HB3 + HB2 + HB1	24	$f_S/24$	48	$f_S/48$ (I) + $f_S/48$ (Q)	$f_S/48 \times 80\%$	14.8

[1] N/A means not applicable.
[2] Ideal SNR improvement due to oversampling + filtering > 10log(bandwidth/$f_S/2$).
[3] TB1 is only supported in DDC 0 and DDC 1.

Table 17. DDC Filter Configurations (f_S = 1300 MSPS)[1]

ADC Sample Rate (MSPS)	DDC Filter Configuration	Real (I) Output		Complex (I/Q) Outputs		Alias-Protected Bandwidth (MHz)
		Decimation Ratio	Sample Rate (MSPS)	Decimation Ratio	Sample Rate (MSPS)	
1300	HB1	1	1300	2	650 (I) + 650 (Q)	520
1300	TB1[2]	N/A	N/A	3	433.33 (I) + 433.33 (Q)	346.67
1300	HB2 + HB1	2	650	4	325 (I) + 325 (Q)	260
1300	TB2 + HB1	3	433.33	6	216.67 (I) + 216.67 (Q)	173.33
1300	HB3 + HB2 + HB1	4	325	8	162.5 (I) + 162.5 (Q)	130
1300	FB2 + HB1	5	260	10	130 (I) + 130 (Q)	104
1300	TB2 + HB2 + HB1	6	216.67	12	108.33 (I) + 108.33 (Q)	86.67
1300	FB2 + TB1[2]	N/A	N/A	15	86.67 (I) + 86.67 (Q)	69.33
1300	HB4 + HB3 + HB2 + HB1	8	162.5	16	81.25 (I) + 81.25 (Q)	65
1300	FB2 + HB2 + HB1	10	130	20	65 (I) + 65 (Q)	52
1300	TB2 + HB3 + HB2 + HB1	12	108.33	24	54.16 (I) + 54.16 (Q)	43.33
1300	HB2 + FB2 + TB1[2]	N/A	N/A	30	43.44 (I) + 43.44 (Q)	34.67
1300	FB2 + HB3 + HB2 + HB1	20	65	40	32.5 (I) + 32.5 (Q)	26
1300	TB2 + HB4 + HB3 + HB2 + HB1	24	54.16	48	27.08 (I) + 27.08 (Q)	21.67

[1] N/A means not applicable.
[2] TB1 is only supported in DDC 0 and DDC 1.

HB4 Filter Description

The first decimate by 2, half-band, low-pass, FIR filter (HB4) uses an 11-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB4 filter is only used when complex outputs (decimate by 16) or real outputs (decimate by 8) are enabled; otherwise, it is bypassed. Table 18 and Figure 79 show the coefficients and response of the HB4 filter.

Table 18. HB4 Filter Coefficients

HB4 Coefficient No.	Normalized Coefficient	Decimal Coefficient (15-Bit)
C1, C11	+0.006042	+99
C2, C10	0	0
C3, C9	−0.049377	−809
C4, C8	0	0
C5, C7	+0.293335	+4806
C6	+0.5	+8192

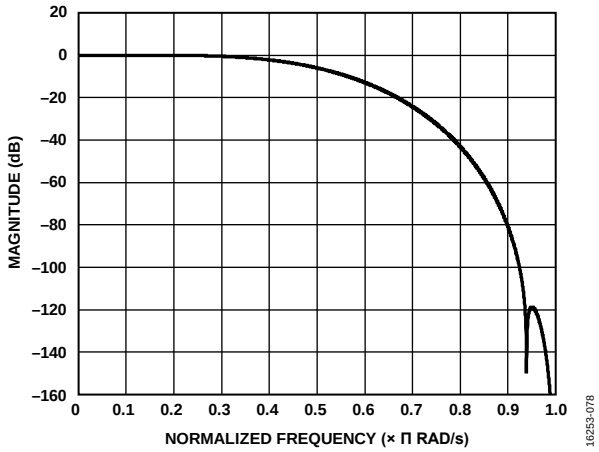


Figure 79. HB4 Filter Response

HB3 Filter Description

The second decimate by 2, half-band, low-pass, FIR filter (HB3) uses an 11-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB3 filter is only used when complex outputs (decimate by 8 or 16) or real outputs (decimate by 4 or 8) are enabled; otherwise, it is bypassed. Table 19 and Figure 80 show the coefficients and response of the HB3 filter.

Table 19. HB3 Filter Coefficients

HB3 Coefficient No.	Normalized Coefficient	Decimal Coefficient (17-Bit)
C1, C11	+0.006638	+435
C2, C10	0	0
C3, C9	−0.051056	−3346
C4, C8	0	0
C5, C7	+0.294418	+19,295
C6	+0.500000	+32,768

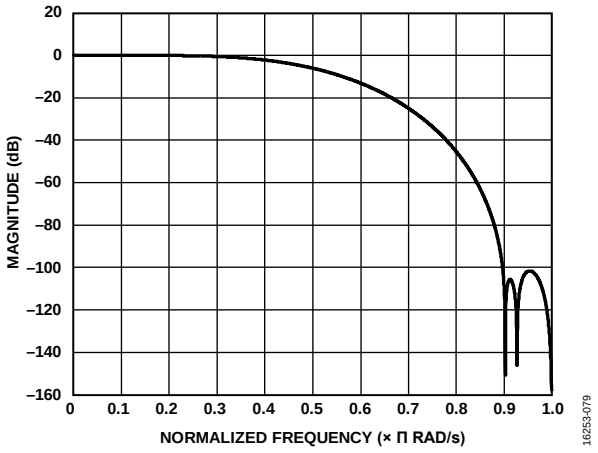


Figure 80. HB3 Filter Response

HB2 Filter Description

The third decimate by 2, half-band, low-pass, FIR filter (HB2) uses a 19-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption.

The HB2 filter is only used when complex or real outputs (decimate by 4, 8, or 16) is enabled; otherwise, it is bypassed.

Table 20 and Figure 81 show the coefficients and response of the HB2 filter.

Table 20. HB2 Filter Coefficients

HB2 Coefficient No.	Normalized Coefficient	Decimal Coefficient (18-Bit)
C1, C19	+0.000671	+88
C2, C18	0	0
C3, C17	−0.005325	−698
C4, C16	0	0
C5, C15	+0.022743	+2981
C6, C14	0	0
C7, C13	−0.074181	−9723
C8, C12	0	0
C9, C11	+0.306091	+40120
C10	+0.5	+65536

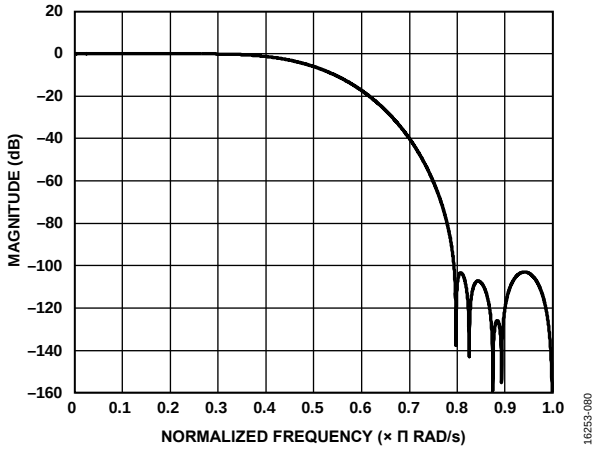


Figure 81. HB2 Filter Response

HB1 Filter Description

The fourth and final decimate by 2, half-band, low-pass, FIR filter (HB1) uses a 63-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB1 filter is always enabled and cannot be bypassed. Table 21 and Figure 82 show the coefficients and response of the HB1 filter.

Table 21. HB1 Filter Coefficients

HB1 Coefficient No.	Normalized Coefficient	Decimal Coefficient (20-Bit)
C1, C63	−0.000019	−10
C2, C62	0	0
C3, C61	+0.000072	+38
C4, C60	0	0
C5, C59	−0.000195	−102
C6, C58	0	0
C7, C57	+0.000443	+232
C8, C56	0	0
C9, C55	−0.000891	−467
C10, C54	0	0
C11, C53	+0.001644	+862
C12, C52	0	0
C13, C51	−0.002840	−1489
C14, C50	0	0
C15, C49	+0.004654	+2440
C16, C48	0	0
C17, C47	−0.007311	−3833
C18, C46	0	0
C19, C45	+0.011122	+5831
C20, C44	0	0
C21, C43	−0.016554	−8679
C22, C42	0	0
C23, C41	0.024420	12803
C24, C40	0	0
C25, C39	−0.036404	−19086
C26, C38	0	0
C27, C37	+0.056866	+29814
C28, C36	0	0
C29, C35	−0.101892	−53421
C30, C34	0	0
C31, C33	+0.316883	+166138
C32	+0.5	+262144

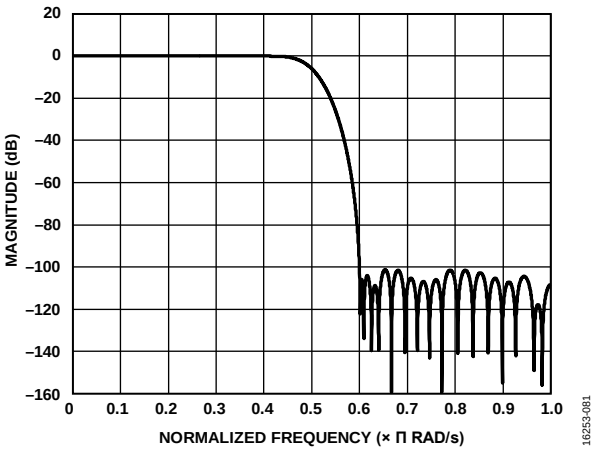


Figure 82. HB1 Filter Response

TB2 Filter Description

The TB2 uses a 26-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The TB2 filter is only used when decimation ratios of 6, 12, or 24 are required. Table 22 and Figure 83 show the coefficients and response of the TB2 filter.

Table 22. TB2 Filter Coefficients

TB2 Coefficient No.	Normalized Coefficient	Decimal Coefficient (19-Bit)
C1, C26	−0.000191	−50
C2, C25	−0.000793	+208
C3, C24	−0.001137	−298
C4, C23	+0.000916	+240
C5, C22	+0.006290	+1649
C6, C21	+0.009823	+2575
C7, C20	+0.000916	+240
C8, C19	−0.023483	−6156
C9, C18	−0.043152	−11312
C10, C17	−0.019318	−5064
C11, C16	+0.071327	+18698
C12, C15	+0.201172	+52736
C13, C14	+0.297756	+78055

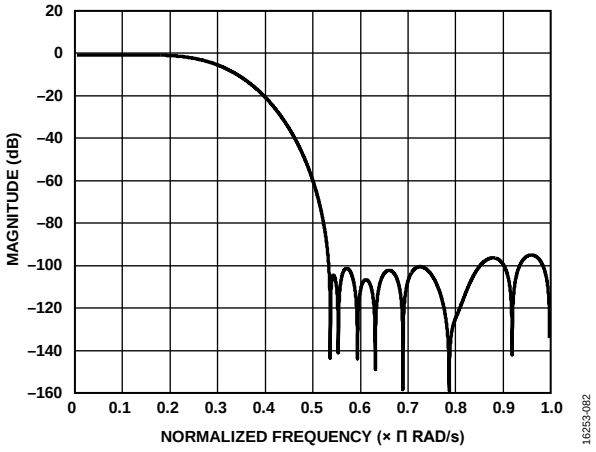


Figure 83. TB2 Filter Response

TB1 Filter Description

The TB1 decimate by 3, low-pass, FIR filter uses a 76-tap, symmetrical, fixed coefficient filter implementation. Table 23 shows the TB1 filter coefficients, and Figure 84 shows the TB1 filter response. TB1 is only supported in DDC 0 and DDC 1.

Table 23. TB1 Filter Coefficients

TB1 Coefficient No.	Normalized Coefficient	Decimal Coefficient (22-Bit)
1, 76	−0.000023	−96
2, 75	−0.000053	−224
3, 74	−0.000037	−156
4, 73	+0.000090	+379
5, 72	+0.000291	+1220
6, 71	+0.000366	+1534
7, 70	+0.000095	+398
8, 69	−0.000463	−1940
9, 68	−0.000822	−3448
10, 67	−0.000412	−1729
11, 66	+0.000739	+3100
12, 65	+0.001665	+6984
13, 64	+0.001132	+4748
14, 63	−0.000981	−4114
15, 62	−0.002961	−12418
16, 61	−0.002438	−10226
17, 60	+0.001087	+4560
18, 59	+0.004833	+20272
19, 58	+0.004614	+19352
20, 57	−0.000871	−3652
21, 56	−0.007410	−31080
22, 55	−0.008039	−33718
23, 54	+0.000053	+222
24, 53	+0.010874	+45608
25, 52	+0.013313	+55840
26, 51	+0.001817	+7620
27, 50	−0.015579	−65344
28, 49	−0.021590	−90556
29, 48	−0.005603	−23502
30, 47	+0.022451	+94167
31, 46	+0.035774	+150046
32, 45	+0.013541	+56796
33, 44	−0.034655	−145352
34, 43	−0.066549	−279128
35, 42	−0.035213	−147694
36, 41	+0.071220	+298720
37, 40	+0.210777	+884064
38, 39	+0.309200	+1296880

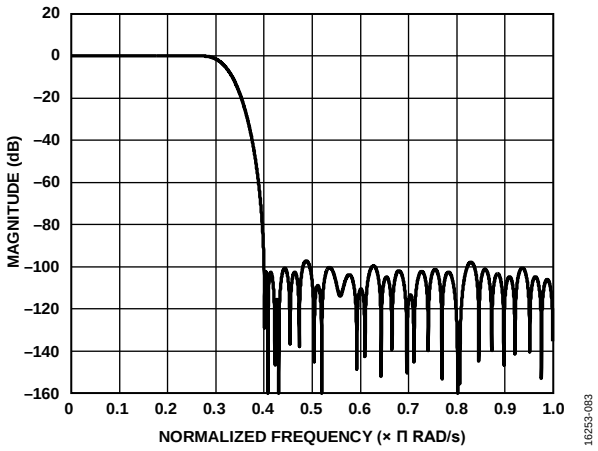


Figure 84. TB1 Filter Response

FB2 Filter Description

The FB2 decimate by 5, low-pass, FIR filter uses a 48-tap, symmetrical, fixed coefficient filter implementation. Table 24 shows the FB2 filter coefficients, and Figure 85 shows the FB2 filter response.

Table 24. FB2 Filter Coefficients

FB2 Coefficient No.	Normalized Coefficient	Decimal Coefficient (21-Bit)
1, 48	+0.000007	7
2, 47	−0.000004	−4
3, 46	−0.000069	−72
4, 45	−0.000244	−256
5, 44	−0.000544	−570
6, 43	−0.000870	−912
7, 42	−0.000962	−1009
8, 41	−0.000448	−470
9, 40	+0.000977	+1024
10, 39	+0.003237	+3394
11, 38	+0.005614	+5887
12, 37	+0.006714	+7040
13, 36	+0.004871	+5108
14, 35	−0.001011	−1060
15, 34	−0.010456	−10964
16, 33	−0.020729	−21736
17, 32	−0.026978	−28288
18, 31	−0.023453	−24592
19, 30	−0.005608	−5880
20, 29	+0.027681	+29026
21, 28	+0.072720	+76252
22, 27	+0.121223	+127112
23, 26	+0.162346	+170232
24, 25	+0.185959	+194992

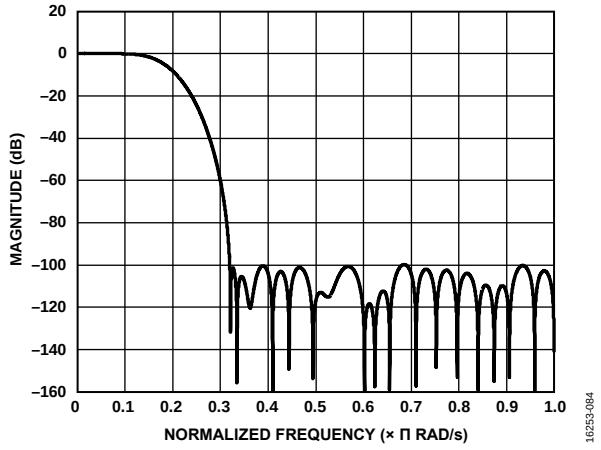


Figure 85. FB2 Filter Response

DDC GAIN STAGE

Each DDC contains an independently controlled gain stage. The gain is selectable as either 0 dB or 6 dB. When mixing a real input signal down to baseband, it is recommended that the user enable the 6 dB of gain to recenter the dynamic range of the signal within the full scale of the output bits.

When mixing a complex input signal down to baseband, the mixer has already recentered the dynamic range of the signal within the full scale of the output bits, and no additional gain is necessary. However, the optional 6 dB gain compensates for low signal strengths. The downsample by 2 portion of the HB1 FIR filter is bypassed when using the complex to real conversion stage. The TB1 filter does not have the 6 dB gain stage.

DDC COMPLEX TO REAL CONVERSION

Each DDC contains an independently controlled complex to real conversion block. The complex to real conversion block reuses the last filter (HB1 FIR) in the filtering stage along with an $f_S/4$ complex mixer to upconvert the signal. After upconverting the signal, the Q portion of the complex mixer is no longer needed and is dropped. The TB1 filter does not support complex to real conversion.

Figure 86 shows a simplified block diagram of the complex to real conversion.

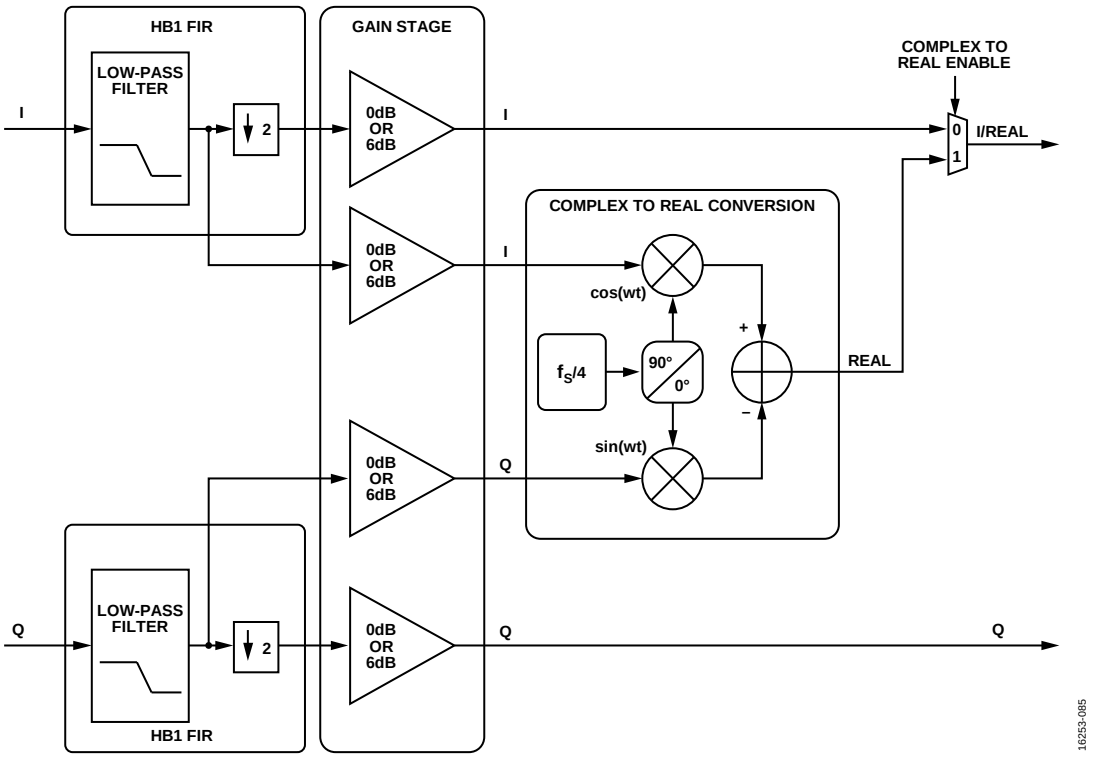


Figure 86. Complex to Real Conversion Block

DDC MIXED DECIMATION SETTINGS

The AD9697 also supports DDCs with different decimation rates. In this scenario, the chip decimation ratio must be set to the lowest decimation ratio of all the DDC channels. Samples of higher decimation ratio DDCs are repeated to match the chip decimation ratio sample rate. Only mixed decimation ratios that are integer multiples of 2 are supported. For example, decimate by 1, 2, 4, 8, or 16 can be mixed together, decimate by 3, 6, 12, 24, or 48 can be mixed together, or decimate by 5, 10, 20, or 40 can be mixed together.

Table 25 shows the DDC sample mapping when the chip decimation ratio is different than the DDC decimation ratio.

For example, if the chip decimation ratio is set to decimate by 4, DDC 0 is set to use the HB2 + HB1 filters (complex outputs, decimate by 4) and DDC 1 is set to use the HB4 + HB3 + HB2 + HB1 filters (real outputs, decimate by 8), then DDC 1 repeats its output data two times for every one DDC 0 output. The resulting output samples are shown in Table 26.

Table 25. Sample Mapping when Chip Decimation Ratio (DCM) Does Not Match DDC DCM

Sample Index	DDC DCM = Chip DCM	DDC DCM = 2 × Chip DCM	DDC DCM = 4 × Chip DCM	DDC DCM = 8 × Chip DCM
0	N	N	N	N
1	N + 1	N	N	N
2	N + 2	N + 1	N	N
3	N + 3	N + 1	N	N
4	N + 4	N + 2	N + 1	N
5	N + 5	N + 2	N + 1	N
6	N + 6	N + 3	N + 1	N
7	N + 7	N + 3	N + 1	N
8	N + 8	N + 4	N + 2	N + 1
9	N + 9	N + 4	N + 2	N + 1
10	N + 10	N + 5	N + 2	N + 1
11	N + 11	N + 5	N + 2	N + 1
12	N + 12	N + 6	N + 3	N + 1
13	N + 13	N + 6	N + 3	N + 1
14	N + 14	N + 7	N + 3	N + 1
15	N + 15	N + 7	N + 3	N + 1
16	N + 16	N + 8	N + 4	N + 2
17	N + 17	N + 8	N + 4	N + 2
18	N + 18	N + 9	N + 4	N + 2
19	N + 19	N + 9	N + 4	N + 2
20	N + 20	N + 10	N + 5	N + 2
21	N + 21	N + 10	N + 5	N + 2
22	N + 22	N + 11	N + 5	N + 2
23	N + 23	N + 11	N + 5	N + 2
24	N + 24	N + 12	N + 6	N + 3
25	N + 25	N + 12	N + 6	N + 3
26	N + 26	N + 13	N + 6	N + 3
27	N + 27	N + 13	N + 6	N + 3
28	N + 28	N + 14	N + 7	N + 3
29	N + 29	N + 14	N + 7	N + 3
30	N + 30	N + 15	N + 7	N + 3
31	N + 31	N + 15	N + 7	N + 3

Table 26. Chip DCM = 4, DDC 0 DCM = 4 (Complex), and DDC 1 DCM = 8 (Real)[1]

	DDC 0		DDC 1	
DDC Input Samples	**Output Port I**	**Output Port Q**	**Output Port I**	**Output Port Q**
N	I0[N]	Q0[N]	I1[N]	Not applicable
N + 1	I0[N]	Q0[N]	I1[N]	Not applicable
N + 2	I0[N]	Q0[N]	I1[N]	Not applicable
N + 3	I0[N]	Q0[N]	I1[N]	Not applicable
N + 4	I0[N + 1]	Q0[N + 1]	I1[N]	Not applicable
N + 5	I0[N + 1]	Q0[N + 1]	I1[N]	Not applicable
N + 6	I0[N + 1]	Q0[N + 1]	I1[N]	Not applicable
N + 7	I0[N + 1]	Q0[N + 1]	I1[N]	Not applicable
N + 8	I0[N + 2]	Q0[N + 2]	I1[N + 1]	Not applicable
N + 9	I0[N + 2]	Q0[N + 2]	I1[N + 1]	Not applicable
N + 10	I0[N + 2]	Q0[N + 2]	I1[N + 1]	Not applicable
N + 11	I0[N + 2]	Q0[N + 2]	I1[N + 1]	Not applicable
N + 12	I0[N + 3]	Q0[N + 3]	I1[N + 1]	Not applicable
N + 13	I0[N + 3]	Q0[N + 3]	I1[N + 1]	Not applicable
N + 14	I0[N + 3]	Q0[N + 3]	I1[N + 1]	Not applicable
N + 15	I0[N + 3]	Q0[N + 3]	I1[N + 1]	Not applicable

[1] DCM means decimation.

DDC EXAMPLE CONFIGURATIONS

Table 27 describes the register settings for multiple DDC example configurations. Bandwidths listed are with <−0.005 dB of pass-band ripple and >100 dB of stop band alias rejection.

Table 27. DDC Example Configurations (per ADC Channel Pair)

Chip Application Layer	Chip Decimation Ratio	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings
Two DDCs	4	Real	10% × f_S	2	0x0200 = 0x22 (two DDCs; I only selected) 0x0201 = 0x02 (chip decimate by 4) 0x0310, 0x0330 = 0x49 (real mixer; 6 dB gain; variable IF; real output; HB3 + HB2 + HB1 filters) 0x0311 = 0x00 (DDC 0 additional decimation ratio selection 0x0331 = 0x00 (DDC 1 additional decimation ratio selection 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC 0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC 1
Two DDCs	4	Complex	20% × f_S	4	0x0200 = 0x02 (two DDCs; I/Q selected) 0x0201 = 0x02 (chip decimate by 4) 0x0310, 0x0330 = 0x40 (real mixer; 6 dB gain; variable IF; complex output; HB2 + HB1 filters) 0x0311 = 0x00 (DDC 0 additional decimation ratio selection 0x0331 = 0x00 (DDC 1 additional decimation ratio selection 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC 0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC 1

Chip Application Layer	Chip Decimation Ratio	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings
Two DDCs	8	Real	5% × f_S	2	0x0200 = 0x22 (two DDCs; I only selected) 0x0201 = 0x03 (chip decimate by 8) 0x0310, 0x0330 = 0x4A (real mixer; 6 dB gain; variable IF; real output; HB4 + HB3 + HB2 + HB1 filters) 0x0311 = 0x00 (DDC 0 additional decimation ratio selection 0x0331 = 0x00 (DDC 1 additional decimation ratio selection 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC 0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC 1
Four DDCs	8	Complex	10% × f_S	8	0x0200 = 0x03 (four DDCs; I/Q selected) 0x0201 = 0x03 (chip decimate by 8) 0x0310, 0x0330, 0x0350, 0x0370 = 0x41 (real mixer; 6 dB gain; variable IF; complex output; HB3 + HB2 + HB1 filters) 0x0311 = 0x00 (DDC 0 additional decimation ratio selection 0x0331 = 0x00 (DDC 1 additional decimation ratio selection 0x0351 = 0x00 (DDC 2 additional decimation ratio selection 0x0371 = 0x00 (DDC 3 additional decimation ratio selection 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC 0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC 1 0x0356, 0x0357, 0x0358, 0x0359, 0x035A, 0x035B, 0x035D, 0x035E, 0x035F, 0x0360, 0x0361, 0x0362 = FTW and POW set as required by application for DDC 2 0x0376, 0x0377, 0x0378, 0x0379, 0x037A, 0x037B, 0x037D, 0x037E, 0x037F, 0x0380, 0x0381, 0x0382 = FTW and POW set as required by application for DDC 3
Four DDCs	8	Real	5% × f_S	4	0x0200 = 0x23 (four DDCs; I only selected) 0x0201 = 0x03 (chip decimate by 8) 0x0310, 0x0330, 0x0350, 0x0370 = 0x4A (real mixer; 6 dB gain; variable IF; real output; HB4 + HB3 + HB2 + HB1 filters) 0x0311 = 0x00 (DDC 0 I input = ADC Channel A; DDC 0 Q input = ADC Channel A) 0x0331 = 0x00 (DDC 1 I input = ADC Channel A; DDC 1 Q input = ADC Channel A) 0x0351 = 0x05 (DDC 2 I input = ADC Channel B; DDC 2 Q input = ADC Channel B) 0x0371 = 0x05 (DDC 3 I input = ADC Channel B; DDC 3 Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC 0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC 1 0x0356, 0x0357, 0x0358, 0x0359, 0x035A, 0x035B, 0x035D, 0x035E, 0x035F, 0x0360, 0x0361, 0x0362 = FTW and POW set as required by application for DDC 2 0x0376, 0x0377, 0x0378, 0x0379, 0x037A, 0x037B, 0x037D, 0x037E, 0x037F, 0x0380, 0x0381, 0x0382 = FTW and POW set as required by application for DDC 3

Chip Application Layer	Chip Decimation Ratio	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings
Four DDCs	16	Complex	5% × f_S	8	0x0200 = 0x03 (four DDCs; I/Q selected) 0x0201 = 0x04 (chip decimate by 16) 0x0310, 0x0330, 0x0350, 0x0370 = 0x42 (real mixer; 6 dB gain; variable IF; complex output; HB4 + HB3 + HB2 + HB1 filters) 0x0311 = 0x00 (DDC 0 I input = ADC Channel A; DDC 0 Q input = ADC Channel A) 0x0331 = 0x00 (DDC 1 I input = ADC Channel A; DDC 1 Q input = ADC Channel A) 0x0351 = 0x05 (DDC 2 I input = ADC Channel B; DDC 2 Q input = ADC Channel B) 0x0371 = 0x05 (DDC 3 I input = ADC Channel B; DDC 3 Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC 0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC 1 0x0356, 0x0357, 0x0358, 0x0359, 0x035A, 0x035B, 0x035D, 0x035E, 0x035F, 0x0360, 0x0361, 0x0362 = FTW and POW set as required by application for DDC 2 0x0376, 0x0377, 0x0378, 0x0379, 0x037A, 0x037B, 0x037D, 0x037E, 0x037F, 0x0380, 0x0381, 0x0382 = FTW and POW set as required by application for DDC 3

[1] f_S is the ADC sample rate.

SIGNAL MONITOR

The signal monitor block provides additional information about the signal being digitized by the ADC. The signal monitor computes the peak magnitude of the digitized signal. This information can be used to drive an AGC loop to optimize the range of the ADC in the presence of real-world signals.

The results of the signal monitor block can be obtained either by reading back the internal values from the SPI port or by embedding the signal monitoring information into the JESD204B interface as special control bits. A global, 24-bit programmable period controls the duration of the measurement. Figure 87 shows the simplified block diagram of the signal monitor block.

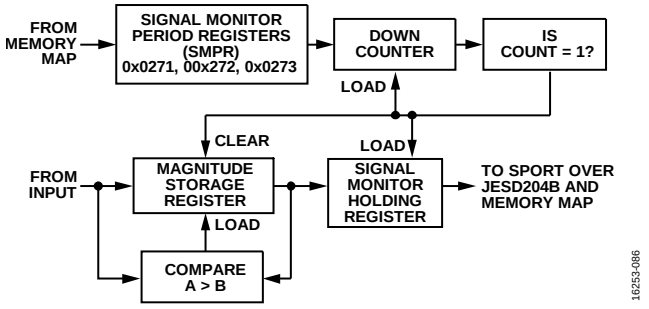


Figure 87. Signal Monitor Block

The peak detector captures the largest signal within the observation period. The detector only observes the magnitude of the signal. The resolution of the peak detector is a 13-bit value, and the observation period is 24 bits and represents converter output samples. The peak magnitude can be derived by using the following equation:

$$Peak\ Magnitude\ (\text{dBFS}) = 20\log(Peak\ Detector\ Value/2^{13})$$

The magnitude of the input port signal is monitored over a programmable time period, which is determined by the signal monitor period register (SMPR). The peak detector function is enabled by setting Bit 1 of Register 0x0270 in the signal monitor control register. The 24-bit SMPR must be programmed before activating this mode.

After enabling peak detection mode, the value in the SMPR is loaded into a monitor period timer, which decrements at the decimated clock rate. The magnitude of the input signal is compared with the value in the internal magnitude storage register (not accessible to the user), and the greater of the two is updated as the current peak level. The initial value of the magnitude storage register is set to the current ADC input signal magnitude. This comparison continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the 13-bit peak level value is transferred to the signal monitor holding register, which can be read through the memory map or output through the SPORT over the JESD204B interface. The monitor period timer is reloaded with the value in the SMPR, and the countdown restarts. In addition, the magnitude of the first input sample is updated in the magnitude storage register, and the comparison and update procedure, as explained previously, continues.

SPORT OVER JESD204B

The signal monitor data can also be serialized and sent over the JESD204B interface as control bits. These control bits must be deserialized from the samples to reconstruct the statistical data. The signal control monitor function is enabled by setting Bits[1:0] of Register 0x0279 and Bit 1 of Register 0x027A. Figure 88 shows two different example configurations for the signal monitor control bit locations inside the JESD204B samples. A maximum of three control bits can be inserted into the JESD204B samples; however, only one control bit is required for the signal monitor. Control bits are inserted from MSB to LSB. If only one control bit is to be inserted (CS = 1), only the most significant control bit is used (see Example Configuration 1 and Example Configuration 2 in Figure 88). To select the SPORT over JESD204B option, program Register 0x0559, Register 0x055A, and Register 0x058F. See Table 44 for more information on setting these bits.

Figure 89 shows the 25-bit frame data that encapsulates the peak detector value. The frame data is transmitted MSB first with five 5-bit subframes. Each subframe contains a start bit that can be used by a receiver to validate the deserialized data. Figure 90 shows the SPORT over JESD204B signal monitor data with a monitor period timer set to 80 samples.

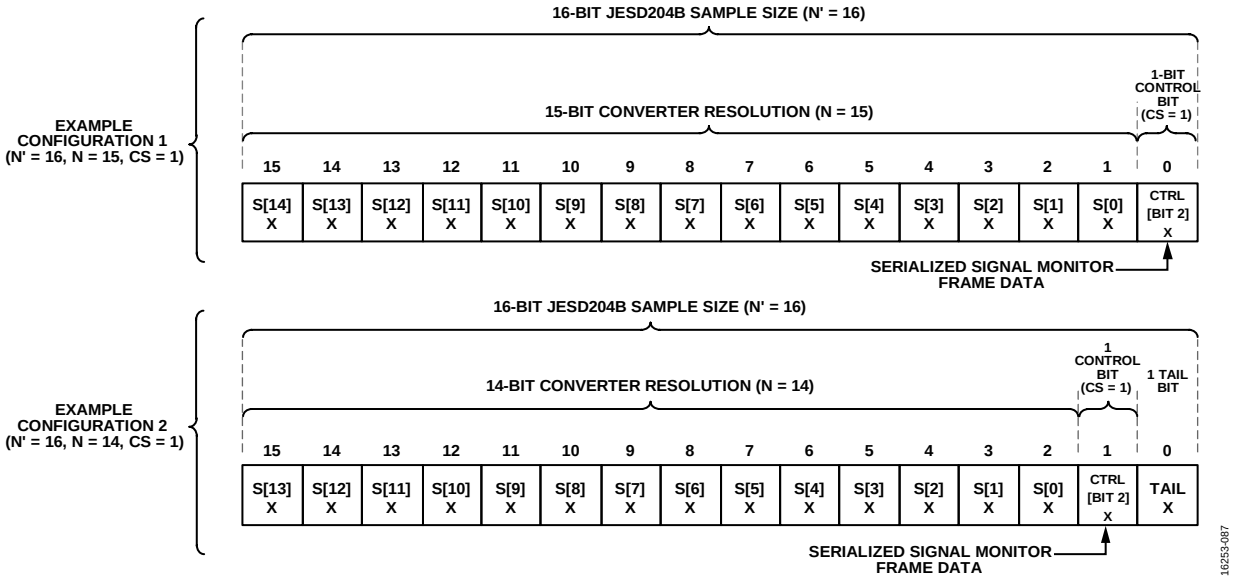


Figure 88. Signal Monitor Control Bit Locations

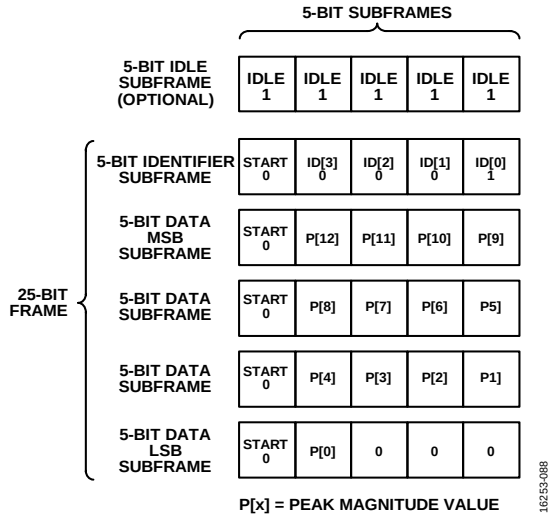


Figure 89. SPORT over JESD204B Signal Monitor Frame Data

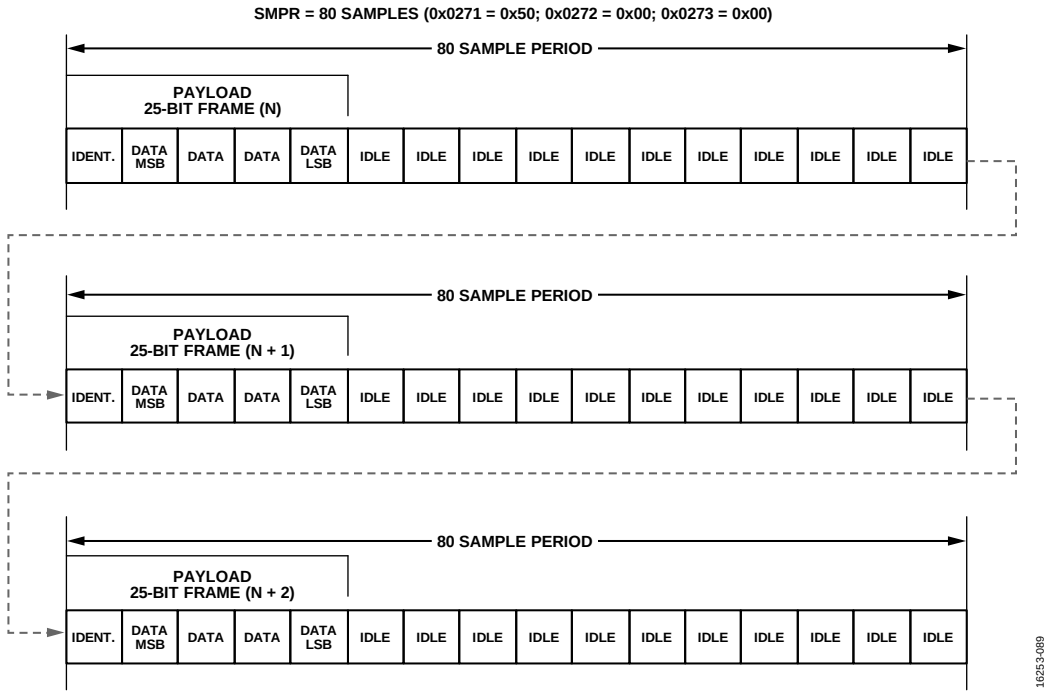


Figure 90. SPORT over JESD204B Signal Monitor Example

DIGITAL OUTPUTS

INTRODUCTION TO THE JESD204B INTERFACE

The AD9697 digital outputs are designed to the JEDEC standard JESD204B, serial interface for data converters. JESD204B is a protocol to link the AD9697 to a digital processing device over a serial interface with lane rates of up to 16 Gbps. The benefits of the JESD204B interface over LVDS include a reduction in required board area for data interface routing, and an ability to enable smaller packages for converter and logic devices.

JESD204B OVERVIEW

The JESD204B data transmit block assembles the parallel data from the ADC into frames and uses 8-bit/10-bit encoding as well as optional scrambling to form serial output data. Lane synchronization is supported through the use of special control characters during the initial establishment of the link. Additional control characters are embedded in the data stream to maintain synchronization thereafter. A JESD204B receiver is required to complete the serial link. For additional details on the JESD204B interface, refer to the JESD204B standard.

The AD9697 JESD204B data transmit block maps up to two physical ADCs or up to eight virtual converters (when DDCs are enabled) over a link. A link can be configured to use one, two, or four JESD204B lanes. The JESD204B specification refers to a number of parameters to define the link, and these parameters must match between the JESD204B transmitter (the AD9697 output) and the JESD204B receiver (the logic device input).

The JESD204B link is described according to the following parameters:

- L is the number of lanes/converter device (lanes/link) (AD9697 value = 1, 2, or 4)
- M is the number of converters/converter device (virtual converters/link) (AD9697 value = 1, 2, 4, or 8)
- F is the octets/frame (AD9697 value = 1, 2, 4, 8, or 16)
- N′ is the number of bits per sample (JESD204B word size) (AD9697 value = 8 or 16)
- N is the converter resolution (AD9697 value = 7 to 16)
- CS is the number of control bits/sample (AD9697 value = 0, 1, 2, or 3)
- K is the number of frames per multiframe (AD9697 value = 4, 8, 12, 16, 20, 24, 28, or 32)
- S is the samples transmitted/single converter/frame cycle (AD9697 value = set automatically based on L, M, F, and N′)
- HD is the high density mode (AD9697 = set automatically based on L, M, F, and N′)
- CF is the number of control words/frame clock cycle/converter device (AD9697 value = 0)

Figure 91 shows a simplified block diagram of the AD9697 JESD204B link. By default, the AD9697 is configured to use two converters and four lanes. Converter A data is output to SERDOUT0± and/or SERDOUT1±, and Converter B is output to SERDOUT2± and/or SERDOUT3±. The AD9697 allows other configurations, such as combining the outputs of both converters onto a single lane, or changing the mapping of the A and B digital output paths. These modes are customizable, and can be set up via the SPI. Refer to the Memory Map section for more details.

By default in the AD9697, the 14-bit converter word from each converter is broken into two octets (eight bits of data). Bit 13 (MSB) through Bit 6 are in the first octet. The second octet contains Bit 5 through Bit 0 (LSB) and two tail bits. The tail bits can be configured as zeros or a pseudorandom number sequence. The tail bits can also be replaced with control bits indicating overrange, SYSREF±, or fast detect output.

The two resulting octets can be scrambled. Scrambling is optional; however, it is recommended to avoid spectral peaks when transmitting similar digital data patterns. The scrambler uses a self-synchronizing, polynomial-based algorithm defined by the equation $1 + x^{14} + x^{15}$. The descrambler in the receiver is a self synchronizing version of the scrambler polynomial.

The two octets are then encoded with an 8-bit/10-bit encoder. The 8-bit/10-bit encoder works by taking eight bits of data (an octet) and encoding them into a 10-bit symbol. Figure 91 shows how the 14-bit data is taken from the ADC, how the tail bits are added, how the two octets are scrambled, and how the octets are encoded into two 10-bit symbols. Figure 92 shows the default data format.

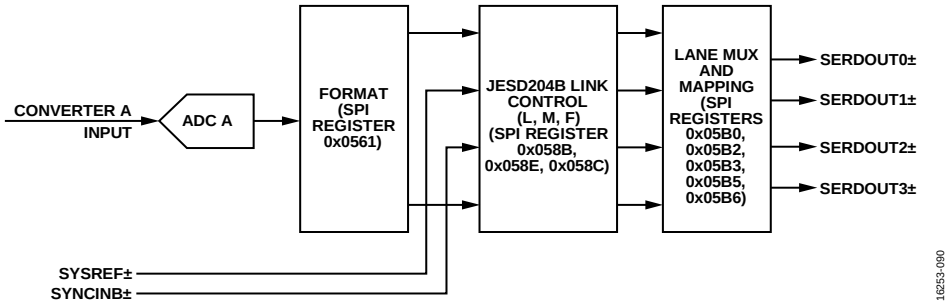


Figure 91. Transmit Link Simplified Block Diagram Showing Full Bandwidth Mode (Register 0x200 = 0x00)

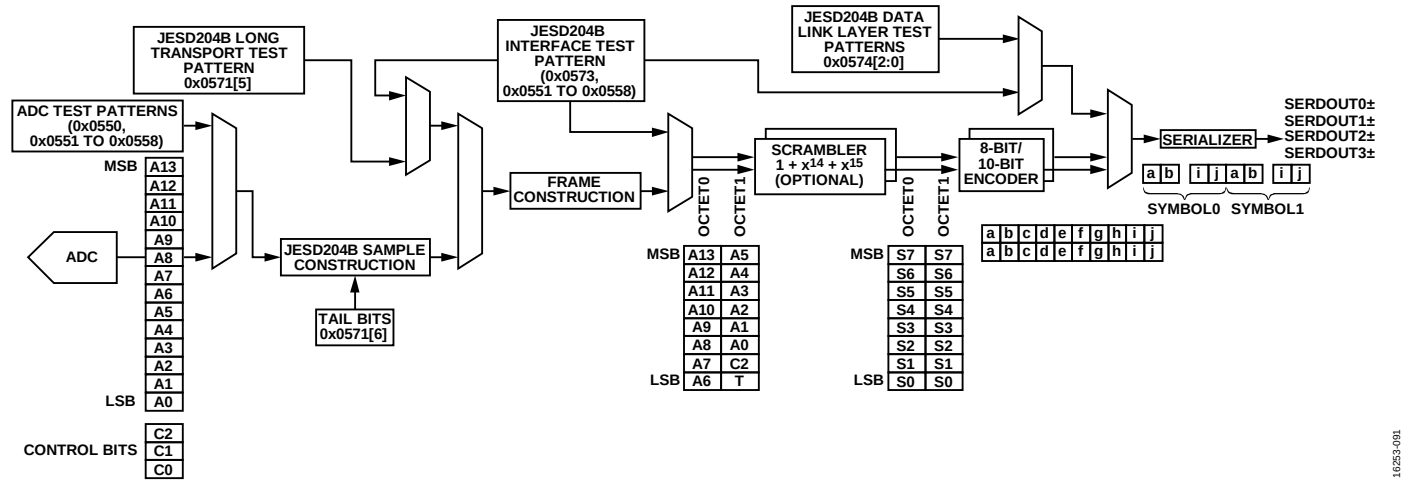


Figure 92. ADC Output Datapath Showing Data Framing

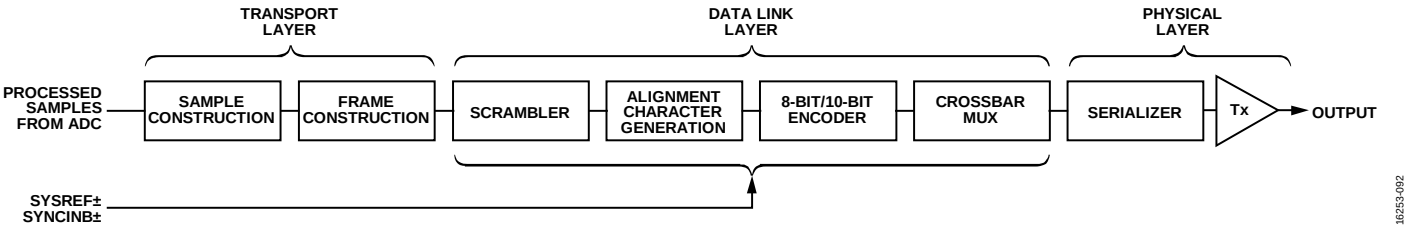


Figure 93. Data Flow

FUNCTIONAL OVERVIEW

The block diagram in Figure 93 shows the flow of data through the JESD204B hardware from the sample input to the physical output. The processing can be divided into layers that are derived from the open source initiative (OSI) model, widely used to describe the abstraction layers of communications systems. These layers are the transport layer, data link layer, and physical layer (serializer and output driver).

Transport Layer

The transport layer handles packing the data (consisting of samples and optional control bits) into JESD204B frames that are mapped to 8-bit octets. The packing of samples into frames are determined by the JESD204B configuration parameters for number of lanes (L), number of converters (M), the number of octets per lane per frame (F), the number of samples per converter per frame (S), and the number of bits in a nibble group (sometimes called the JESD204 word size – N').

Samples are mapped in order starting from Converter 0, then Converter 1, and so on until Converter M – 1. If S > 1, each sample from the converter is mapped before mapping the samples from the next converter. Each sample is mapped into words formed by appending converter control bits, if enabled, to the LSBs of each sample. The words are then padded with tail bits, if necessary, to form nibble groups (NGs) of the appropriate size as determined by the N' parameter. The following equation can be used to determine the number of tail bits within a nibble group (JESD204B word):

$$T = N' - N - CS$$

Data Link Layer

The data link layer is responsible for the low level functions of passing data across the link. These include optionally scrambling the data, inserting control characters during the initial lane alignment sequence (ILAS) and for frame and multiframe synchronization monitoring, and encoding 8-bit octets into 10-bit symbols. The data link layer is also responsible for sending the ILAS, which contains the link configuration data used by the receiver to verify the settings in the transport layer.

Physical Layer

The physical layer consists of the high speed circuitry clocked at the serial clock rate. In this layer, parallel data is converted into one, two, or four lanes of high speed differential serial data.

JESD204B LINK ESTABLISHMENT

The AD9697 JESD204B transmitter (Tx) interface operates in Subclass 0 or Subclass 1 as defined in the JEDEC Standard JESD204B (July 2011 specification). The link establishment process is divided into the following steps: code group synchronization, initial lane alignment sequence, and user data and error correction.

Code Group Synchronization (CGS)

CGS is the process by which the JESD204B receiver finds the boundaries between the 10-bit symbols in the stream of data. During the CGS phase, the JESD204B transmit block transmits /K/ characters (/K28.5/ symbols). The receiver must locate the /K/ characters in its input data stream using clock and data recovery (CDR) techniques.

The receiver issues a synchronization request by asserting the SYNCINB± pin of the AD9697 low. The JESD204B Tx then begins sending /K/ characters. Once the receiver has synchronized, it waits for the correct reception of at least four consecutive /K/ symbols. It then deasserts SYNCINB±. The AD9697 then transmits an ILAS on the following local multiframe clock (LMFC) boundary.

For more information on the code group synchronization phase, refer to the JEDEC Standard JESD204B, July 2011, Section 5.3.3.1.

The SYNCINB± pin operation can also be controlled by the SPI. The SYNCINB± signal is a differential dc-coupled LVDS mode signal by default, but it can also be driven single-ended. For more information on configuring the SYNCINB± pin operation, refer to Register 0x0572.

The SYNCINB± pins can also be configured to run in CMOS (single-ended) mode by setting Bit 4 in Register 0x0572. When running SYNCINB± in CMOS mode, connect the CMOS SYNCINB signal to Pin 21 (SYNCINB+) and leave Pin 20 (SYNCINB−) disconnected.

Initial Lane Alignment Sequence (ILAS)

The ILAS phase follows the CGS phase and begins on the next LMFC boundary after SYNCINB± deassertion. The ILAS consists of four mulitframes, with an /R/ character marking the beginning and an /A/ character marking the end. The ILAS begins by sending an /R/ character followed by 0 to 255 ramp data for one multiframe. On the second multiframe, the link configuration data is sent, starting with the third character. The second character is a /Q/ character to confirm that the link configuration data follows. All undefined data slots are filled with ramp data. The ILAS sequence is never scrambled.

The ILAS sequence construction is shown in Figure 94. The four multiframes include the following:

- Multiframe 1 begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 2 begins with an /R/ character followed by a /Q/ character (/K28.4/), followed by link configuration parameters over 14 configuration octets (see Table 28) and ends with an /A/ character. Many of the parameter values are of the value – 1 notation.
- Multiframe 3 begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 4 begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).

User Data and Error Detection

After the initial lane alignment sequence is complete, the user data (ADC samples) is sent. During transmission of the user data, a mechanism called character replacement monitors the frame clock and multiframe clock alignment. This mechanism replaces the last octet of a frame or multiframe with an /F/ or /A/ alignment characters when the data meets certain conditions. These conditions are different for unscrambled and scrambled data. The scrambling operation is enabled by default, but it can be disabled using the SPI.

For scrambled data, any 0xFC character at the end of a frame is replaced by an /F/, and any 0x7C character at the end of a multiframe is replaced with an /A/. The JESD204B receiver (Rx) checks for /F/ and /A/ characters in the received data stream and verifies that they only occur in the expected locations. If an unexpected /F/ or /A/ character is found, the receiver handles the situation by using dynamic realignment or asserting the SYNCINB± signal for more than four frames to initiate a resynchronization. For unscrambled data, if the final octet of two subsequent frames are equal, the second octet is replaced with an /F/ symbol if it is at the end of a frame, and an /A/ symbol if it is at the end of a multiframe.

Insertion of alignment characters can be modified using SPI. The frame alignment character insertion (FACI) is enabled by default. More information on the link controls is available in the Memory Map section, Register 0x0571.

8-Bit/10-Bit Encoder

The 8-bit/10-bit encoder converts 8-bit octets into 10-bit symbols and inserts control characters into the stream when needed. The control characters used in JESD204B are shown in Table 28. The 8-bit/10-bit encoding ensures that the signal is dc balanced by using the same number of ones and zeros across multiple symbols.

The 8-bit/10-bit interface has options that can be controlled via the SPI. These operations include bypass and invert. These options are troubleshooting tools for the verification of the digital front end (DFE). Refer to the Memory Map section, Register 0x0572, Bits[2:1] for information on configuring the 8-bit/10-bit encoder.

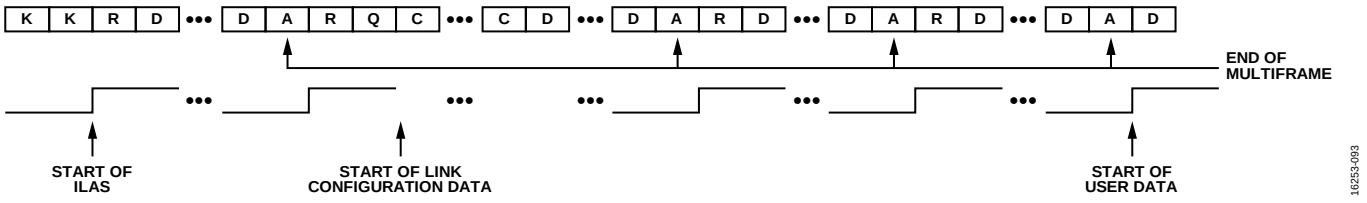


Figure 94. Initial Lane Alignment Sequence

Table 28. AD9697 Control Characters Used in JESD204B

Abbreviation	Control Symbol	8-Bit Value	10-Bit Value, RD[1] = −1	10-Bit Value, RD[1] = +1	Description
/R/	/K28.0/	000 11100	001111 0100	110000 1011	Start of multiframe
/A/	/K28.3/	011 11100	001111 0011	110000 1100	Lane alignment
/Q/	/K28.4/	100 11100	001111 0100	110000 1101	Start of link configuration data
/K/	/K28.5/	101 11100	001111 1010	110000 0101	Group synchronization
/F/	/K28.7/	111 11100	001111 1000	110000 0111	Frame alignment

[1] RD means running disparity.

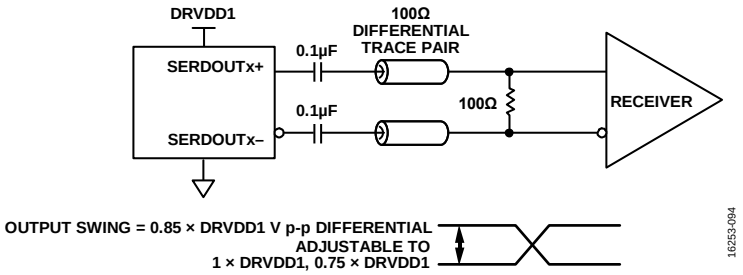


Figure 95. AC-Coupled Digital Output Termination Example

PHYSICAL LAYER (DRIVER) OUTPUTS

Digital Outputs, Timing, and Controls

The AD9697 physical layer consists of drivers that are defined in the JEDEC Standard JESD204B, July 2011. The differential digital outputs are powered up by default. The drivers use a dynamic 100 Ω internal termination to reduce unwanted reflections.

Place a 100 Ω differential termination resistor at each receiver input to result in a nominal 0.85 × DRVDD1 V p-p swing at the receiver (see Figure 95). The swing is adjustable through the SPI registers. AC coupling is recommended to connect to the receiver. See the Memory Map section (Register 0x05C0 to Register 0x05C3 in Table 44) for more details.

The AD9697 digital outputs can interface with custom ASICs and field programmable gate array (FPGA) receivers, providing superior switching performance in noisy environments. Single point-to-point network topologies are recommended with a single differential 100 Ω termination resistor placed as close to the receiver inputs as possible.

If there is no far end receiver termination, or if there is poor differential trace routing, timing errors can result. To avoid such timing errors, it is recommended that the trace length be less than six inches, and that the differential output traces be close together and at equal lengths.

Figure 96 to Figure 98 show an example of the digital outputs data eye, jitter histogram, and bathtub curve for one AD9697 lane running at 16 Gbps. The format of the output data is twos complement by default. To change the output data format, see the Memory Map section (Register 0x0561 in Table 44) for more details.

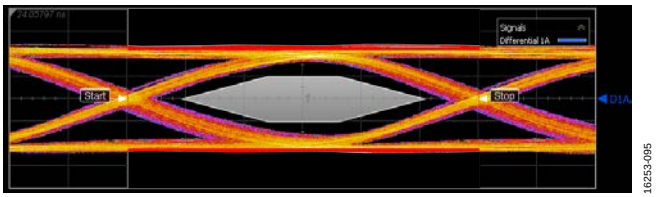


Figure 96. Digital Outputs Data Eye, External 100 Ω Terminations at 16 Gbps

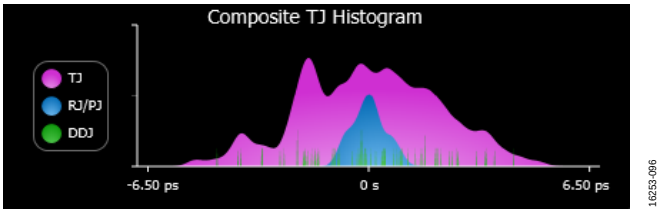


Figure 97. Digital Outputs Jitter Histogram, External 100 Ω Terminations at 16 Gbps

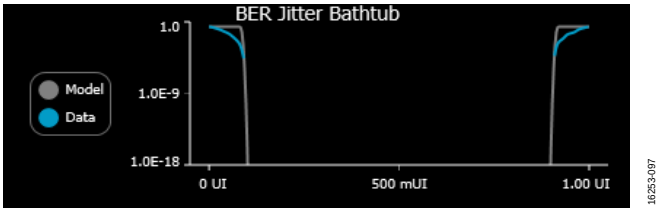


Figure 98. Digital Outputs Bathtub Curve, External 100 Ω Terminations at 16 Gbps

De-Emphasis

De-emphasis enables the receiver eye diagram mask to be met in conditions where the interconnect insertion loss does not meet the JESD204B specification. Use the de-emphasis feature only when the receiver is unable to recover the clock due to excessive insertion loss. Under normal conditions, it is disabled to conserve power. Additionally, enabling and setting too high a de-emphasis value on a short link can cause the receiver eye diagram to fail. Use the de-emphasis setting with caution because it can increase electromagnetic interference (EMI). See the Memory Map section (Register 0x05C4 to Register 0x05CA in Table 44) for more details.

Phase-Locked Loop (PLL)

The PLL generates the serializer clock, which operates at the JESD204B lane rate. The status of the PLL lock can be checked in the PLL locked status bit (Register 0x056F, Bit 7). This read only bit notifies the user if the PLL achieved a lock for the specific setup. Register 0x056F also has a loss of lock (LOL) sticky bit (Bit 3) that notifies the user that a loss of lock is detected. The sticky bit can be reset by issuing a JESD204B link restart (Register 0x0571, Bit 0 = 0x1, followed by Register 0x0571, Bit 0 = 0x0). Refer to Table 30 for the reinitialization of the link following a link power cycle.

The JESD204B lane rate control, Bits[7:4] of Register 0x056E, must be set to correspond with the lane rate. Table 29 shows the lane rates supported by the AD9697 using Register 0x056E.

Table 29. AD9697 Register 0x056E Supported Lane Rates

Value	Lane Rate
0x00	Lane rate = 6.75 Gbps to 13.5
0x10	Lane rate = 3.375 Gbps to 6.75 Gbps (default)
0x30	Lane rate = 13.5 Gbps to 16 Gbps
0x50	Lane rate = 1.6875 Gbps to 3.375 Gbps

SETTING UP THE AD9697 DIGITAL INTERFACE

To ensure proper operation of the AD9697 at startup, some SPI writes are required to initialize the link. Additionally, these registers must be written every time the ADC is reset. Any one of the following resets warrants the initialization routine for the digital interface:

- Hard reset, as with power-up.
- Power-up using the PDWN pin.
- Power-up using the SPI via Register 0x0002, Bits[1:0].
- SPI soft reset by setting Register 0x0000 = 0x81.
- Datapath soft reset by setting Register 0x0001 = 0x02.
- JESD204B link power cycle by setting Register 0x0571, Bit 0 = 0x1, then 0x0.

The initialization SPI writes are as shown in Table 30.

Table 30. AD9697 JESD204B Initialization

Register	Value	Comment
0x1228	0x4F	Reset JESD204B start-up circuit
0x1228	0x0F	JESD204B start-up circuit in normal operation
0x1222	0x00	JESD204B PLL force normal operation
0x1222	0x04	Reset JESD204B PLL calibration
0x1222	0x00	JESD204B PLL normal operation
0x1262	0x08	Clear loss of lock bit
0x1262	0x00	Loss of lock bit normal operation

The AD9697 has one JESD204B link. The serial outputs (SERDOUT0± to SERDOUT3±) are considered to be part of one JESD204B link. The basic parameters that determine the link setup are

- Number of lanes per link (L)
- Number of converters per link (M)
- Number of octets per frame (F)

If the internal DDCs are used for on-chip digital processing, M represents the number of virtual converters. The virtual converter mapping setup is shown in Table 11.

By default in the AD9697, the 14-bit converter word from each converter is broken into two octets (eight bits of data). Bit 13 (MSB) through Bit 6 are in the first octet. The second octet contains Bit 5 through Bit 0 (LSB) and two tail bits. The tail bits can be configured as zeros or a pseudorandom number sequence. The tail bits can also be replaced with control bits indicating overrange, SYSREF±, or fast detect output. Control bits are filled and inserted MSB first such that enabling CS = 1 activates Control Bit 2, enabling CS = 2 activates Control Bit 2 and Control Bit 1, and enabling CS = 3 activates Control Bit 2, Control Bit 1, and Control Bit 0.

The maximum lane rate allowed by the AD9697 is 16 Gbps. The lane rate is related to the JESD204B parameters using the following equation:

$$Lane\ Rate = \frac{M \times N' \times \left(\frac{10}{8}\right) \times f_{OUT}}{L}$$

where $f_{OUT} = f_{ADC_CLOCK}/Decimation\ Ratio$

The decimation ratio (DCM) is the parameter programmed in Register 0x0201.

Use the following procedure to configure the output:

1. Power down the link.
2. Select the JESD204B link configuration options.
3. Configure the detailed options.
4. Set output lane mapping (optional).
5. Set additional driver configuration options (optional).
6. Power up the link.
7. Initialize the JESD204B link by issuing the commands described in Table 30.

Register 0x056E must be programmed according to the lane rate calculated. Refer to the Phase-Locked Loop (PLL) section for more details.

Table 31 and Table 32 show the JESD204B output configurations supported for both N′ = 16, N'=12, and N′ = 8 for a given number of virtual converters. Take care to ensure that the serial lane rate for a given configuration is within the supported range of 1.6875 Gbps to 16 Gbps.

Table 31. JESD204B Output Configurations for N′ = 16[1]

Number of Virtual Converters Supported (Same as M)	JESD204B Serial Lane Rate[2]	Supported Decimation Rates				JESD204B Transport Layer Settings[3]								
		Lane Rate = 1.6875 Gbps to 3.375 Gbps	Lane Rate = 3.375 Gbps to 6.75 Gbps	Lane Rate = 6.75 Gbps to 13.5 Gbps	Lane Rate = 13.5 Gbps to 16 Gbps	L	M	F	S	HD	N	N'	CS	K
1	20 × f_{OUT}	2, 4, 5, 6	1, 2, 3	1	N/A	1	1	2	1	0	8 to 16	16	0 to 3	See Note 4
	20 × f_{OUT}	2, 4, 5, 6	1, 2, 3	1	N/A	1	1	4	2	0	8 to 16	16	0 to 3	See Note 4
	10 × f_{OUT}	1, 2, 3	1,	N/A	N/A	2	1	1	1	1	8 to 16	16	0 to 3	See Note 4
	10 × f_{OUT}	1, 2, 3	1	N/A	N/A	2	1	2	2	0	8 to 16	16	0 to 3	See Note 4
	5 × f_{OUT}	1	N/A	N/A	N/A	4	1	1	2	1	8 to 16	16	0 to 3	See Note 4
	5 × f_{OUT}	1	N/A	N/A	N/A	4	1	2	4	0	8 to 16	16	0 to 3	See Note 4
2	40 × f_{OUT}	4, 8, 10, 12	2, 4, 5, 6	1, 2, 3	1	1	2	4	1	0	8 to 16	16	0 to 3	See Note 4
	40 × f_{OUT}	4, 8, 10, 12	2, 4, 5, 6	1, 2, 3	1	1	2	8	2	0	8 to 16	16	0 to 3	See Note 4
	20 × f_{OUT}	4, 5, 6	1, 2, 3	1	N/A	2	2	2	1	0	8 to 16	16	0 to 3	See Note 4
	20 × f_{OUT}	2, 4, 5, 6	1, 2, 3	1	N/A	2	2	4	2	0	8 to 16	16	0 to 3	See Note 4
	10 × f_{OUT}	1, 2, 3	1	N/A	N/A	4	2	1	1	1	8 to 16	16	0 to 3	See Note 4
	10 × f_{OUT}	1, 2, 3	1	N/A	N/A	4	2	2	2	0	8 to 16	16	0 to 3	See Note 4
4	80 × f_{OUT}	8, 16, 20, 24	4, 8, 10, 12	2, 4, 6	2	1	4	8	1	0	8 to 16	16	0 to 3	See Note 4
	40 × f_{OUT}	4, 8, 10, 12	2, 4, 5, 6	1, 2, 3	1	2	4	4	1	0	8 to 16	16	0 to 3	See Note 4
	40 × f_{OUT}	4, 8, 10, 12	2, 4, 5, 6	1, 2, 3	1	2	4	8	2	0	8 to 16	16	0 to 3	See Note 4
	20 × f_{OUT}	2, 4, 5, 6	1, 2, 3	1	N/A	4	4	2	1	0	8 to 16	16	0 to 3	See Note 4
	20 × f_{OUT}	2, 4, 5, 6	1, 2, 3	1	N/A	4	4	4	2	0	8 to 16	16	0 to 3	See Note 4
8	160 × f_{OUT}	16, 40, 48	8, 16, 20, 24	4, 8, 12	4	1	8	16	1	0	8 to 16	16	0 to 3	See Note 4
	80 × f_{OUT}	8, 16, 20, 24	4, 8, 10, 12	2, 4, 6	2	2	8	8	1	0	8 to 16	16	0 to 3	See Note 4
	40 × f_{OUT}	4, 8, 10, 12	2, 4, 6	2	N/A	4	8	4	1	0	8 to 16	16	0 to 3	See Note 4
	40 × f_{OUT}	4, 8, 10, 12	2, 4, 6	2	N/A	4	8	8	2	0	8 to 16	16	0 to 3	See Note 4

[1] Due to the internal clock requirements, only certain decimation rates are supported for certain link parameters.

[2] JESD204B transport layer descriptions are as follows: L is the number of lanes per converter device (lanes per link); M is the number of virtual converters per converter device (virtual converters per link); F is the octets per frame; S is the samples transmitted per virtual converter per frame cycle; HD is the high density mode; N is the virtual converter resolution (in bits); N' is the total number of bits per sample (JESD204B word size); CS is the number of control bits per conversion sample; K is the number of frames per multiframe.

[3] f_{ADC_CLK} is the ADC sample rate; DCM = chip decimation ratio; f_{OUT} is the output sample rate = f_{ADC_CLK}/DCM; SLR is the JESD204B serial lane rate. The following equations must be met due to internal clock divider requirements: SLR ≥ 1.6875 Gbps and SLR ≤ 16 Gbps; SLR/40 ≤ f_{ADC_CLK}; least common multiple (20 × DCM × f_{OUT}/SLR, DCM) ≤ 64. When the SLR is ≤ 16,000 Mbps and > 13,500 Mbps, Register 0x056E must be set to 0x30. When the SLR is ≤ 13,500 Mbps and ≥ 6750 Mbps, Register 0x056E must be set to 0x00. When the SLR is < 6750 Mbps and ≥ 3375 Mbps, Register 0x056E must be set to 0x10. When the SLR is < 3375 Mbps and ≥ 1687.5 Mbps, Register 0x056E must be set to 0x50.

[4] Only valid K × F values that are divisible by 4 are supported: for F = 1, K = 20, 24, 28, 32; for F = 2, K = 12, 16, 20, 24, 28, 32; for F = 4, K = 8, 12, 16, 20, 24, 28, 32; for F = 8, K = 4, 8, 12, 16, 20, 24, 28, 32; and for F = 16, K = 4, 8, 12, 16, 20, 24, 28, 32.

Table 32. JESD204B Output Configurations (N' = 12)[1]

No. of Virtual Converters Supported (Same Value as M)	Serial Lane Rate[2]	Supported Decimation Rates				JESD204B Transport Layer Settings[3]								
		Lane Rate = 1.6875 Gbps to 3.375 Gbps	Lane Rate = 3.375 Gbps to 6.75 Gbps	Lane Rate = 6.75 Gbps to 13.5 Gbps	Lane Rate = 13.5 Gbps to 16 Gbps	L	M	F	S	HD	N	N'	L	K
1	15 × f_{OUT}	3	N/A	N/A	N/A	1	1	3	2	0	8 to 12	12	0 to 3	See Note 4
	7.5 × f_{OUT}	N/A	N/A	N/A	N/A	2	1	3	4	1	8 to 12	12	0 to 3	See Note 4
	7.5 × f_{OUT}	N/A	N/A	N/A	N/A	2	1	6	8	0	8 to 12	12	0 to 3	See Note 4
	5 × f_{OUT}	1	N/A	N/A	N/A	3	1	1	2	1	8 to 12	12	0 to 3	See Note 4
2	30 × f_{OUT}	3, 6	3	N/A	N/A	1	2	3	1	0	8 to 12	12	0 to 3	See Note 4
	15 × f_{OUT}	3	N/A	N/A	N/A	2	2	3	2	0	8 to 12	12	0 to 3	See Note 4
	10 × f_{OUT}	1, 2, 3	1	N/A	N/A	3	2	1	1	1	8 to 12	12	0 to 3	See Note 4
	7.5 × f_{OUT}	N/A	N/A	N/A	N/A	4	2	3	4	0	8 to 12	12	0 to 3	See Note 4
4	60 × f_{OUT}	6, 12	3, 6	3	N/A	1	4	6	1	0	8 to 12	12	0 to 3	See Note 4
	30 × f_{OUT}	3, 6	3	N/A	N/A	2	4	3	1	0	8 to 12	12	0 to 3	See Note 4
	20 × f_{OUT}	2, 4, 5, 6	1, 2, 3	1	N/A	3	4	2	1	1	8 to 12	12	0 to 3	See Note 4
	15 × f_{OUT}	3	N/A	N/A	N/A	4	4	3	2	0	8 to 12	12	0 to 3	See Note 4
8	60 × f_{OUT}	6, 12	6	N/A	N/A	2	8	6	1	0	8 to 12	12	0 to 3	See Note 4
	30 × f_{OUT}	6	N/A	N/A	N/A	4	8	3	1	0	8 to 12	12	0 to 3	See Note 4

[1] Due to the internal clock requirements, only certain decimation rates are supported for certain link parameters.

[2] f_{ADC_CLK} is the ADC sample rate; DCM is the chip decimation ratio; f_{OUT} is the output sample rate = f_{ADC_CLK}/DCM; SLR is the JESD204B serial lane rate. The following equations must be met due to internal clock divider requirements: SLR ≥ 1.6875 Gbps and SLR ≤ 16 Gbps; SLR/40 ≤ f_{ADC_CLK}; least common multiple (20 × DCM × f_{OUT}/SLR, DCM) ≤ 64. When the SLR is ≤ 16,000 Mbps and > 13,500 Mbps, Register 0x056E must be set to 0x30. When the SLR is ≤ 13,500 Mbps and ≥ 6750 Mbps, Register 0x056E must be set to 0x00. When the SLR is < 6750 Mbps and ≥ 3375 Mbps, Register 0x056E must be set to 0x10. When the SLR is < 3375 Mbps and ≥ 1687.5 Mbps, Register 0x056E must be set to 0x50.

[3] JESD204B transport layer descriptions are as follows: L is the number of lanes per converter device (lanes per link); M is the number of virtual converters per converter device (virtual converters per link); F is the octets per frame; S is the samples transmitted per virtual converter per frame cycle; HD is the high density mode; N is the virtual converter resolution (in bits); N' is the total number of bits per sample (JESD204B word size); CS is the number of control bits per conversion sample; K is the number of frames per multiframe.

[4] Only valid K × F values that are divisible by 4 are supported: for F = 1, K = 20, 24, 28, 32; for F = 2, K = 12, 16, 20, 24, 28, 32; for F = 4, K = 8, 12, 16, 20, 24, 28, 32; for F = 8, K = 4, 8, 12, 16, 20, 24, 28, 32; and for F = 16, K = 4, 8, 12, 16, 20, 24, 28, 32.

Table 33. JESD204B Output Configurations for N′ = 8[1]

No. of Virtual Converters Supported (Same Value as M)	Serial Lane Rate[2]	Supported decimation rates				JESD204B Transport Layer Settings[3]								
		Lane Rate = 1.6875 Gbps to 3.375 Gbps	Lane Rate = 3.375 Gbps to 6.75 Gbps	Lane Rate = 6.75 Gbps to 13.5 Gbps	Lane Rate = 13.5 Gbps to 16 Gbps	L	M	F	S	HD	N	N'	CS	K
1	10 × f_{OUT}	1, 2, 3	1	N/A	N/A	1	1	1	1	0	7 to 8	8	0 to 1	See Note 4
1	10 × f_{OUT}	1, 2, 3	1	N/A	N/A	1	1	2	2	0	7 to 8	8	0 to 1	See Note 4
1	5 × f_{OUT}	1	N/A	N/A	N/A	2	1	1	2	0	7 to 8	8	0 to 1	See Note 4
1	5 × f_{OUT}	1	N/A	N/A	N/A	2	1	2	4	0	7 to 8	8	0 to 1	See Note 4
1	5 × f_{OUT}	1	N/A	N/A	N/A	2	1	4	8	0	7 to 8	8	0 to 1	See Note 4
1	2.5 × f_{OUT}	N/A	N/A	N/A	N/A	4	1	1	4	0	7 to 8	8	0 to 1	See Note 4
1	2.5 × f_{OUT}	N/A	N/A	N/A	N/A	4	1	2	8	0	7 to 8	8	0 to 1	See Note 4
2	20 × f_{OUT}	2, 4, 5, 6	1, 2, 3	1	N/A	1	2	2	1	0	7 to 8	8	0 to 1	See Note 4
2	10 × f_{OUT}	1, 2, 3	1	N/A	N/A	2	2	1	1	0	7 to 8	8	0 to 1	See Note 4
2	10 × f_{OUT}	1, 2, 3	1	N/A	N/A	2	2	2	2	0	7 to 8	8	0 to 1	See Note 4
2	5 × f_{OUT}	1	N/A	N/A	N/A	4	2	1	2	0	7 to 8	8	0 to 1	See Note 4
2	5 × f_{OUT}	1	N/A	N/A	N/A	4	2	2	4	0	7 to 8	8	0 to 1	See Note 4
2	5 × f_{OUT}	1	N/A	N/A	N/A	4	2	4	8	0	7 to 8	8	0 to 1	See Note 4

[1] Due to the internal clock requirements, only certain decimation rates are supported for certain link parameters.

[2] f_{ADC_CLK} is the ADC sample rate; DCM is the chip decimation ratio; f_{OUT} is the output sample rate = f_{ADC_CLK}/DCM; SLR is the JESD204B serial lane rate. The following equations must be met due to internal clock divider requirements: SLR ≥ 1.6875 Gbps and SLR ≤ 16 Gbps; SLR/40 ≤ f_{ADC_CLK}; least common multiple (20 × DCM × f_{OUT}/SLR, DCM) ≤ 64. When the SLR is ≤ 16,000 Mbps and > 13,500 Mbps, Register 0x056E must be set to 0x30. When the SLR is ≤ 13,500 Mbps and ≥ 6750 Mbps, Register 0x056E must be set to 0x00. When the SLR is < 6750 Mbps and ≥ 3375 Mbps, Register 0x056E must be set to 0x10. When the SLR is < 3375 Mbps and ≥ 1687.5 Mbps, Register 0x056E must be set to 0x50.

[3] JESD204B transport layer descriptions are as follows: L is the number of lanes per converter device (lanes per link); M is the number of virtual converters per converter device (virtual converters per link); F is the octets per frame; S is the samples transmitted per virtual converter per frame cycle; HD is the high density mode; N is the virtual converter resolution (in bits); N' is the total number of bits per sample (JESD204B word size); CS is the number of control bits per conversion sample; K is the number of frames per multiframe.

[4] Only valid K × F values that are divisible by 4 are supported: for F = 1, K = 20, 24, 28, 32; for F = 2, K = 12, 16, 20, 24, 28, 32; for F = 4, K = 8, 12, 16, 20, 24, 28, 32; for F = 8, K = 4, 8, 12, 16, 20, 24, 28, 32; and for F = 16, K = 4, 8, 12, 16, 20, 24, 28, 32.

Example Setup 1—Full Bandwidth Mode

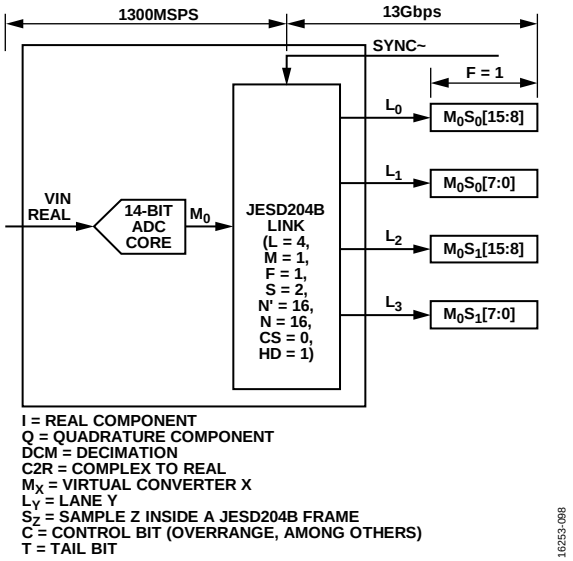


Figure 99. Full Bandwidth Mode

The AD9697 is set up as shown in Figure 99, with the following configurations:

- Two 14-bit converters at 1300 MSPS.
- Full bandwidth application layer mode.
- Decimation filters bypassed.

The JESD204B output configuration is as follows:

- Two virtual converters required (see Table 31).
- Output sample rate (f_{OUT}) = 1300/1 = 1300 MSPS.

The JESD204B supported output configurations are as follows (see Table 31):

- N′ = 16 bits.
- N = 14 bits.
- L = 4, M = 1, and F = 1.
- CS = 0.
- K = 32.
- Output serial lane rate:
  - 6.5 Gbps per lane (L = 4).
  - 13 Gbps per lane (L = 2).
- PLL control register:
  - Register 0x056E is set to 0x10 (L = 4).
  - Register 0x056E is set to 0x00 (L = 2).

Example Setup 2—ADC with DDC Option (Two ADCs Plus Two DDCs)

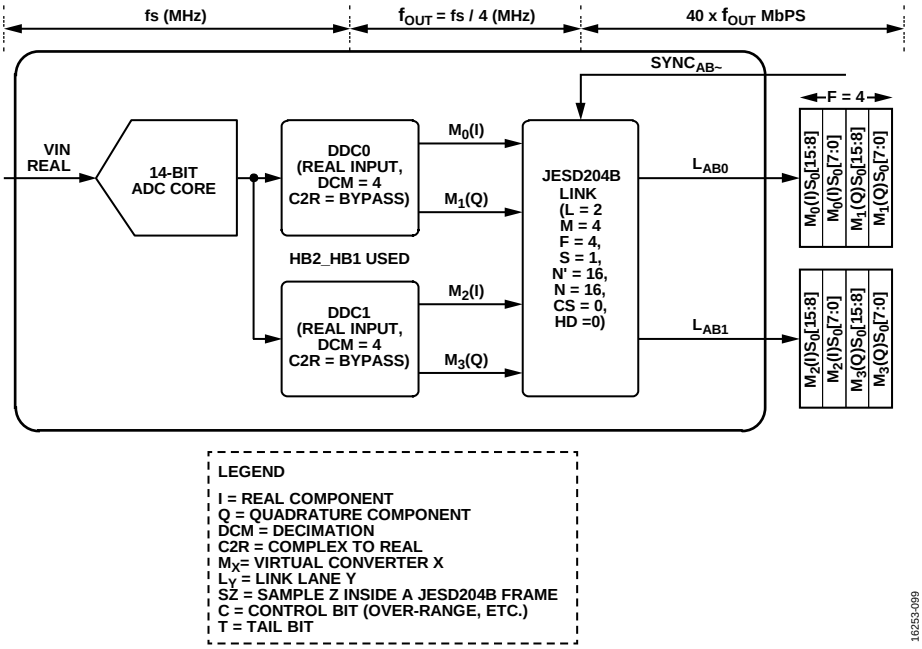


Figure 100. Two ADCs Plus Two DDCs Mode (L = 4, M = 4, F = 2, S = 1)

This example shows the flexibility in the digital and lane configurations for the AD9697. The sample rate is 1300 MSPS; whereas the outputs are all combined in a combination of either two or four lanes, depending on the input/output speed capability of the receiving device.

The AD9697 is set up as shown in Figure 100, with the following configuration:

- One 14-bit converter at 1300 MSPS.
- Two DDC application layer mode with complex outputs (I/Q).
- Chip decimation ratio = 4.
- DDC decimation ratio = 4 (see the Memory Map section).

The JESD204B output configuration is as follows:

- Four virtual converters required (see Table 31).
- Output sample rate (f_{OUT}) = 1300 MSPS/4 = 325 MSPS.

The JESD204B supported output configurations are as follows (see Table 31):

- N′ = 16 bits.
- N = 14 bits.
- L = 2, M = 4, and F = 4, or L = 4, M = 4, and F = 4.
- CS = 0.
- K = 32.
- Output serial lane rate = 6.5 Gbps per lane (L = 4), 13 Gbps per lane (L = 2)

For L = 2, set the PLL control register, Register 0x056E, to 0x00.
For L = 4, set the PLL control register, Register 0x056E, to 0x10.

DETERMINISTIC LATENCY

Both ends of the JESD204B link contain various clock domains distributed throughout each system. Data traversing from one clock domain to a different clock domain can lead to ambiguous delays in the JESD204B link. These ambiguities lead to non-repeatable latencies across the link from one power cycle or link reset to the next. Section 6 of the JESD204B specification addresses the issue of deterministic latency with mechanisms defined as Subclass 1 and Subclass 2.

The AD9697 supports JESD204B Subclass 0 and Subclass 1 operation. Register 0x0590, Bit 5 sets the subclass mode for the AD9697; the default mode is the Subclass 1 operating mode (Register 0x0590, Bit 5 = 1). If deterministic latency is not a system requirement, Subclass 0 operation is recommended and the SYSREF± signal may not be required. Even in Subclass 0 mode, the SYSREF± signal may be required in an application where multiple AD9697 devices must be synchronized with each other. This topic is addressed in the Timestamp Mode section.

SUBCLASS 0 OPERATION

If there is no requirement for multichip synchronization while operating in Subclass 0 mode (Register 0x0590, Bit 5 = 0), the SYSREF± input can be left disconnected. In this mode, the relationship of the JESD204B clocks between the JESD204B transmitter and receiver are arbitrary but does not affect the ability of the receiver to capture and align the lanes within the link.

SUBCLASS 1 OPERATION

The JESD204B protocol organizes data samples into octets, frames, and multiframes as described in the Transport Layer section. The LMFC is synchronous with the beginnings of these multiframes. In Subclass 1 operation, the SYSREF± signal synchronizes the LMFCs for each device in a link or across multiple links (within the AD9697, SYSREF± also synchronizes the internal sample dividers). This synchronization is shown in Figure 101. The JESD204B receiver uses the multiframe boundaries and buffering to achieve consistent latency across lanes (or even multiple devices), and to achieve a fixed latency between power cycles and link reset conditions.

Deterministic Latency Requirements

Several key factors are required for achieving deterministic latency in a JESD204B Subclass 1 system:

- SYSREF± signal distribution skew within the system must be less than the desired uncertainty for the system.
- SYSREF± setup and hold time requirements must be met for each device in the system.
- The total latency variation across all lanes, links, and devices must be ≤1 LMFC period (see Figure 101). This includes both variable delays and the variation in fixed delays from lane to lane, link to link, and device to device in the system.

Setting Deterministic Latency Registers

The JESD204B receive buffer in the logic device buffers data starting on the LMFC boundary. If the total link latency in the system is near an integer multiple of the LMFC period, it is possible that from one power cycle to the next, the data arrival time at the receive buffer may straddle an LMFC boundary. To ensure deterministic latency in this case, a phase adjustment of the LMFC at either the transmitter or receiver must be performed. Typically, adjustments to accommodate the receive buffer are made to the LMFC of the receiver. In the AD9697, this adjustment can be made using the LMFC offset bits (Register 0x0578, Bits[4:0]). These bits delay the LMFC in frame clock increments, depending on the F parameter, which is the number of octets per lane per frame). For F = 1, every fourth setting (0, 4, 8, …, and so on) results in a one frame clock shift. For F = 2, every other setting (0, 2, 4, …, and so on) results in a 1-frame clock shift. For all other values of F, each setting results in a 1-frame clock shift.

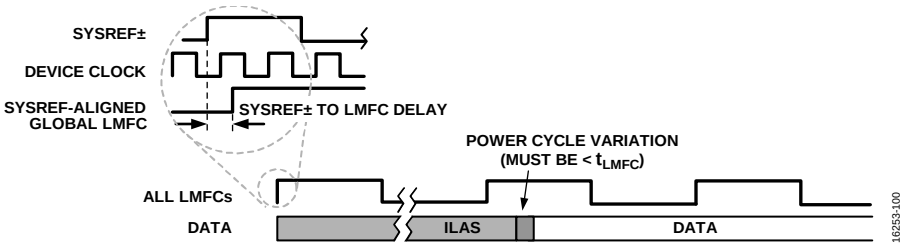


Figure 101. SYSREF± and LMFC

Figure 102 shows that, in the case where the link latency is near an LMFC boundary, the local LMFC of the AD9697 can be delayed to in turn delay the data arrival time at the receiver. Figure 103 shows how the LMFC of the receiver is delayed to accommodate the receive buffer timing. Refer to the applicable JESD204B receiver user guide for details on making this adjustment. If the total latency in the system is not near an integer multiple of the LMFC period, or if the appropriate adjustments are made to the LMFC phase at the clock source, it is still possible to have variable latency from one power cycle to the next. In this case, check for the possibility that the setup and hold time requirements for the SYSREF± signal are not being met. Perform this check by reading the SYSREF± setup and hold monitor register (Register 0x0128).

This function is described in the SYSREF± Setup/Hold Window Monitor section.

If reading Register 0x0128 indicates a timing problem, there are adjustments that can made in the AD9697. Changing the SYSREF± level used for alignment is possible using the SYSREF± transition select bit (Register 0x0120, Bit 4). Also, changing which edge of the clock is used to capture SYSREF± can be performed using the clock edge select bit (Register 0x0120, Bit 3). Both of these options are described in the SYREF± Control Features section. If neither of these measures help achieve an acceptable setup and hold time, adjusting the phase of SYSREF± and/or the device clock (CLK±) may be required.

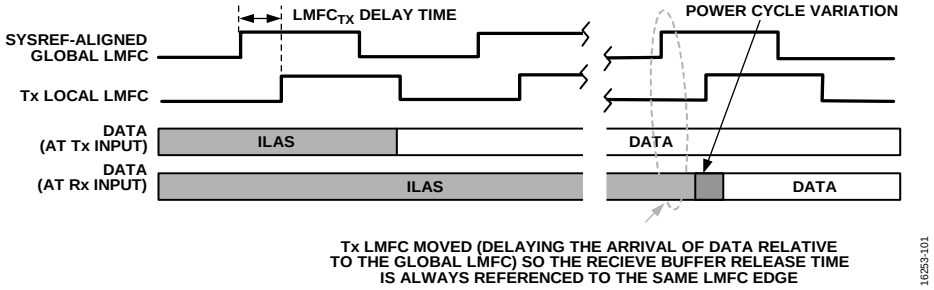


Figure 102. Adjusting the JESD204B Tx LMFC in the AD9697

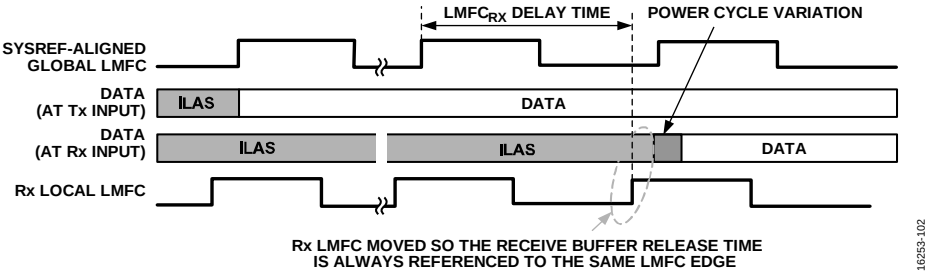


Figure 103. Adjusting the JESD204B Rx LMFC in the Logic Device

MULTICHIP SYNCHRONIZATION

The flowchart shown in Figure 105 describes the internal mechanism for multichip synchronization in the AD9697. There are two methods by which multichip synchronization can take place, as determined by the chip synchronization mode bit (Register 0x1FF , Bit 0). Each method involves different applications of the SYSREF± signal.

NORMAL MODE

The default sate of the chip synchronization mode bit is 0, which configures the AD9697 for normal chip synchronization. The JESD204B standard specifies the use of SYSREF± to provide deterministic latency within a single link. This same concept, when applied to a system with multiple converters and logic devices, can also provide multichip synchronization. In Figure 105, this is referred to as normal mode. Following the process outlined in the flowchart ensures that the AD9697 is configured appropriately. Consult the logic devices user intellectual property (IP) guide to ensure that the JESD204B receivers are configured appropriately.

TIMESTAMP MODE

For all AD9697 full bandwidth operating modes, the SYSREF± input can also be used to timestamp samples. This is another method by which multiple devices can achieve synchronization. This is especially effective when synchronizing multiple converters to one or more logic devices. The logic devices buffer the data streams, identify the time stamped samples, and align them. When the chip synchronization mode bit (Register 0x1FF, Bit 0) is set to 1, the timestamp method is used for synchronization of multiple channels and/or devices. In timestamp mode, the clocks are not reset but instead, the coinciding sample is time stamped using the JESD204B control bits of that sample. To operate in timestamp mode, the following additional settings are necessary:

- Continuous or N-shot SYSREF enabled (Register 0x0120, Bits[2:1] = 1 or 2).
- At least one control bit must be enabled (CS > 0, Register 0x058F, Bits[7:6] = 1, 2, or 3).
- Set the function for one of the control bits to SYSREF:
  - Register 0x0559, Bits[2:0] = 5 if using Control Bit 0.
  - Register 0x0559, Bits[6:4] = 5 if using Control Bit 1.
  - Register 0x055A, Bits[2:0] = 5 if using Control Bit 2.

Enable control bits MSB first. In other words, if only using one control bit (CS = 1), then Control Bit 2 must be enabled. If two control bits are used, then Control Bits[2:1] must be enabled. Figure 104 shows how the input sample coincident with SYSREF± is time stamped and ultimately output of the ADC. In this example, there are two control bits and Control Bit 1 is the bit indicating which sample was coincident with the SYSREF rising edge. If so desired, the SYSREF timestamp delay register (Register 0x0123) can be used to adjust the timing of which sample is time stamped.

Note that time stamping is not supported by any AD9697 operating modes that use decimation.

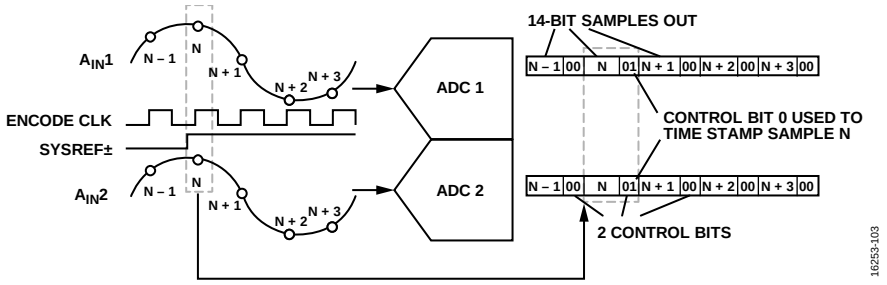


Figure 104. AD9697 Timestamping—CS = 2 (Register 0x058F, Bits[7:6] = 2), Control Bit 1 is SYSREF± (Register 0x0559, Bits[6:4] = 5)

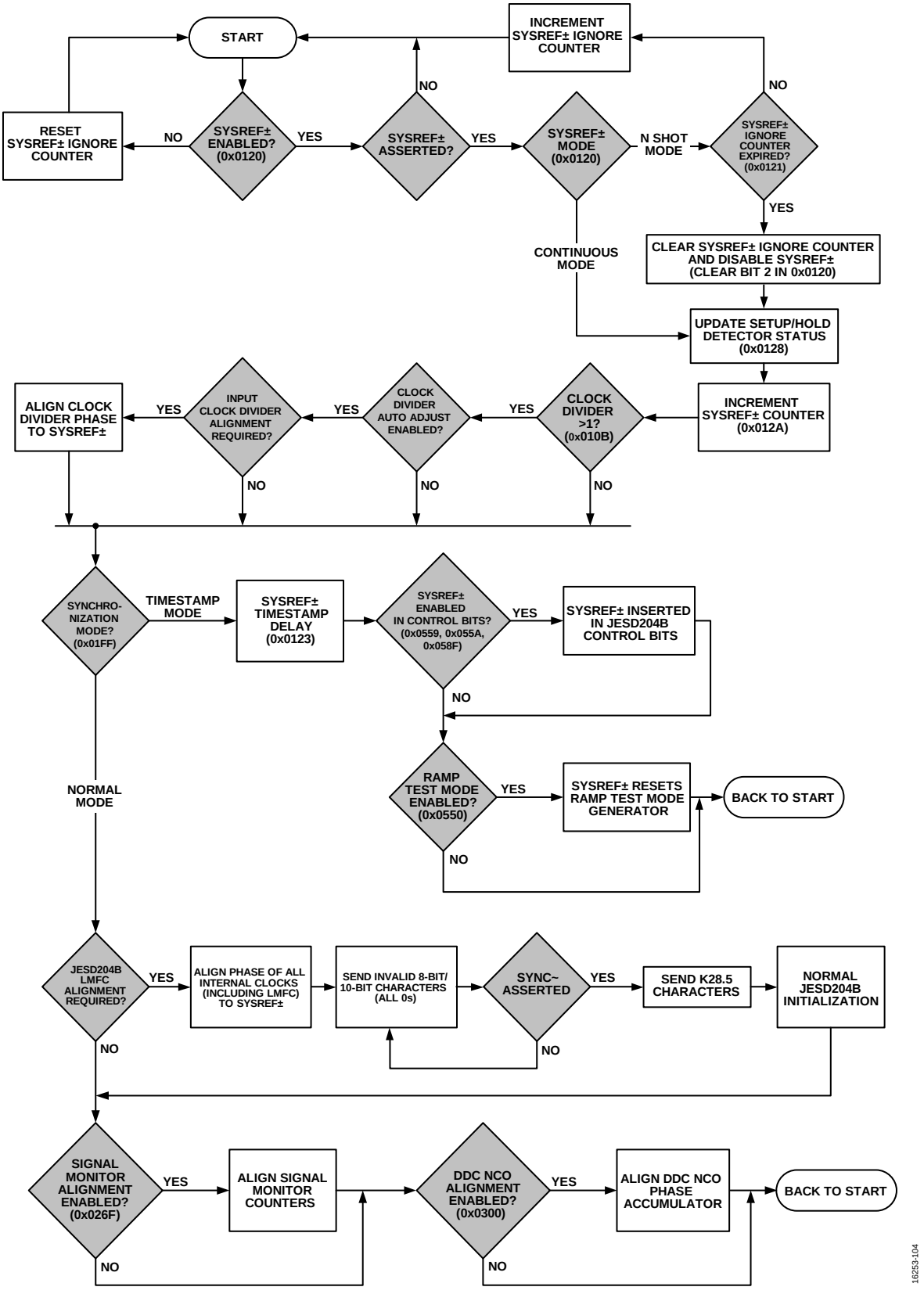


Figure 105. SYSREF± Capture Scenarios and Multichip Synchronization

SYSREF± INPUT

The SYSREF± input signal is used as a high accuracy system reference for deterministic latency and multichip synchronization. The AD9697 accepts a single-shot or periodic input signal. The SYSREF± mode select bits (Register 0x0120, Bits[2:1]) select the input signal type and also arm the SYSREF± state machine when set. If in single- (or N) shot mode (Register 0x0120, Bits[2:1] = 2), the SYSREF± mode select bit self clears after the appropriate SYSREF± transition is detected. The pulse width must have a minimum width of two CLK± periods. If the clock divider (Register 0x010B, Bits[2:0]) is set to a value other than divide by 1, then multiply this minimum pulse width requirement by the divide ratio (for example, if set to divide by 8, the minimum pulse width is 16 CLK± cycles). When using a continuous SYSREF± signal (Register 0x0120, Bits[2:1] = 1), the period of the SYSREF± signal must be an integer multiple of the LMFC. Derive the LMFC using the following formula:

$$LMFC = ADC\ Clock/S \times K$$

where:
S is the JESD204B parameter for number of samples per converter.
K is JESD204B parameter for number of frames per multiframe.

The input clock divider, DDCs, signal monitor block, and JESD204B link are all synchronized using the SYSREF± input when in normal synchronization mode (Register 0x01FF, Bits[1:0] = 0). The SYSREF± input can also be used to time stamp an ADC sample to provide a mechanism for synchronizing multiple AD9697 devices in a system. For the highest level of timing accuracy, SYSREF± must meet the setup and hold requirements relative to the CLK± input. There are several features in the AD9697 to ensure these requirements are met (see the SYREF± Control Features section).

SYREF± Control Features

SYSREF± is used, along with the input clock (CLK±), as part of a source synchronous timing interface and requires setup and hold timing requirements of 117 ps and −96 ps, relative to the input clock (see Figure 106). The AD9697 has several features to meet these requirements. First, the SYSREF± sample event can be defined as either a synchronous low to high transition or synchronous high to low transition. Second, the AD9697 allows the SYSREF± signal to be sampled using either the rising edge or falling edge of the input clock. Figure 106, Figure 107, Figure 108, and Figure 109 show all four possible combinations.

The third SYSREF± related feature available is the ability to ignore a programmable number (up to 16) of SYSREF± events. The SYSREF± ignore feature is enabled by setting the SYSREF± mode register (Register 0x0120, Bits[2:1]) to 2'b10, which is labeled as N shot mode. The AD9697 is able to ignore N SYSREF± events, which is useful to handle periodic SYSREF± signals that require time to settle after startup. Ignoring SYSREF± until the clocks in the system have settled avoids an inaccurate SYSREF± trigger. Figure 110 shows an example of the SYSREF± ignore feature when ignoring three SYSREF± events.

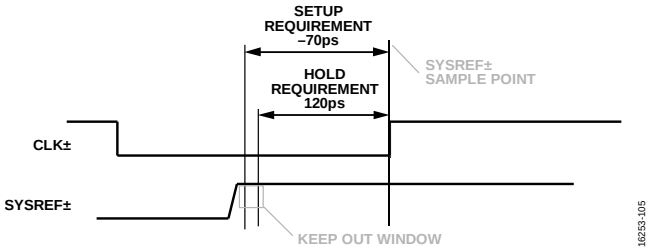


Figure 106. SYSREF± Setup and Hold Time Requirements; SYSREF± Low to High Transition Using the Rising Edge Clock (Default)

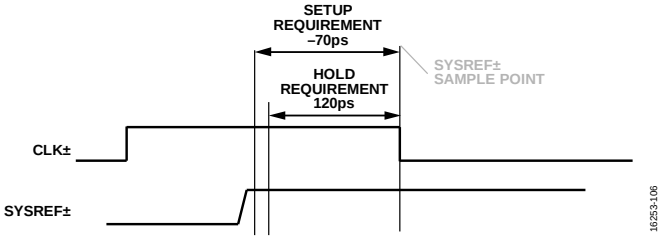


Figure 107. SYSREF± Low to High Transition Using Falling Edge Clock Capture (Register 0x0120, Bit 4 = 1'b0 and Register 0x0120, Bit 3 = 1'b1)

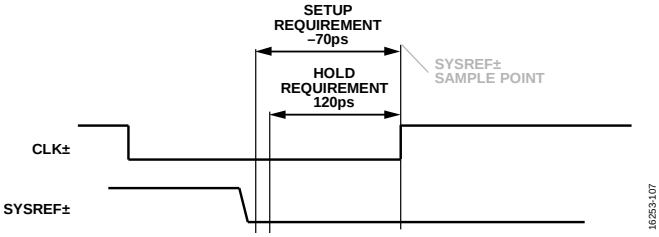


Figure 108. SYSREF± High to Low Transition Using Rising Edge Clock Capture (Register 0x0120, Bit 4 = 1'b1 and Register 0x0120, Bit 3 = 1'b0)

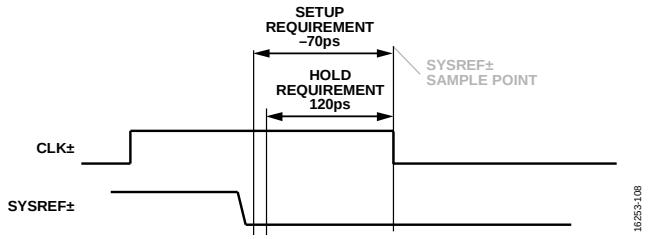


Figure 109. SYSREF± High to Low Transition Using Falling Edge Clock Capture (Register 0x0120, Bit 4= 1'b1 and Register 0x0120, Bit 3 = 1'b1)

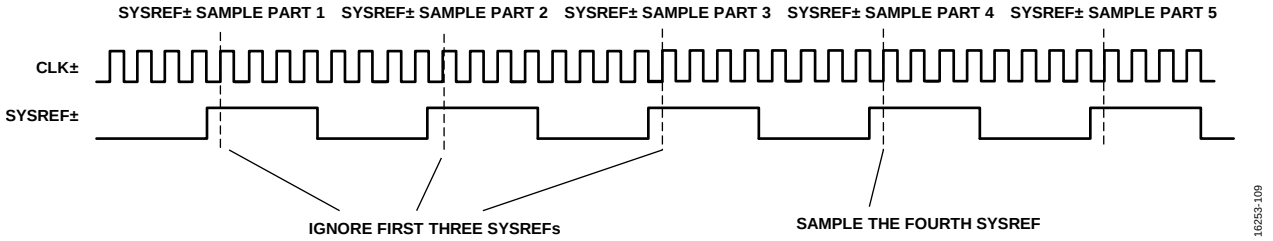


Figure 110. SYSREF± Ignore Example; SYSREF± Ignore Count Bits (Register 0x0121, Bits[3:0]) = 3

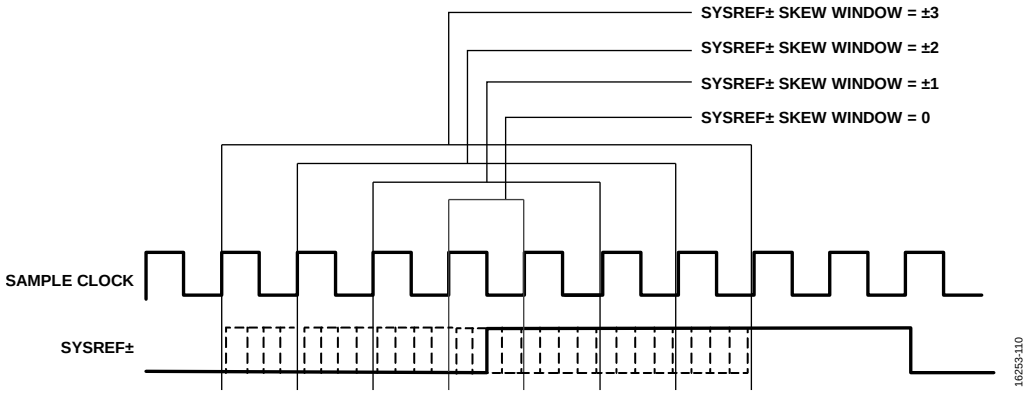


Figure 111. SYSREF± Skew Window

When in continuous SYSREF± mode (Register 0x0120, Bits[2:1] = 1), the AD9697 monitors the placement of the SYSREF± leading edge compared to the internal LMFC. If the SYSREF± edge is captured with a clock edge other than the one that is aligned with LMFC, the AD9697 initiates a resynchronization of the link. Because the input clock rates for the AD9697 can be up to 4 GHz, the AD9697 provides another SYSREF± related feature that makes it possible to accommodate periodic SYSREF± signals where cycle accurate capture is not feasible or not required. For these scenarios, the AD9697 has a programmable SYSREF± skew window that allows the internal dividers to remain undisturbed, unless SYSREF± occurs outside the skew window. The resolution of the SYSREF± skew window is set in sample clock cycles. If the SYSREF± negative skew window is 1 and the positive skew window is 1, then the total skew window is ±1 sample clock cycles, meaning that, as long as SYSREF± is captured within ±1 sample clock cycle of the clock that is aligned with LMFC, the link continues to operate normally. If the SYSREF± has jitter, which can cause a misalignment between SYSREF± and the LMFC, the system continues to run without a resynchronization, while still allowing the device to monitor for larger errors not caused by jitter. For the AD9697, the positive and negative skew window is controlled by the SYSREF± window negative bits (Register 0x0122, Bits[3:2]) and the SYSREF± window positive bits (Register 0x0122, Bits[1:0]). Figure 111 shows information on the location of the skew window settings relative to Phase 0 of the internal dividers. Negative skew is defined as occurring before the internal dividers reach Phase 0 and positive skew is defined after the internal dividers reach Phase 0.

SYSREF± SETUP/HOLD WINDOW MONITOR

To ensure a valid SYSREF± signal capture, the AD9697 has a SYSREF± setup/hold window monitor. This feature allows the system designer to determine the location of the SYSREF± signals relative to the CLK± signals by reading back the amount of setup/hold margin on the interface through the memory map. Figure 112 and Figure 113 show the setup and hold status values for different phases of SYSREF±.

The setup detector returns the status of the SYSREF± signal before the CLK± edge, and the hold detector returns the status of the SYSREF signal after the CLK± edge. Register 0x0128 stores the status of SYSREF± and lets the user know if the SYSREF± signal is captured by the ADC.

Table 34 describes the contents of Register 0x0128 and how to interpret them.

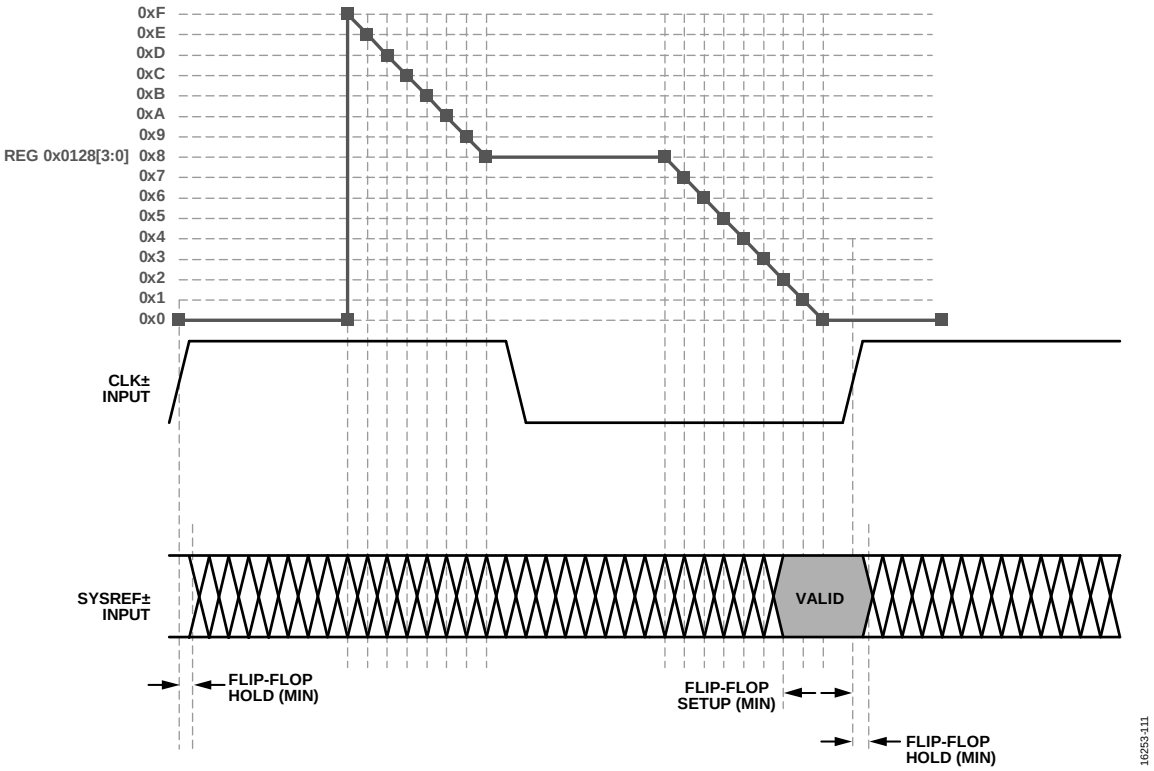


Figure 112. SYSREF± Setup Detector

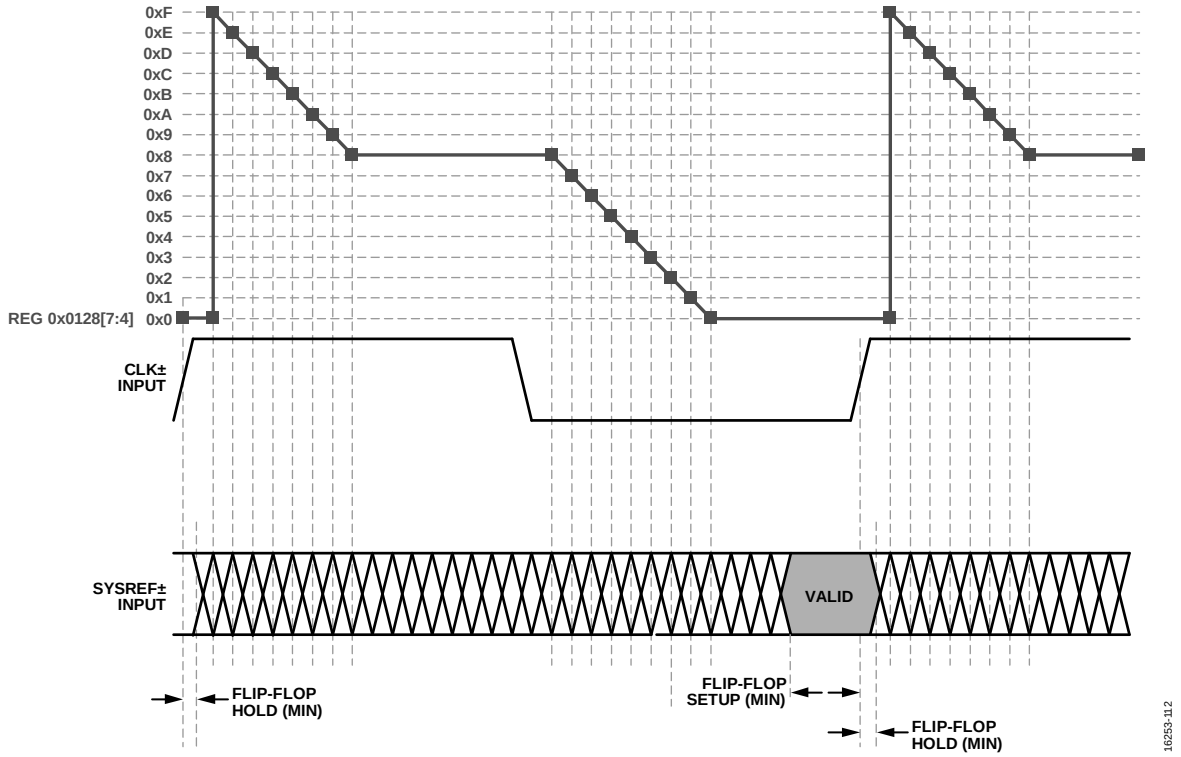


Figure 113. SYSREF± Hold Detector

Table 34. SYSREF± Setup/Hold Monitor, Register 0x0128

Register 0x0128, Bits[7:4] Hold Status	Register 0x0128, Bits[3:0] Setup Status	Description
0x0	0x0 to 0x7	Possible setup error. The smaller this number, the smaller the setup margin.
0x0 to 0x8	0x8	No setup or hold error (best hold margin).
0x8	0x9 to 0xF	No setup or hold error (best setup and hold margin).
0x8	0x0	No setup or hold error (best setup margin).
0x9 to 0xF	0x0	Possible hold error. The larger this number, the smaller the hold margin.
0x0	0x0	Possible setup or hold error.

LATENCY

END TO END TOTAL LATENCY

Total latency in the AD9697 is dependent on the chip application mode and the JESD204B configuration. For any given combination of these parameters, the latency is deterministic, however, the value of this deterministic latency must be calculated as described in the Example Latency Calculations section.

Table 35 shows the combined latency through the ADC and DSP for the different chip application modes supported by the AD9697. Table 36 shows the latency through the JESD204B block for each application mode based on the M/L ratio. For both tables, latency is typical and is in units of the encode clock. The latency through the JESD204B block does not depend on the output data type (real or complex). Therefore, data type is not included in Table 35 and Table 36.

To determine the total latency, select the appropriate ADC + DSP latency from Table 35 and add it to the appropriate JESD204B latency from Table 36. Example calculations are provided in the following section.

EXAMPLE LATENCY CALCULATIONS

Example Configuration 1 is as follows:

- ADC application mode = full bandwidth
- Real outputs
- L = 4, M = 1, F = 1, S = 2 (JESD204B mode)
- M/L = 0.25
- Latency = 31 + 44 = 75 encode clocks

Example Configuration 2 is as follows:

- ADC application mode = DCM4
- Complex outputs
- L = 2, M = 2, F = 2, S = 1 (JESD204B mode)
- M/L = 1
- Latency = 162 + 50 = 212 encode clocks

LMFC REFERENCED LATENCY

Some FPGA vendors may require the end user to know LMFC referenced latency to make appropriate deterministic latency adjustments. If they are required, the latency values in Table 35 and Table 36 can be used for the analog input to LMFC and LMFC to data output latency values, respectively.

Table 35. Latency Through the ADC + DSP Blocks (Number of Sample Clocks)[1]

Chip Application Mode	Enabled Filters	ADC + DSP Latency
Full Bandwidth	Not applicable	31
DCM1 (Real)	HB1	90
DCM2 (Complex)	HB1	90
DCM3 (Complex)	TB1	102
DCM2 (Real)	HB2 + HB1	162
DCM4 (Complex)	HB2 + HB1	162
DCM3 (Real)	TB2 + HB1	212
DCM6 (Complex)	TB2 + HB1	212
DCM4 (Real)	HB3 +HB2 + HB1	292
DCM8 (Complex)	HB3 +HB2 + HB1	292
DCM5 (Real)	FB2 + HB1	380
DCM10 (Complex)	FB2 + HB1	380
DCM6 (Real)	TB2 + HB2 + HB1	424
DCM12 (Complex)	TB2 + HB2 + HB1	424
DCM15 (Real)	FB2 + TB1	500
DCM8 (Real)	HB4 + HB3 + HB2 + HB1	552
DCM16 (Complex)	HB4 + HB3 + HB2 + HB1	552
DCM10 (Real)	FB2 + HB2 + HB1	694
DCM20 (Complex)	FB2 + HB2 + HB1	694
DCM12 (Real)	TB2 + HB3 + HB2 + HB1	814
DCM24 (Complex)	TB2 + HB3 + HB2 + HB1	814
DCM30 (Complex)	HB2 + FB2 + TB1	836
DCM20 (Real)	FB2 + HB3 + HB2 + HB1	1420
DCM40 (Complex)	FB2 + HB3 + HB2 + HB1	1420
DCM24 (Real)	TB2 + HB4 + HB3 + HB2 + HB1	1594
DCM48 (Complex)	TB2 + HB4 + HB3 + HB2 + HB1	1594

[1] DCMx indicates the decimation ratio.

Table 36. Latency Through JESD204B Block (Number of Sample Clocks)[1]

	M/L Ratio[2]						
Chip Application Mode	**0.125**	**0.25**	**0.5**	**1**	**2**	**4**	**8**
Full Bandwidth	82	44	25	14	7	9	3
DCM1	82	44	25	14	7	N/A	N/A
DCM2	160	84	46	27	14	7	N/A
DCM3	237	124	67	39	21	11	N/A
DCM4	315	164	88	50	27	14	9
DCM5	N/A	203[3]	109[3]	62[3]	43[3]	N/A	N/A
DCM6	N/A	243	130	73	39	21	14
DCM8	N/A	323	172	96	50	27	18
DCM10	N/A	N/A	213	119	62	33	22
DCM12	N/A	N/A	255	142	73	39	27
DCM15	N/A	N/A	318[4]	176[4]	90[4]	47[4]	33[4]
DCM16	N/A	N/A	339[4]	188[4]	96[4]	50[4]	35[4]
DCM20	N/A	N/A	N/A	233	119	62	43
DCM24	N/A	N/A	N/A	279	142	73	51
DCM30	N/A	N/A	N/A	348[4]	176[4]	90[4]	62[4]
DCM40	N/A	N/A	N/A	N/A	233[4]	119[4]	82[4]
DCM48	N/A	N/A	N/A	N/A	279[4]	142[4]	97[4]

[1] N/A means not applicable and indicates that the application mode is not supported at the M/L ratio listed.
[2] M/L ratio is the number of converters divided by the number of lanes for the configuration.
[3] The application mode at the M/L ratio listed is only supported in real output mode.
[4] The application mode at the M/L ratio listed is only supported in complex output mode.

TEST MODES

ADC TEST MODES

The AD9697 has various test options that aid in the system level implementation. The AD9697 has ADC test modes that are available in Register 0x0550. These test modes are described in Table 37. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back end blocks, and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting and some are not. The pseudorandom number (PN) generators from the PN sequence tests can be reset by setting Bit 4 or Bit 5 of Register 0x0550. These tests can be performed with or without an analog signal (if present, the analog signal is ignored); however, they do require an encode clock.

If application mode is set to select a DDC mode of operation, the test modes must be enabled for each DDC enabled. The test patterns can be enabled via Bit 0 of Register 0x0327, Register 0x0347, Register 0x0367, and Register 0x0387 depending on which DDC(s) are selected. The (I) data uses the test patterns selected, and the (Q) data does not output test patterns. For more information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

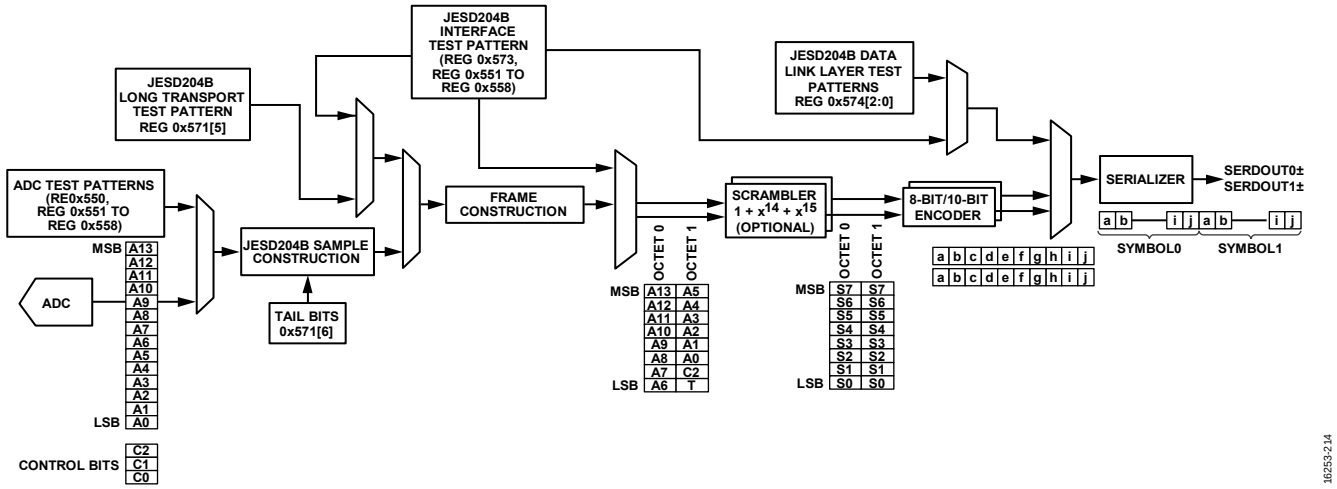


Figure 114. ADC Output Datapath Showing Data Framing

Table 37. ADC Test Modes[1]

Output Test Mode Bit Sequence	Pattern Name	Expression	Default/ Seed Value	Sample (N, N + 1, N + 2, …)
0000	Off (default)	N/A	N/A	N/A
0001	Midscale short	0000 0000 0000	N/A	N/A
0010	Positive full-scale short	01 1111 1111 1111	N/A	N/A
0011	Negative full-scale short	10 0000 0000 0000	N/A	N/A
0100	Checkerboard	10 1010 1010 1010	N/A	0x1555, 0x2AAA, 0x1555, 0x2AAA, 0x1555
0101	PN sequence long	$x^{23} + x^{18} + 1$	0x3AFF	0x3FD7, 0x0002, 0x26E0, 0x0A3D, 0x1CA6
0110	PN sequence short	$x^9 + x^5 + 1$	0x0092	0x125B, 0x3C9A, 0x2660, 0x0C65, 0x0697
0111	One-/zero-word toggle	11 1111 1111 1111	N/A	0x0000, 0x3FFF, 0x0000, 0x3FFF, 0x0000
1000	User input	Register 0x0551 to Register 0x0558	N/A	User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], User Pattern 1[15:2] … for repeat mode. User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], 0x0000 … for single mode.
1111	Ramp output	(x) % 2^{14}	N/A	(x) % 2^{14}, (x +1) % 2^{14}, (x +2) % 2^{14}, (x +3) % 2^{14}

[1] N/A means not applicable.

JESD204B BLOCK TEST MODES

In addition to the ADC pipeline test modes, the AD9697 also has flexible test modes in the JESD204B block. These test modes are listed in Register 0x0573 and Register 0x0574. These test patterns can be injected at various points along the output datapath. These test injection points are shown in Figure 114. Table 38 describes the various test modes available in the JESD204B block. For the AD9697, a transition from test modes (Register 0x0573 ≠ 0x00) to normal mode (Register 0x0573 = 0x00) requires an SPI soft reset. This is done by writing 0x81 to Register 0x0000 (self cleared).

Transport Layer Sample Test Mode

The transport layer samples are implemented in the AD9697 as defined by Section 5.1.6.3 in the JEDEC JESD204B specification. These tests are shown in Register 0x0571, Bit 5. The test pattern is equivalent to the raw samples from the ADC.

Interface Test Modes

The interface test modes are described in Register 0x0573, Bits[3:0]. These test modes are also explained in Table 38. The interface tests can be injected at various points along the data. See Figure 114 for more information on the test injection points. Register 0x0573, Bits[5:4] show where these tests are injected.

Table 39, Table 40, and Table 41 show examples of some of the test modes when injected at the JESD sample input, PHY 10-bit input, and scrambler 8-bit input. UPx in the tables represent the user pattern control bits from the customer register map.

Table 38. JESD204B Interface Test Modes

Output Test Mode Bit Sequence	Pattern Name	Expression	Default
0000	Off (default)	Not applicable	Not applicable
0001	Alternating checker board	0x5555, 0xAAAA, 0x5555, …	Not applicable
0010	1/0 word toggle	0x0000, 0xFFFF, 0x0000, …	Not applicable
0011	31-bit PN sequence	$x^{31} + x^{28} + 1$	0x0003AFFF
0100	23-bit PN sequence	$x^{23} + x^{18} + 1$	0x003AFF
0101	15-bit PN sequence	$x^{15} + x^{14} + 1$	0x03AF
0110	9-bit PN sequence	$x^{9} + x^{5} + 1$	0x092
0111	7-bit PN sequence	$x^{7} + x^{6} + 1$	0x07
1000	Ramp output	(x) % 2^{16}	Ramp size depends on test injection point
1110	Continuous/repeat user test	Register 0x0551 to Register 0x0558	User Pattern 1 to User Pattern 4, then repeat
1111	Single user test	Register 0x0551 to Register 0x0558	User Pattern 1 to User Pattern 4, then zeros

Table 39. JESD204B Sample Input for M = 2, S = 2, N' = 16 (Register 0x0573, Bits[5:4] = 'b00)

Frame No.	Converter No.	Sample No.	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0	0	0x5555	0x0000	(x) % 2^{16}	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	0	1	0x5555	0x0000	(x) % 2^{16}	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	1	0	0x5555	0x0000	(x) % 2^{16}	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	1	1	0x5555	0x0000	(x) % 2^{16}	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
1	0	0	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	0	1	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	1	0	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	1	1	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
2	0	0	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	0	1	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	1	0	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	1	1	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
3	0	0	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	0	1	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	1	0	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	1	1	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
4	0	0	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	0	1	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	1	0	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	1	1	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000

Table 40. Physical Layer 10-Bit Input (Register 0x0573, Bits[5:4] = 'b01)

10-Bit Symbol Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0x155	0x000	(x) % 2^{10}	0x125	0x3FD	UP1[15:6]	UP1[15:6]
1	0x2AA	0x3FF	(x + 1) % 2^{10}	0x2FC	0x1C0	UP2[15:6]	UP2[15:6]
2	0x155	0x000	(x + 2) % 2^{10}	0x26A	0x00A	UP3[15:6]	UP3[15:6]
3	0x2AA	0x3FF	(x + 3) % 2^{10}	0x198	0x1B8	UP4[15:6]	UP4[15:6]
4	0x155	0x000	(x + 4) % 2^{10}	0x031	0x028	UP1[15:6]	0x000
5	0x2AA	0x3FF	(x + 5) % 2^{10}	0x251	0x3D7	UP2[15:6]	0x000
6	0x155	0x000	(x + 6) % 2^{10}	0x297	0x0A6	UP3[15:6]	0x000
7	0x2AA	0x3FF	(x + 7) % 2^{10}	0x3D1	0x326	UP4[15:6]	0x000
8	0x155	0x000	(x + 8) % 2^{10}	0x18E	0x10F	UP1[15:6]	0x000
9	0x2AA	0x3FF	(x + 9) % 2^{10}	0x2CB	0x3FD	UP2[15:6]	0x000
10	0x155	0x000	(x + 10) % 2^{10}	0x0F1	0x31E	UP3[15:6]	0x000
11	0x2AA	0x3FF	(x + 11) % 2^{10}	0x3DD	0x008	UP4[15:6]	0x000

Table 41. Scrambler 8-Bit Input (Register 0x0573, Bits[5:4] = 'b10)

8-Bit Octet Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0x55	0x00	(x) % 2^{8}	0x49	0xFF	UP1[15:9]	UP1[15:9]
1	0xAA	0xFF	(x + 1) % 2^{8}	0x6F	0x5C	UP2[15:9]	UP2[15:9]
2	0x55	0x00	(x + 2) % 2^{8}	0xC9	0x00	UP3[15:9]	UP3[15:9]
3	0xAA	0xFF	(x + 3) % 2^{8}	0xA9	0x29	UP4[15:9]	UP4[15:9]
4	0x55	0x00	(x + 4) % 2^{8}	0x98	0xB8	UP1[15:9]	0x00
5	0xAA	0xFF	(x + 5) % 2^{8}	0x0C	0x0A	UP2[15:9]	0x00
6	0x55	0x00	(x + 6) % 2^{8}	0x65	0x3D	UP3[15:9]	0x00
7	0xAA	0xFF	(x + 7) % 2^{8}	0x1A	0x72	UP4[15:9]	0x00
8	0x55	0x00	(x + 8) % 2^{8}	0x5F	0x9B	UP1[15:9]	0x00
9	0xAA	0xFF	(x + 9) % 2^{8}	0xD1	0x26	UP2[15:9]	0x00
10	0x55	0x00	(x + 10) % 2^{8}	0x63	0x43	UP3[15:9]	0x00
11	0xAA	0xFF	(x + 11) % 2^{8}	0xAC	0xFF	UP4[15:9]	0x00

Data Link Layer Test Modes

The data link layer test modes are implemented in the AD9697 as defined by Section 5.3.3.8.2 in the JEDEC JESD204B specification. These tests are shown in Register 0x0574, Bits[2:0]. Test patterns inserted at this point are useful for verifying the functionality of the data link layer. When the data link layer test modes are enabled, disable SYNCINB± by writing 0xC0 to Register 0x0572.

SERIAL PORT INTERFACE (SPI)

The AD9697 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the Serial Control Interface Standard (Rev. 1.0).

CONFIGURATION USING THE SPI

Three pins define the SPI of the AD9697 ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 42). The SCLK (serial clock) pin is used to synchronize the read and write data presented to and from the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 42. Serial Port Interface Pins

Mnemonic	Function
SCLK	Serial clock. The serial shift clock input that is used to synchronize serial interface, reads, and writes.
SDIO	Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active low control that gates the read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 4 and Table 5.

Other modes involving the CSB pin are available. The CSB pin can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB can stall high between bytes to allow additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued, which allows the SDIO pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the Serial Control Interface Standard (Rev. 1.0).

HARDWARE INTERFACE

The pins described in Table 42 comprise the physical interface between the user programming device and the serial port of the AD9697. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

Do not activate the SPI port during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9697 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI ACCESSIBLE FEATURES

Table 43 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the Serial Control Interface Standard (Rev. 1.0). The AD9697 device specific features are described in the Memory Map section.

Table 43. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode.
Clock	Allows the user to access the clock divider via the SPI.
DDC	Allows the user to set up decimation filters for different applications.
Test Input/Output	Allows the user to set test modes to have known data on output bits.
Output Mode	Allows the user to set up outputs.
SERDES Output Setup	Allows the user to vary SERDES settings such as swing and emphasis.

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is divided into the following sections:

- Analog Devices SPI registers (Register 0x0000 to Register 0x000F)
- Clock/SYSREF/chip power-down pin control registers (Register 0x003F to Register 0x0201)
- Fast detect and signal monitor control registers (Register 0x0245 to Register 0x027A)
- DDC function registers (Register 0x0300 to Register 0x03CD)
- Digital outputs and test modes registers (Register 0x0550 to Register 0x05CB)
- Programmable filter control and coefficients registers (Register 0x0DF8 to Register 0x0F7F)
- VREF/analog input control registers (Register 0x18A6 to Register 0x1A4D)

Table 44 (see the Memory Map section) documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x0561, the output sample mode register, has a hexadecimal default value of 0x01, which means that Bit 0 = 1, and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on this function and others, see Table 44.

Open and Reserved Locations

All address and bit locations that are not included in Table 44 are not currently supported for this device. Write unused bits of a valid address location with 0s unless the default value is set otherwise. Writing to these locations is required only when part of an address location is unassigned (for example, Address 0x0561). If the entire address location is open (for example, Address 0x0013), do not write to this address location.

Default Values

After the AD9697 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table 44.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."
- X denotes a don't care bit.

SPI Soft Reset

After issuing a soft reset by programming 0x81 to Register 0x0000, the AD9697 requires 5 ms to recover. When programming the AD9697 for application setup, ensure that an adequate delay is programmed into the firmware after asserting the soft reset and before starting the device setup.

MEMORY MAP REGISTERS

All address locations that are not included in Table 44 are not currently supported for this device and must not be written.

Table 44. Memory Map Registers

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
Analog Devices SPI Registers							
0x0000	SPI Configuration A	7	Soft reset mirror (self clearing)		Whenever a soft reset is issued, the user must wait 5 ms before writing to any other register; this provides sufficient time for the boot loader to complete.	0x0	R/WC
				0	Do nothing.		
				1	Reset the SPI and registers (self clearing).		
		6	LSB first mirror	1	Least significant bit shifted first for all SPI operations.	0x0	R/W
				0	Most significant bit shifted first for all SPI operations.		
		5	Address ascension mirror	0	Multibyte SPI operations cause addresses to auto decrement.	0x0	R/W
				1	Multibyte SPI operations cause addresses to auto increment.		
		[4:3]	Reserved		Reserved.	0x0	R
		2	Address ascension	0	Multibyte SPI operations cause addresses to auto decrement.	0x0	R/W
				1	Multibyte SPI operations cause addresses to auto increment.		
		1	LSB first	1	Least significant bit shifted first for all SPI operations.	0x0	R/W
				0	Most significant bit shifted first for all SPI operations.		
		0	Soft reset (self clearing)		Whenever a soft reset is issued, the user must wait 5 ms before writing to any other register; this provides sufficient time for the boot loader to complete.	0x0	R/WC
				0	Do nothing.		
				1	Reset the SPI and registers (self clearing).		
0x0001	SPI Configuration B	[7:2]	Reserved		Reserved.	0x0	R
		1	Datapath soft reset (self clearing)	0	Normal operation.	0x0	R/WC
				1	Datapath soft reset (self clearing).		
		0	Reserved		Reserved.	0x0	R

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0002	Chip configuration (local)	[7:2]	Reserved		Reserved.	0x0	R
		[1:0]	Power mode		Power modes.	0x0	R/W
				00	Normal mode (power-up).		
				10	Standby mode. Digital datapath clocks disabled; JESD204B interface enabled.		
				11	Power-down mode. Digital datapath clocks disabled; digital datapath held in reset; JESD204B interface disabled.		
0x0003	Chip type	[7:0]	Chip type		Chip type.	0x3	R
				0x3	High speed ADC.		
0x0004	Chip ID LSB	[7:0]	Chip ID LSB [7:0]		Chip ID.		R
				0xDE	AD9697.		
0x0005	Chip ID MSB	[7:0]	Chip ID MSB [15:8]		Chip ID.	0x0	R
0x0006	Chip grade	[7:4]	Chip speed grade		Chip speed grade.	0x0	R
				0x00	1300 MSPS.		
		[3:0]	Reserved		Reserved.	DNC	R
0x000A	Scratch pad	[7:0]	Scratch pad		Chip scratch pad register. This register provides a consistent memory location for software debug.	0x0	R/W
0x000B	SPI revision	[7:0]	SPI revision		SPI revision register.	0x1	R
				0x01	Revision 1.0.		
				00000001	Revision 1.0.		
0x000C	Vendor ID LSB	[7:0]			Vendor ID [7:0].	0x56	R
0x000D	Vendor ID MSB	[7:0]			Vendor ID [15:8].	0x04	R
0x000F	Transfer	[7:1]	Reserved		Reserved.	0x0	R
		0	Chip transfer		Self clearing chip transfer bit. This bit is used to update the DDC phase increment and phase offset registers when the DDC phase update mode bit (Register 0x0300, Bit 7) = 1. This setting makes it possible to synchronously update the DDC mixer frequencies. It is also used to update the coefficients for the programmable filter (PFILT).	0x0	R/W
				0	Do nothing. This bit it is only cleared after the transfer completes.		
				1	Self clearing bit used to synchronize the transfer of data from master to slave registers.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
Clock/SYSREF±/Chip Power-Down Pin Control Registers							
0x003F	Chip power-down pin (local)	7	Local chip power-down pin disable		Function is determined by Register 0x0040, Bits[7:6].	0x0	R/W
				0	Power-down pin (PDWN/STBY) enabled (default).		
				1	Power-down pin (PDWN/STBY) disabled/ignored.		
		[6:0]	Reserved		Reserved.	0x0	R
0x0040	Chip Pin Control 1	[7:6]	Global chip power-down pin functionality		External power-down pin functionality. Assertion of the external power-down pin (PDWN/STBY) has higher priority than the power mode control bits (Register 0x0002, Bits[1:0]). The PDWN/STBY pin is only used when Register 0x0040, Bits[7:6] = 00 or 01.	0x0	R/W
				00	Power-down pin (default). Assertion of the external power-down pin (PDWN/STBY) causes the chip to enter full power-down mode.		
				01	Standby-pin. Assertion of the external power-down pin (PDWN/STBY) causes the chip to enter standby mode.		
				10	Pin disabled. Power-down pin (PDWN/STBY) is ignored.		
		[5:3]	GPIO2 pin functionality		GPIO2 pin functionality.	0x7	R/W
				110	Pin functionality determined by Register 0x0041, Bits[7:4].		
				111	Disabled. Configured as input with weak pull-down (default).		
		[2:0]	Chip FD/GPIO1 pin functionality		FD/GPIO1 pin functionality.	0x7	R/W
				000	Fast detect output.		
				001	JESD204B LMFC output.		
				110	Pin functionality determined by Register 0x0041, Bits[3:0].		
				111	Disabled. Configured as input with weak pull-down. (default)		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0041	Chip Pin Control 2	[7:4]	GPIO2 pin secondary functionality		GPIO2 pin secondary functionality. Only used when Register 0x0040, Bits[5:3] = 110.	0x0	R/W
				0000	Chip GPIO2 input (NCO channel selection).		
		[3:0]	Chip FD/GPIO1 pin secondary functionality		FD/GPIO1 pin secondary functionality. Only used when Register 0x0040, Bits[2:0] = 110.	0x0	R/W
				0000	Chip GPIO1 input (NCO channel selection).		
				0001	Chip transfer input.		
				1000	Master next trigger output (MNTO).		
				1001	Slave next trigger input (SNTI).		
0x0042	Chip Pin Control 3	[7:4]	Reserved	1111	Reserved	0xF	R
		[3:0]	Chip GPIO1 pin functionality		GPIO1 pin functionality.	0x0	R/W
				0000	Chip GPIO1 input (NCO channel selection).		
				1000	Master next trigger output (MNTO).		
				1001	Slave next trigger input (SNTI).		
				1111	Disabled (configured as an input with a weak pull down).		
0x0108	Clock divider control	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Input clock divider (CLK± pins)	00	Divide by 1.	0x0	R/W
				01	Divide by 2.		
				11	Divide by 4.		
0x0109	Clock divider phase (local)	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Clock divider phase offset	0000	0 input clock cycles delayed.	0x0	R/W
				0001	1/2 input clock cycles delayed (invert clock).		
				0010	1 input clock cycles delayed.		
				…	…		
				1110	7 input clock cycles delayed.		
				1111	7 1/2 input clock cycles delayed.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x010A	Clock divider and SYSREF± control	7	Clock divider autophase adjust enable		Clock divider autophase adjust enable. When enabled, Register 0x0129, Bits[3:0] contain the phase of the divider when SYSREF± occurred. The actual divider phase offset = Register 0x0129, Bits[3:0] + Register 0x0109, Bits[3:0].	0x0	R/W
				0	Clock divider phase is not changed by SYSREF± (disabled).		
				1	Clock divider phase is automatically adjusted by SYSREF± (enabled).		
		[6:4]	Reserved		Reserved.	0x0	R
		[3:2]	Clock divider negative skew window		Clock divider negative skew window (measured in 1/2 input device clocks). Number of 1/2 clock cycles before the input device clock by which captured SYSREF± transitions are ignored. Only used when Register 0x010A, Bit 7 = 1. Register 0x010A, Bits[3:2] + Register 0x010A, Bits[1:0] < Register 0x0108, Bits[2:0]; this allows some uncertainty in the sampling of SYSREF± without disturbing the input clock divider. Also, SYSREF± must be disabled (Register 0x0120, Bits[2:1] = 0x0) when changing this control field.	0x0	R/W
				0	No negative skew. SYSREF± must be captured accurately.		
				1	1/2 device clock of negative skew.		
				10	1 device clocks of negative skew.		
				11	1 1/2 device clocks of negative skew.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[1:0]	Clock divider positive skew window		Clock divider positive skew window (measured in 1/2 input device clocks). Number of clock cycles after the input device clock by which captured SYSREF± transitions are ignored. Only used when Register 0x010A, Bit 7 = 1. Register 0x010A, Bits[3:2] + Register 0x010A, Bits[1:0] < Register 0x0108, Bits[2:0]; this allows some uncertainty in the sampling of SYSREF± without disturbing the input clock divider. Also, SYSREF± must be disabled (Register 0x0120, Bits[2:1] = 0x0) when changing this control field.	0x0	R/W
				0	No positive skew. SYSREF± must be captured accurately.		
				1	1/2 device clock of positive skew.		
				10	1 device clocks of positive skew.		
				11	1 1/2 device clocks of positive skew.		
0x010B	Clock divider SYSREF status	[7:4]	Reserved		Reserved	0x0	R
		[3:0]	Clock divider SYSREF± offset		Clock divider phase status (measured in 1/2 clock cycles). Internal clock divider phase of the captured SYSREF± signal applied to the phase offset. Only used when Register 0x010A, Bit 7 = 1. When Register 0x010A, Bit 7 = 1, Register 0x010A, Bits[3:2] = 0, and Register 0x010A, Bits[1:0] = 0, clock divider SYSREF± offset = Register 0x0129, Bits[3:0].	0x0	R
0x0110	Clock delay control	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Clock delay mode select		Clock delay mode select. Used in conjunction with Register 0x0111 and Register 0x0112.	0x0	R/W
				000	No clock delay.		
				010	Fine delay. Only Delay Step 0 to Delay Step 16 are valid.		
				011	Fine delay (lowest jitter). Only Delay Step 0 to Delay Step 16 are valid.		
				100	Fine delay. All 192 delay steps valid.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
				110	Fine delay enabled (all 192 delay steps valid). Super fine delay enabled (all 128 delay steps valid).		
0x0111	Clock super fine delay (local)	[7:0]	Clock super fine delay adjust		Clock super fine delay adjust. This is an unsigned control to adjust the super fine sample clock delay in 0.25 ps steps. These bits are only used when Register 0x0110, Bits[2:0] = 010 or 110. 0x00 = 0 delay steps. … 0x08 = 8 delay steps. … 0x80 = 128 delay steps.	0x0	R/W
0x0112	Clock fine delay (local)	[7:0]	Set clock fine delay		Clock fine delay adjust. This is an unsigned control to adjust the fine sample clock skew in 1.725 ps steps. These bits are only used when Register 0x0110, Bits[2:0] = 0x2, 0x3, 0x4, or 0x6. 0x00 = 0 delay steps. … 0x08 = 8 delay steps. … 0xC0 = 192 delay steps. Minimum = 0. Maximum = 192. Increment = 1. Unit = delay steps.	0xC0	R/W
0x0113	Digital clock super fine delay	[7:0]	Digital clock super fine delay adjust		Digital clock super fine delay adjust. This is an unsigned control to adjust the super fine sample clock delay in 0.25ps steps. These bits are only used when Register 0x0110, Bits[2:0] = 010 or 110. 0x00 = 0 delay steps. … 0x08 = 8 delay steps. … 0x80 = 128 delay steps.	0x0	R/W

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0114	Digital clock fine delay	[7:0]	Set digital clock fine delay		Digital clock fine delay adjust. This is an unsigned control to adjust the fine sample clock skew in 1.725 ps steps. These bits are only used when Register 0x0110, Bits[2:0] = 0x2, 0x3, 0x4 or 0x6. 0x00 = 0 delay steps. … 0x08 = 8 delay steps. … 0xC0 = 192 delay steps. Minimum = 0. Maximum = 192. Increment = 1. Unit = delay steps.	0xC0	R/W
0x011A	Clock detection control	[7:5]	Reserved		Reserved.	0x0	R/W
		[4:3]	Clock detection threshold		Clock detection threshold.	0x1	R/W
				01	Threshold 1 for sample rate ≥ 300 MSPS.		
				11	Threshold 2 for sample rate <300 MSPS.		
		[2:0]	Reserved		Reserved	0x6	R/W
0x011B	Clock status	[7:1]	Reserved		Reserved.	0x0	R
		0	Input clock detect		Clock detection status.	0x0	R
				0	Input clock not detected.		
				1	Input clock detected/locked.		
0x011C	Clock Duty Cycle Stabilizer 1 (DCS1) control (local)	[7:2]	Reserved		Reserved	0x0	R/W
		1	DCS1 enable		Clock DCS1 enable.	0x1	R/W
				0	DCS1 bypassed.		
				1	DCS1 enabled.		
		0	DCS1 power-up		Clock DCS1 power-up.	0x1	R/W
				0	DCS1 powered down.		
				1	DCS1 powered up.		
0x011E	Clock Duty Cycle Stabilizer 2 (DCS2) control	[7:2]	Reserved		Reserved.	0x0	R/W
		1	DCS2 enable		Clock DCS2 enable.	0x1	R/W
				0	DCS2 bypassed.		
				1	DCS2 enabled.		
		0	DCS2 power-up		Clock DCS2 power-up.	0x1	R/W
				0	DCS2 powered down.		
				1	DCS2 powered up.		
0x0120	SYSREF± Control 1	7	Reserved		Reserved.	0x0	R
		6	SYSREF± flag reset	0	Normal flag operation.	0x0	R/W
				1	SYSREF± flags held in reset (setup/hold error flags cleared).		
		5	Reserved		Reserved.	0x0	R

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
		4	SYSREF± transition select	0	SYSREF± is valid on low to high transitions using the selected CLK± edge. When changing this setting, SYSREF± mode select must be set to disabled.	0x0	R/W
				1	SYSREF± is valid on high to low transitions using the selected CLK± edge. When changing this setting, SYSREF± mode select must be set to disabled.		
		3	CLK± edge select	0	Captured on rising edge of CLK± input.	0x0	R/W
				1	Captured on falling edge of CLK± input.		
		[2:1]	SYSREF± mode select	0	Disabled.	0x0	R/W
				1	Continuous.		
				10	N shot.		
				11	Next trigger mode.		
		0	Reserved		Reserved.	0x0	R
0x0121	SYSREF± Control 2	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	SYSREF± N shot ignore counter select	0000	Next SYSREF± only (do not ignore).	0x0	R/W
				0001	Ignore the first SYSREF± transition.		
				0010	Ignore the first two SYSREF± transitions.		
				0011	Ignore the first three SYSREF± transitions.		
				…			
				1110	Ignore the first 14 SYSREF± transitions.		
				1111	Ignore the first 15 SYSREF± transitions.		
0x0122	SYSREF± Control 3	[7:4]	Reserved		Reserved	0x0	R
		[3:2]	SYSREF± window negative		Negative skew window (measured in sample clocks). Number of clock cycles before the sample clock by which captured SYSREF± transitions are ignored.	0x0	R/W
				00	No negative skew. SYSREF± must be captured accurately.		
				01	One sample clock of negative skew.		
				10	Two sample clocks of negative skew.		
				11	Three sample clocks of negative skew.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[1:0]	SYSREF± window negative		Positive skew window (measured in sample clocks). Number of clock cycles before the sample clock by which captured SYSREF± transitions are ignored.	0x0	R/W
				00	No positive skew. SYSREF± must be captured accurately.		
				01	One sample clock of positive skew.		
				10	Two sample clocks of positive skew.		
				11	Three sample clocks of positive skew.		
0x0123	SYSREF± Control 4	7	Reserved		Reserved.	0x0	R
		[6:0]	SYSREF± timestamp delay		SYSREF± timestamp delay (in converter sample clock cycles). 0: 0 sample clock cycle delay. 1: 1 sample clock cycle delay. … 127: 127 sample clock cycle delay.	0x40	R/W
0x0128	SYSREF± Status 1	[7:4]	SYSREF± hold status		SYSREF± hold status.	0x0	R
		[3:0]	SYSREF± setup status		SYSREF± setup status.	0x0	R
0x0129	SYSREF± Status 2	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Clock divider phase when SYSREF± is captured		SYSREF± divider phase. These bits represent the phase of the divider when SYSREF± is captured. 0000 = in phase. 0001 = SYSREF± is ½ cycle delayed from clock. 0010 = SYSREF± is 1 cycle delayed from clock. 0011 = 1½ input clock cycles delayed. 0100 = 2 input clock cycles delayed. 0101 = 2½ input clock cycles delayed. … 1111 = 7½ input clock cycles delayed.	0x0	R
0x012A	SYSREF± Status 3	[7:0]	SYSREF± counter, Bits[7:0] increments when a SYSREF± is captured		SYSREF± count. Running counter that increments whenever a SYSREF± event is captured. Reset by Register 0x0120, Bit 6. Wraps around at 255. Only read these bits while Register 0x0120, Bits[2:1] are set to disabled.	0x0	R

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x01FF	Chip sync mode	[7:1]	Reserved		Reserved.	0x0	R
		0	Synchronization mode	0x0	JESD204B synchronization mode. The SYSREF± signal resets all internal clock dividers. Use this mode when synchronizing multiple chips as specified in the JESD204B standard. If the phase of any of the dividers must change, the JESD204B link goes down.	0x0	R/W
				0x1	Timestamp mode. The SYSREF± signal does not reset the internal clock dividers. In this mode, the JESD204B link and the signal monitor are not affected by the SYSREF± signal. The SYSREF± signal simply time stamps a sample as it passes through the ADC and is used as a control bit in the JESD204B output word.		
Chip Operating Mode Control Registers							
0x0200	Chip mode	[7:6]	Reserved		Reserved.	0x0	R/W
		5	Chip Q ignore		Chip real (I) only selection.	0x0	R/W
				0	Both real (I) and complex (Q) selected.		
				1	Only real (I) selected. Complex (Q) is ignored.		
		4	Reserved		Reserved.	0x0	R
		[3:0]	Chip application mode	0000	Full bandwidth mode (default).	0x0	R/W
				0001	One DDC mode (DDC 0).		
				0010	Two DDC mode (DDC 0 and DDC 1 only).		
				0011	Four DDC mode (DDC 0, DDC 1, DDC 2, and DDC 3).		
0x0201	Chip decimation ratio	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Chip decimation ratio		Chip decimation ratio.	0x0	R/W
				0000	Full sample rate (decimate by 1, DDCs are bypassed).		
				0001	Decimate by 2.		
				1000	Decimate by 3.		
				0010	Decimate by 4.		
				0101	Decimate by 5.		
				1001	Decimate by 6.		
				0011	Decimate by 8.		
				0110	Decimate by 10.		
				1010	Decimate by 12.		
				0111	Decimate by 15.		
				0100	Decimate by 16.		
				1101	Decimate by 20.		
				1011	Decimate by 24.		
				1110	Decimate by 30.		
				1111	Decimate by 40.		
				1100	Decimate by 48.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
Fast Detect and Signal Monitor Control Registers							
0x0245	Fast detect control (local)	[7:4]	Reserved		Reserved.	0x0	R
		3	Force FD pin	0 1	Normal operation of fast detect pin. Force a value on fast detect pin (see Bit 2 in this register).	0x0	R/W
		2	Force value of FD pin		The fast detect output pin for this channel is set to this value when the output is forced.	0x0	R/W
		1	Reserved		Reserved.	0x0	R
		0	Enable fast detect output	0 1	Fast detect disabled. Fast detect enabled.	0x0	R/W
0x0247	Fast detect upper LSB (local)	[7:0]	Fast detect upper threshold		LSBs of fast detect upper threshold. Eight LSBs of the programmable 13-bit upper threshold compared to the fine ADC magnitude	0x0	R/W
0x0248	Fast detect upper MSB (local)	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Fast detect upper threshold		LSBs of fast detect upper threshold. Eight LSBs of the programmable 13-bit upper threshold compared to the fine ADC magnitude.	0x0	R/W
0x0249	Fast detect low LSB (local)	[7:0]	Fast detect lower threshold		LSBs of the fast detect lower threshold. Eight LSBs of the programmable 13-bit lower threshold compared to the fine ADC magnitude.	0x0	R/W
0x024A	Fast detect low MSB (local)	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Fast detect lower threshold		LSBs of fast detect lower threshold. Eight LSBs of the programmable 13-bit lower threshold compared to the fine ADC magnitude.	0x0	R/W
0x024B	Fast detect dwell LSB (local)	[7:0]	Fast detect dwell time		LSBs of fast detect dwell time counter target. This is a load value for a 16-bit counter that determines how long the ADC data must remain below the lower threshold before the FD pin is reset to 0.	0x0	R/W
0x024C	FAST detect dwell MSB (local)	[7:0]	Fast detect dwell time		LSBs of fast detect dwell time counter target. This is a load value for a 16-bit counter that determines how long the ADC data must remain below the lower threshold before the FD pin is reset to 0.	0x0	R/W

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x026F	Signal monitor sync control	[7:2]	Reserved		Reserved.	0x0	R
		1	Signal monitor next synchronization mode		Signal monitor next synchronization mode.	0x0	R/W
				0	Continuous mode.		
				1	Next synchronization mode. Only the next valid edge of SYSREF± pin synchronizes the signal monitor block. Subsequent edges of the SYSREF± pin are ignored. After the next SYSREF± is found, Register 0x026F, Bit 0 is cleared. The SYSREF± pin must be an integer multiple of the signal monitor period for this function to operate correctly in continuous mode.		
		0	Signal monitor synchronization mode		Signal monitor synchronization enable.	0x0	R/W
				0	Synchronization disabled.		
				1	If Register 0x026F, Bit 1 = 1, only the next valid edge of the SYSREF± pin is used to synchronize the signal monitor block. Subsequent edges of the SYSREF± pin are ignored. After the next SYSREF± is received, this bit is cleared. The SYSREF± input pin must be enabled to synchronize the signal monitor blocks.		
0x0270	Signal monitor control (local)	[7:2]	Reserved		Reserved.	0x0	R
		1	Peak detector	0	Peak detector disabled.	0x0	R/W
				1	Peak detector enabled.		
		0	Reserved		Reserved.	0x0	R
0x0271	Signal Monitor Period 0 (local)	[7:0]	Signal monitor period [7:0]		This 24-bit value sets the number of output clock cycles over which the signal monitor performs its operation. Only even values are supported.	0x80	R/W
0x0272	Signal Monitor Period 1 (local)	[7:0]	Signal monitor period [15:8]			0x0	R/W
0x0273	Signal Monitor Period 2 (local)	[7:0]	Signal monitor period [23:16]			0x0	R/W
0x0274	Signal monitor status control (local)	[7:5]	Reserved		Reserved.	0x0	R
		4	Result update	1	Update signal monitor status, Register 0x0275 to Register 0x0278. Self clearing.	0x0	R/WC
		3	Reserved		Reserved.	0x0	R
		[2:0]	Result selection	001	Peak detector placed on status readback signals.	0x1	R/W

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0275	Signal Monitor Status 0 (local)	[7:0]	Signal monitor result [7:0]		Signal monitor status result. This 20-bit value contains the status result calculated by the signal monitor block.	0x0	R
0x0276	Signal Monitor Status 1 (local)	[7:0]	Signal monitor result [15:8]		Signal monitor status result.	0x0	R
0x0277	Signal Monitor Status 2 (local)	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Signal monitor result [19:16]		Signal monitor status result.	0x0	R
0x0278	Signal monitor status frame counter (local)	[7:0]	Period count result		Signal monitor frame counter status bits. The frame counter increments whenever the period counter expires.	0x0	R
0x0279	Signal monitor serial framer control (local)	[7:2]	Reserved		Reserved.	0x0	R
		[1:0]	Signal monitor SPORT over JESD204B enable	00 11	Disabled. Enabled.	0x0	R/W
0x027A	SPORT over JESD204B input selection (local)	[7:6]	Reserved		Reserved.	0x0	R
		1	SPORT over JESD204B input selection		Signal monitor serial framer input selection. When each individual bit is a 1, the corresponding signal statistics information is sent within the frame.	0x1	R/W
				0 1	Disabled. Peak detector data inserted in serial frame.		
		0	Reserved		Reserved	0x0	R
DDC Function Registers (See the Digital Downconverter (DDC) Section)							
0x0300	DDC sync control	7	DDC FTW/POW/ MAW/MBW update mode		Select DDC FTW/POW/ MAW/MBW update mode.	0x0	R/W
				0 1	Instantaneous/continuous update. The FTW/POW/ MAW/MBW values are updated immediately. The FTW/POW/MAW/ MBW values are updated synchronously when the chip transfer bit (Register 0x000F, Bit 0) is set.		
		[6:5]	Reserved		Reserved.	0x0	R
		4	DDC NCO soft reset		This bit can be used to synchronize all the NCOs inside the DDC blocks.	0x0	R/W
				0 1	Normal operation. DDC held in reset.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[3:2]	Reserved		Reserved.	0x0	R
		1	DDC next sync	0	Continuous mode. The SYSREF± frequency must be an integer multiple of the NCO frequency for this function to operate correctly in continuous mode.	0x0	R/W
				1	Only the next valid edge of the SYSREF± pin is used to synchronize the NCO in the DDC block. Subsequent edges of the SYSREF± pin are ignored. After the next SYSREF is found, the DDC synchronization enable bit (Register 0x0300, Bit 0) is cleared.		
		0	DDC synchronization mode		The SYSREF± input pin must be enabled to synchronize the DDCs.	0x0	R/W
				0	Synchronization disabled.		
				1	If the DDC next sync bit (Register 0x0300, Bit 1) = 1, only the next valid edge of the SYSREF± pin is used to synchronize the NCO in the DDC block. Subsequent edges of the SYSREF± pin are ignored. After the next SYSREF± is received, this bit is cleared.		
0x0310	DDC 0 control	7	Reserved	0	Reserved	0x0	R/W
		6	DDC 0 gain select		Gain can be used to compensate for the 6 dB loss associated with mixing an input signal down to baseband and filtering out its negative component.	0x0	R/W
				0	0 dB gain.		
				1	6 dB gain (multiply by 2).		
		[5:4]	DDC 0 intermediate frequency (IF) mode	00	Variable IF mode.	0x0	R/W
				01	0 Hz IF mode.		
				10	$f_S/4$ Hz IF mode.		
				11	Test mode.		
		3	DDC 0 complex to real enable	0	Complex (I and Q) outputs contain valid data.	0x0	R/W
				1	Real (I) output only. Complex to real enabled. Uses extra f_S /4 mixing to convert to real.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[2:0]	DDC 0 decimation rate select		Decimation filter selection.	0x0	R/W
				000	HB1 + HB2 filter selection: decimate by 2 (complex to real enabled), or decimate by 4 (complex to real disabled).		
				001	HB1 + HB2 + HB3 filter selection: decimate by 4 (complex to real enabled), or decimate by 8 (complex to real disabled).		
				010	HB1 + HB2 + HB3 + HB4 filter selection: decimate by 8 (complex to real enabled), or decimate by 16 (complex to real disabled).		
				011	HB1 filter selection: decimate by 1 (complex to real enabled), or decimate by 2 (complex to real disabled).		
				100	HB1 + TB2 filter selection: decimate by 3 (complex to real enabled), or decimate by 6 (complex to real disabled).		
				101	HB1 + HB2 + TB2 filter selection: decimate by 6 (complex to real enabled), or decimate by 12 (complex to real disabled).		
				110	HB1 + HB2 + HB3 + TB2 filter selection: decimate by 12 (complex to real enabled), or decimate by 24 (complex to real disabled).		
				111	Decimation determined by Register 0x0311, Bits[7:4].		
0x0311	DDC 0 input select	[7:4]	DDC 0 decimation rate select		Only valid when Register 0x0310, Bits[2:0] = 3'b111.	0x0	R/W
				0	TB2 + HB4 + HB3 + HB2 + HB1 filter selection: decimate by 48 (complex to real disabled), or decimate by 24 (complex to real enabled).		
				10	FB2 + HB1 filter selection: decimate by 10 (complex to real disabled) or decimate by 5 (complex to real enabled).		
				11	FB2 + HB2 + HB1 filter selection: decimate by 20 (complex to real disabled), or decimate by 10 (complex to real enabled).		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
				100	FB2 + HB3 + HB2 + HB1 filter selection: decimate by 40 (complex to real disabled), or decimate by 20 (complex to real enabled).		
				111	TB1 filter selection: decimate by 3 (decimate by 1.5 not supported).		
				1000	FB2 + TB1 filter selection: decimate by 15 (decimate by 7.5 not supported).		
				1001	HB2 + FB2 + TB1 filter selection: decimate by 30 (decimate by 15 not supported).		
		[3:0]	Reserved		Reserved.	0x0	R
0x0314	DDC 0 NCO control	[7:4]	DDC 0 NCO channel select mode		For edge control, the internal counter wraps after the Register 0x0314, Bits[3:0] value is reached.	0x0	R/W
				0	Use Register 0x0314, Bits[3:0].		
				1	2'b0, GPIO2 and GPIO1.		
				1000	Increment internal counter on rising edge of the GPIO1 pin.		
				1010	Increment internal counter on rising edge of the GPIO2 pin.		
		[3:0]	DDC 0 NCO register map channel select		NCO channel select register map control.	0x0	R/W
				0	Select NCO Channel 0.		
				1	Select NCO Channel 1.		
				10	Select NCO Channel 2.		
				11	Select NCO Channel 3.		
				100	Select NCO Channel 4.		
				101	Select NCO Channel 5.		
				110	Select NCO Channel 6.		
				111	Select NCO Channel 7.		
				1000	Select NCO Channel 8.		
				1001	Select NCO Channel 9.		
				1010	Select NCO Channel 10.		
				1011	Select NCO Channel 11.		
				1100	Select NCO Channel 12.		
				1101	Select NCO Channel 13.		
				1110	Select NCO Channel 14.		
				1111	Select NCO Channel 15.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0315	DDC 0 phase control	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DDC 0 phase update index		Indexes the NCO channel whose phase and offset gets updated. The update method is based on the DDC phase update mode, which may be continuous or require chip transfer.	0x0	R/W
				0000	Update NCO Channel 0.		
				0001	Update NCO Channel 1.		
				0010	Update NCO Channel 2.		
				0011	Update NCO Channel 3.		
0x0316	DDC 0 Phase Increment 0	[7:0]	DDC 0 phase increment [7:0]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x0317	DDC 0 Phase Increment 1	[7:0]	DDC 0 phase increment [15:8]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x0318	DDC 0 Phase Increment 2	[7:0]	DDC 0 phase increment [23:16]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x0319	DDC 0 Phase Increment 3	[7:0]	DDC 0 phase increment [31:24]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x031A	DDC 0 Phase Increment 4	[7:0]	DDC 0 phase increment [39:32]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x031B	DDC 0 Phase Increment 5	[7:0]	DDC 0 phase increment [47:40]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x031D	DDC 0 Phase Offset 0	[7:0]	DDC 0 phase offset [7:0]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x031E	DDC 0 Phase Offset 1	[7:0]	DDC 0 phase offset [15:8]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x031F	DDC 0 Phase Offset 2	[7:0]	DDC 0 phase offset [23:16]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x0320	DDC 0 Phase Offset 3	[7:0]	DDC 0 phase offset [31:24]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x0321	DDC 0 Phase Offset 4	[7:0]	DDC 0 phase offset [39:32]		Twos complement phase offset value for the NCO (POW).	0x0	R/W

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0322	DDC 0 Phase Offset 5	[7:0]	DDC 0 phase offset [47:40]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x0327	DDC 0 test enable	[7:2]	Reserved		Reserved.	0x0	R
		1	Reserved		Reserved.	0x0	R
		0	DDC 0 I output test mode enable		I samples always use the Test Mode A block. The test mode is selected using the channel dependent bits (Register 0x0550, Bits[3:0]).	0x0	R/W
				0	Test mode disabled.		
				1	Test mode enabled.		
0x0330	DDC 1 control	7	Reserved	0	Reserved.	0x0	R/W
		6	DDC 1 gain select		Gain can be used to compensate for the 6 dB loss associated with mixing an input signal down to baseband and filtering out its negative component.	0x0	R/W
				0	0 dB gain.		
				1	6 dB gain (multiply by 2).		
		[5:4]	DDC 1 intermediate frequency (IF) mode	00	Variable IF mode.	0x0	R/W
				01	0 Hz IF mode.		
				10	$f_S/4$ Hz IF mode.		
				11	Test mode.		
		3	DDC 1 Complex to real enable	0	Complex (I and Q) outputs contain valid data.	0x0	R/W
				1	Real (I) output only. Complex to real enabled. Uses extra $f_S/4$ mixing to convert to real.		
		[2:0]	DDC 1 decimation rate select		Decimation filter selection.	0x0	R/W
				000	HB1 + HB2 filter selection: decimate by 2 (complex to real enabled), or decimate by 4 (complex to real disabled).		
				001	HB1 + HB2 + HB3 filter selection: decimate by 4 (complex to real enabled), or decimate by 8 (complex to real disabled).		
				010	HB1 + HB2 + HB3 + HB4 filter selection: decimate by 8 (complex to real enabled), or decimate by 16 (complex to real disabled).		
				011	HB1 filter selection: decimate by 1 (complex to real enabled), or decimate by 2 (complex to real disabled).		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
				100	HB1 + TB2 filter selection: decimate by 3 (complex to real enabled), or decimate by 6 (complex to real disabled).		
				101	HB1 + HB2 + TB2 filter selection: decimate by 6 (complex to real enabled), or decimate by 12 (complex to real disabled).		
				110	HB1 + HB2 + HB3 + TB2 filter selection: decimate by 12 (complex to real enabled), or decimate by 24 (complex to real disabled).		
				111	Decimation determined by Register 0x0331, Bits[7:4].		
0x0331	DDC 1 input select	[7:4]	DDC 1 decimation rate select		Only valid when Register 0x0310, Bits[2:0] = 3'b111.	0x0	R/W
				0	TB2 + HB4 + HB3 + HB2 + HB1 filter selection: decimate by 48 (complex to real disabled), or decimate by 24 (complex to real enabled).		
				10	FB2 + HB1 filter selection: decimate by 10 (complex to real disabled), or decimate by 5 (complex to real enabled).		
				11	FB2 + HB2 + HB1 filter selection: decimate by 20 (complex to real disabled), or decimate by 10 (complex to real enabled).		
				100	FB2 + HB3 + HB2 + HB1 filter selection: decimate by 40 (complex to real disabled), or decimate by 20 (complex to real enabled).		
				111	TB1 filter selection: decimate by 3 (decimate by 1.5 not supported).		
				1000	FB2 + TB1 filter selection: decimate by 15 (decimate by 7.5 not supported).		
				1001	HB2 + FB2 + TB1 filter select: decimate by 30 (decimate by 15 not supported).		
		[3:0]	Reserved		Reserved.	0x0	R

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0334	DDC 1 NCO control	[7:4]	DDC 1 NCO channel select mode		For edge control, the internal counter wraps after the Register 0x0334, Bits[3:0] value is reached.	0x0	R/W
				0	Use Register 0x0314, Bits[3:0].		
				1	2'b0, GPIO2, and GPIO1.		
				1000	Increment internal counter when rising edge of the GPIO1 pin.		
				1010	Increment internal counter when rising edge of the GPIO2 pin.		
		[3:0]	DDC 1 NCO register map channel select		NCO channel select register map control.	0x0	R/W
				0	Select NCO Channel 0.		
				1	Select NCO Channel 1.		
				10	Select NCO Channel 2.		
				11	Select NCO Channel 3.		
				100	Select NCO Channel 4.		
				101	Select NCO Channel 5.		
				110	Select NCO Channel 6.		
				111	Select NCO Channel 7.		
				1000	Select NCO Channel 8.		
				1001	Select NCO Channel 9.		
				1010	Select NCO Channel 10.		
				1011	Select NCO Channel 11.		
				1100	Select NCO Channel 12.		
				1101	Select NCO Channel 13.		
				1110	Select NCO Channel 14.		
				1111	Select NCO Channel 15.		
0x0335	DDC 1 phase control	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DDC 1 phase update index		Indexes the NCO channel whose phase and offset gets updated. The update method is based on the DDC phase update mode, which may be continuous or require chip transfer.	0x0	R/W
				0000	Update NCO Channel 0.		
				0001	Update NCO Channel 1.		
				0010	Update NCO Channel 2.		
				0011	Update NCO Channel 3.		
0x0336	DDC 1 Phase Increment 0	[7:0]	DDC 1 phase increment [7:0]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x0337	DDC 1 Phase Increment 1	[7:0]	DDC 1 phase increment [15:8]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0338	DDC 1 Phase Increment 2	[7:0]	DDC 1 phase increment [23:16]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x0339	DDC 1 Phase Increment 3	[7:0]	DDC 1 phase increment [31:24]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x033A	DDC 1 Phase Increment 4	[7:0]	DDC 1 phase increment [39:32]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x033B	DDC 1 Phase Increment 5	[7:0]	DDC 1 phase increment [47:40]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x033D	DDC 1 Phase Offset 0	[7:0]	DDC 1 phase offset [7:0]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x033E	DDC 1 Phase Offset 1	[7:0]	DDC 1 phase offset [15:8]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x033F	DDC 1 Phase Offset 2	[7:0]	DDC 1 phase offset [23:16]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x0340	DDC 1 Phase Offset 3	[7:0]	DDC 1 phase offset [31:24]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x0341	DDC 1 Phase Offset 4	[7:0]	DDC 1 phase offset [39:32]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x0342	DDC 1 Phase Offset 5	[7:0]	DDC 1 phase offset [47:40]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x0347	DDC 1 test enable	[7:2]	Reserved		Reserved.	0x0	R
		1	Reserved		Reserved.	0x0	R
		0	DDC 1 I output test mode enable		I samples always use the Test Mode A block. The test mode is selected using the channel dependent bits, Register 0x0550, Bits[3:0].	0x0	R/W
				0	Test mode disabled.		
				1	Test mode enabled.		
0x0350	DDC 2 control	7	Reserved	0	Reserved.	0x0	R/W
		6	DDC 2 gain select		Gain can be used to compensate for the 6 dB loss associated with mixing an input signal down to baseband and filtering out its negative component.	0x0	R/W
				0	0 dB gain.		
				1	6 dB gain (multiply by 2).		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[5:4]	DDC 2 intermediate frequency (IF) mode	00	Variable IF mode.	0x0	R/W
				01	0 Hz IF mode.		
				10	$f_S/4$ Hz IF mode.		
				11	Test mode.		
		3	DDC 2 complex to real enable	0	Complex (I and Q) outputs contain valid data.	0x0	R/W
				1	Real (I) output only. Complex to real enabled. Uses extra $f_S/4$ mixing to convert to real.		
		[2:0]	DDC 2 decimation rate select		Decimation filter selection.	0x0	R/W
				000	HB1 + HB2 filter selection: decimate by 2 (complex to real enabled), or decimate by 4 (complex to real disabled).		
				001	HB1 + HB2 + HB3 filter selection: decimate by 4 (complex to real enabled), or decimate by 8 (complex to real disabled).		
				010	HB1 + HB2 + HB3 + HB4 filter selection: decimate by 8 (complex to real enabled), or decimate by 16 (complex to real disabled).		
				011	HB1 filter selection: decimate by 1 (complex to real enabled), or decimate by 2 (complex to real disabled).		
				100	HB1 + TB2 filter selection: decimate by 3 (complex to real enabled), or decimate by 6 (complex to real disabled).		
				101	HB1 + HB2 + TB2 filter selection: decimate by 6 (complex to real enabled), or decimate by 12 (complex to real disabled).		
				110	HB1 + HB2 + HB3 + TB2 filter selection: decimate by 12 (complex to real enabled), or decimate by 24 (complex to real disabled).		
				111	Decimation determined by Register 0x0351, Bits[7:4].		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0351	DDC 2 input select	[7:4]	DDC 2 decimation rate select		Only valid when Register 0x0310, Bits[2:0] = 3'b111.	0x0	R/W
				0	TB2 + HB4 + HB3 + HB2 + HB1 filter selection: decimate by 48 (complex to real disabled), or decimate by 24 (complex to real enabled).		
				10	FB2 + HB1 filter selection: decimate by 10 (complex to real disabled), or decimate by 5 (complex to real enabled).		
				11	FB2 + HB2 + HB1 filter selection: decimate by 20 (complex to real disabled), or decimate by 10 (complex to real enabled).		
				100	FB2 + HB3 + HB2 + HB1 filter selection: decimate by 40 (complex to real disabled), or decimate by 20 (complex to real enabled).		
		[3:0]	Reserved		Reserved.	0x0	R
0x0354	DDC 2 NCO control	[7:4]	DDC 2 NCO channel select mode		For edge control, the internal counter wraps after the Register 0x0354, Bits[3:0] value is reached.	0x0	R/W
				0	Use Register 0x0314, Bits[3:0].		
				1	2'b0, GPIO2, and GPIO1.		
				1000	Increment internal counter when rising edge of the GPIO1 pin.		
				1010	Increment internal counter when rising edge of the GPIO2 pin.		
		[3:0]	DDC 2 NCO register map channel select		NCO channel select register map control.	0x0	R/W
				0	Select NCO Channel 0.		
				1	Select NCO Channel 1.		
				10	Select NCO Channel 2.		
				11	Select NCO Channel 3.		
				100	Select NCO Channel 4.		
				101	Select NCO Channel 5.		
				110	Select NCO Channel 6.		
				111	Select NCO Channel 7.		
				1000	Select NCO Channel 8.		
				1001	Select NCO Channel 9.		
				1010	Select NCO Channel 10.		
				1011	Select NCO Channel 11.		
				1100	Select NCO Channel 12.		
				1101	Select NCO Channel 13.		
				1110	Select NCO Channel 14.		
				1111	Select NCO Channel 15.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0355	DDC 2 phase control	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DDC 2 phase update index		Indexes the NCO channel whose phase and offset gets updated. The update method is based on the DDC phase update mode, which may be continuous or require chip transfer.	0x0	R/W
				0000	Update NCO Channel 0.		
				0001	Update NCO Channel 1.		
				0010	Update NCO Channel 2.		
				0011	Update NCO Channel 3.		
0x0356	DDC 2 Phase Increment 0	[7:0]	DDC 2 phase increment [7:0]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x0357	DDC 2 Phase Increment 1	[7:0]	DDC 2 phase increment [15:8]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x0358	DDC 2 Phase Increment 2	[7:0]	DDC 2 phase increment [23:16]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x0359	DDC 2 Phase Increment 3	[7:0]	DDC 2 phase increment [31:24]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x035A	DDC 2 Phase Increment 4	[7:0]	DDC 2 phase increment [39:32]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x035B	DDC 2 Phase Increment 5	[7:0]	DDC 2 phase increment [47:40]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x035D	DDC 2 Phase Offset 0	[7:0]	DDC 2 phase offset [7:0]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x035E	DDC 2 Phase Offset 1	[7:0]	DDC 2 phase offset [15:8]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x035F	DDC 2 Phase Offset 2	[7:0]	DDC 2 phase offset [23:16]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x0360	DDC 2 Phase Offset 3	[7:0]	DDC 2 phase offset [31:24]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x0361	DDC 2 Phase Offset 4	[7:0]	DDC 2 phase offset [39:32]		Twos complement phase offset value for the NCO (POW).	0x0	R/W

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0362	DDC 2 Phase Offset 5	[7:0]	DDC 2 phase offset [47:40]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x0367	DDC 2 test enable	[7:2]	Reserved		Reserved.	0x0	R
		1	Reserved		Reserved.	0x0	R
		0	DDC 2 I output test mode enable		I samples always use the Test Mode A block. The test mode is selected using the channel dependent bits, Register 0x0550, Bits[3:0].	0x0	R/W
				0	Test mode disabled.		
				1	Test mode enabled.		
0x0370	DDC 3 control	7	Reserved	0	Reserved.	0x0	R/W
				1	Complex mixer (I and Q must be from separate, real and imaginary quadrature ADC receive channels; analog demodulator).		
		6	DDC 3 gain select		Gain can be used to compensate for the 6 dB loss associated with mixing an input signal down to baseband and filtering out its negative component.	0x0	R/W
				0	0 dB gain.		
				1	6 dB gain (multiply by 2).		
		[5:4]	DDC 3 intermediate frequency (IF) mode	00	Variable IF mode.	0x0	R/W
				01	0 Hz IF mode.		
				10	$f_S/4$ Hz IF mode.		
				11	Test mode.		
		3	DDC 3 complex to real enable	0	Complex (I and Q) outputs contain valid data.	0x0	R/W
				1	Real (I) output only. Complex to real enabled. Uses extra $f_S/4$ mixing to convert to real.		
		[2:0]	DDC 3 decimation rate select		Decimation filter selection.	0x0	R/W
				000	HB1 + HB2 filter selection: decimate by 2 (complex to real enabled), or decimate by 4 (complex to real disabled).		
				001	HB1 + HB2 + HB3 filter selection: decimate by 4 (complex to real enabled), or decimate by 8 (complex to real disabled).		
				010	HB1 + HB2 + HB3 + HB4 filter selection: decimate by 8 (complex to real enabled), or decimate by 16 (complex to real disabled).		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
				011	HB1 filter selection: decimate by 1 (complex to real enabled), or decimate by 2 (complex to real disabled).		
				100	HB1 + TB2 filter selection: decimate by 3 (complex to real enabled), or decimate by 6 (complex to real disabled).		
				101	HB1 + HB2 + TB2 filter selection: decimate by 6 (complex to real enabled), or decimate by 12 (complex to real disabled).		
				110	HB1 + HB2 + HB3 + TB2 filter selection: decimate by 12 (complex to real enabled), or decimate by 24 (complex to real disabled).		
				111	Decimation determined by Register 0x0371, Bits[7:4].		
0x0371	DDC 3 input select	[7:4]	DDC 3 decimation rate select		Only valid when Register 0x0310, Bits[2:0] = 3'b111.	0x0	R/W
				0	TB2 + HB4 + HB3 + HB2 + HB1 filter selection: decimate by 48 (complex to real disabled), or decimate by 24 (complex to real enabled).		
				10	FB2 + HB1 filter selection: decimate by 10 (complex to real disabled), or decimate by 5 (complex to real enabled)		
				11	FB2 + HB2 + HB1 filter selection: decimate by 20 (complex to real disabled), or decimate by 10 (complex to real enabled)		
				100	FB2 + HB3 + HB2 + HB1 filter selection: decimate by 40 (complex to real disabled), or decimate by 20 (complex to real enabled)		
		[3:0]	Reserved		Reserved.	0x0	R

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0374	DDC 3 NCO control	[7:4]	DDC 3 NCO channel select mode		For edge control, the internal counter wraps after the Register 0x0374, Bits[3:0] value is reached.	0x0	R/W
				0	Use Register 0x0314, Bits[3:0].		
				1	2'b0, GPIO2, GPIO 1.		
				1000	Increment internal counter when rising edge of the GPIO1 pin.		
				1010	Increment internal counter when rising edge of the GPIO2 pin.		
		[3:0]	DDC 3 NCO register map channel select		NCO channel select register map control.	0x0	R/W
				0	Select NCO Channel 0.		
				1	Select NCO Channel 1.		
				10	Select NCO Channel 2.		
				11	Select NCO Channel 3.		
				100	Select NCO Channel 4.		
				101	Select NCO Channel 5.		
				110	Select NCO Channel 6.		
				111	Select NCO Channel 7.		
				1000	Select NCO Channel 8.		
				1001	Select NCO Channel 9.		
				1010	Select NCO Channel 10.		
				1011	Select NCO Channel 11.		
				1100	Select NCO Channel 12.		
				1101	Select NCO Channel 13.		
				1110	Select NCO Channel 14.		
				1111	Select NCO Channel 15.		
0x0375	DDC 3 phase control	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DDC 3 phase update index		Indexes the NCO channel whose phase and offset gets updated. The update method is based on the DDC phase update mode, which may be continuous or require chip transfer.	0x0	R/W
				0000	Update NCO Channel 0.		
				0001	Update NCO Channel 1.		
				0010	Update NCO Channel 2.		
				0011	Update NCO Channel 3.		
0x0376	DDC 3 Phase Increment 0	[7:0]	DDC 3 phase increment [7:0]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x0377	DDC 3 Phase Increment 1	[7:0]	DDC 3 phase increment [15:8]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0378	DDC 3 Phase Increment 2	[7:0]	DDC 3 phase increment [23:16]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x0379	DDC 3 Phase Increment 3	[7:0]	DDC 3 phase increment [31:24]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x037A	DDC 3 Phase Increment 4	[7:0]	DDC 3 phase increment [39:32]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x037B	DDC 3 Phase Increment 5	[7:0]	DDC 3 phase increment [47:40]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x037D	DDC 3 Phase Offset 0	[7:0]	DDC 3 phase offset [7:0]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x037E	DDC 3 Phase Offset 1	[7:0]	DDC 3 phase offset [15:8]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x037F	DDC 3 Phase Offset 2	[7:0]	DDC 3 phase offset [23:16]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x0380	DDC 3 Phase Offset 3	[7:0]	DDC 3 phase offset [31:24]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x0381	DDC 3 Phase Offset 4	[7:0]	DDC 3 phase offset [39:32]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x0382	DDC 3 Phase Offset 5	[7:0]	DDC 3 phase offset [47:40]		Twos complement phase offset value for the NCO (POW).	0x0	R/W
0x0387	DDC 3 test enable	[7:2]	Reserved		Reserved.	0x0	R
		1	Reserved		Reserved.	0x0	R
		0	DDC 3 I output test mode enable		I samples always use the Test Mode A block. The test mode is selected using the channel dependent bits, Register 0x0550, Bits[3:0].	0x0	R/W
				0	Test mode disabled.		
				1	Test mode enabled.		
0x0390	DDC 0 Phase Increment Fractional A0	[7:0]	DDC 0 Phase Increment Fractional A [7:0]		Numerator correction term for the modulus phase accumulator (MAW).	0x0	R/W
0x0391	DDC 0 Phase Increment Fractional A1	[7:0]	DDC 0 Phase Increment Fractional A [15:8]		Numerator correction term for the MAW.	0x0	R/W
0x0392	DDC 0 Phase Increment Fractional A2	[7:0]	DDC 0 Phase Increment Fractional A [23:16]		Numerator correction term for the MAW.	0x0	R/W

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0393	DDC 0 Phase Increment Fractional A3	[7:0]	DDC 0 Phase Increment Fractional A [31:24]		Numerator correction term for the MAW.	0x0	R/W
0x0394	DDC 0 Phase Increment Fractional A4	[7:0]	DDC 0 Phase Increment Fractional A [39:32]		Numerator correction term for the MAW.	0x0	R/W
0x0395	DDC 0 Phase Increment Fractional A5	[7:0]	DDC 0 Phase Increment Fractional A [47:40]		Numerator correction term for the MAW.	0x0	R/W
0x0398	DDC 0 Phase Increment Fractional B0	[7:0]	DDC 0 Phase Increment Fractional B [7:0]		Denominator correction term for the modulus phase accumulator (MBW).	0x0	R/W
0x0399	DDC 0 Phase Increment Fractional B1	[7:0]	DDC 0 Phase Increment Fractional B [15:8]		Denominator correction term for the MBW.	0x0	R/W
0x039A	DDC 0 Phase Increment Fractional B2	[7:0]	DDC 0 Phase Increment Fractional B [23:16]		Denominator correction term for the MBW.	0x0	R/W
0x039B	DDC 0 Phase Increment Fractional B3	[7:0]	DDC 0 Phase Increment Fractional B [31:24]		Denominator correction term for the MBW.	0x0	R/W
0x039C	DDC 0 Phase Increment Fractional B4	[7:0]	DDC 0 Phase Increment Fractional B [39:32]		Denominator correction term for the MBW.	0x0	R/W
0x039D	DDC 0 Phase Increment Fractional B5	[7:0]	DDC 0 Phase Increment Fractional B [47:40]		Denominator correction term for the MBW.	0x0	R/W
0x03A0	DDC 1 Phase Increment Fractional A0	[7:0]	DDC 1 Phase Increment Fractional A [7:0]		Numerator correction term for the modulus phase accumulator (MAW).	0x0	R/W
0x03A1	DDC 1 Phase Increment Fractional A1	[7:0]	DDC 1 Phase Increment Fractional A [15:8]		Numerator correction term for the MAW.	0x0	R/W
0x03A2	DDC 1 Phase Increment Fractional A2	[7:0]	DDC 1 Phase Increment Fractional A [23:16]		Numerator correction term for the MAW.	0x0	R/W
0x03A3	DDC 1 Phase Increment Fractional A3	[7:0]	DDC 1 Phase Increment Fractional A [31:24]		Numerator correction term for the MAW.	0x0	R/W
0x03A4	DDC 1 Phase Increment Fractional A4	[7:0]	DDC 1 Phase Increment Fractional A [39:32]		Numerator correction term for the MAW.	0x0	R/W
0x03A5	DDC 1 Phase Increment Fractional A5	[7:0]	DDC 1 Phase Increment Fractional A [47:40]		Numerator correction term for the MAW.	0x0	R/W
0x03A8	DDC 1 Phase Increment Fractional B0	[7:0]	DDC 1 Phase Increment Fractional B [7:0]		Denominator correction term for the MBW.	0x0	R/W
0x03A9	DDC 1 Phase Increment Fractional B1	[7:0]	DDC 1 Phase Increment Fractional B [15:8]		Denominator correction term for the MBW.	0x0	R/W
0x03AA	DDC 1 Phase Increment Fractional B2	[7:0]	DDC 1 Phase Increment Fractional B [23:16]		Denominator correction term for the MBW.	0x0	R/W
0x03AB	DDC 1 Phase Increment Fractional B3	[7:0]	DDC 1 Phase Increment Fractional B [31:24]		Denominator correction term for the MBW.	0x0	R/W

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x03AC	DDC 1 Phase Increment Fractional B4	[7:0]	DDC 1 Phase Increment Fractional B [39:32]		Denominator correction term for the MBW.	0x0	R/W
0x03AD	DDC 1 Phase Increment Fractional B5	[7:0]	DDC 1 Phase Increment Fractional B [47:40]		Denominator correction term for the MBW.	0x0	R/W
0x03B0	DDC 2 Phase Increment Fractional A0	[7:0]	DDC 2 Phase Increment Fractional A [7:0]		Numerator correction term for the MAW.	0x0	R/W
0x03B1	DDC 2 Phase Increment Fractional A1	[7:0]	DDC 2 Phase Increment Fractional A [15:8]		Numerator correction term for the MAW.	0x0	R/W
0x03B2	DDC 2 Phase Increment Fractional A2	[7:0]	DDC 2 Phase Increment Fractional A [23:16]		Numerator correction term for the MAW.	0x0	R/W
0x03B3	DDC 2 Phase Increment Fractional A3	[7:0]	DDC 2 Phase Increment Fractional A [31:24]		Numerator correction term for the MAW.	0x0	R/W
0x03B4	DDC 2 Phase Increment Fractional A4	[7:0]	DDC 2 Phase Increment Fractional A [39:32]		Numerator correction term for the MAW.	0x0	R/W
0x03B5	DDC 2 Phase Increment Fractional A5	[7:0]	DDC 2 Phase Increment Fractional A [47:40]		Numerator correction term for the MAW.	0x0	R/W
0x03B8	DDC 2 Phase Increment Fractional B0	[7:0]	DDC 2 Phase Increment Fractional B [7:0]		Denominator correction term for the MBW.	0x0	R/W
0x03B9	DDC 2 Phase Increment Fractional B1	[7:0]	DDC 2 Phase Increment Fractional B [15:8]		Denominator correction term for the MBW.	0x0	R/W
0x03BA	DDC 2 Phase Increment Fractional B2	[7:0]	DDC 2 Phase Increment Fractional B [23:16]		Denominator correction term for the MBW.	0x0	R/W
0x03BB	DDC 2 Phase Increment Fractional B3	[7:0]	DDC 2 Phase Increment Fractional B [31:24]		Denominator correction term for the MBW.	0x0	R/W
0x03BC	DDC 2 Phase Increment Fractional B4	[7:0]	DDC 2 Phase Increment Fractional B [39:32]		Denominator correction term for the MBW.	0x0	R/W
0x03BD	DDC 2 Phase Increment Fractional B5	[7:0]	DDC 2 Phase Increment Fractional B [47:40]		Denominator correction term for the MBW.	0x0	R/W
0x03C0	DDC 3 Phase Increment Fractional A0	[7:0]	DDC 3 Phase Increment Fractional A [7:0]		Numerator correction term for the MAW.	0x0	R/W
0x03C1	DDC 3 Phase Increment Fractional A1	[7:0]	DDC 3 Phase Increment Fractional A [15:8]		Numerator correction term for the MAW.	0x0	R/W
0x03C2	DDC 3 Phase Increment Fractional A2	[7:0]	DDC 3 Phase Increment Fractional A [23:16]		Numerator correction term for the MAW.	0x0	R/W
0x03C3	DDC 3 Phase Increment Fractional A3	[7:0]	DDC 3 Phase Increment Fractional A [31:24]		Numerator correction term for the MAW.	0x0	R/W
0x03C4	DDC 3 Phase Increment Fractional A4	[7:0]	DDC 3 Phase Increment Fractional A [39:32]		Numerator correction term for the MAW.	0x0	R/W

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x03C5	DDC 3 Phase Increment Fractional A5	[7:0]	DDC 3 Phase Increment Fractional A [47:40]		Numerator correction term for the MAW.	0x0	R/W
0x03C8	DDC 3 Phase Increment Fractional B0	[7:0]	DDC 3 Phase Increment Fractional B [7:0]		Denominator correction term for the MBW.	0x0	R/W
0x03C9	DDC 3 Phase Increment Fractional B1	[7:0]	DDC 3 Phase Increment Fractional B [15:8]		Denominator correction term for the MBW.	0x0	R/W
0x03CA	DDC 3 Phase Increment Fractional B2	[7:0]	DDC 3 Phase Increment Fractional B [23:16]		Denominator correction term for the MBW.	0x0	R/W
0x03CB	DDC 3 Phase Increment Fractional B3	[7:0]	DDC 3 Phase Increment Fractional B [31:24]		Denominator correction term for the MBW.	0x0	R/W
0x03CC	DDC 3 Phase Increment Fractional B4	[7:0]	DDC 3 Phase Increment Fractional B [39:32]		Denominator correction term for the MBW.	0x0	R/W
0x03CD	DDC 3 Phase Increment Fractional B5	[7:0]	DDC 3 Phase Increment Fractional B [47:40]		Denominator correction term for the MBW.	0x0	R/W
Digital Outputs and Test Mode Registers							
0x0550	ADC test mode control (local)	7	User pattern selection		Test mode user pattern selection. These bits are only used when TMODE_GEN_SEL is in user input mode (TMODE_GEN_SEL = 1000). Otherwise, they are ignored. User Pattern 1 is found in the USR_PAT_1_ MSB and USR_PAT_1_LSB registers. User Pattern 2 is found in the USR_PAT_2_ MSB and USR_PAT_2_LSB registers, and so on.	0x0	R/W
				0	Continuous/repeat pattern. Place each user pattern (User Pattern 1 through User Pattern 4) on the output for 1 clock cycle and then repeat. (Output User Pattern 1, User Pattern 2, User Pattern 3, User Pattern 4, User Pattern 1, User Pattern 2, User Pattern 3, User Pattern 4, User Pattern 1, User Pattern 2, User Pattern 3, User Pattern 4, and so on).		
				1	Single Pattern. Place each User Pattern (User Pattern 1 through User Pattern 4) on the output for 1 clock cycle and then output all zeros. (Output User Pattern 1 through User Pattern 4, then output all zeros).		
		6	Reserved		Reserved.	0x0	R

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
		5	Reset pseudorandom long generator		Test mode long pseudorandom number test generator reset.	0x0	R/W
				0	Long pseudorandom enabled.		
				1	Long pseudorandom held in reset.		
		4	Reset pseudorandom short generator		Test mode short pseudorandom number Test generator reset.	0x0	R/W
				0	Short pseudorandom enabled.		
				1	Short pseudorandom held in reset.		
		[3:0]	Test mode selection		Test mode generation selection.	0x0	R/W
				0000	Off; normal operation.		
				0001	Midscale short.		
				0010	Positive full scale.		
				0011	Negative full scale.		
				0100	Alternating checker board.		
				0101	Pseudorandom sequence, long.		
				0110	Pseudorandom sequence, short.		
				0111	1/0 word toggle.		
				1000	User pattern test mode (used with TMODE_USR_PAT_SEL and the User Pattern 1 through User Pattern 4 registers).		
					1111: ramp output.		
0x0551	User Pattern 1 LSB	[7:0]	User Pattern 1 [7:0]		User Test Pattern 1 LSB.	0x0	R/W
0x0552	User Pattern 1 MSB	[7:0]	User Pattern 1 [15:8]		User Test Pattern 1 LSB.	0x0	R/W
0x0553	User Pattern 2 LSB	[7:0]	User Pattern 2 [7:0]		User Test Pattern 2 LSB.	0x0	R/W
0x0554	User Pattern 2 MSB	[7:0]	User Pattern 2 [15:8]		User Test Pattern 2 LSB.	0x0	R/W
0x0555	User Pattern 3 LSB	[7:0]	User Pattern 3 [7:0]		User Test Pattern 3 LSB.	0x0	R/W
0x0556	User Pattern 3 MSB	[7:0]	User Pattern 3 [15:8]		User Test Pattern 3 LSB.	0x0	R/W
0x0557	User Pattern 4 LSB	[7:0]	User Pattern 4 [7:0]		User Test Pattern 4 LSB.	0x0	R/W
0x0558	User Pattern 4 MSB	[7:0]	User Pattern 4 [15:8]		User Test Pattern 4 LSB.	0x0	R/W

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0559	Output Mode Control 1	[7:4]	Converter control Bit 1 selection	0000	Tie low (1'b0).	0x0	R/W
				0001	Overrange bit.		
				0010	Signal monitor bit.		
				0011	Fast detect (FD) bit.		
				0101	SYSREF±.		
		[3:0]	Converter control Bit 0 selection	0000	Tie low (1'b0).	0x0	R/W
				0001	Overrange bit.		
				0010	Signal monitor bit.		
				0011	Fast detect (FD) bit.		
				0101	SYSREF±.		
0x055A	Output Mode Control 2	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Converter control Bit 2 selection	0000	Tie low (1'b0).	0x1	R/W
				0001	Overrange bit.		
				0010	Signal monitor bit.		
				0011	Fast detect (FD) bit.		
				0101	SYSREF±.		
0x0561	Output sample mode	[7:3]	Reserved		Reserved.	0x0	R/W
		2	Sample invert	0	ADC sample data is not inverted.	0x0	R/W
				1	ADC sample data is inverted.		
		[1:0]	Data format select	00	Offset binary.	0x1	R/W
				01	Twos complement (default).		
0x0562	Output overrange clear	[7:0]	Data format overrange clear		Overrange clear bits (one bit for each virtual converter).	0x0	R/W
				0	Overrange bit enabled.		
				1	Overrange bit cleared. Writing a 1 to the overrange clear bit clears the corresponding overrange sticky bit.		
0x0563	Output overrange status	[7:0]	Data format overrange		Overrange sticky bit status (one bit for each virtual converter).	0x0	R
				0	No overrange occurred		
				1	Overrange occurred. Writing a 1 to the overrange clear bit clears the corresponding overrange sticky bit.		
0x056E	PLL control	[7:4]	JESD204B lane rate control	0011	Lane rate = 13.5 Gbps to 16 Gbps.	0x3	R/W
				0000	Lane rate = 6.75 Gbps to 13.5 Gbps.		
				0001	Lane rate = 3.375 Gbps to 6.75 Gbps.		
				0101	Lane rate = 1.6875 Gbps to 3.375 Gbps.		
		[3:0]	Reserved		Reserved.	0x0	R

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x056F	PLL status	7	PLL lock status	0	Not locked.	0x0	R
				1	Locked.		
		[6:4]	Reserved		Reserved.	0x0	R
		3	PLL loss of lock		Loss of lock sticky bit.		
				1	Indicates a loss of lock occurred at some time; cleared by setting Register 0x0571, Bit 0.		
		[2:0]	Reserved		Reserved		
0x0571	JESD204B Link Control 1	7	Standby mode	0	Standby mode forces zeros for all converter samples.	0x0	R/W
				1	Standby mode forces code group synchronization (K28.5 characters).		
		6	Tail bit (t) PN	0	Disable.	0x0	R/W
				1	Enable.		
		5	Long transport layer test	0	JESD204B test samples disabled.	0x0	R/W
				1	JESD204B test samples enabled; long transport layer test sample sequence (as specified in JESD204B Section 5.1.6.3) sent on all link lanes.		
		4	Lane synchronization	0	Disable FACI uses /K28.7/.	0x1	R/W
				1	Enable FACI uses /K28.3/ and /K28.7/.		
		[3:2]	ILAS sequence mode	00	Initial lane alignment sequence disabled (JESD204B, Section 5.3.3.5).	0x1	R/W
				01	Initial lane alignment sequence enabled (JESD204B, Section 5.3.3.5).		
				11	Initial lane alignment sequence always on test mode (JESD204B data link layer test mode) where repeated lane alignment sequence (as specified in JESD204B, Section 5.3.3.8.2) sent on all lanes.		
		1	FACI	0	Frame alignment character insertion enabled (JESD204B, Section 5.3.3.4).	0x0	R/W
				1	Frame alignment character insertion disabled; for debug only (JESD204B, Section 5.3.3.4).		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	Link control	0	JESD204B serial transmit link enabled. Transmission of the /K28.5/ characters for code group synchronization is controlled by the SYNCINB± pin.	0x0	R/W
				1	JESD204B serial transmit link powered down (held in reset and clock gated).		
0x0572	JESD204B Link Control 2	[7:6]	SYNCINB± pin control	00	Normal mode.	0x0	R/W
				10	Ignore SYNCINB± (force CGS).		
				11	Ignore SYNCINB± (force ILAS/user data).		
		5	SYNCINB± pin invert	0	SYNCINB± pin not inverted.	0x0	R/W
				1	SYNCINB± pin inverted.		
		4	SYNCINB± pin type	0	LVDS differential pair SYNC input.	0x0	R/W
				1	CMOS single-ended SYNC input.		
		3	Reserved		Reserved.	0x0	R
		2	8-bit/10-bit bypass	0	8-bit/10-bit enabled.	0x0	R/W
				1	8-bit/10-bit bypassed (the most significant 2 bits are 0).		
		1	8-bit/10-bit bit invert	0	Normal.	0x0	R/W
				1	Invert a, b, c, d, e, f, g, h, l, and j symbols.		
		0	Reserved		Reserved.	0x0	R/W
0x0573	JESD204B Link Control 3	[7:6]	Checksum mode	00	Checksum is the sum of all 8-bit registers in the link configuration table.	0x0	R/W
				01	Checksum is the sum of all individual link configuration fields (LSB aligned).		
				10	Checksum is disabled (set to zero). For test purposes only.		
				11	Unused.		
		[5:4]	Test injection point	0	N' sample input.	0x0	R/W
				1	10 bit data at 8-bit/10-bit output (for PHY testing)		
				10	8-bit data at scrambler input.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[3:0]	JESD204B test mode patterns	0	Normal operation (test mode disabled).	0x0	R/W
				1	Alternating checkerboard.		
				10	1/0 word toggle.		
				11	31-bit PN sequence ($x^{31} + x^{28} + 1$).		
				100	23-bit PN sequence ($x^{23} + x^{18} + 1$).		
				101	15-bit PN sequence ($x^{15} + x^{14} + 1$).		
				110	9-bit PN sequence ($x^{9} + x^{5} + 1$).		
				111	7-bit PN sequence ($x^{7} + x^{6} + 1$).		
				1000	Ramp output.		
				1110	Continuous/repeat user test.		
				1111	Single user test.		
0x0574	JESD204B Link Control 4	[7:4]	ILAS delay	0	Transmit ILAS on first LMFC after SYNCINB± deasserted.	0x0	R/W
				1	Transmit ILAS on second LMFC after SYNCINB± deasserted.		
				10	Transmit ILAS on third LMFC after SYNCINB± deasserted.		
				11	Transmit ILAS on fourth LMFC after SYNCINB± deasserted.		
				100	Transmit ILAS on fifth LMFC after SYNCINB± deasserted.		
				101	Transmit ILAS on sixth LMFC after SYNCINB± deasserted.		
				110	Transmit ILAS on seventh LMFC after SYNCINB± deasserted.		
				111	Transmit ILAS on eighth LMFC after SYNCINB± deasserted.		
				1000	Transmit ILAS on ninth LMFC after SYNCINB± deasserted.		
				1001	Transmit ILAS on tenth LMFC after SYNCINB± deasserted.		
				1010	Transmit ILAS on eleventh LMFC after SYNCINB± deasserted.		
				1011	Transmit ILAS on twelfth LMFC after SYNCINB± deasserted.		
				1100	Transmit ILAS on thirteenth LMFC after SYNCINB± deasserted.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
				1101	Transmit ILAS on fourteenth LMFC after SYNCINB± deasserted.		
				1110	Transmit ILAS on fifteenth LMFC after SYNCINB± deasserted.		
				1111	Transmit ILAS on sixteenth LMFC after SYNCINB± deasserted.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	Link layer test mode	000	Normal operation (link layer test mode disabled).	0x0	R/W
				001	Continuous sequence of /D21.5/ characters.		
				010	Reserved.		
				011	Reserved.		
				100	Modified RPAT test sequence.		
				101	JSPAT test sequence.		
				110	JTSPAT test sequence.		
				111	Reserved.		
0x0578	JESD204B LMFC offset	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	LMFC phase offset value		Local multiframe clock (LMFC) phase offset value. Reset value for the LMFC phase counter when SYSREF± is asserted. Used for deterministic delay applications.	0x0	R/W
0x0580	JESD204B device identification (DID) configuration	[7:0]	JESD204B Tx DID value		JESD204B serial DID number.	0x0	R/W
0x0581	JESD204B bank identification (BID) configuration	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	JESD204B Tx BID value		JESD204B serial BID number (extension to DID).	0x0	R/W
0x0583	JESD204B Lane Identification 0 (LID0) configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 0 LID value		JESD204B serial LID number for Lane 0.	0x0	R/W
0x0584	JESD204B LID1 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 1 LID value		JESD204B serial LID number for Lane 1.	0x1	R/W
0x0585	JESD204B LID2 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 2 LID value		JESD204B serial LID number for Lane 2.	0x2	R/W
0x0586	JESD204B LID3 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 3 LID value		JESD204B serial LID number for Lane 3.	0x3	R/W
0x058B	JESD204B scrambling and number of lanes (L) configuration	7	JESD204B scrambling (SCR)	0	JESD204B scrambler disabled (SCR = 0).	0x1	R/W
				1	JESD204B scrambler enabled (SCR = 1).		
		[6:5]	Reserved		Reserved.	0x0	R

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[4:0]	JESD204B lanes (L)	0x0	One lane per link (L = 1).	0x3	R/W
				0x1	Two lanes per link (L = 2).		
				0x3	Four lanes per link (L = 4).		
0x058C	JESD204B link number of octets per frames (F)	[7:0]	JESD204B F configuration		JESD204B number of octets per frame (F = JESD204B_F_CONFIG + 1).	0x0	R/W
				0	F = 1.		
				1	F = 2.		
				10	F = 3.		
				11	F = 4.		
				101	F = 6.		
				111	F = 8.		
				1111	F = 16.		
0x058D	JESD204B link number of frames per multiframe (K)	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JESD204B K configuration		JESD204B number of frames per multi-frame (K = JESD204B_K_CONFIG + 1). Only values where F × K which are divisible by 4 can be used.	0x1F	R/W
0x058E	JESD204B link number of converters (M)	[7:0]	JESD204B M configuration		JESD204B number of converters per link/device (M = JESD204B_M_CFG).	0x1	R/W
				0	Link connected to one virtual converter (M = 1).		
				1	Link connected to two virtual converters (M = 2).		
				11	Link connected to four virtual converters (M = 4).		
				111	Link connected to eight virtual converters (M = 8).		
0x058F	JESD204B number of control bits (CS) and ADC resolution (N)	[7:6]	Number of control bits (CS) per sample	0	No control bits (CS = 0)	0x0	R/W
				1	1 control bit (CS = 1), Control Bit 2 only.		
				10	2 control bits (CS = 2), Control Bit 2 and Control Bit 1 only.		
				11	3 control bits (CS = 3), all control bits (2, 1,and 0).		
		5	Reserved		Reserved.	0x0	R
		[4:0]	ADC converter resolution (N)	00110	N = 7-bit resolution.	0xF	R/W
				00111	N = 8-bit resolution.		
				01000	N = 9-bit resolution.		
				01001	N = 10-bit resolution.		
				01010	N = 11-bit resolution.		
				01011	N = 12-bit resolution.		
				01100	N = 13-bit resolution.		
				01101	N = 14-bit resolution.		
				01110	N = 15-bit resolution.		
				01111	N = 16-bit resolution.		
0x0590	JESD204B SCV NP configuration	[7:5]	Subclass support	000	Subclass 0.	0x1	R/W
				001	Subclass 1.		
		[4:0]	ADC number of bits per sample (N')	00111	N' = 8.	0xF	R/W
				01111	N' = 16.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0591	JESD204B JV S configuration	[7:5]	Reserved		Reserved.	0x1	R
		[4:0]	Samples per converter frame cycle (S)		Samples per converter frame cycle (S = Register 0x0591, Bits[4:0]+1)	0x0	R
0x0592	JESD204B HD CF configuration	7	HD value	0	High density format disabled.	0x0	R
				1	High density format enabled.		
		[6:5]	Reserved		Reserved.	0x0	R
		[4:0]	Control words per frame clock cycle per link (CF)		Number of control words per frame clock cycle per link (CF = Register 0x0592, Bits[4:0]).	0x0	R
0x05A0	JESD204B Checksum 0 configuration	[7:0]	Checksum 0 value for SERDOUT0±		Serial Checksum Value for Lane 0. Automatically calculated for each lane. Sum(all link configuration parameters for Lane 0) mod 256.	0xC3	R
0x05A1	JESD204B Checksum 1 configuration	[7:0]	Checksum 1 value for SERDOUT1±		Serial Checksum Value for Lane 1. Automatically calculated for each lane. Sum(all link configuration parameters for Lane 1) mod 256.	0xC4	R
0x05A2	JESD204B Checksum 2 configuration	[7:0]	Checksum 2 value for SERDOUT2±		Serial Checksum Value for Lane 2. Automatically calculated for each lane. Sum(all link configuration parameters for each lane) mod 256.	0xC5	R
0x05A3	JESD204B Checksum 3 configuration	[7:0]	Checksum 3 value for SERDOUT3±		Serial Checksum Value for Lane 3. Automatically calculated for each lane. Sum(all link configuration parameters for Lane 3) mod 256.	0xC6	R
0x05B0	JESD204B lane power-down	7	Reserved		Reserved.	0x0	R
		6	JESD204B Lane 3 power-down		Physical Lane 3 force power-down.	0x0	R/W
		5	Reserved		Reserved.	0x0	R
		4	JESD204B Lane 2 power-down		Physical Lane 2 force power-down.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		2	JESD204B Lane 1 power-down		Physical Lane 1 force power-down.	0x0	R/W
		1	Reserved		Reserved.	0x0	R
		0	JESD204B Lane 0 power-down		Physical Lane 0 force power-down.	0x0	R/W
0x05B2	JESD204B Lane Assignment 1	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT0± lane assignment		Physical Lane 0 assignment.	0x0	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x05B3	JESD204B Lane Assignment 2	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT1± lane assignment		Physical Lane 1 assignment.	0x1	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1		
				10	Logical Lane 2		
				11	Logical Lane 3.		
0x05B5	JESD204B Lane Assignment 3	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT2± lane assignment		Physical Lane 2 assignment.	0x2	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
0x05B6	JESD204B Lane Assignment 4	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT3± lane assignment		Physical Lane 3 assignment.	0x3	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
0x05BF	SERDOUTx± data invert	7	Reserved		Reserved.	0x0	R/W
		6	Invert SERDOUT3± data		Invert SERDOUT3± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		5	Reserved		Reserved.	0x0	R/W
		4	Invert SERDOUT2± data		Invert SERDOUT2± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		3	Reserved		Reserved.	0x0	R/W
		2	Invert SERDOUT1± data		Invert SERDOUT1± data	0x0	R/W
				0	Normal.		
				1	Invert.		
		1	Reserved		Reserved.	0x0	R/W
		0	Invert SERDOUT0± data		Invert SERDOUT0± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
0x05C0	JESD204B Swing Adjust 1	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT0± voltage swing adjust		Output swing level for SERDOUT0±.	0x1	R/W
				0	1.0 × DRVDD1.		
				1	0.850 × DRVDD1.		
				2	0.750 × DRVDD1.		
0x05C1	JESD204B Swing Adjust 2	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT1± voltage swing adjust		Output swing level for SERDOUT1±.	0x1	R/W
				0	1.0 × DRVDD1.		
				1	0.850 × DRVDD1.		
				2	0.750 × DRVDD1.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x05C2	JESD204B Swing Adjust 3	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT2± voltage swing adjust		Output swing level for SERDOUT2±.	0x1	R/W
				0	1.0 × DRVDD1.		
				1	0.850 × DRVDD1.		
				2	0.750 × DRVDD1.		
0x05C3	JESD204B Swing Adjust 4	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT3± voltage swing adjust		Output swing level for SERDOUT3±.	0x1	R/W
				0	1.0 × DRVDD1.		
				1	0.850 × DRVDD1.		
				2	0.750 × DRVDD1.		
0x05C4	SERDOUT0± pre-emphasis select	7	Post tap enable		Post tab enable.	0x0	R/W
				0	Disable.		
				1	Enable.		
		[6:4]	Set post tap level for SERDOUT0±		Set post tap level.	0x0	R/W
				000	0 dB.		
				001	3 dB.		
				010	6 dB.		
				011	9 dB.		
				100	12 dB.		
		[3:0]	Reserved		Reserved.	0x0	R/W
0x05C6	SERDOUT1± pre-emphasis select	7	Post tap enable		Post tab enable.	0x0	R/W
				0	Disable.		
				1	Enable.		
		[6:4]	Set post tap level for SERDOUT1		Set post tap level.	0x0	R/W
				000	0 dB.		
				001	3 dB.		
				010	6 dB.		
				011	9 dB.		
				100	12 dB.		
		[3:0]	Reserved		Reserved.	0x0	R/W
0x05C8	SERDOUT2± pre-emphasis select	7	Post tap enable		Post tab enable.	0x0	R/W
				0	Disable.		
				1	Enable.		
		[6:4]	Set post tap level for SERDOUT2		Set post tap level.	0x0	R/W
				000	0 dB.		
				001	3 dB.		
				010	6 dB.		
				011	9 dB.		
				100	12 dB.		
		[3:0]	Reserved		Reserved.	0x0	R/W
0x05CA	SERDOUT3± pre-emphasis select	7	Post tap enable		Post tab enable.	0x0	R/W
				0	Disabled		
				1	Enabled.		
		[6:4]	Set post tap level for SERDOUT3±		Set post tap level.	0x0	R/W
				000	0 dB.		
				001	3 dB.		
				010	6 dB.		
				011	9 dB.		
				100	12 dB.		
		[3:0]	Reserved		Reserved.	0x0	R/W

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1222	JESD204B PLL calibration	[7:0]	JESD204B PLL calibration		See Table 30.	0x00	R/W
				0x00	JESD204B PLL normal operation.		
				0x04	Reset JESD204B PLL calibration.		
0x1228	JESD204B PLL start-up control	[7:0]	JESD204B PLL start-up control		See Table 30.	0x0F	R/W
				0x00	JESD204B start-up circuit in normal operation.		
				0x4F	Reset JESD204B start-up circuit.		
0x1262	JESD204B PLL LOL bit control	[7:0]	JESD204B PLL LOL bit control		See Table 30.	0x00	R/W
				0x00	Loss of lock bit normal operation.		
				0x80	Clear loss of lock bit.		
Programmable Filter Control and Coefficients Registers							
0x0DF8	Programmable filter control	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Programmable filter mode		Programmable filter (PFILT) mode.	0x0	R/W
				000	Disabled (filters bypassed).		
				001	Single filter (Filter X only). DOUT_I[n] = DIN_I[n] × X_I[n].		
				010	Single filter (Filter X and Filter Y together). DOUT_I[n] = DIN_I[n] × XY_I[n].		
				100	Cascaded filters (Filter X to Filter Y). DOUT_I[n] = DIN_I[n] × X_I[n] × Y_I[n].		
				111	Real 96-tab filter. DOUT_I[n] × XY_I[n].		
0x0DF9	PFILT gain	7	Reserved		Reserved.	0x0	R
		[6:4]	PFILT Y gain		Programmable filter (PFILT) Y gain 100 = reserved. 101 = reserved. 110 = −12 dB loss. 111 = −6 dB loss. 000: 0 dB gain. 001: +6 dB gain. 010: +12 dB gain. 011: reserved.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		[2:0]	PFILT X gain		Programmable filter (PFILT) X gain. 100 = reserved. 101 = reserved. 110 = −12 dB loss. 111 = −6 dB loss. 000: 0 dB gain. 001: +6 dB gain. 010: +12 dB gain. 011: reserved.	0x0	R/W

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0E00 to 0x0E7F	Programmable Filter X Coefficient x	[7:0]	Programmable Filter X Coefficient 0 to Programmable Filter X Coefficient 127		Refer to the I coefficient table (Table 14) in the Programmable Finite Impulse Response (FIR) Filters section for details. Coefficients are only applied after the chip transfer bit (Register 0x000F, Bit 0) is set.	0x0	R/W
0x0F00 to 0x0F7F	Programmable Filter Y Coefficient x	[7:0]	Programmable Filter Y Coefficient 0 to Programmable Filter Y Coefficient 127		Refer to the I coefficient table (Table 14) in in the Programmable Finite Impulse Response (FIR) Filters section for details. Coefficients are only applied after the chip transfer bit (Register 0x000F, Bit 0) is set.	0x0	R/W
VREF/Analog Input Control Registers							
0x0701	DC Offset Calibration Control 1 (local)	7	DC Offset Calibration Enable 1	0 1	Disabled (must set to 0 when Register 0x073B, Bit 7 = 1). Enabled (must set to 1 when Register 0x073B, Bit 7 = 0).	0x0	R/W
		[6:0]	Reserved	110	Reserved.	0x6	R
0x073B	DC Offset Calibration Control 2 (local)	7	DC Offset Calibration Enable 2	0 1	Enabled (must set to 0 when Register 0x0701, Bit 7 = 1). Disabled (must set to 1 when Register 0x0701, Bit 7 = 0).	0x1	R/W
		[6:0]	Reserved	111111	Reserved.	0x3F	R
0x18A6	VREF control	[7:1]	Reserved		Reserved.	0x0	R
		0	VREF control	0 1	Internal reference. External reference.	0x0	R/W
0x18E3	External VCM buffer control	7	Reserved		Reserved.	0x0	R
		6	External VCM buffer	0 1	Disable. Enable.	0x0	R/W
		[5:0]	External VCM buffer [5:0]		See the Input Common Mode section.	0x0	R/W

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x18E6	Temperature diode export	[7:0]	Temperature diode location select		See the Temperature Diode section.	0x0	R/W
				0x00	Central diode. VREF pin = high-Z.		
				0x01	Central diode. VREF pin = 1× diode voltage output.		
				0x02	Central diode. VREF pin = 20× diode voltage output.		
				0x03	Central diode. VREF pin = GND.		
				0x40	ADC core diode. VREF pin = high-Z.		
				0x41	ADC core diode. VREF pin = 1× diode voltage output.		
				0x42	ADC core diode. VREF pin = 20× diode voltage output.		
				0x43	ADC core diode. VREF pin = GND.		
0x1908	Analog input control (local)	[7:3]	Reserved		Reserved.	0x0	R
		2	Enable dc coupling	0	Analog input optimized for ac coupling.	0x0	R/W
				1	Analog input optimized for dc coupling.		
		[1:0]	Reserved		Reserved.	0x0	R
0x1910	Input full-scale control (local)	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	TRM VREF 1.8 V		Full-scale voltage setting.	0xD	R/W
				0	2.04 V p-p differential.		
				1010	1.36 V p-p differential.		
				1011	1.47 V p-p differential.		
				1100	1.59 V p-p differential.		
				1101	1.70 V p-p differential.		
				1110	1.81 V p-p differential.		
				1111	1.93 V p-p differential.		
0x1A4C	Buffer Control 1 (local)	[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	Buffer Control P		Input buffer main current (P).	0x1E	R/W
				00110	Buffer current set to 120 µA.		
				01000	Buffer current set to 160 µA.		
				01010	Buffer current set to 200 µA.		
				01100	Buffer current set to 240 µA.		
				01110	Buffer current set to 280 µA.		
				10000	Buffer current set to 320 µA.		
				10010	Buffer current set to 360 µA.		
				10100	Buffer current set to 400 µA.		
0x1A4D	Buffer Control 2 (local)	[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	Buffer Control N		Input buffer main current (N).	0x1E	R/W
				00110	Buffer current set to 120 µA.		
				01000	Buffer current set to 160 µA.		
				01010	Buffer current set to 200 µA.		
				01100	Buffer current set to 240 µA.		
				01110	Buffer current set to 280 µA.		
				10000	Buffer current set to 320 µA.		
				10010	Buffer current set to 360 µA.		
				10100	Buffer current set to 400 µA.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1B03	Buffer Control 3 (local)	[7:0]	Buffer Control 3		Buffer Control 3.	0x00	R/W
				0x00	Setting 1		
				0x02	Setting 2		
0x1B08	Buffer Control 4 (local)	[7:0]	Buffer Control 4		Buffer Control 4.	0x01	R/W
				0x01	Setting 1		
				0xC1	Setting 2		
0x1B10	Buffer Control 5 (local)	[7:0]	Buffer Control 5		Buffer Control 5.	0x00	R/W
				0x00	Setting 1		
				0x1C	Setting 2		

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

The power supplies required to power the AD9697 are shown in Table 45.

Table 45. Typical Power Supplies for AD9697

Domain	Voltage (V)	Tolerance (%)
AVDD1	0.95	±2.5
AVDD1_SR	0.95	±2.5
DVDD	0.95	±2.5
DRVDD1	0.95	±2.5
AVDD2	1.8	±5
DRVDD2	1.8	±5
SPIVDD	1.8	±5
AVDD3	2.5	±2.5

For applications requiring an optimal high power efficiency and low noise performance, it is recommended that the ADP5054 quad switching regulator be used to convert the 6.0 V or 12 V input rails to intermediate rails (1.3 V, 2.4 V, and 3.0 V). These intermediate rails are then postregulated by very low noise, low dropout (LDO) regulators (ADP1763, ADP7159, and ADP151). Figure 115 shows the recommended power supply scheme for the AD9697.

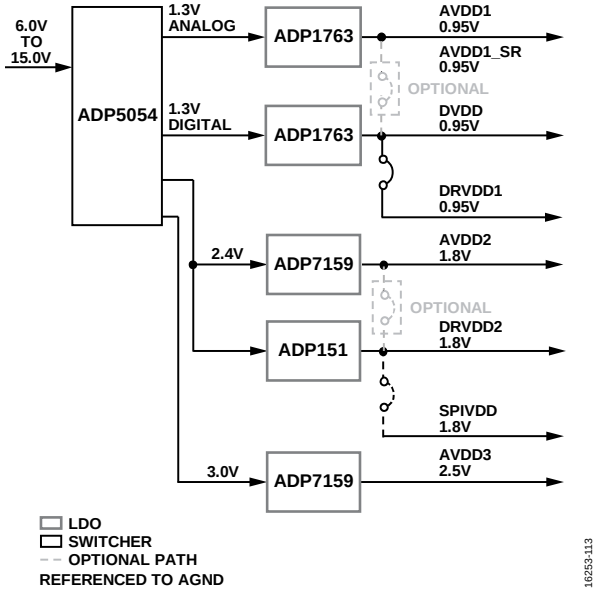


Figure 115. High Efficiency, Low Noise Power Solution for the AD9697

It is not necessary to split all of these power domains in all cases. The recommended solution shown in Figure 115 provides the lowest noise, highest efficiency power delivery system for the AD9697. If only one 0.975 V supply is available, route to AVDD1 first and then tap it off and isolate it with a ferrite bead or a filter choke, preceded by decoupling capacitors for AVDD1_SR, DVDD, and DRVDD1, in that order. Figure 116 shows the simplified schematic. Alternatively, the LDOs can be bypassed altogether and the AD9697 can be driven directly from the dc-to-dc converter. Note that this approach has risks in that there may be more power supply noise injected into the power supply domains of the ADC. To minimize noise, follow the layout guidelines of the dc-to-dc converter.

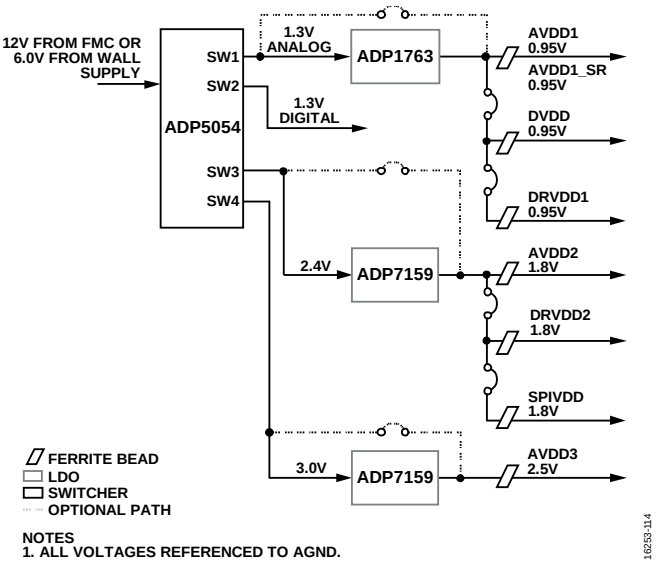


Figure 116. Simplified Power Solution for the AD9697

The user can employ several different decoupling capacitors to cover both high and low frequencies. These capacitors must be located close to the point of entry at the PCB level and close to the devices, with minimal trace lengths.

LAYOUT GUIDELINES

The ADC evaluation board can be used as a guide to follow good layout practices. The evaluation board layout is set up in such a way as to

- Minimize clock coupling to the analog inputs.
- Provide enough power and ground planes for the various supply domains while reducing cross coupling.
- Provide adequate thermal relief to the ADC.

Figure 117 shows the overall layout scheme used for the AD9697 evaluation board.

AVDD1_SR (PIN 57) AND AGND_SR (PIN 56 AND PIN 60)

AVDD1_SR (Pin 57) and AGND_SR (Pin 56 and Pin 60) can be used to provide a separate power supply node to the SYSREF± circuits of AD9697. If running in Subclass 1, the AD9697 can support periodic one-shot or gapped signals. To minimize the coupling of this supply into the AVDD1 supply node, adequate supply bypassing is needed.

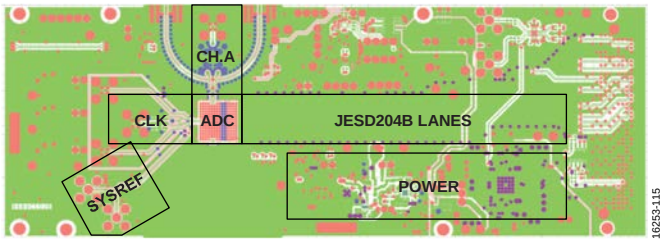


Figure 117. Recommended PCB Layout for the AD9697

OUTLINE DIMENSIONS

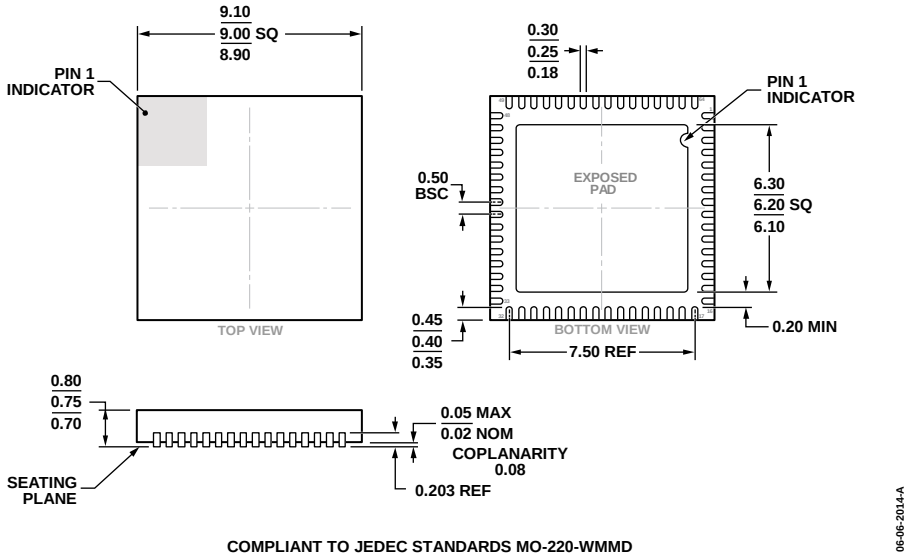


Figure 118. 64-Lead Lead Frame Chip Scale Package [LFCSP]
9 mm × 9 mm Body and 0.75 mm Package Height
(CP-64-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
AD9697BCPZ-1300	−40°C to +105°C	64-Lead Lead Frame Chip Scale Package [LFCSP]	CP-64-17
AD9697BCPZRL7-1300	−40°C to +105°C	64-Lead Lead Frame Chip Scale Package [LFCSP]	CP-64-17
AD9695-1300EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] The AD9695-1300EBZ can be used to evaluate the AD9697.

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