GENERAL DESCRIPTION

The XRK69774 is a PLL based LVCMOS Clock Generator targeted for high performance and low skew clock distribution applications. The XRK69774 can select between one of two reference inputs and provides 15 LVCMOS outputs - 14 outputs (2 banks of 5 and 1 bank of 4) for clock distribution and 1 for feedback.

The XRK69774 has two LVCMOS inputs to support clock redundancy. Switching the internal reference clock is controlled by the control input, CLK_SEL.

The XRK69774 uses PLL technology to frequency lock its outputs to the input reference clock. The divider in the feedback path will determine the frequency of the VCO. Each of the separate output banks can individually divide down the VCO output frequency. This allows the XRK69774 to generate a multitude of different bank frequency ratios and output-to-input frequency ratios.

The outputs of the XRK69774 can be immobilized, in the low state, by use of the stop clock feature. Global output disabling and reset can be achieved with the control input $\overline{\text{MR}}$/OE.

The XRK69774 has an output frequency range of 8.33MHz to125MHz and an input frequency range of 4.16MHz to 62.5MHz.

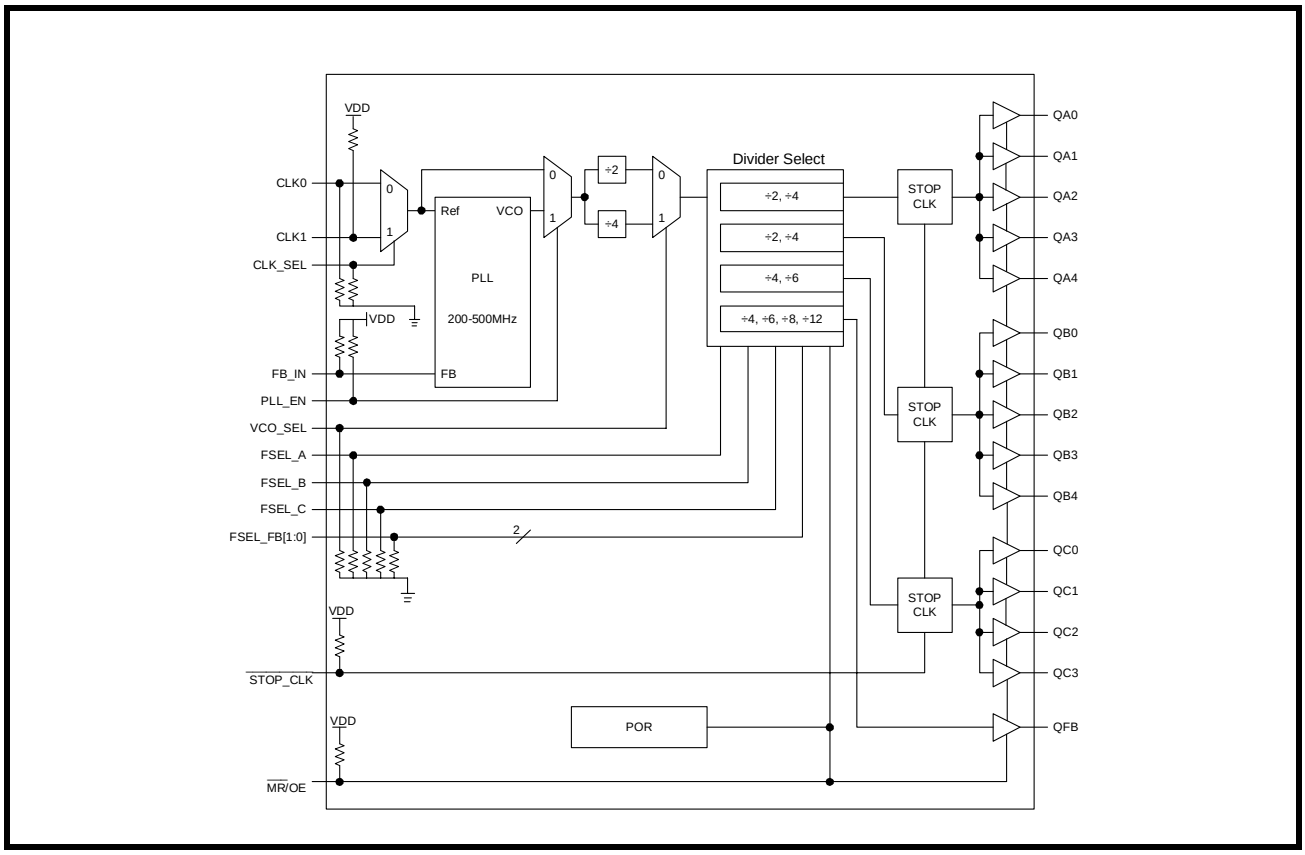
FEATURES

- Fully Integrated PLL
- 15 LVCMOS outputs
  - 2 banks with 5 outputs and 1 with 4 outputs each
  - 1 dedicated feedback for frequency control
  - Output Frequency of each Bank can be individually controlled
- VCO Range 200MHz to 500MHz
- Output freq. range: 8.33MHz to 125MHz
- Max Output Skew of 175ps
- Max Cycle-to-cycle jitter: 90ps
- LVCMOS inputs for reference clock source

APPLICATIONS

- System Clock generator
- Zero Delay Buffer

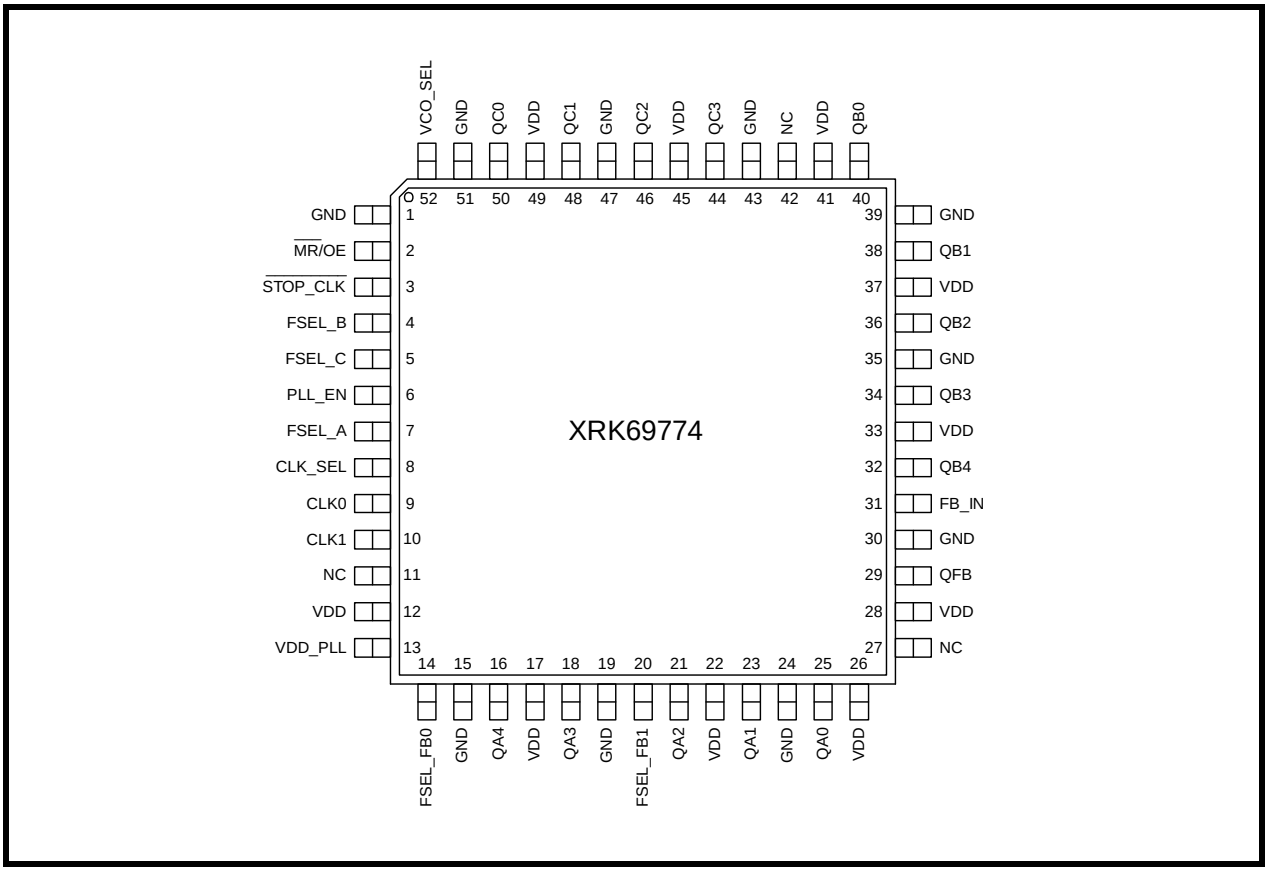
FIGURE 1. BLOCK DIAGRAM OF THE XRK69774



PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRK69774CR	52-LEAD LQFP	0°C to +70°C
XRK69774IR	52-LEAD LQFP	-40°C to +85°C

FIGURE 2. PIN OUT OF THE XRK69774



PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
1,15, 19, 24, 30, 35, 39, 43, 47, 51	GND	POWER	Power supply ground
2	$\overline{MR}$/OE	INPUT	Master reset and output enable. High = output enabled, Low = device reset & outputs tri-stated ***NOTE:*** *25kΩ Pull-Up resistor.*
3	$\overline{STOP\_CLK}$	INPUT	Clock input for serial control ***NOTE:*** *25kΩ Pull-Up resistor.*
7 4 5	FSEL_A, FSEL_B, FSEL_C	INPUT	Select inputs for control of feedback divide value. ***NOTE:*** *Each input has a 25kΩ Pull-Down resistor.*
6	PLL_EN	INPUT	PLL bypass High = PLL Enabled. Low = PLL bypass ***NOTE:*** *25kΩ Pull-Up resistor.*
8	CLK_SEL	INPUT	CLK0 or CLK1 Select. High = CLK1 selected, Low = CLK0 selected ***NOTE:*** *25kΩ Pull-Down resistor.*
9 10	CLK0 CLK1	INPUT INPUT	PLL Reference Clock Inputs ***NOTE:*** *CLK1 has 25kΩ Pull-Up resistor. CLK0 has 25kΩ Pull-Down resistor.*
11, 27, 42	NC	-	NO CONNECT
12, 17, 22, 26, 28, 33, 37, 41, 45, 49	VDD	POWER	Power supply
13	VDD_PLL	POWER	Analog supply for PLL
14 20	FSEL_FB0 FSEL_FB1	INPUT INPUT	Frequency Divider Select for QFB output ***NOTE:*** *Each input has a 25kΩ Pull-Down resistor.*
16, 18,21, 23, 25	QA[4:0]	OUTPUT	Clock outputs (Bank A)
29	QFB	OUTPUT	Feedback clock output
31	FB_IN	INPUT	Feedback input ***NOTE:*** *25kΩ Pull-Up resistor.*
32, 34, 36, 38, 40	QB[4:0]	OUTPUT	Clock outputs (Bank B)
44, 46, 48, 50	QC[3:0]	OUTPUT	Clock outputs (Bank C)
52	VCO_SEL	INPUT	VCO select. high = VCO/1, low = VCO/2. ***NOTE:*** *25kΩ Pull-Down resistor.*

1.0 ELECTRICAL SPECIFICATIONS

TABLE 1: GENERAL SPECIFICATIONS

SYMBOL	CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNIT
V_{TT}	Output Termination Voltage			VDD÷2		V
ESD_{MM}	ESD Protection (Machine model)		200			V
ESD_{HBM}	ESD Protection (Human body model)		2000			V
LU	Latch-up Immunity		200			mA
C_{IN}	Input capacitance	Per input		4		pf

TABLE 2: ABSOLUTE MAXIMUM RATINGS

SYMBOL	CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage		-0.3		3.9	V
V_{IN}	DC Input Voltage		-0.3		V_{DD} + 0.3	V
V_{OUT}	DC Output Voltage		-0.3		V_{DD} + 0.3	V
I_{IN}	DC Input Current				+/-20	mA
I_{OUT}	DC Output Current				+/-50	mA
T_S	Storage Temperature		-65		125	°C

TABLE 3: DC CHARACTERISTICS (V_{DD} = 3.3V +/- 5%)

SYMBOL	CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNIT
V_{DD_PLL}	PLL Supply Voltage	LVCMOS	3.0		V_{DD}	V
V_{IH}	Input High Voltage	LVCMOS	2.0		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	LVCMOS			0.8	V
V_{OH}	Output High Voltage	IOH=-24mA	2.4			V
V_{OL}	Output Low Voltage	IOL = 24mA IOL = 12mA			0.55 0.30	V
Z_{OUT}	Output Impedance			14 -17		Ω
I_{PU}	Input Pull-Up/Down Current	V_{IN} = GND or V_{DD}			±200	µA
I_{DD_PLL}	PLL Supply Current	@ V_{DD_PLL} Pin		5.0	7.5	mA
I_{DDQ}	Quiescent Supply Current	All V_{DD} pins			8	mA

TABLE 4: AC CHARACTERISTICS (V_{DD} = 3.3V +/- 5%)

SYMBOL	CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNIT
f_{REF}	Input reference frequency	÷8 feedback	25.0		62.5	MHz
		÷12 feedback	16.6		41.6	MHz
		÷16 feedback	12.5		31.25	MHz
		÷24 feedback	8.33		20.83	MHz
		÷32 feedback	6.25		15.625	MHz
		÷48 feedback	4.16		10.41	MHz
		PLL bypass mode			250	MHz
f_{VCO}	VCO frequency range		200		500	MHz
f_{MAX}	Output frequency	÷4 output	50.0		125	MHz
		÷8 output	25.0		62.5	MHz
		÷12 output	16.6		41.6	MHz
		÷16 output	12.5		31.25	MHz
		÷24 output	8.33		20.83	MHz
t_{PW}	CLKx pulse width		2.0			ns
It_R, It_F	Input CLKx Rise/Fall time	0.8V to 2.0V			1	ns
$t_{(\varnothing)}$	Propagation Delay (static phase offset)[a]	CLK to FB_IN f_{REF} = 50MHz & FB = ÷8	-250		+100	ps
$t_{SK(O)}$	Output to output skew	Bank A (QAx to QAy)			100	ps
		Bank B (QBx to QBy)			125	ps
		Bank C (QCx to QCy)			100	ps
		all outputs (QXy to QWz)			175	ps
DC	Output duty cycle		47	50	53	%
Ot_R, Ot_F	Output Rise/Fall time	0.55 to 2.4V	0.1		1.0	ns
t_{PLZ}, t_{PHZ}	Output Disable Time				10	ns
t_{PZL}, t_{PZH}	Output Enable Time				10	ns
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter Time	All outputs @ same frequency			90	ps
$t_{JIT(PER)}$	Period Jitter	All outputs @ same frequency			90	ps
$t_{JIT(\varnothing)}$	I/O Phase Jitter (rms) VCO= 400MHz	÷8 feedback			15	ps
		÷12 feedback			49	ps
		÷16 feedback			18	ps
		÷24 feedback			22	ps
		÷32 feedback			26	ps
		÷48 feedback			34	ps

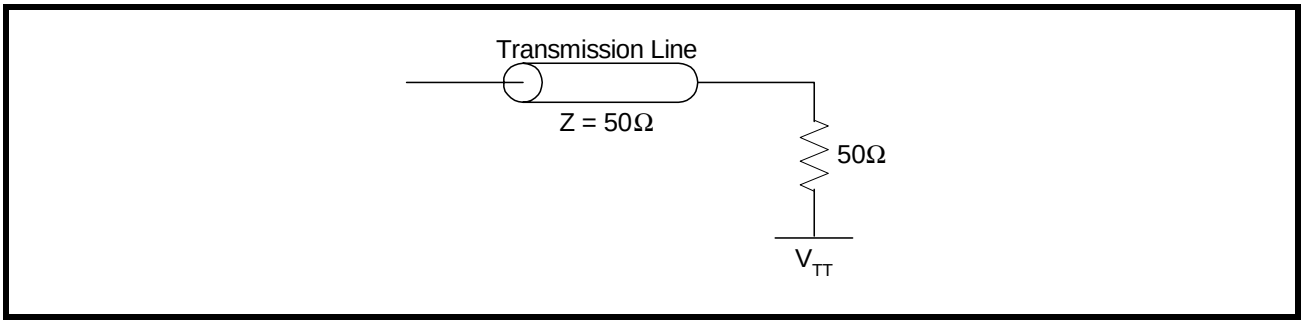
NOTE:

a. $t_{(\varnothing)}$ = +50ps ± (1÷ (120 x f_{REF})) for any reference frequency.

TABLE 5: AC CHARACTERISTICS (V_{DD} = 3.3V +/- 5%)

SYMBOL	CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNIT
BW	PLL closed loop bandwidth	÷8 feedback		0.50-1.80		MHz
		÷12 feedback		0.30-1.00		MHz
		÷16 feedback		0.25-0.70		MHz
		÷24 feedback		0.17-0.40		MHz
		÷32 feedback		0.12-0.30		MHz
		÷48 feedback		0.07-0.20		MHz
t_{LOCK}	Maximum PLL Lock Time				10	ms

FIGURE 3. TEST LOAD



2.0 CONFIGURATION TABLES

TABLE 6: FUNCTION CONTROLS

CONTROL PIN	DEFAULT	LOGIC 0	LOGIC 1
$\overline{MR}$/OE	1	Resets the output divide circuitry and serial interface, tri-states all outputs	Enables all outputs - normal operation
PLL_EN	1	PLL bypass mode enabled. This is a test mode in which the reference clock is provided to the output dividers in place of the VCO output.	PLL enabled - normal operation
STOP_CLK	1	QA[4:0], QB[4:0] and QC[3:0] outputs disabled in Low state.	Outputs enabled, normal operation
CLK_SEL	0	CLK0 selected as PLL reference	CLK1 selected
VCO_SEL	0	VCO ÷ 2	VCO ÷ 4

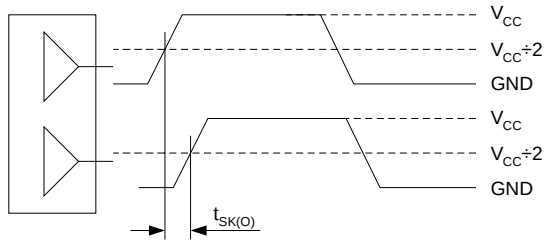
TABLE 7: BANK OUTPUT DIVIDER CONTROLS

INPUT		OUTPUT	INPUT		OUTPUT	INPUT		OUTPUT
VC0_SEL	FSEL_A	QA[4:0]	VCO_SEL	FSEL_B	QB[4:0]	VC0_SEL	FSEL_C	QC[3:0]
0	0	÷4	0	0	÷4	0	0	÷8
0	1	÷8	0	1	÷8	0	1	÷12
1	0	÷8	1	0	÷8	1	0	÷16
1	1	÷16	1	1	÷16	1	1	÷24

TABLE 8: FEEDBACK DIVIDER CONTROL

VCO_SEL	FSEL_FB1	FSEL_FB0	QFB
0	0	0	÷8
0	0	1	÷16
0	1	0	÷12
0	1	1	÷24
1	0	0	÷16
1	0	1	÷32
1	1	0	÷24
1	1	1	÷48

FIGURE 4. OUTPUT-TO-OUTPUT SKEW $t_{SK(O)}$



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device.

FIGURE 5. PROPOGATION DELAY ($t_{(Ø)}$, STATIC PHASE OFFSET) TEST REFERENCE

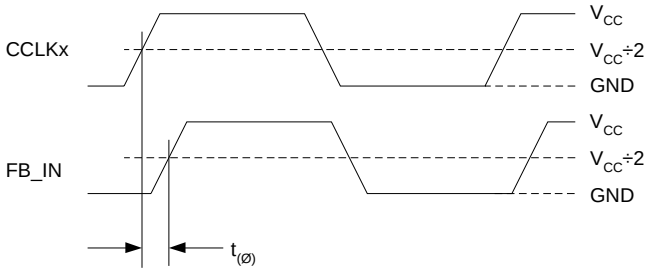
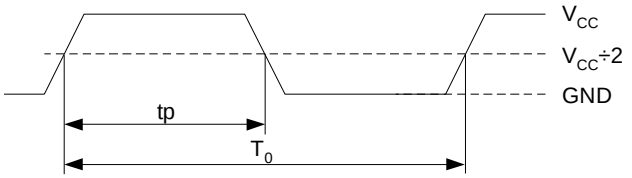


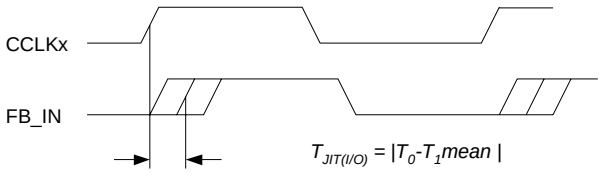
FIGURE 6. OUTPUT DUTY CYCLE (DC)



$DC=t_P/T_0 \times 100\%$

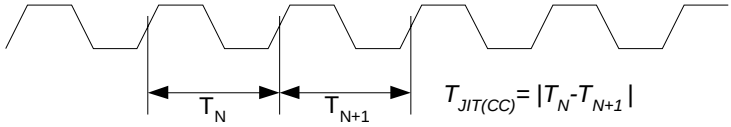
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

FIGURE 7. I/O JITTER



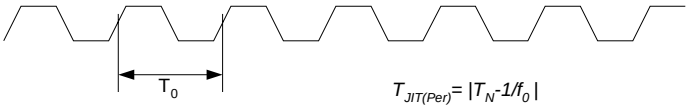
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

FIGURE 8. CYCLE-TO-CYCLE JITTER



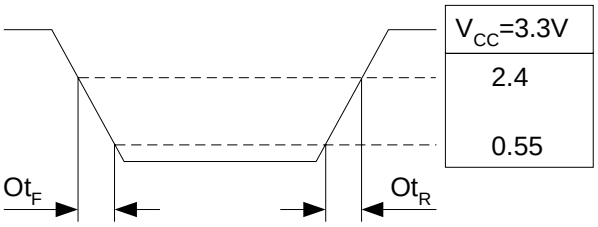
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

FIGURE 9. PERIOD JITTER



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

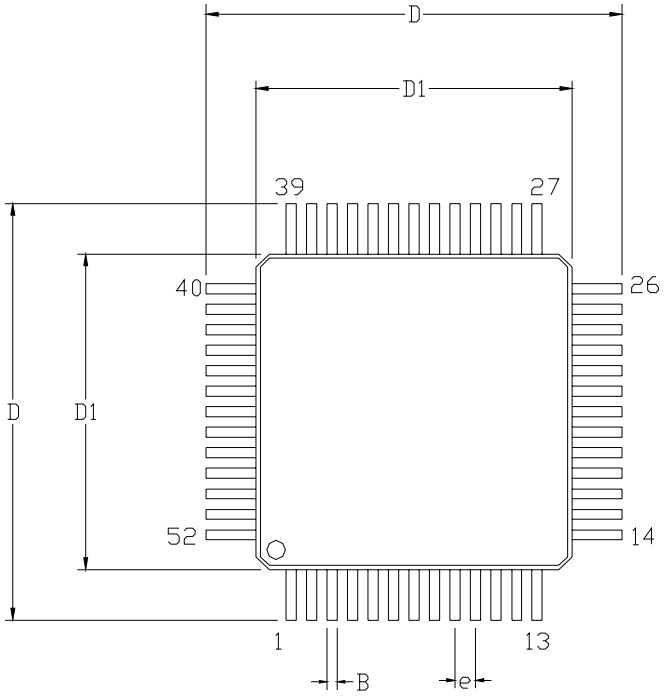
FIGURE 10. OUTPUT TRANSITION TIME TEST REFERENCE

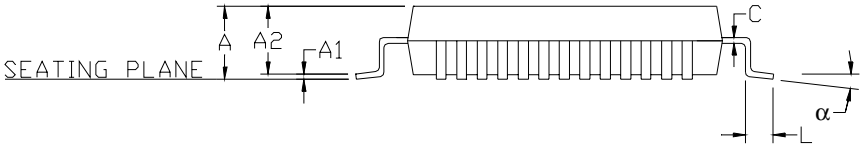


PACKAGE DIMENSIONS

52 LEAD LOW-PROFILE QUAD FLAT PACK
(10 mm x 10 mm X 1.4 mm LQFP, 1.0 mm Form)

Rev. 1.00





Note: The control dimension is in millimeters.

	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.055	0.063	1.40	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.010	0.014	0.25	0.35
C	0.004	0.009	0.11	0.23
D	0.465	0.480	11.80	12.20
D1	0.390	0.398	9.90	10.10
e	0.0256 BSC		0.65 BSC	
L	0.029	0.041	0.73	1.03
α	0°	7°	0°	7°

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
P1.0.0	April 7, 2006	Initial release
P1.0.1	April 10, 2006	General Description edit last line to: ...input frequency range of 4.16MHz to 62.5MHz.

NOTICE