DATA SHEET

GPCE063A

16-Bit Sound Controller with

32K X 16 Flash Memory

Oct. 04, 2013

Version 1.8

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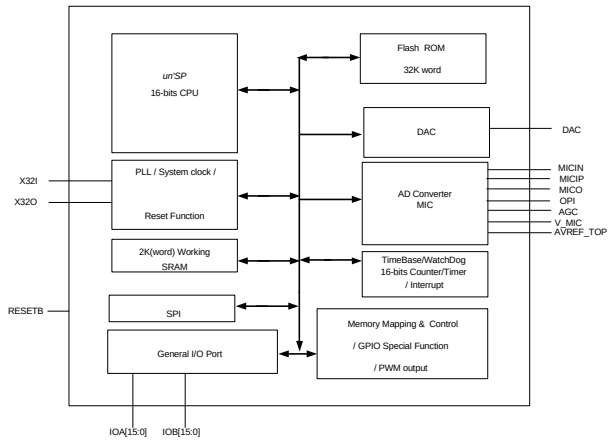
16-BIT SOUND CONTROLLER WITH 32K X 16 FLASH MEMORY

1. GENERAL DESCRIPTION

The GPCE063A, a 16-bit architecture product, carries the newest 16-bit microprocessor, *μ'nSP*™ (pronounced as *micro-n-SP*), developed by Sunplus Technology. This high processing speed assures the *μ'nSP*™ is capable of handling complex digital signal processes easily and rapidly. Therefore, GPCE063A is applicable to the areas of digital sound process and voice recognition. The operating voltage of 2.7V through 3.6V and speed of 0.16MHz through 49.152MHz yield the GPCE063A to be easily used in varieties of applications. The memory capacity includes 32K-word flash memory plus a 2K-word working SRAM. Other features include 32 programmable multi-functional I/Os, three 16-bit timers/counters, 32768Hz Real Time Clock, Low Voltage Reset/Detection, eight channels 12-bit ADC (one channel built-in MIC amplifier with auto gain controller), 14-bit DAC output and many others.

2. BLOCK DIAGRAM



3. FEATURES

- 16-bit *μ'nSP*™ microprocessor
- CPU clock: 0.16MHz - 49.152MHz
- Operating voltage: 2.7V - 3.6V
- Program Flash Operating voltage: 2.7V - 3.6V
- IO PortA & B operating voltage: 2.7V - 5.5V
- 32K-word flash memory
- 2K-word working SRAM
- Software-based audio processing
- Standby mode for power saving
- Three 16-bit timers/counters
- One 14-bit DAC output
- 32 general I/Os (bit programmable)
- Key wakeup function (IOA0 - 15)
- PLL feature for system clock
- 32768Hz Real Time Clock (RTC)
- Eight channels of 12-bit AD converter
- ADC external top reference voltage
- Built-in microphone amplifier and AGC function
- Low voltage reset and low voltage detection
- Watchdog enable (option)
- ICE function for development and download into flash memory
- Security function to protect code to be read and written
- One SPI serial interface I/O
- Data retention > 10 years

4. APPLICATION FIELD

- Voice recognition products
- Intelligent interactive talking toys
- Advanced educational toys
- Kid's learning products
- Kid's storybook
- General speech synthesizer
- Long duration audio products
- Recording / playback products

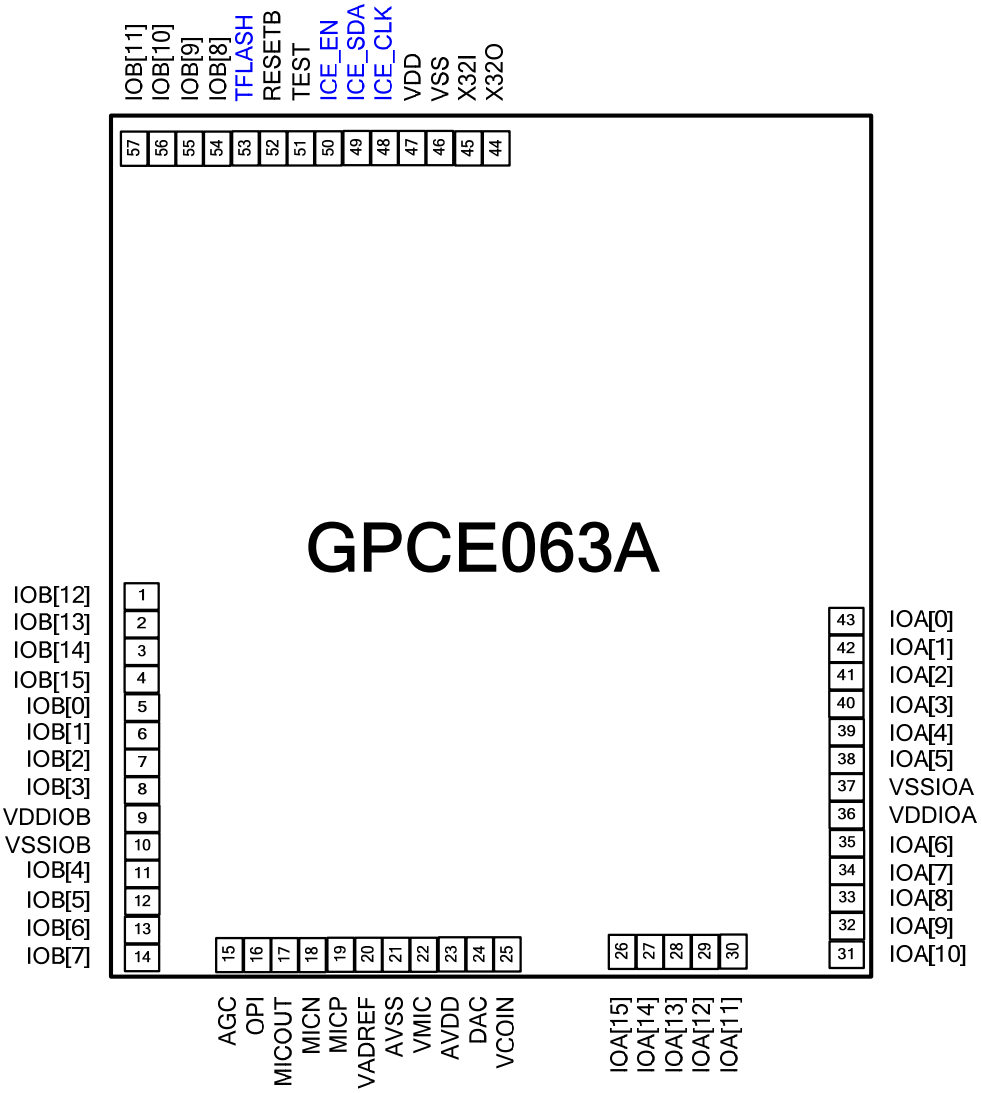
5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	LQFP 64 PIN No.	Type	Description
PORT A, Port B				
IOA[15:0]	26-35, 38-43	28-37, 40-45	I/O	IOA[15:0]: bi-directional I/O ports It can be programmed as wakeup I/O pins
IOB[15:0]	4-1, 57-54, 14-11, 8-5	6-3, 64-61, 16-13, 10-7	I/O	IOB [15:0]: bi-directional I/O ports
Power & GND				
VDDIOA	36	38	P	Power vdd for Port A
VSSIOA	37	39	G	Power gnd for Port A
VDDIOB	9	11	P	Power vdd for Port B
VSSIOB	10	12	G	Power gnd for Port B
AVDD	23	25	P	Power vdd for AD,DA (3.3V)
AVSS	21	23	G	Power gnd for AD,DA
VDD	47	54	P	Power vdd for Core + PLL (3.3V)
VSS	46	53	G	Power gnd for Core + PLL
CLK SYSTEM/ ICE INTERFACE				
X32I	45	52	I	32K Oscillator crystal input
X32O	44	51	O	32K Oscillator crystal output
OPTION				
TEST	51	58	I	TEST Mode selection pin, high is test mode and low is normal mode (Pad internal pull low)
TFLASH	53	60	I	TEST flash Mode selection pin, high is test mode and low is normal mode (Pad internal pull low)
DAC				
DAC	24	26	O	Audio DAC output
ADC				
MICP	19	21	I	MIC amplifier input positive (Internal Floating)
MICN	18	20	I	MIC amplifier input negative (refer to application circuit)
MICOUT	17	19	O	MIC amplifier output (refer to application circuit)
OPI	16	18	I	Audio amplifier negative input (refer to application circuit)
AGC	15	17	IO	AGC by pass filter (refer to application circuit)
VMIC	22	24	O	Microphone power supply
VADREF	20	22	O	AVREF_DA reference pin
PLL				
VCOIN	25	27	I	PLL low pass filter input
Other Signal				
RESETB	52	59	I	System reset pin (active low) (internal 47Kohm pull high resistor)
ICE_EN	50	57	I	ICE enable pin
ICE_CLK	48	55	I	ICE clock input pin
ICE_SDA	49	56	I/O	ICE data pin
Total: 57 pads				

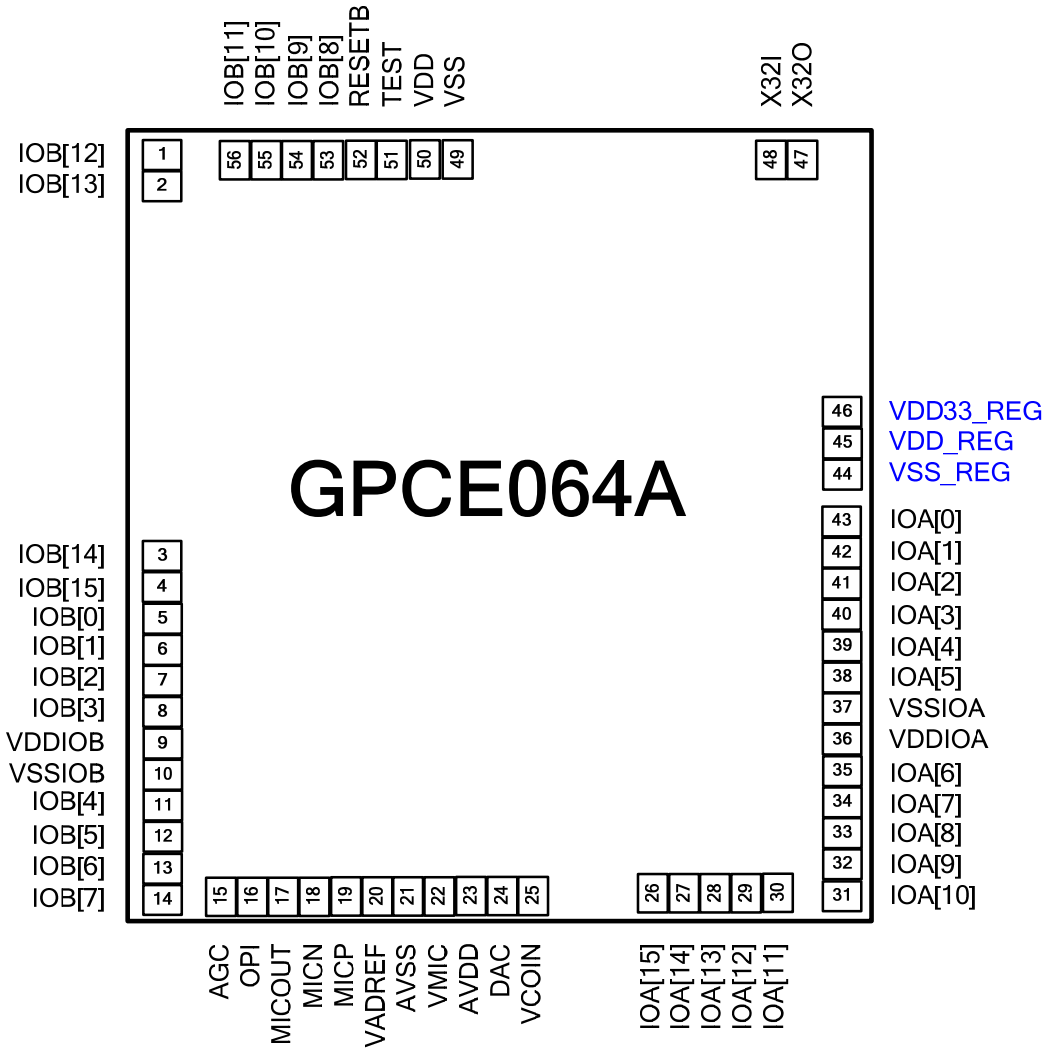
5.1. GPCE063A PAD Assignment

Important Note:

Please refer to pad assignment of both GPCE063A and GPCE064A, blue words mean their differences. Because there's some system circuit in built-in regulator of GPCE064A, user must connect regulator power input VDD_REG to power input, and connect regulator output VDD33_REG to capacitance 2.2uF even if there's no need to use this regulator.



5.2. GPCE064A PAD Assignment



5.3. GPCE063A PIN Map

Important Note:

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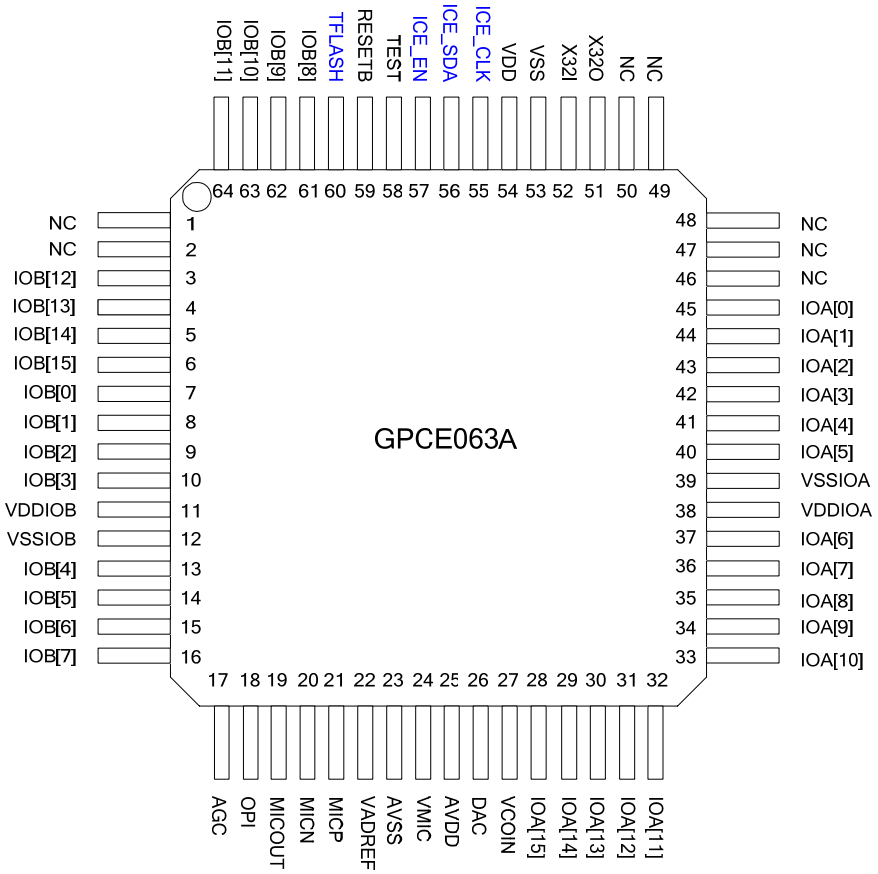
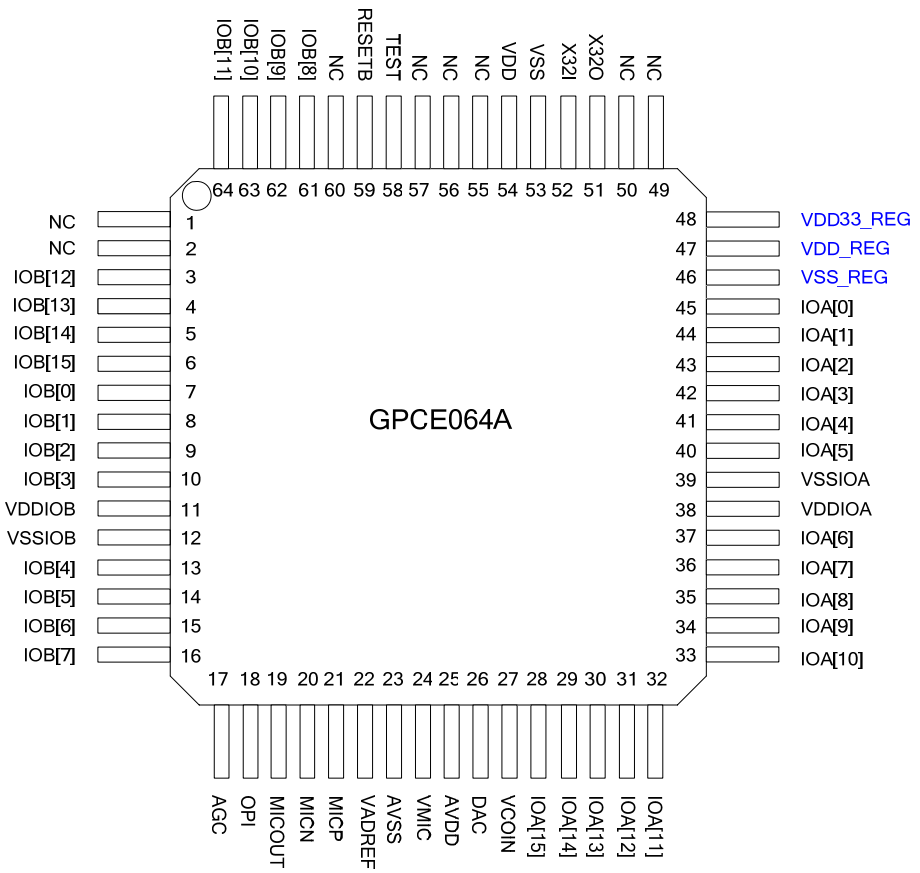
LQFP64



5.4. GPCE064A PIN Map

LQFP64



6.FUNCTIONAL DESCRIPTIONS

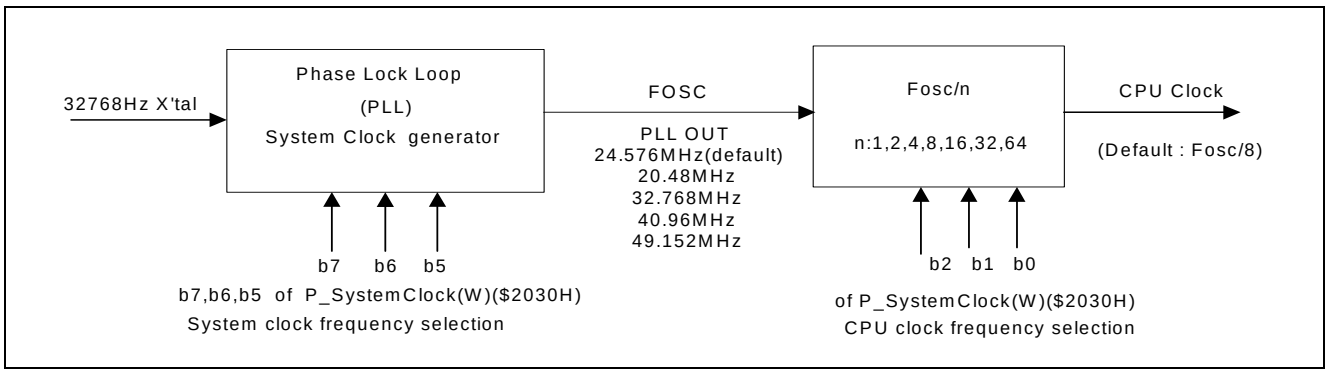
6.1. CPU

GPCE063A is equipped with a 16-bit μ'nSP™, the newest 16-bit microprocessor by Sunplus and pronounced as micro-n-SP. Eight registers are involved in μ'nSP™: R1 - R4 (General-purpose registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP) and SR (Segment Register). The interrupts include three FIQs (Fast Interrupt Request) and eight IRQs (Interrupt Request), plus one software-interrupt, BREAK.

6.2. Memory

6.2.1. SRAM

The amount of SRAM is 2K-word (including Stack), ranged from $0000 through $07FF with access speed of two CPU clock cycles.



6.2.2. Flash Memory

Flash memory ($8000 ~ $FFFF) is a high-speed memory with access speed of two CPU clock cycles. FLASH erase and program functions must be used in IDE tools.

6.3. PLL, Clock, Power Mode

6.3.1. PLL (Phase Lock Loop)

The purpose of PLL is to provide a base frequency (32768Hz) and to pump the frequency from 20.48MHz to 49.152MHz for system clock (F_{OSC}). The default PLL frequency is 24.576MHz.

6.3.1.1. System Clock

Basically, the system clock is provided by PLL and programmed by the Port_SystemClock (W) to determine the frequency of clock for system. The default system clock F_{OSC} = 24.576MHz and CPU clock is F_{OSC}/8 if not specified. The initial CPU clock is Fosc/8 after system wakes up and to be adjusted to needed CPU clock by programming the Port_SystemClock (W). This avoids Flash ROM reading failure when system wakes up.

6.3.1.2. 32768Hz RTC

The Real Time Clock (RTC) is normally used in watch, clock or other time related products. A 2Hz-RTC (1/2 seconds) function is loaded in GPCE063A. The RTC counts the timing as well as to wake CPU up whenever RTC occurs. Since the RTC is generated each 0.5 seconds, time can be traced by the numbers of RTC occurrence. In addition, GPCE063A supports 32768Hz oscillator in normal mode and auto-power-saving mode. In normal mode, 32768Hz OSC always runs at the highest power consumption. In auto-power-saving mode, however, it runs in normal mode for the first 7.5 seconds and changes back to power-saving mode automatically to save powers.

6.4. Standby Mode

The GPCE063A features a power savings mode (or called standby mode) for low power applications. To enter standby mode, the desired key wakeup port (IOA[15:0]) must be configured to input first. And read the Port_IOA_Data to latch the IOA state before entering the standby mode. Also remember to enable the corresponding interrupt source(s) for wakeup. After that, stop the CPU clock by writing $5555 into Port_SystemSleep(W) to enter standby mode. In such mode, SRAM and I/Os remain in the previous states until CPU being awakened. The wakeup sources in GPCE063A include KEY wake up (IOA[15:0]), RTC wakeup, and IRQ1 – IRQ7. After GPCE063A is awakened, CPU will continue to execute the program from the location it slept. Programmer can also enable or disable the 32768Hz RTC when CPU is in standby mode.

6.5. Low Voltage Detection and Low Voltage Reset

6.5.1. Low Voltage Detection (LVD)

The Low Voltage Detect (LVD) reports the circumstance of present voltage. There are four LVD levels available: 2.6V, 2.8V, 3.0V, and 3.2V. Those levels can be programmed via P_LVD_Ctrl. As an example, suppose LVD is given to 2.8V. When the voltage drops below 2.8V, the b12 of P_LVD_Ctrl is read as HIGH. In such state, program can be designed to react this condition.

6.5.2. Low Voltage Reset

In addition to LVD, GPCE063A has another important function, Low Voltage Reset (LVR). With the LVR function, a reset signal is generated to reset system when the operating voltage drops below LVR level. Without LVR, the CPU becomes unstable and malfunctions when the operating voltage drops below LVR level. The LVR will reset all functions to the initial operational (stable) states when the voltage drops below LVR level.

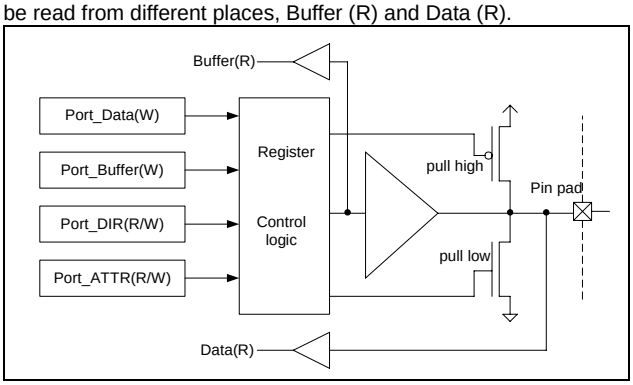
6.6. Interrupt

The GPCE063A has 13 interrupt sources, grouped into two types, FIQ (Fast Interrupt Request) and IRQ (Interrupt request). The priority of FIQ is higher than IRQ. FIQ is the high-priority interrupt while IRQ is the lower one. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt sources.

Interrupt Source	Interrupt Name / FIQ Name	IRQ Priority
Timer A	IRQ0_TMA/FIQ_TMA	1(High)
Timer B	IRQ1_TMB/FIQ_TMB	2
Timer C	IRQ2_TMC/FIQ_TMC	3
SPI	IRQ3_SPI/FIQ_SPI	4
Key wakeup	IRQ5_KEY/FIQ_KEY	5
EXT1	IRQ5_EXT1/FIQ_EXT1	6
EXT2	IRQ5_EXT2/FIQ_EXT2	7
4096Hz	IRQ6_4KHz/FIQ_4KHz	8
2048Hz	IRQ6_2KHz/FIQ_2KHz	9
512Hz	IRQ6_512Hz/FIQ_512Hz	10
64Hz	IRQ7_64Hz/FIQ_64Hz	11
16Hz	IRQ7_16Hz_FIQ_16Hz	12
2Hz	IRQ7_2Hz/FIQ_2Hz	13(Low)

6.7. I/O

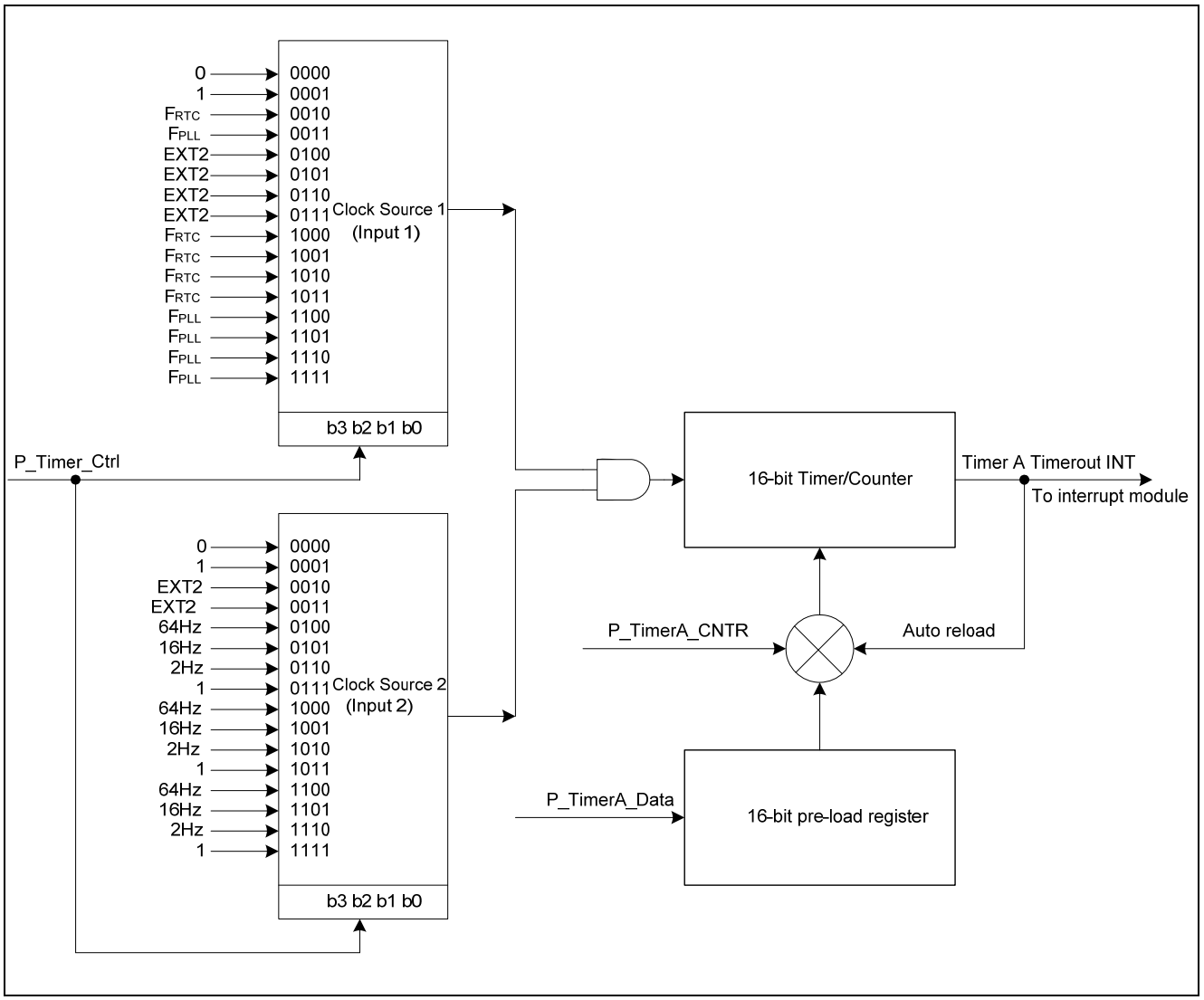
Three I/O ports are built-in GPCE063A - PortA and PortB, total has 32 bit-programmable I/Os. The PortA is a general purpose I/O with programmable wakeup capability, i.e. IOA [15:0] is the key wakeup port. To activate key wakeup function, latch data on Port_IOA_Data and enable the key wakeup function. Wakeup is triggered when PortA's state is different from at the time latched. Furthermore, the I/O ports can be operated at 5V level, higher than the CPU core which is a 3V level system. Suppose system operating voltage is running at 3.3V and VDDIO (power for I/O) operates from 3.3V to 5.5V. In such condition, the I/O pad is capable of operating from 0V through VDDIO. The following diagram is an I/O schematic. Although data can be written into the same register through Port_Data and Port_Buffer, they can be read from different places, Buffer (R) and Data (R).



In addition to a general purpose I/O port function, PortA/B also shares/carries some special functions. A summary of PortA/B special functions is listed as follows:

6.8. Special Function in Port

Port	Special Function	Function Description	Note
IOA0	IO_PWM	IO_PWM output	Refer to Timer section
IOA1	IROUT	IR Output	-
IOA2	-	-	-
IOA3	-	-	-
IOA4	High driving I/O	-	-
IOA5	High driving I/O	-	-
IOA6	High driving I/O	-	-
IOA7	High driving I/O	-	-
IOA8	Feedback Input1	-	Refer to below Example 1
	EXT1	External interrupt source 1 (negative edge triggered)	Set IOA8 as floating input mode
IOA9	Feedback Output1	Work with IOA8 by adding a RC circuit between them to get an OSC to EXT1 interrupt	Set IOA9 as inverted output
IOA10	Feedback Input2	-	Refer to below Example 1
	EXT2	External interrupt source 2 (negative edge triggered)	Set IOA10 as floating input mode
IOA11	Feedback Output2	Work with IOA10 by adding a RC circuit between them to get an OSC to EXT2 interrupts	Set IOA11 as inverted output
IOA12	SPI CS	SPI chip select	Refer to SPI section
IOA13	SPI CK	SPI clock	Refer to SPI section
IOA14	SPI TX	SPI data output	Refer to SPI section
IOA15	SPI RX	SPI data input	Refer to SPI section
IOB0	AN0	ADC Channel 0	Refer to ADC section
IOB1	AN1	ADC Channel 1	Refer to ADC section
IOB2	AN2	ADC Channel 2	Refer to ADC section
IOB3	AN3	ADC Channel 3	Refer to ADC section
IOB4	AN4	ADC Channel 4	Refer to ADC section
IOB5	AN5	ADC Channel 5	Refer to ADC section
IOB6	AN6	ADC Channel 6	Refer to ADC section
IOB7	AN7	ADC Channel 7	Refer to ADC section



PWM: Pulse Width Modulation

Refer to the above table, the configuration of IOA9, IOA10, IOA11, and IOA12 involves feedback function in which an OSC frequency can be obtained from EXT1 (EXT2) by simply adding a RC circuit between IOA8 (IOA10) and IOA9 (IOA11).

6.9. Timer / Counter

GPCE063A provides three 16-bit timers/counters - TimerA, TimerB and TimerC or so called universal counters. The clock sources of Timer A/B/C are from clock source Input 1 and clock source Input 2 (see below table) which perform AND operation to form the varieties of combinations. When timer overflows, a timeout signal (TAOUT) is sent to CPU interrupt module to generate a timer interrupt signal. In addition, Timer A/B/C hardware interrupt events can be used to latch the DAC audio output and trigger ADC conversion.

Example to Timer A, sending a write signal into TMA_CNT, the value of TMA_DATA (value=N) will reload into TMA_CNT and set an appropriated clock source. Timer wills up-count from N, N+1, N+2… 0XFFFF. An INT signal is generated at the moment of timer rolling over from “0xFFFF” to “0x0000”, and an INT signal is processed by INT controller immediately. At the same time, N will be reloaded into TMA_CNT and start counting again.

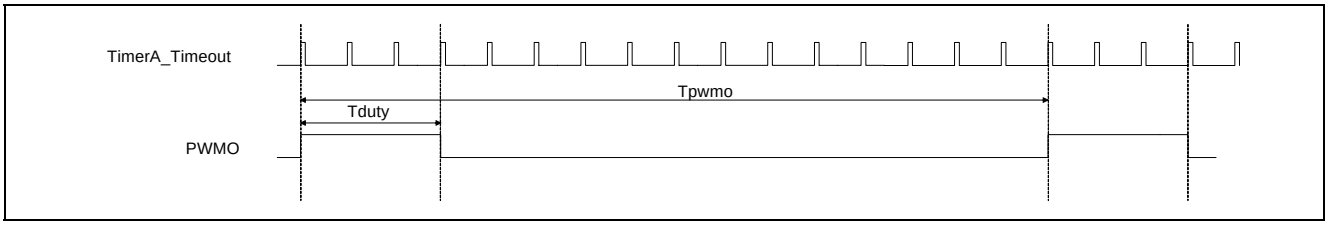
In Timer A, the clock Input 1 is a high frequency source and clock Input 2 is a low frequency clock source. The combination of clock Input 1 and 2 provides varieties of speeds to TimerA/CounterA - “1” representing pass signal (not gating), and “0” meaning timer deactivated. For instance, if Input 1=”1”, the clock is depending on Input 2. If Input 1=”0”, the TimerA is deactivated. The EXT1/ETX2 is the external clock source 1 and external clock source 2.

TMXSEL	Input 1	Input 2
0000	'0'	'0'
0001	'1'	'1'
0010	F_{RTC}	EXT2
0011	F_{PLL}	EXT2
0100	EXT2	64Hz
0101	EXT2	16Hz
0110	EXT2	2Hz
0111	EXT2	'1'
1000	F_{RTC}	64Hz
1001	F_{RTC}	16Hz
1010	F_{RTC}	2Hz
1011	F_{RTC}	'1'
1100	F_{PLL}	64Hz
1101	F_{PLL}	16Hz
1110	F_{PLL}	2Hz
1111	F_{PLL}	'1'

Generally speaking, the clock source A and C are fast clock sources and source B comes from RTC system (32768Hz). Therefore, clock source B can be utilized as a precise counter for time counting, e.g., the 2Hz clock can be used for real time counting.

6.9.1. IO PWM

One IO PWMs which duty is selected from 1/16 to 14/16. The following figure is an example of 3/16-duration cycle. The PWMO waveform is made by selecting a pulse width through Port_PWM_Ctrl. As a result, each 16 cycles will generate a pulse width defined in control port. These PWM signals can be applied for controlling the speed of motor or other devices.



6.9.2. Timebase

Timebase, generated by 32768Hz crystal oscillator, is a combination of frequency selection. Furthermore, timebase generates 4KHz, 2KHz, 512Hz, 64Hz, 16Hz and 2Hz interrupt sources (FIQ6/IRQ6, FIQ7/IRQ7) for Real-Time-Clock.

6.10. Sleep Mode, Wakeup, Halt Mode, and Watchdog

6.10.1. Sleep and Wakeup Modes

1) Sleep: After power-on reset, IC starts running until a sleep command is issued. When a sleep command is accepted, IC will turn the system clock (PLL) off. After all, it enters sleep mode.
2) Wakeup: CPU awaking from sleep mode requires a wakeup signal to turn the system clock (PLL) on. The FIQ/IRQ signal makes CPU to complete the wakeup process and initialization. The CPU wakeup source is given in the following table.

Wakeup Source
FIQ source
Timer A interrupt
Timer B interrupt
Timer C interrupt
SPI interrupt
EXT1/EXT2/KEY
RTC

6.10.2. Watchdog Reset

The GPCE063A provides another important feature, watchdog reset. With the watchdog function, a reset signal is generated to reset system when watchdog counter is overflow and the flash information block option of OPTION_WDOG_EN is enabled.

The purpose of watchdog is to monitor whether the system operates normally. Within a certain period, watchdog register must be cleared. If it is not cleared, CPU assumes the program has been running in an abnormal condition and therefore, the CPU will reset the system to the initial state and start running the program all over again.

6.11. Soft Reset Protection

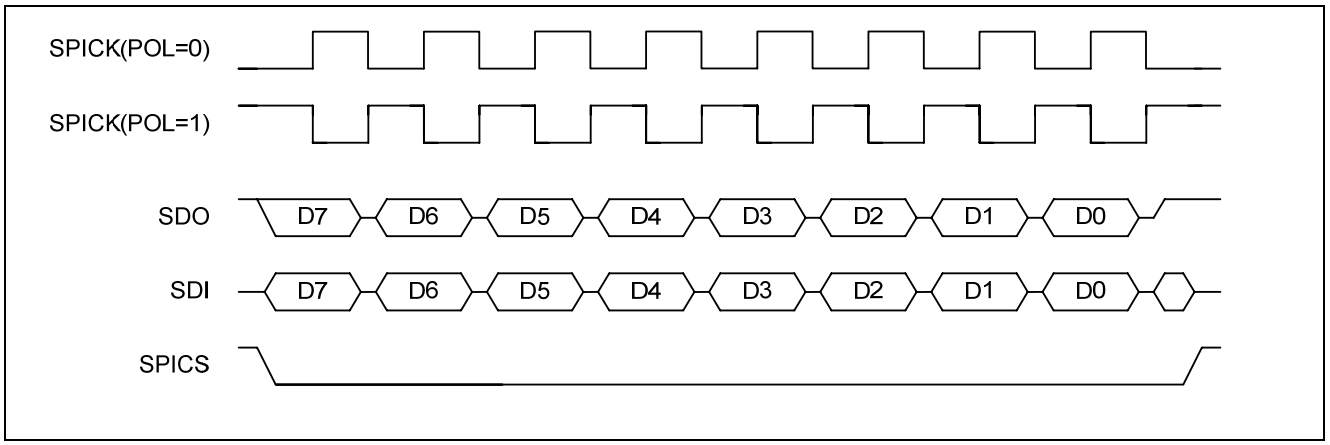
Writing $5555 into P_System_Reset will reset the whole system, same as hardware reset (pull low RESETB pin), except a flag will set on in P_System_LVD_Ctrl(R/W).

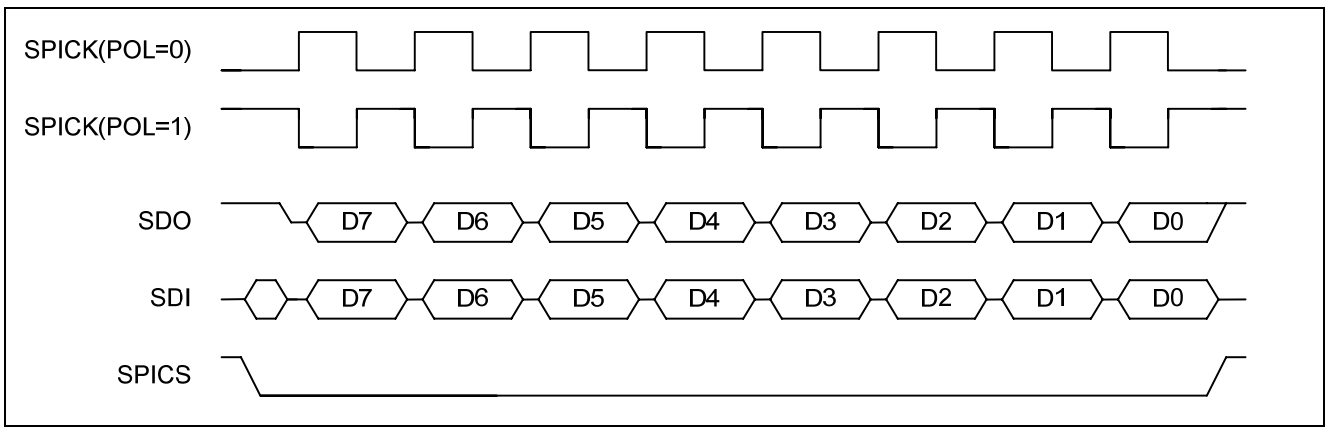
6.12. ADC (Analog to Digital Converter) / DAC

The GPCE063A has eight channels of 12-bit ADC (Analog to Digital Converter). The function of an ADC is to convert analog signal to digital signal, e.g. a voltage level into a digital word. The eight channels of ADC can be seven channels of line-in from IOB [7:0] or one channel microphone (MIC) input through amplifier and AGC controller. The MIC amplifier circuit is capable of reducing common mode noise by transmitting signals through differential MIC Inputs (MICN, MICP). Moreover, an external resistor can be applied to adjust microphone gain and time of AGC operating. The AD needs to select source of line-in before conversion. The ADC take pad(AVDD) as voltage reference .

6.13. SPI

A Serial Peripheral Interface (SPI) controller is built-in GPCE063A to facilitate communicating with other devices and components. There are four control signals on SPI - SPICS (IOA12), SPICK (IOA13), SDI (IOA14), and SDO (IOA15).





6.14. Audio Algorithm

The following speech types can be used in GPCE063A: PCM, SACM_S200, SACM_S480, SACM_S530, SACM_S720, SACM_A1600, SACM_A1601, SACM_A3600, SACM_DVR520, SACM_DVR1600, SACM_DVR3200, and SACM_DVR4800. For melody synthesis, GPCE063A supports SACM_MS01 (FM) and SACM_MS02 (wave-table) synthesizers.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 4.0V
PortA/B Pad Supply Voltage	V_{IO}	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see DC Electrical Characteristics.

7.2. DC Characteristics (VDD = 3.3V, VDDIO = 4.5V (PortA & B), T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.7	3.3	3.6	V	-
Operating Current	I_{OP}	-	25	-	mA	F_{OSC} = 49.152MHz, AD, DAC disable, no load
Standby Current	I_{STB}	-	-	2.0	μA	Disable 32KHz crystal
				6.0	μA	Enable 32KHz,Disable PLL(F_{OSC})
Input High Level	V_{IH}	0.7VDD_{IO}	-	-	V	-
Input Low Level	V_{IL}	-	-	0.3VDD_{IO}	V	-
Output DAC Current (AUD1, AUD2)	I_{AUD}	-	-4	-	mA	For one channel DAC
Output High Current	I_{OH}	-	-10	-	mA	V_{OH} = 0.9VDDIO
Output Low Current (PA[3:0], PB[7:0])	I_{OL}	-	13	-	mA	V_{OL} = 0.1VDDIO
Output Low Current (PA[7:4])	I_{OL}	-	30	-	mA	-
Input Pull-Low Resister (PA15:0, PB15:8)	R_{PL}	-	110	-	KΩ	V_{IN} = VDDIO
Input Pull-Low Resister (PB[7:0])	R_{PL}	-	900	-	KΩ	V_{IN} = VDDIO
Input Pull-High Resister (PA15:0, PB15:0)	R_{PH}	-	100	-	KΩ	V_{IN} = VSS

7.3. DC Characteristics (VDD = 3.3V, VDDIO = 3.3V (PortA & B), T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.7	3.3	3.6	V	-
Operating Current	I_{OP}	-	25	-	mA	F_{OSC} = 49.152MHz, AD, DAC disable, no load
Standby Current	I_{STB}	-	-	2.0	μA	Disable 32KHz crystal
				6.0	μA	Enable 32KHz,Disable PLL(F_{OSC})
Input High Level	V_{IH}	0.7VDD_{IO}	-	-	V	-
Input Low Level	V_{IL}	-	-	0.3VDD_{IO}	V	-
Output DAC Current (AUD1, AUD2)	I_{AUD}	-	-3.0	-	mA	For one channel DAC

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Output High Current	I_{OH}	-	-5.0	-	mA	V_{OH} = 0.9VDDIO
Output Low Current (PA[3:0], PB[7:0])	I_{OL}	-	7	-	mA	V_{OL} = 0.1VDDIO
Output Low Current (PA[7:4])	I_{OL}	-	17	-	mA	-
Input Pull-Low Resister (PA15:0, PB15:8)	R_{PL}	-	190	-	KΩ	V_{IN} = VDDIO
Input Pull-Low Resister (PB[7:0])	R_{PL}	-	1400	-	KΩ	V_{IN} = VDDIO
Input Pull-High Resister (PA15:0, PB15:0)	R_{PH}	-	160	-	KΩ	V_{IN} = VSS

7.4. ADC Characteristics (AVDD = 3.3V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
ADC LINE_IN Input Voltage Range from IOB[7:0]	VINL (Note 1)	VSS-0.3	-	AVDD+0.3	V
ADC Microphone Input Voltage Range	VINM	VSS-0.3	-	AVDD+0.3	V
Resolution of ADC	RESO	-	-	12	bits
Signal-to-Noise Plus Distortion of ADC from Line in	SINAD (Note 4)	-	56	-	dB
Effective Number of Bit	ENOB (Note 5)	8.0	9.0	-	bits
Integral Non-Linearity of ADC	INL	-	±3.0	-	LSB (Note 3)
Differential Non-Linearity of ADC	DNL (Note 6)	-	±1	-	LSB
AD Conversion Rate	F_{CONV}	-	-	F_{CPU}/256	Hz
Microphone Amplifier Gain (Note 7)	A_{MIC}	-	-	42	dB

Note1: Internal protection diodes clamp the analog input to AVDD and VSS. These diodes allow the analog input to swing from (VSS-0.3V) to (AVDD+0.3V) without causing damage to the devices.

Note2: LSB means Least Significant Bit. With VINL = 2.6V, 1LSB = 2.6V/2^12 = 0.635mV.

Note3: The SINAD testing condition at VINLp-p = 0.8*AVDD, F_{CONV} = Fcpu/512 = 49MHz/256 = 192KHz, Fin=1.0KHz Sine waves at AVDD = 3.0V from the IOB [7:0] input.

Note4: ENOB = (SINAD-1.76)/6.02.

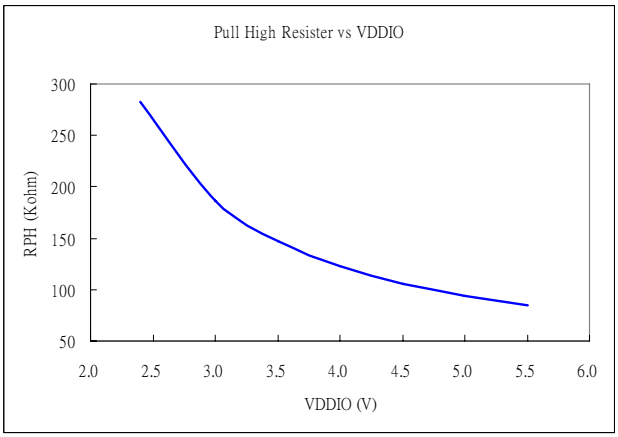
Note5: The ADC of GPCE063A can guarantee 12 bits no missing code.

Note6: The microphone amplifier maximum gain = 15 * (60K/(1.5K+REXT) V/V. The REXT is external resistor between OPI and MICOUT. The gain is 132V/V (=42dB) when REXT is 5.1K.

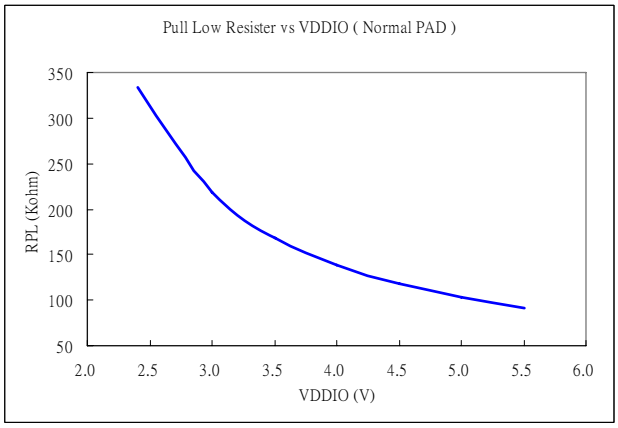
7.5. DAC Characteristics (AVDD = 3.3V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Resolution of DAC	RESO	-	-	14	bit
Signal to Noise Ratio of DAC	SNR	-	84	-	dB
Sample Rate	F_S	-	-	400K	Hz
THD+N at FS	F_{OUT} = 1K Hz	-	-60	-	dB

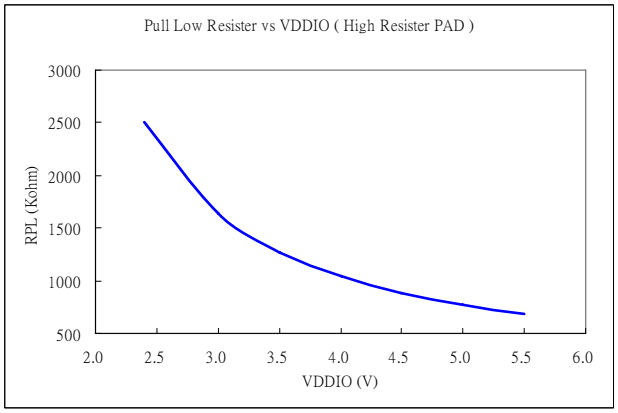
7.6. Pull High Resister and VDDIO



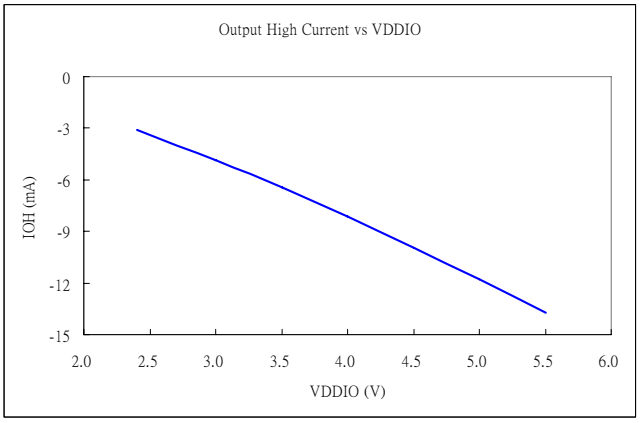
7.7. Pull Low Resister and VDDIO(Normal PAD)



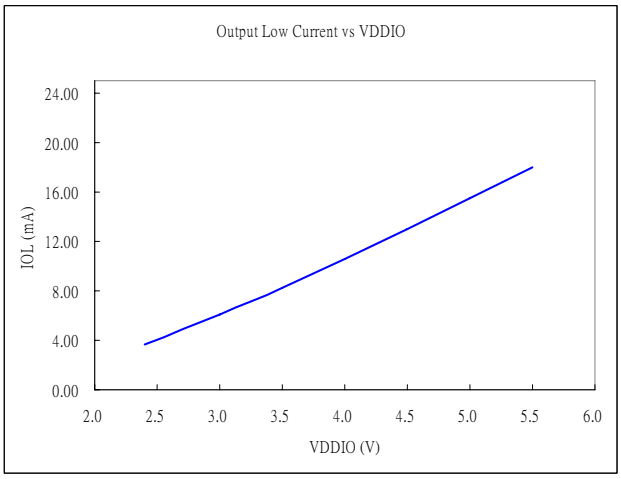
7.8. Pull Low Resister and VDDIO(IOB[7:0] PAD with input high)



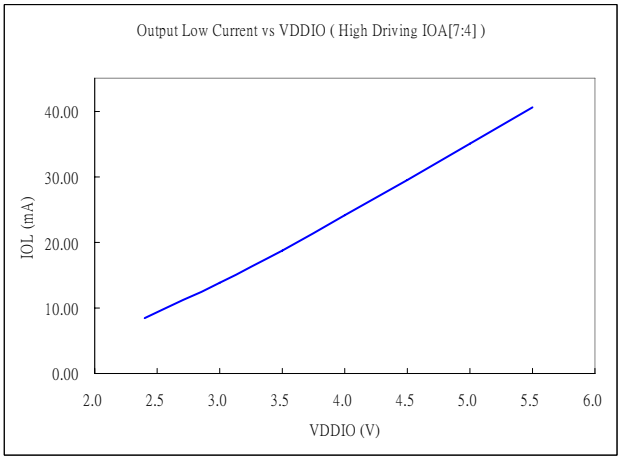
7.9. I/O Output High Current IOH and VDDIO



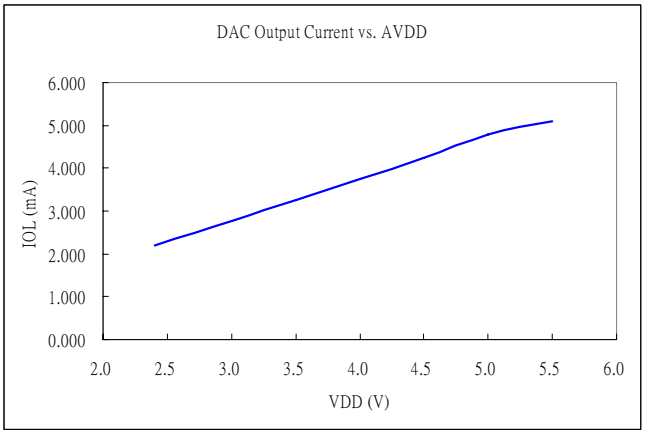
7.10. I/O Output Low Current I_{OL} and VDDIO(Normal Pad)



7.11. I/O Output Low Current I_{OL} and VDDIO(High driving pad)

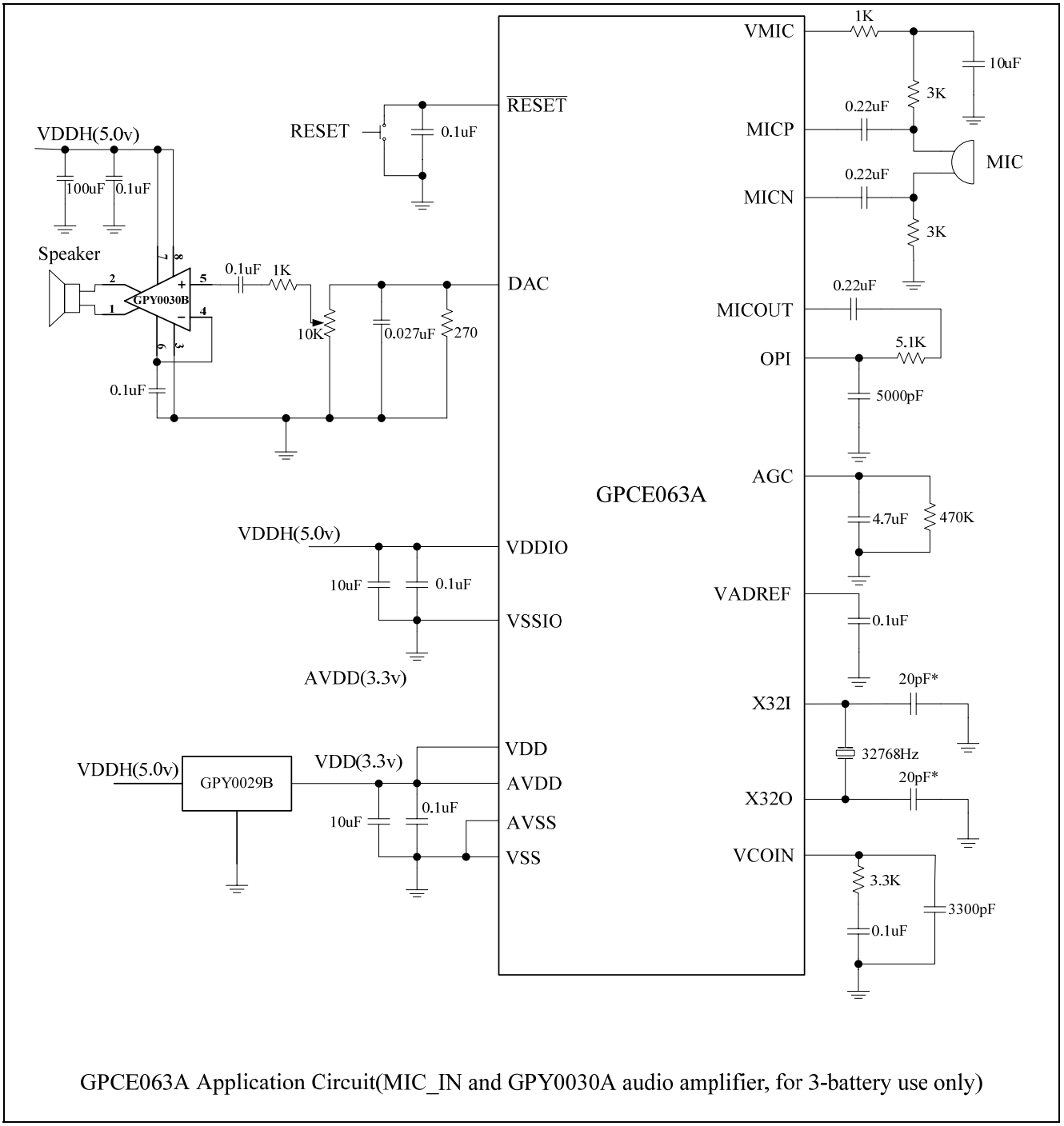


7.12. DAC Output Current IOL and AVDD



8. APPLICATION CIRCUITS

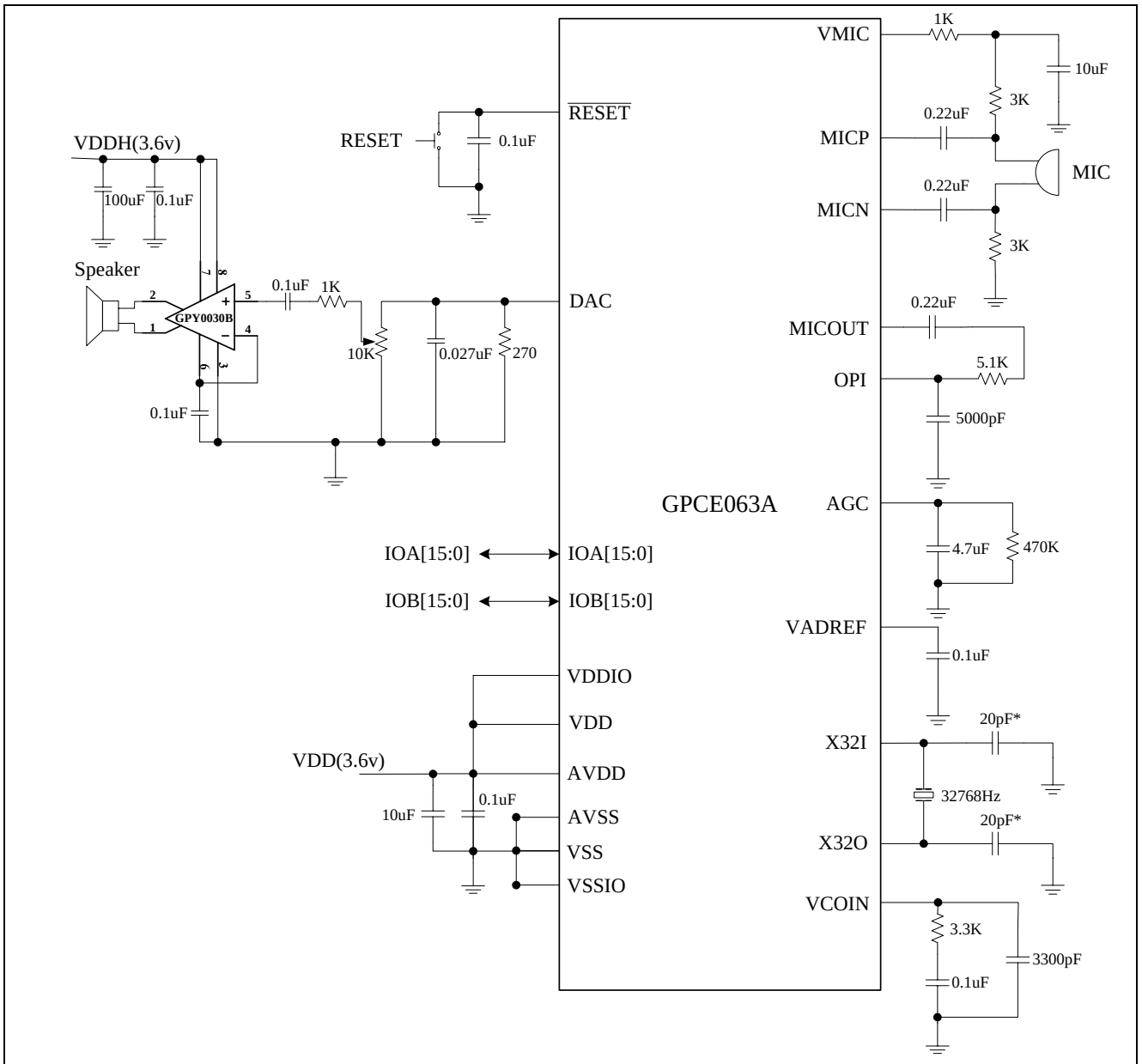
8.1. Application Circuit (1)



GPCE063A Application Circuit(MIC_IN and GPY0030A audio amplifier, for 3-battery use only)

Note*: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~35K and CL1=CL2 =20~30pF (including PCB parasitic loading, for example, user should apply additional 14~24pF on X32I and X32O if PCB parasitic loading is 6pF)

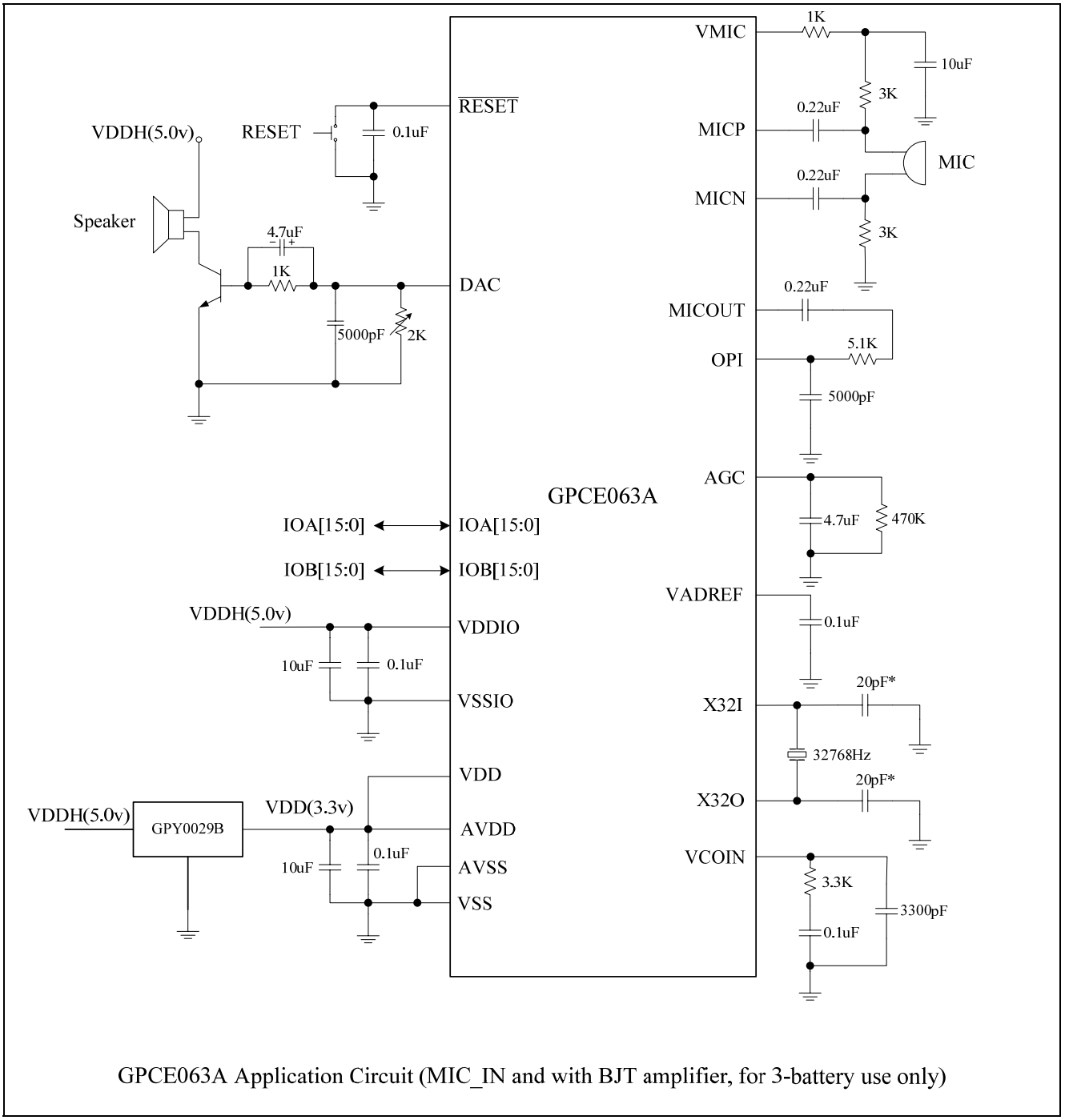
8.2. Application Circuit (2)



GPCE063A Application Circuit (MIC_IN and GPY0030A audio amplifier, for 2-battery use only)

Note*: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~35K and CL1=CL2 =20~30pF (including PCB parasitic loading, for example, user should apply additional 14~24pF on X32I and X32O if PCB parasitic loading is 6pF)

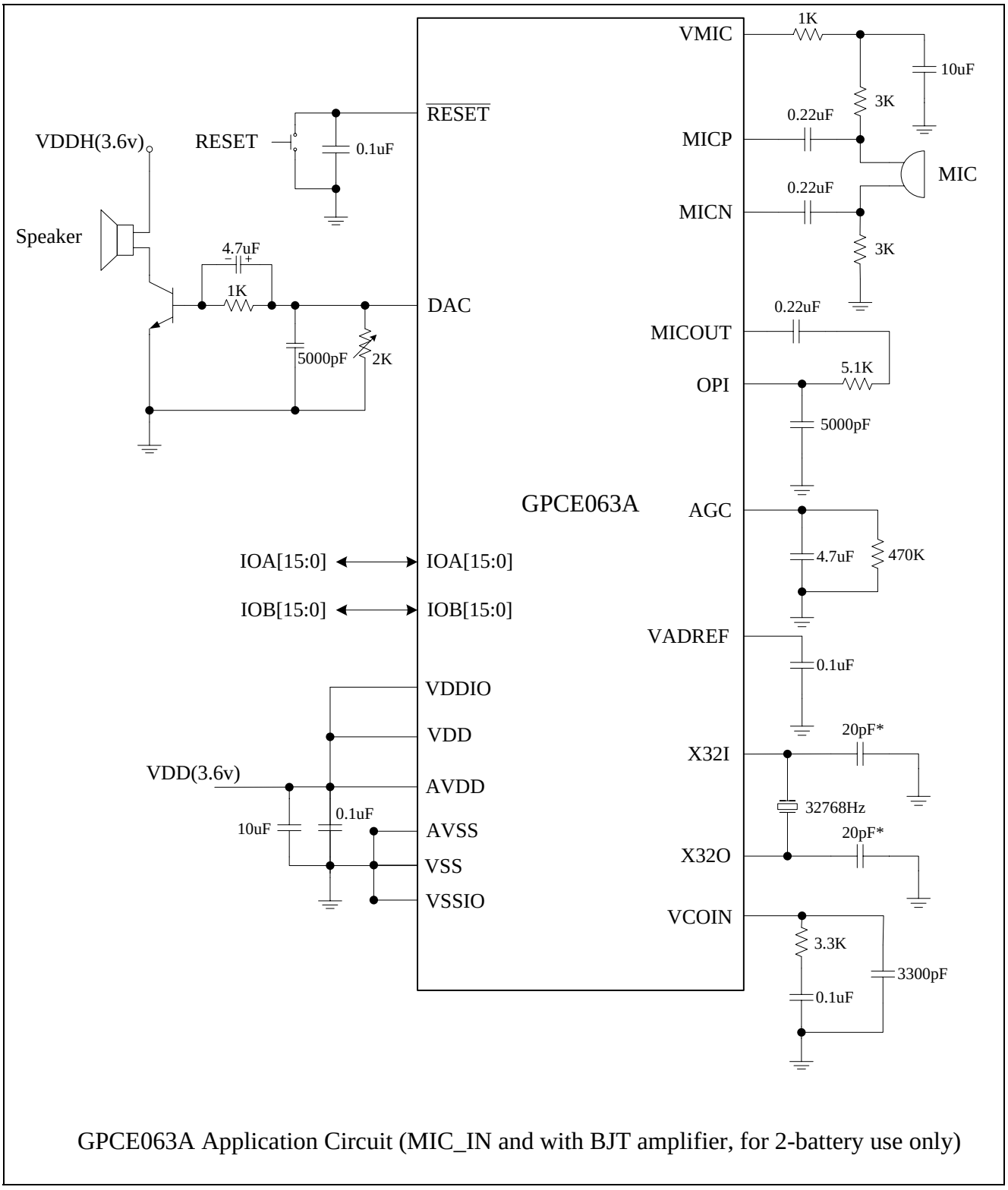
8.3. Application Circuit (3)



GPCE063A Application Circuit (MIC_IN and with BJT amplifier, for 3-battery use only)

Note*: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~35K and CL1=CL2 =20~30pF (including PCB parasitic loading, for example, user should apply additional 14~24pF on X32I and X32O if PCB parasitic loading is 6pF)

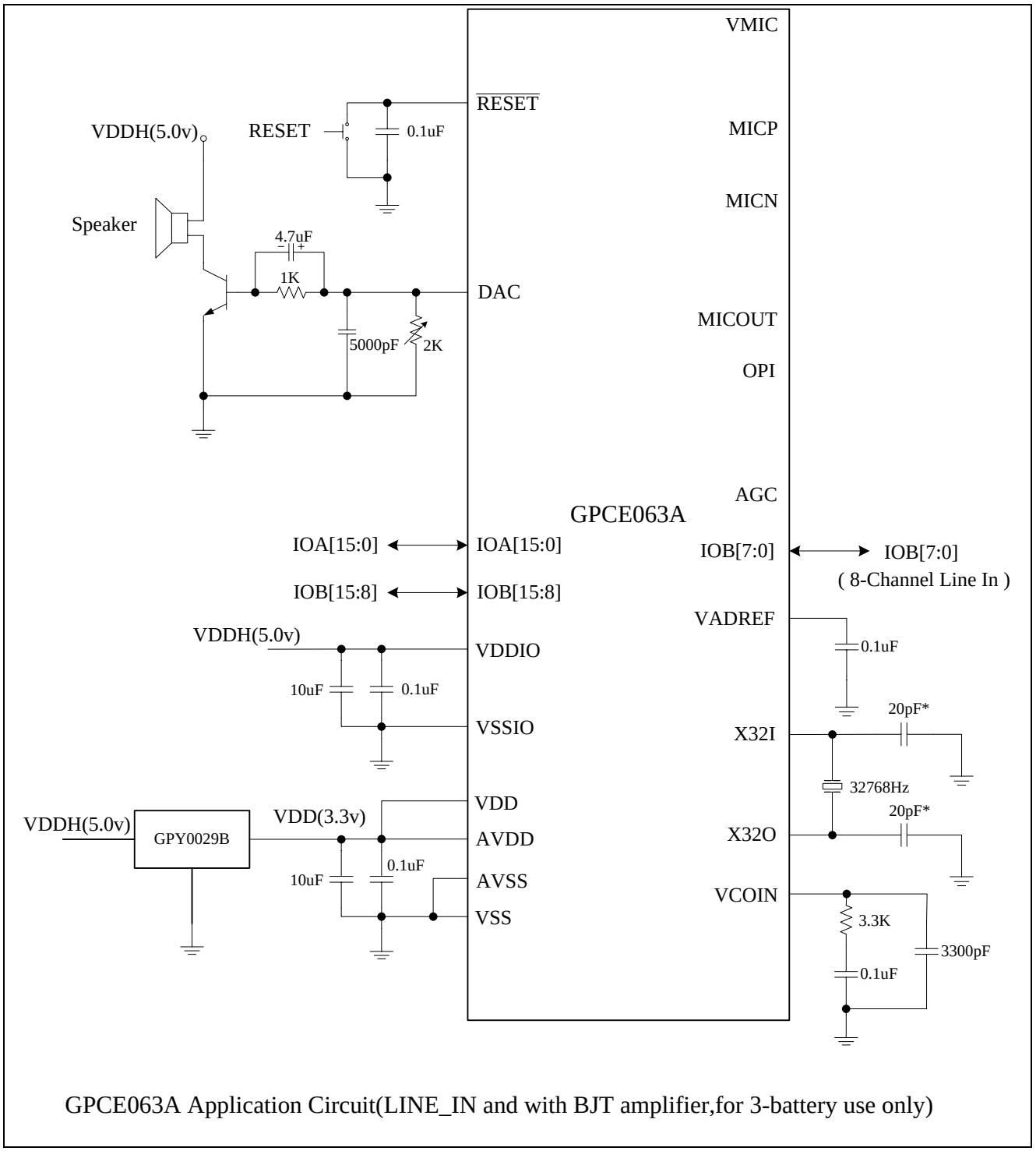
8.4. Application Circuit (4)



GPCE063A Application Circuit (MIC_IN and with BJT amplifier, for 2-battery use only)

Note*: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~35K and CL1=CL2 =20~30pF (including PCB parasitic loading, for example, user should apply additional 14~24pF on X32I and X32O if PCB parasitic loading is 6pF)

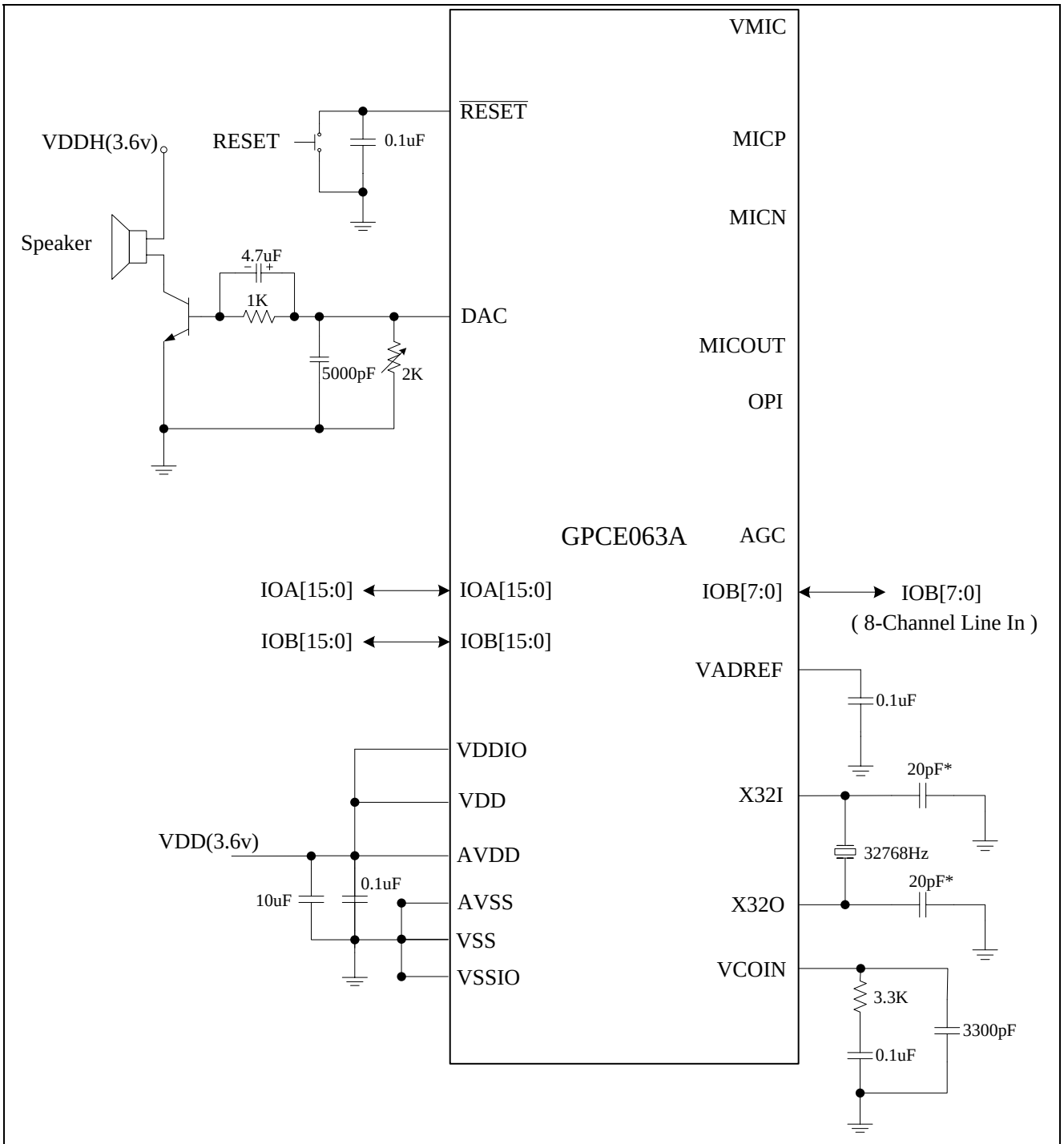
8.5. Application Circuit (5)



GPCE063A Application Circuit(LINE_IN and with BJT amplifier,for 3-battery use only)

Note*: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~35K and CL1=CL2 =20~30pF (including PCB parasitic loading, for example, user should apply additional 14~24pF on X32I and X32O if PCB parasitic loading is 6pF)

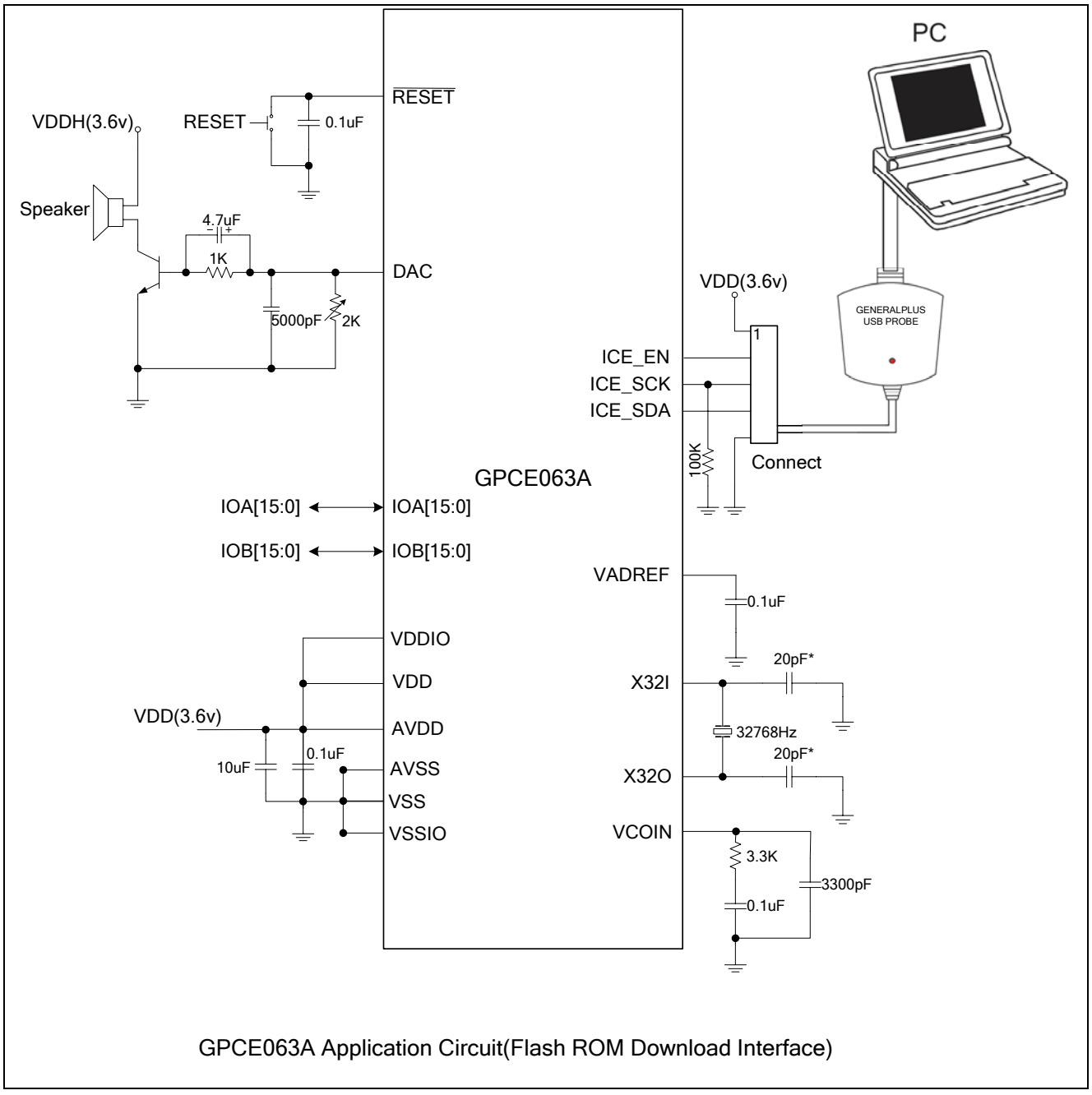
8.6. Application Circuit (6)



GPCE063A Application Circuit(LINE_IN and with BJT amplifier,for 2-battery use only)

Note*: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~35K and CL1=CL2 =20~30pF (including PCB parasitic loading, for example, user should apply additional 14~24pF on X32I and X32O if PCB parasitic loading is 6pF)

8.7. Application Circuit (7)



GPCE063A Application Circuit(Flash ROM Download Interface)

Note*: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~35K and CL1=CL2 =20~30pF (including PCB parasitic loading, for example, user should apply additional 14~24pF on X32I and X32O if PCB parasitic loading is 6pF)

9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPCE063A-NnnV-C	Chip form
GPCE063A-NnnV-QL02x	Halogen Free Package

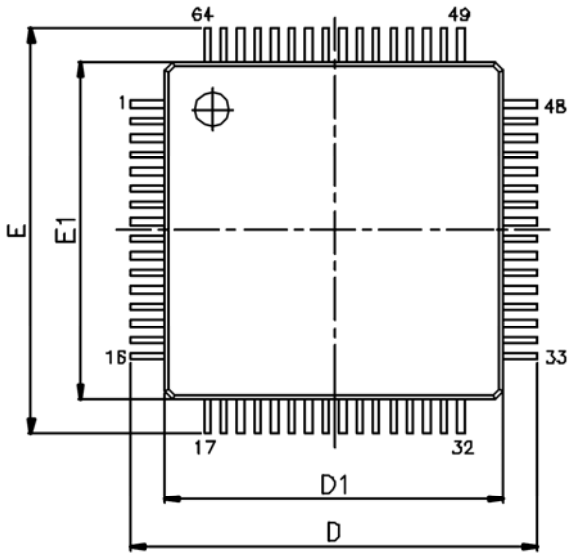
Note1: Code number is assigned for customer.

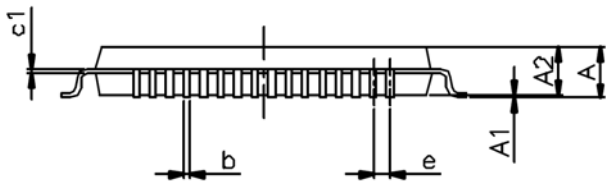
Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

9.2. Package Information

LQFP 64 Outline Dimensions





Symbol	Dimension in mm		
	Min.	Typ.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c1	0.09	-	0.16
D	12.00		
D1	10.00		
E	12.00		
E1	10.00		
e	0.50 BSC.		

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11. REVISION HISTORY

Date	Revision #	Description	Page
Oct 04, 2013	1.8	1. Add COMAIR logo to the cover page 2. update X32K crystal's capacitance note in application circuit	
Nov. 18, 2011	1.7	Modify 8.7 Application Circuit (7).	26
Jan. 07, 2011	1.6	Modify 6.5.2 Low Voltage Reset and remove the timing diagram	11
Oct. 13, 2010	1.5	Modify 3.FEATURES.	4
Dec. 11, 2009	1.4	1. Modify 5.3 GPCE063A PIN Map. 2. Modify 6.9.1 IO PWM. 3. Modify 6.12 ADC (Analog to Digital Converter) / DAC.	8 14 15
Oct. 02, 2009	1.3	1. Modify 5.1. GPCE063A Pad Assignment. 2. Add 5.2. GPCE064A Pad Assignment. 3. Modify 5.3 GPCE063A Pin Map. 4. Add 5.4 GPCE064A Pin Map.	6 7 8 9
Aug. 17, 2009	1.2	1. Modify 3.FEATURES. 2. Modify 8.APPLICATION CIRCUITS.	4 18-24
Dec. 16, 2008	1.1	Modify the Package Information in section 9.2.	25
Aug. 01, 2008	1.0	Release to 1.0	27
Apr. 08, 2008	0.1	Original	15