FAN1654

1.5A LDO, DDR Bus Termination Regulator

Features

- Sinks and sources 1A continuous, 1.5A peak
- -40°C to +125°C Operating Range
- Load regulation: (VDDQ/2) ± 40mV
- 5mA VREF buffer tracks VTT
- On-chip thermal limiting
- Power-enhanced eTSSOP™-16 package
- Low Current Shutdown Mode
- Output Short Circuit Protection

Applications

- DDR terminators

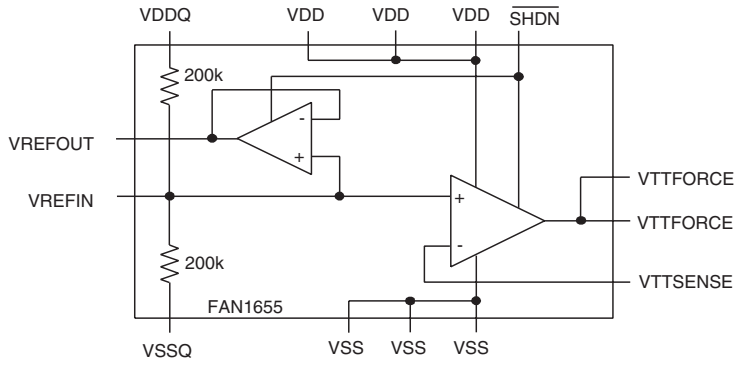
Description

The FAN1654 is a low-cost bi-directional LDO specifically designed for terminating DDR memory bus. It can both sink and source up to 1A continuous, 1.5A peak, providing enough current for most DDR applications. Load regulation meets the JEDEC spec, VTT = (VDDQ/2) ± 40mV.

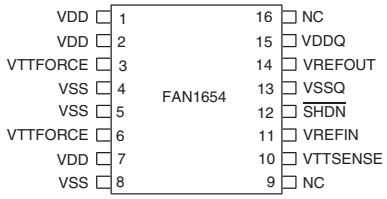
The FAN1654 includes a buffered reference voltage capable of supplying up to 5mA current. On-chip thermal limiting provides protection against a combination of power overload and ambient temperature that would create an excessive junction temperature. A shutdown input puts the FAN1654 into a low power mode for laptop computer applications.

The FAN1654 regulator is available in a power-enhanced eTSSOP™-16 package, and the standard SOIC-14

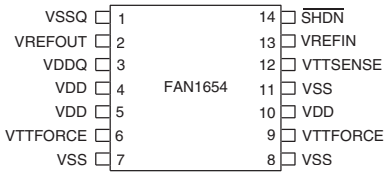
Block Diagram



Pin Assignments



16-Lead Plastic eTSSOP-16
θ_{JC} = 4˚C/W*
*With package power slug soldered to 0.5 square inch copper area over backside ground plane of internal power plane



14-Lead Plastic SOIC
θ_{JC} = 37˚C/W, θ_{JA} = 88˚C/W

Pin Definitions

Pin Number*	Pin Name	Pin Function Description
1, 2, 7 (4, 5, 10)	VDD	**VDD.** Input power for the LDO.
3, 6 (6, 9)	VTTFORCE	**VTT Force Output.**
4, 5, 8 (7, 8, 11)	VSS	**Power Ground.**
10 (12)	VTTSENSE	**VTT Sense**. Feedback for remote sense of the VTT voltage.
11 (13)	VREFIN	**VREFIN**. Alternative input for direct control of VTTOUT and VREFOUT.
12 (14)	$\overline{\text{SHDN}}$	**Shutdown.** This active low shutdown turns off both VTT and VREFOUT. This pin has an internal pull-down, and must be externally driven high for the IC to be on.
13 (1)	VSSQ	**Signal Ground.**
14 (2)	VREFOUT	**Buffered Voltage Reference Output.**
15 (3)	VDDQ	**VDDQ Input.** Attach this pin to the VDDQ supply to generate VTT and VREFOUT.
9,16	NC	No Internal Connection

* Pin Numbers in brackets are for the SOIC-14 package

Typical Application

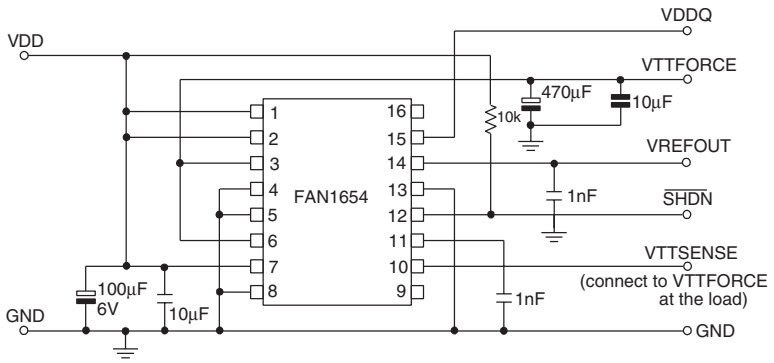


Figure 1. (eTSSOP pinout shown)

Typical Performance Characteristics

Quiescent Current vs. Temperature

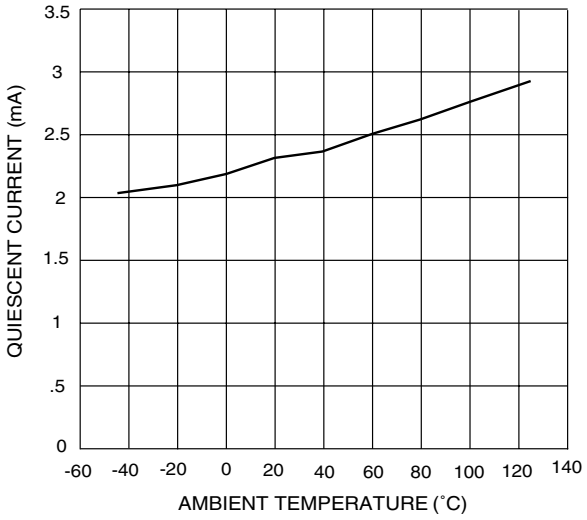


Figure 2

V_{REF} Output Change vs. I_{REF}

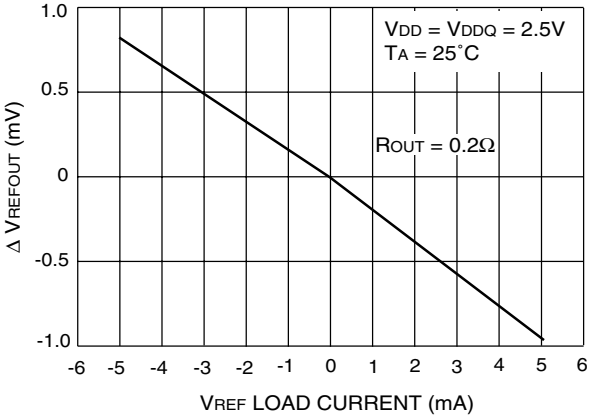


Figure 3

V_{TT} Load Current

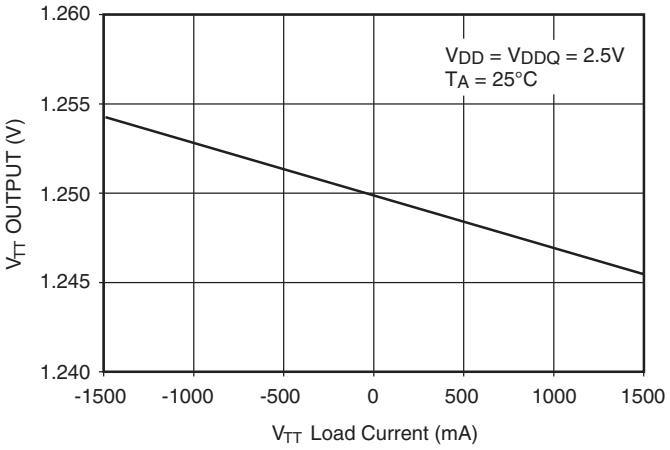


Figure 4

Absolute Maximum Ratings

Supply Voltage VDD, VDDQ	6V
Junction Temperature, T_J	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C
Power Dissipation, P_D	1.4W

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VDD		2.3	2.5	3.6	V
Supply Voltage VDDQ		2.2	2.5	3.0	V
Ambient Operating Temperature		-40		125	°C
VREFIN		1.1	1.25	1.5	V

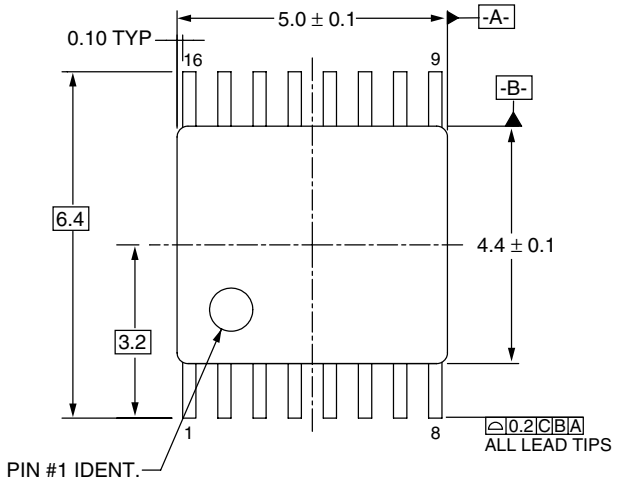
Electrical Characteristics

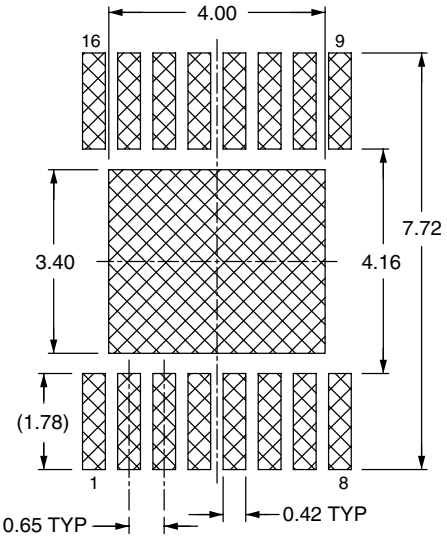
(VDD = VDDQ = 2.5V ± 0.2V, and T_A = 25°C using circuit in Figure 1, unless otherwise noted.)
The • denotes specifications which apply over the specified operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
VTT Output Voltage	I_{OUT} = 0A, VREFIN = open					
	VDDQ = 2.3V	•	1.135	1.150	1.165	V
	VDDQ = 2.5V	•	1.235	1.250	1.265	V
	VDDQ = 2.7V	•	1.335	1.350	1.365	V
	I_{OUT} = ±1A, VREFIN = open					
	VDDQ = 2.3V		1.110	1.150	1.190	V
	VDDQ = 2.5V		1.210	1.250	1.290	V
	VDDQ = 2.7V		1.310	1.350	1.390	V
VTT Output Slew Rate	Cload = 10µF			0.1		V/µsec
VTT Leakage Current	$\overline{SHDN}$ = 0V	•	-50		50	µA
VTT Current Limit				±2		A
VREFIN Input Impedance				100		KΩ
VREFOUT Output Voltage	No load					
	VREFIN = 1.150V	•	1.145	1.150	1.155	V
	VREFIN = 1.250V	•	1.245	1.250	1.255	V
	VREFIN = 1.350V	•	1.345	1.350	1.355	V
VREFOUT Output Current	VDDQ = 2.3V	•	-5		5	mA
VREFOUT Leakage Current	$\overline{SHDN}$ = 0V	•	-10		10	µA
$\overline{SHDN}$ Logic High		•	1.667			V
$\overline{SHDN}$ Logic Low		•			0.800	V
IDD Supply Current	No load, $\overline{SHDN}$ = 2.7V	•		3	10	mA
VDDQ Leakage Current	$\overline{SHDN}$ = 0V	•		6	10	µA
VDD Leakage Current	$\overline{SHDN}$ = 0V	•		3	50	µA
$\overline{SHDN}$ Input Current	$\overline{SHDN}$ = 2.7V	•		50	75	µA
Over-Temperature Shutdown				155		°C
Over-Temperature Hysteresis				30		°C

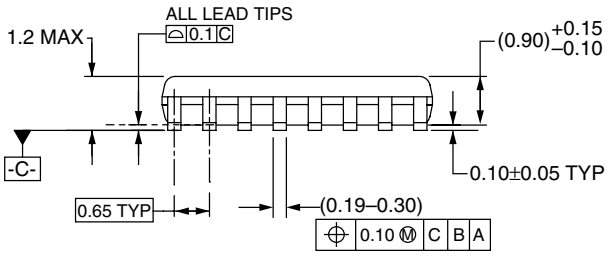
Mechanical Dimensions

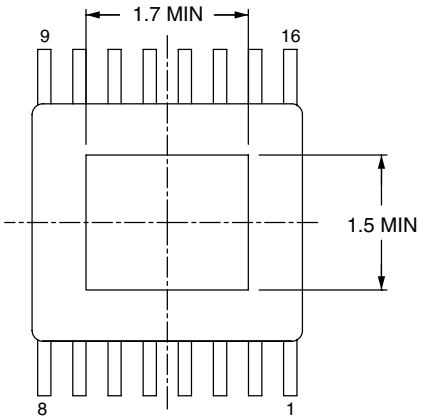
16 Lead eTSSOP



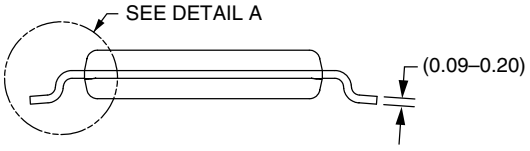


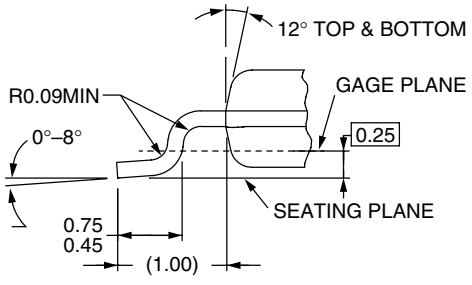
LAND PATTERN RECOMMENDATION





BOTTOM VIEW





DETAIL A

NOTES:

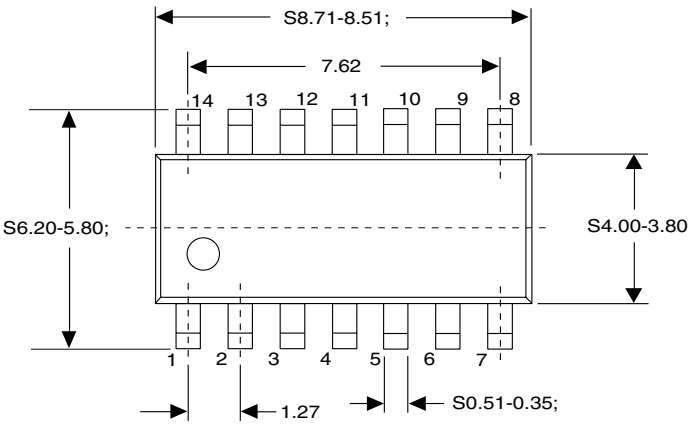
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ABT, DATED 10/97.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND THE BAR EXTENSIONS.
D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

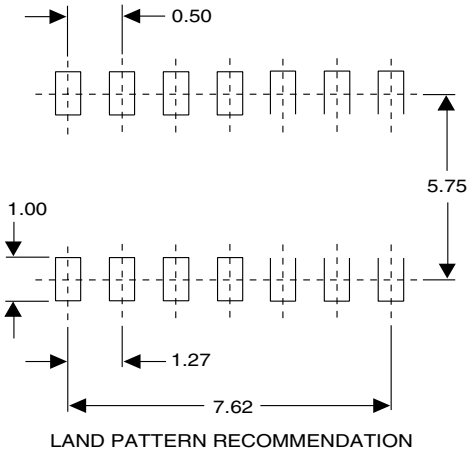
Mechanical Dimensions

14-Lead SOIC

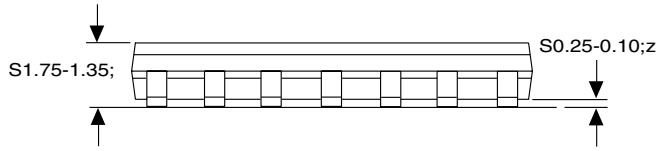
NOTES:

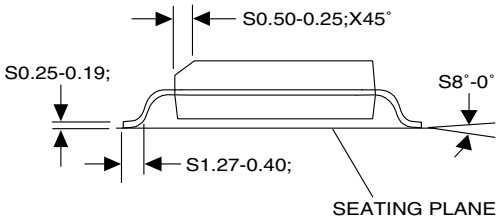
1. This package conforms to JEDEC MS-012, variation AB, ISSUEC dated May, 1990.
2. All dimensions are in millimeters
3. Standard lead finished
   200 microinches / 5.08 microns min.
   Lead/Tin (solder) oncopper





LAND PATTERN RECOMMENDATION





Ordering Information

Product Number	Package
FAN1654MTF	eTSSOP-16
FAN1654MTFX	eTSSOP-16 in tape and reel
FAN1654M	SOIC-14
FAN1654MX	SOIC-14 in tape and reel

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