0.01GHz – 20 GHz Low Phase Noise Amplifier APM-7099

1. Device Overview

1.1 General Description

The APM-7099 is a broadband distributed, low phase noise driver amplifier designed to provide a saturated +25 dBm output power with low DC power consumption. This amplifier uses GaAs HBT technology for low phase noise, and is optimized to drive our NLTL multiplier line. It can also provides sufficient power to drive the LO port of an S-diode mixer from 10 MHz to 15 GHz or of an H or L diode mixer from 10 MHz to 20 GHz. This amplifier can be operated with a variety of bias conditions for both low power and high-power applications.

PA Module

Bare Die

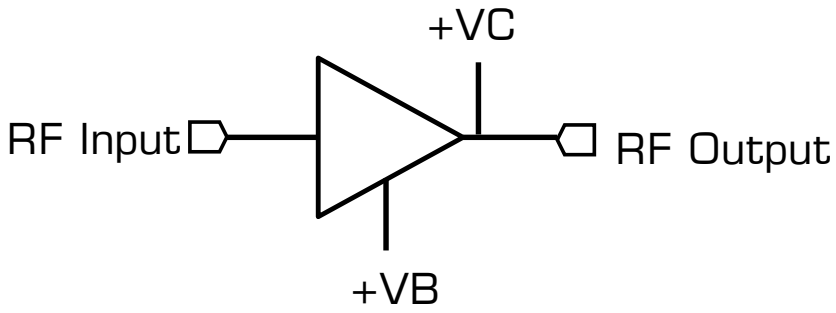
1.2 Features

- -167 dBc/Hz phase noise at 10 kHz offset frequency
- +25 dBm output power
- Low DC power consumption
- Positive-only biasing
- No sequencing required
- Unconditionally stable
- .s2p S-Parameters: APM-7099CH.s2p

1.3 Applications

- Mobile test and measurement equipment
- Radar and satellite communications
- 5G Transceivers
- Driver amplifier for S, H, and L – diode mixers
- NLTL Driver
- Suitable as a T3 driver

1.4 Functional Block Diagram



1.5 Part Ordering Options[1]

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
APM-7099CH	Wire Bondable Die	Bare Die	**RoHS**	Active	EAR99
APM-7099PA	Connectorized Module	PA	**RoHS**	Active	EAR99

[1] Refer to our website for a list of definitions for terminology presented in this table.

Table of Contents

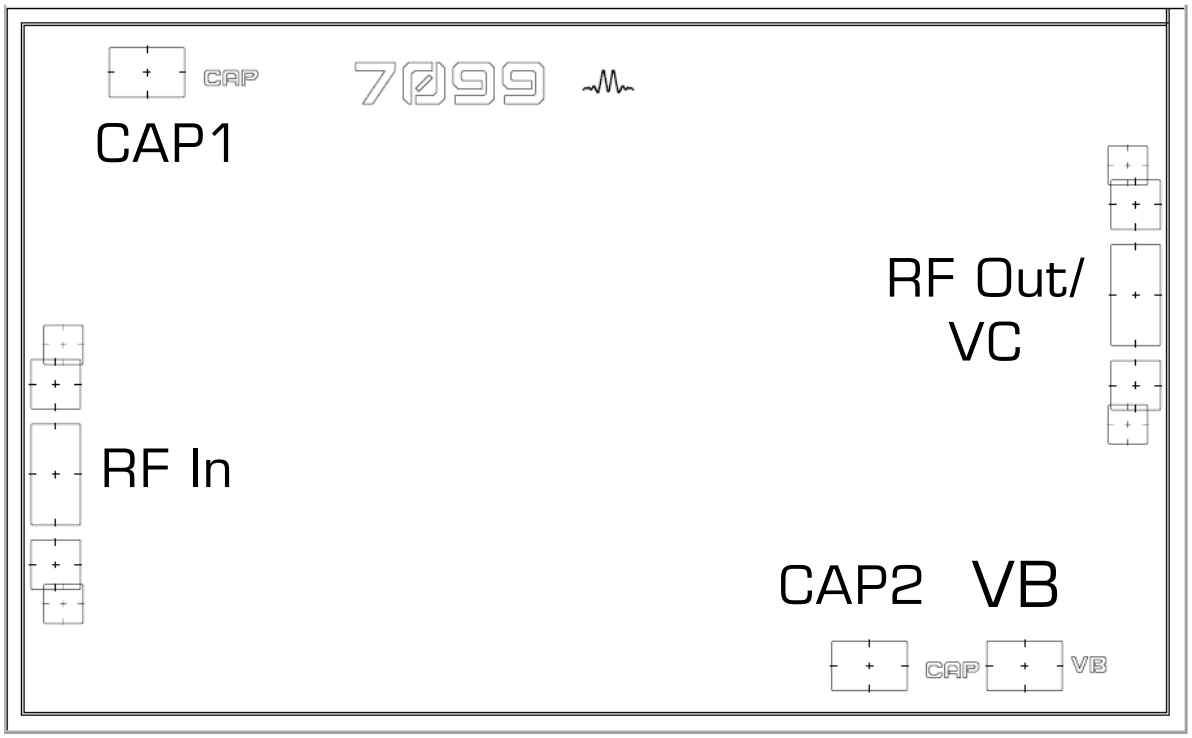
Revision History

Revision Code	Revision Date	Comment
-	October 2020	Datasheet Initial Release
A	March 2021	Updated maximum input power and min specs

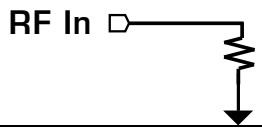
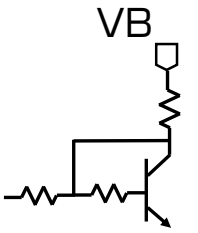
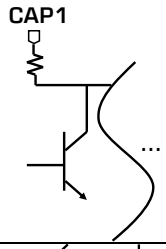
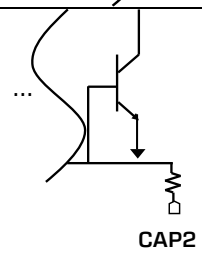
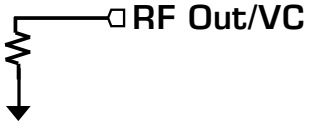
2. APM-7099 Port Configurations and Functions

2.1 APM-7099CH Port Diagram

A port diagram of the APM-7099CH is shown below.

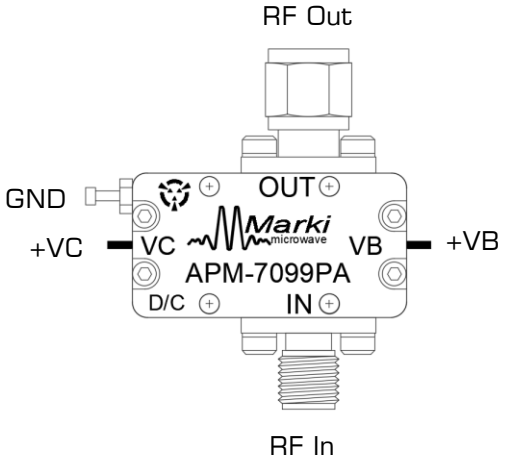


2.2 APM-7099CH Port Functions

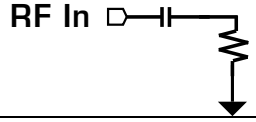
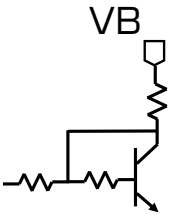
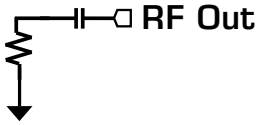
Port	Function	Description	Equivalent Circuit for Package
RF In	RF Input	This is the RF Input port of the amplifier die. It is RF matched to 50 Ω, and is DC coupled. RF input pad is GSG with 175 µm pitch.	
VB	Current Mirror Bias Port	Port VB is the DC voltage bias pad for the current mirror that control the collector current supplied to the amplifier. Larger voltages result in a higher current draw through port RF Out/VC, effectively functioning as a gain control pin of the amplifier. See section 3.6 for performance at different bias conditions.	
CAP1	Off-Chip Cap Port 1	CAP1 is a pad that allows the user to attach additional off chip bypass capacitance to the VC supply line. A 0.1µF capacitor is recommended	
CAP2	Off-Chip Cap Port 2	CAP2 is a pad that allows the user to attach additional off chip bypass capacitance to provide adequate AC grounding termination. A 0.1µF capacitor is recommended	
RF Out/VC	RF Output and Collector Supply Port	This is the amplifier die's RF Output and positive VC supply voltage port. It is RF matched to 50 Ω and is DC coupled. RF output pad is GSG with 175 µm pitch. Must have less than 7:1 VSWR when operating with voltage larger 8V on VC	
GND	Ground	Backside of the IC must be connected to a DC/RF ground with high thermal and electrical conductivity.	

2.3 APM-7099PA Port Diagram

A port diagram of the APM-7099PA is shown below.



2.4 APM-7099PA Port Functions

Port	Function	Description	Equivalent Circuit for Package
RF In	RF Input	This is the RF Input port of the amplifier die. It is RF matched to 50 Ω and has built-in DC blocking capacitors.	
VC	Collector DC Supply Port	Port VC is the DC voltage supply for that supplies the amplifier's collector current. It is connected internally through the amplifier die's RF output port.	
VB	Base Current Mirror Bias Port	Port VB is the DC voltage bias for the current mirror that controls collector current supplied to the amplifier. Larger voltages result in a higher current draw through port VC, effectively functioning as a gain control pin of the amplifier. See section 3.6 for performance at different bias conditions.	
RF Out	RF Output	This is the amplifier's RF Output. It is RF matched to 50 Ω and has built-in DC blocking capacitors. Must have less than 7:1 VSWR when operating with voltage larger 8V on VC	
GND	Ground	Housing or outside of the coaxial cables must be connected to a DC/RF ground potential with high thermal and electrical conductivity.	

3. Specifications

3.1 Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may become inoperable or have a reduced lifetime.

Parameter	Maximum Rating	Units
Collector Positive Bias Voltage (VC)	9	V
Positive Bias Current (Ic)	225	mA
Positive DC Current Mirror Voltage (VB)	9	V
RF Input Power (10 MHz – 3GHz)	+12	dBm
RF Input Power (3 GHz – 20 GHz)	+15	dBm
Output Load VSWR	7:1	-
Operating Temperature	-40 to +85	°C
Storage Temperature	-65 to +150	°C
θ_{JC}, Junction to Ambient Thermal Resistance	56	°C/W
Max Junction Temperature for MTTF > 1E6 hours	125	°C
Max Power Dissipation for MTTF of 1E6 hours at 85°C Baseplate Temperature	709	mW

3.2 Package Information

Parameter	Details	Rating
ESD	Human Body Model (HBM), per MIL-STD-750, Method 1020	TBD
Weight	APM-7099PA	15.0g

3.3 Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

Recommended Operating Conditions – CH bare die package[2]	Min	Nominal	Max	Units
T_A, Ambient Temperature	-40	+25	+85	°C
Power Supply DC Voltage (VC)	+5	+8	+9	V
Power Supply DC Current (Ic) (No RF Input)[2, 3]	38	72	132	mA
Power Supply DC Current (with RF Input)[4]	-	-	180	mA

Recommended Operating Conditions – PA connectorized module package[5]	Min	Nominal	Max	Units
T_A, Ambient Temperature	-40	+25	+40	°C
Power Supply DC Voltage (VC)	+5	+8	+9	V
Power Supply DC Current (Ic) (No RF Input)[2, 3]	38	72	132	mA
Power Supply DC Current (with RF Input)[4]	-	-	225	mA
Bias Voltage (VB)	+5	+7	+9	V
Input Power for Saturation	+10	+11	+12	dBm

3.4 Sequencing Requirements

There is no sequencing required to power up or power down the amplifier.

Amplifier must have an output load connected during operation.

[2] Ic should be modified by changing bias voltage VB to maintain junction temperature within MTTF target for given operating conditions.
[3] Recommended operating current conditions without RF input applied. Please see typical performance plots on page 12 for relationship between RF input power and DC current draw.
[4] Operation above recommended max power supply DC current will result in reduced MTTF.
[5] Module conditions provided for laboratory conditions. For use in test systems with extended lifetimes bare die operating conditions should be followed.

3.5 Electrical Specifications

The electrical specifications apply at T_A=+25°C in a 50Ω system.

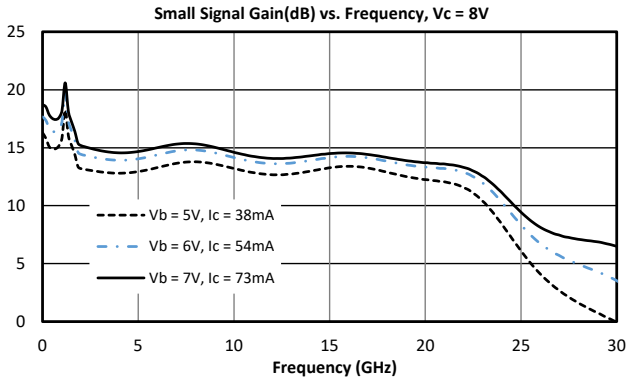
Min and Max limits apply only to our connectorized units and are guaranteed at T_A=+25°C. Die are 100% DC tested and RF tested on a per lot basis

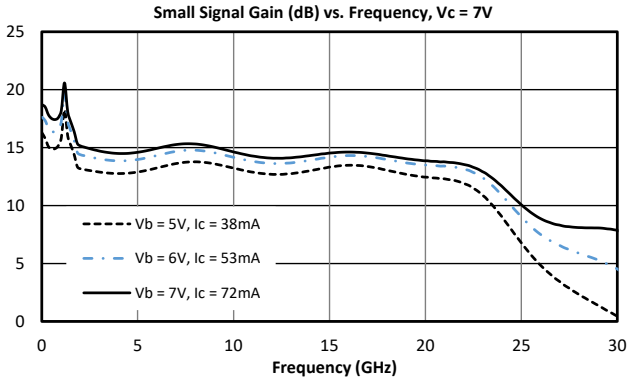
Parameter	Test Conditions	Frequency	Min	Typical	Units
Saturated Output Power[6]	8V/7V bias	10 MHz – 15 GHz	19	25	dBm
		15 GHz – 20 GHz		23	
Small Signal Gain	8V/7V bias, -15 dBm Input Power	10 MHz – 15 GHz	10	14	dB
		15 GHz – 20 GHz		12	
Input Return Loss		10 MHz – 20 GHz		14	
Output Return Loss		10 MHz – 20 GHz		20	
Reverse Isolation		10 MHz – 20 GHz		36	
Noise Figure	-30 dBm Input Power	10 MHz – 20 GHz		5	
Collector Current[7], Ic	8V/6V	-		53	mA
	8V/7V	-		72	
	8V/8V	-		96	
Current Mirror Current, Ib	8V/6V	-		3.4	
	8V/7V	-		4.2	
	8V/8V	-		5	
Input IP3 (IIP3)	8V/7V bias, -15 dBm Input Power	10 MHz – 20 GHz		12	dBm
Output IP3 (OIP3)		10 MHz – 20 GHz		24	
Output P_{1dB}	8V/7V bias	10 MHz – 20 GHz		23	
Input Power for Saturation	8V/7V bias	10 MHz – 20 GHz		+12	dBm
Phase Noise @ 10 kHz Offset	+12 dBm Input power	1 GHz		-167	dBc/Hz

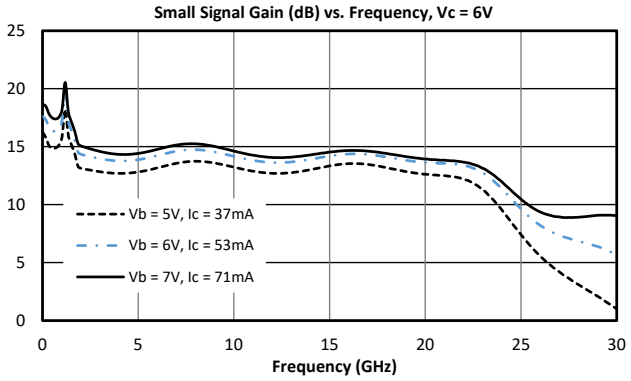
[6] Saturated Output Power specification defined using the APM-7099PA P3dB compression curve shown in section 3.7.

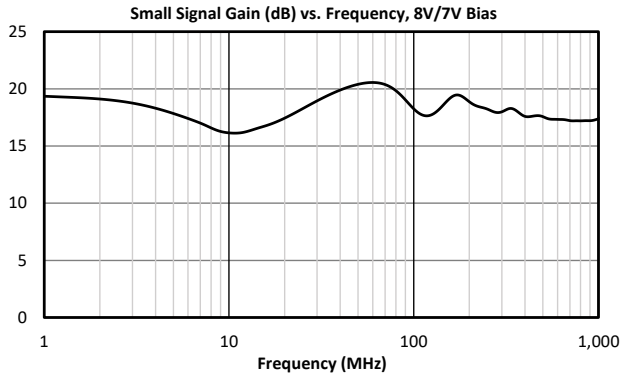
[7] Bias conditions for Ic and Ib tested with no RF input power. See section 3.7 for DC current vs. RF power. Bias conditions presented as VC/VB.

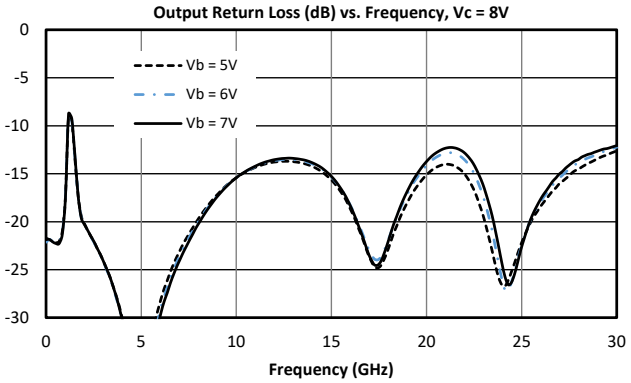
3.6 APM-7099CH Typical Performance Plots

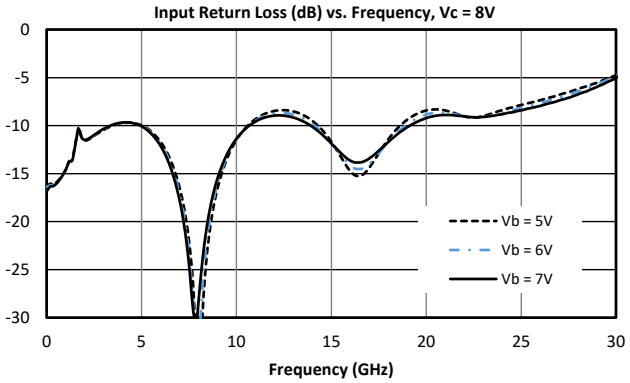


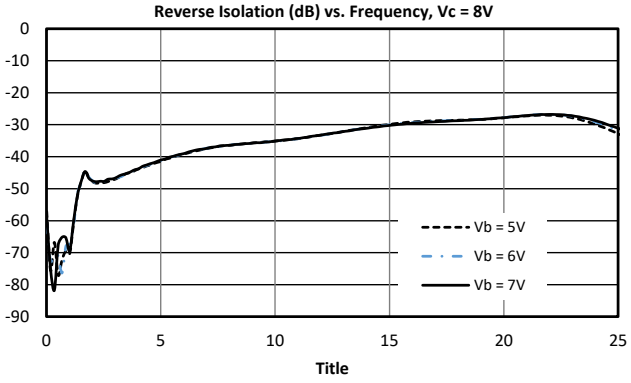






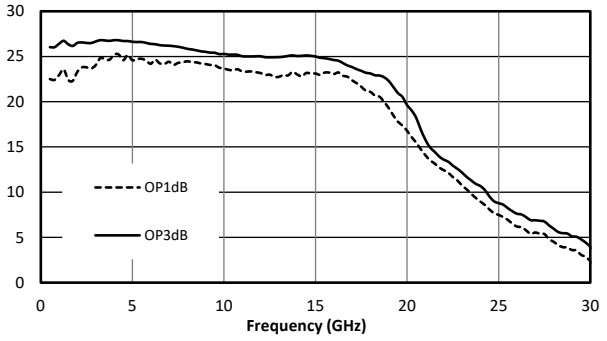




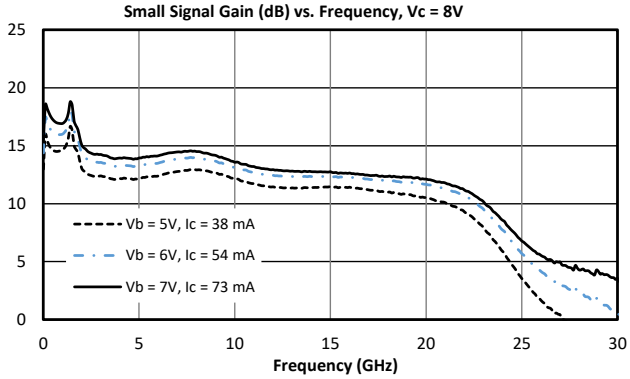


3.7 APM-7099PA Typical Performance Plots

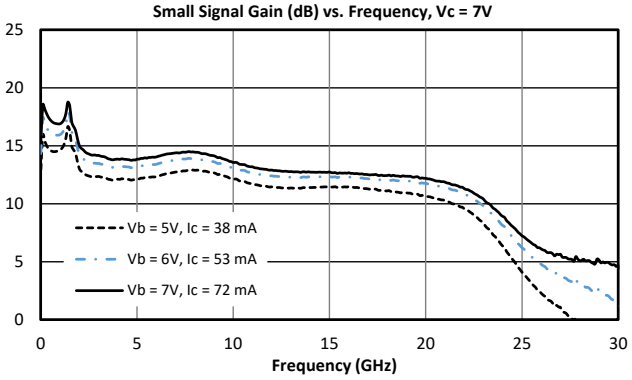
Output Comp. Points (dBm) vs. Frequency, 8V/7V



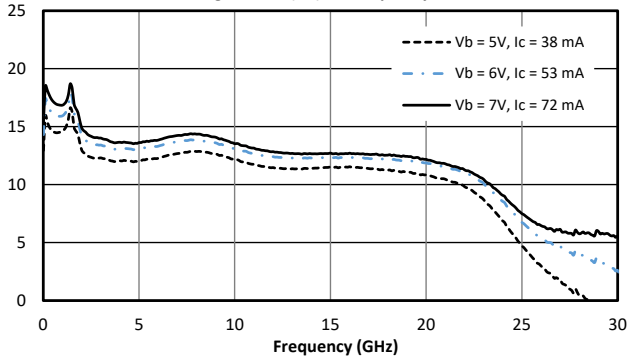
Small Signal Gain (dB) vs. Frequency, Vc = 8V



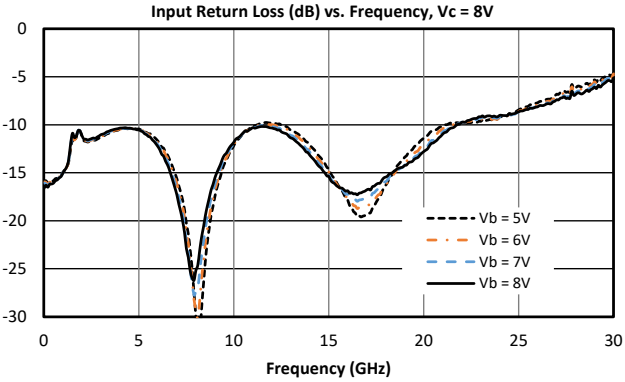
Small Signal Gain (dB) vs. Frequency, Vc = 7V



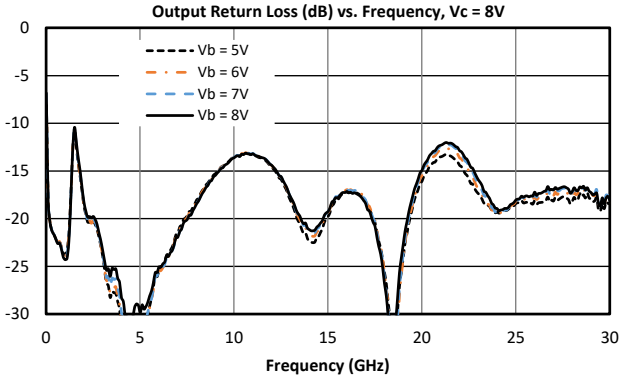
Small Signal Gain (dB) vs. Frequency, Vc = 6V



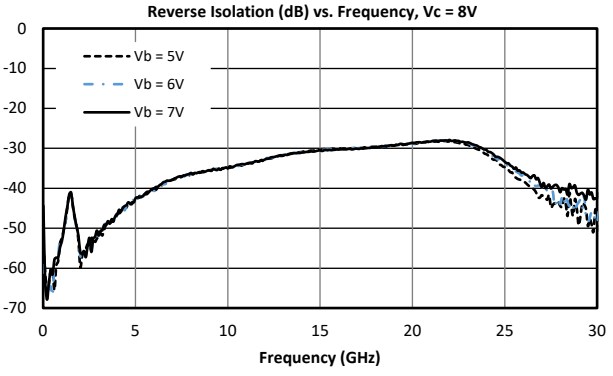
Input Return Loss (dB) vs. Frequency, Vc = 8V



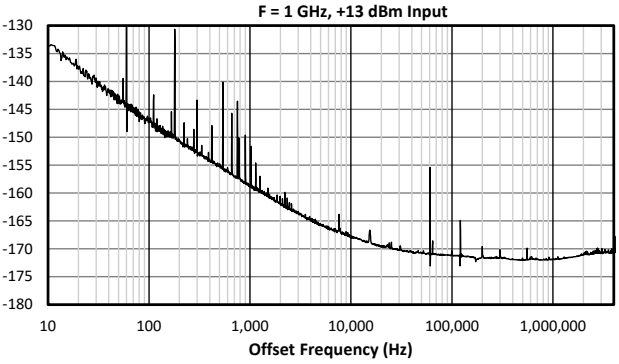
Output Return Loss (dB) vs. Frequency, Vc = 8V



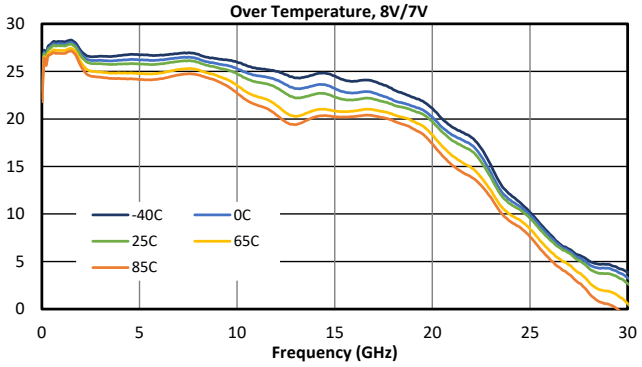
Reverse Isolation (dB) vs. Frequency, Vc = 8V



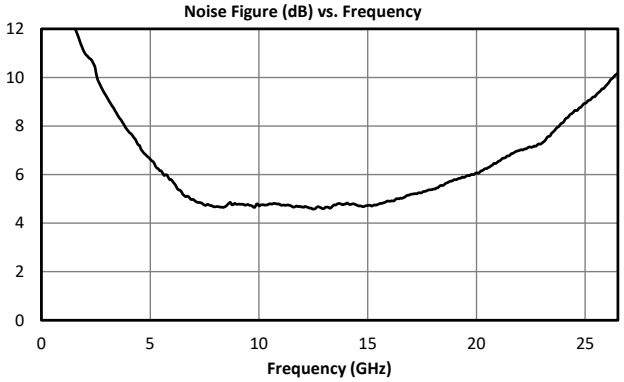
Residual Phase Noise (dBc/Hz) vs. Offset Frequency
F = 1 GHz, +13 dBm Input



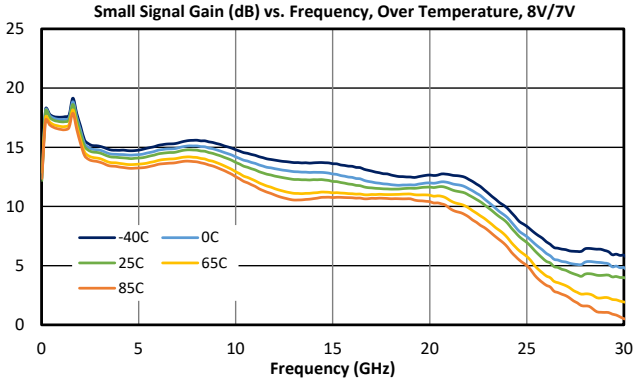
Saturated Output Power (dBm) vs. Frequency, Over Temperature, 8V/7V



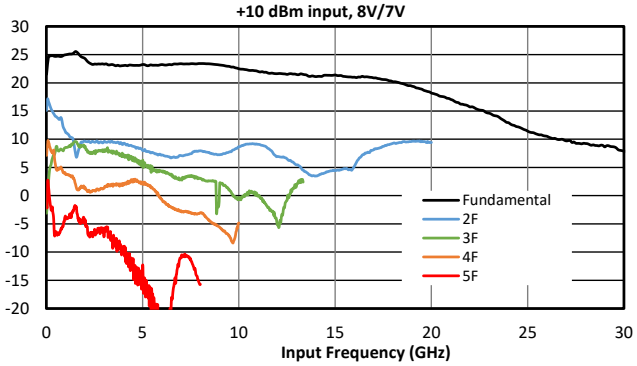
Noise Figure (dB) vs. Frequency



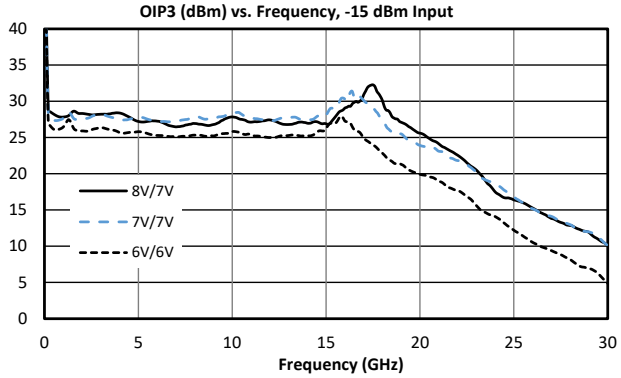
Small Signal Gain (dB) vs. Frequency, Over Temperature, 8V/7V



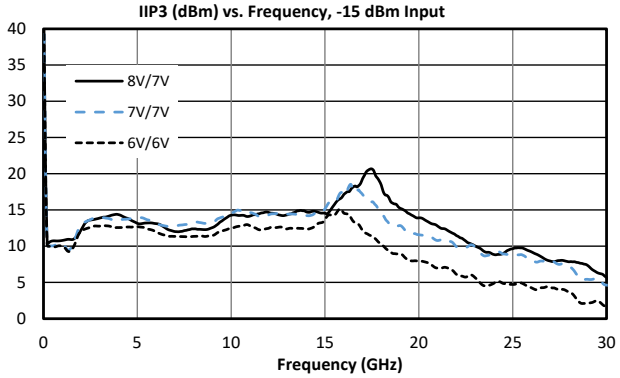
Harmonic Response (dBm) vs. Input Frequency, +10 dBm input, 8V/7V



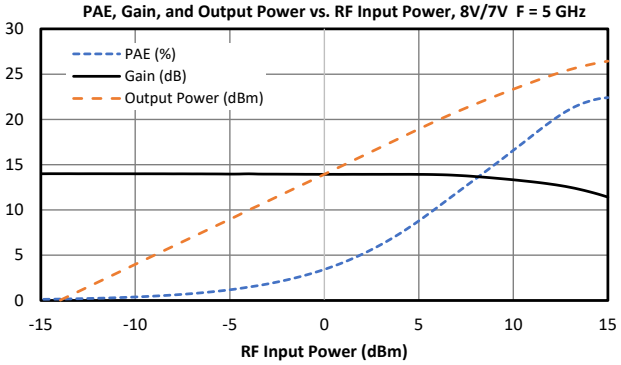
OIP3 (dBm) vs. Frequency, -15 dBm Input



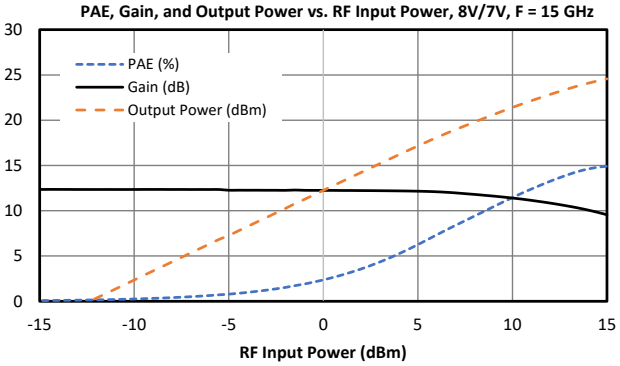
IIP3 (dBm) vs. Frequency, -15 dBm Input

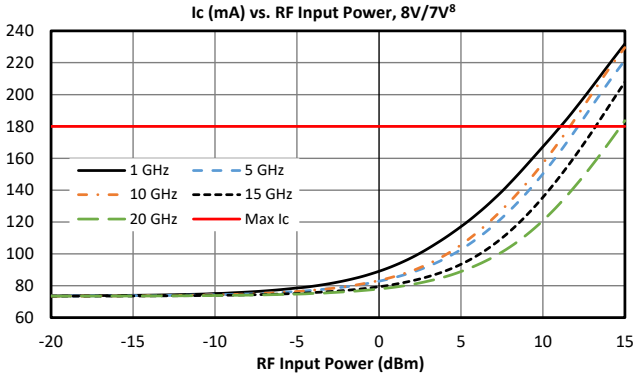


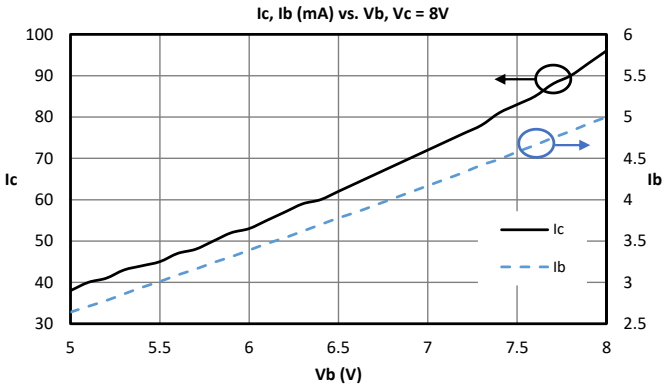
PAE, Gain, and Output Power vs. RF Input Power, 8V/7V F = 5 GHz



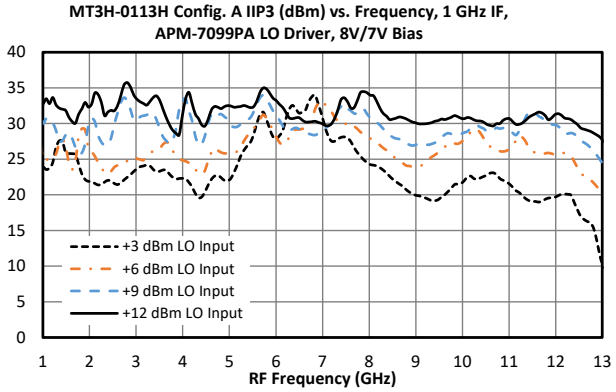
PAE, Gain, and Output Power vs. RF Input Power, 8V/7V, F = 15 GHz

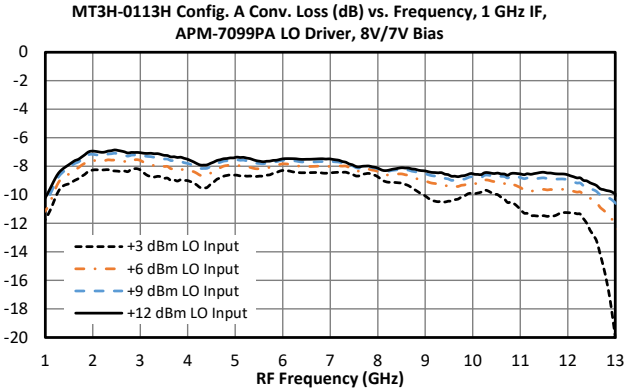


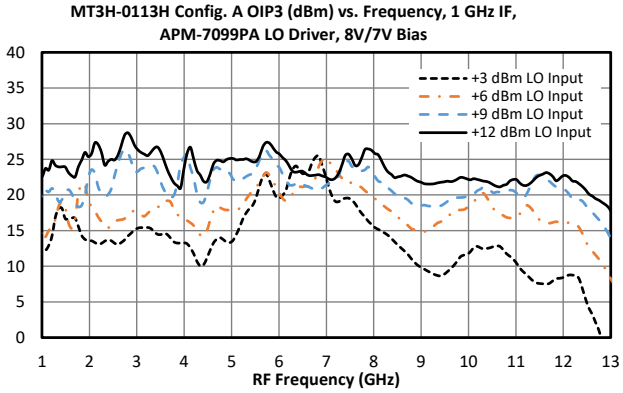




3.8 Typical Performance Plots of Marki MT3H-0113H with APM-7099PA LO Driver[9]

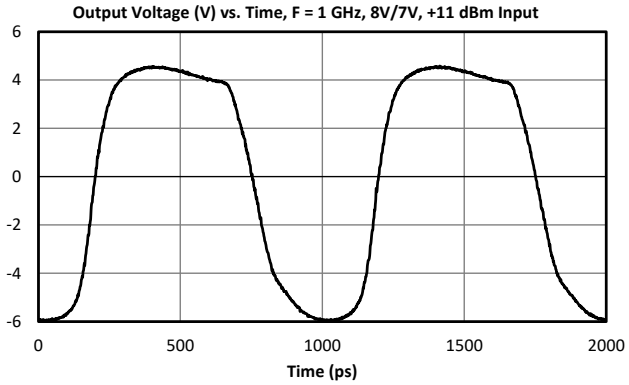


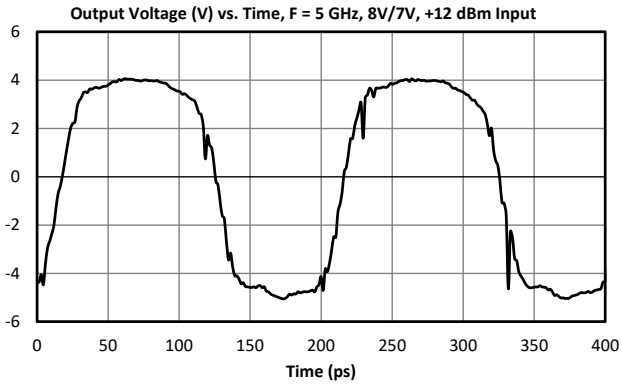


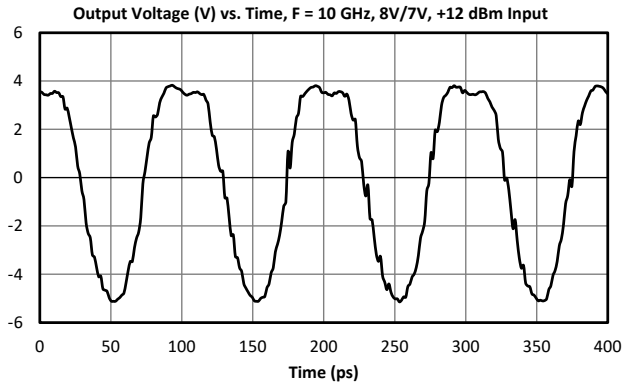


[8] Operation above Max Ic Limit = 180mA, will result in reduced MTTF
[9] LO Input Powers specified as the input power into the APM-7099PA LO driver

3.9 Time Domain Plots[10]







3.10 Harmonic Generation

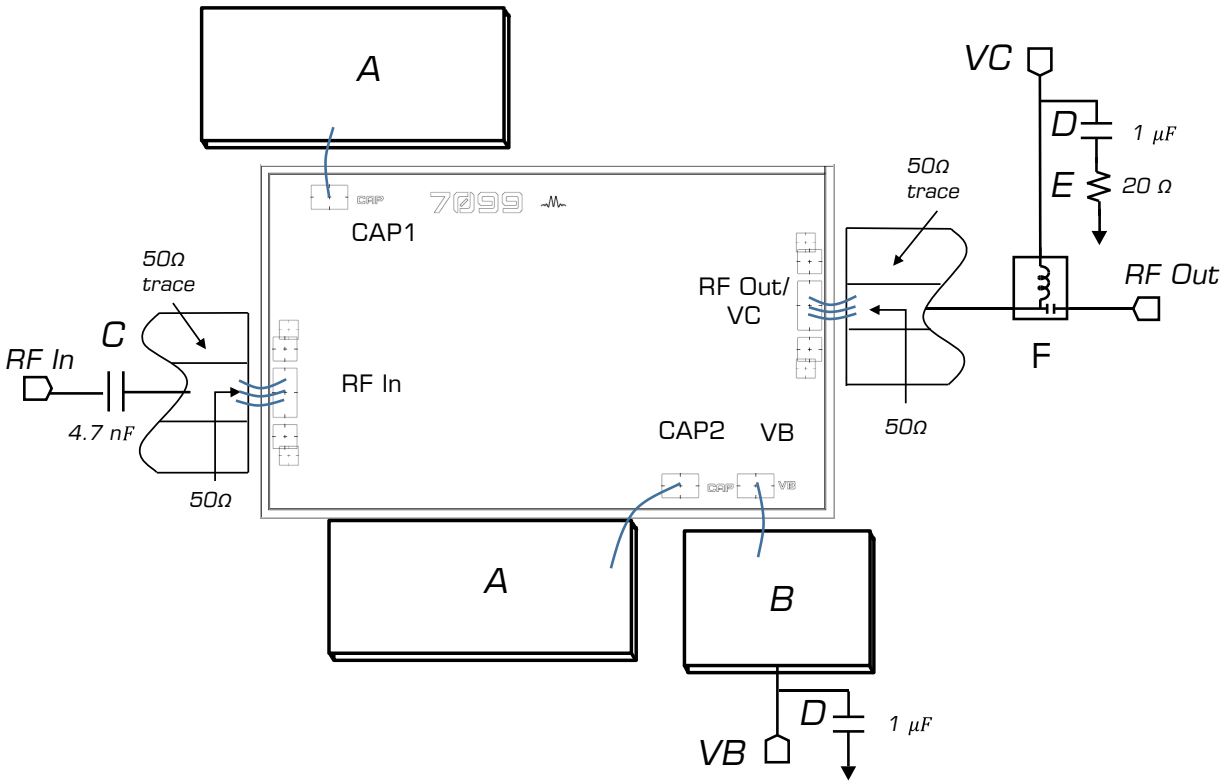
The APM-7099's harmonic generation can be controlled by adjusting the supply and bias voltages. Decreasing the base voltage VB will increase the even harmonic generation and odd harmonic suppression. To increase the odd harmonic generation and even harmonic suppression, decrease the collector voltage VC. The optimal bias condition for even harmonic generation is VC = 8V and VB = 5V, while the optimal bias condition for odd harmonic generation is VC = 5V and VB = 8V.

[10] Fast rise time is desirable for linear T3 mixer operation.

4. Application Information

4.1 APM-7099CH Application Circuit

Below is the recommended application circuit for the APM-7099CH.

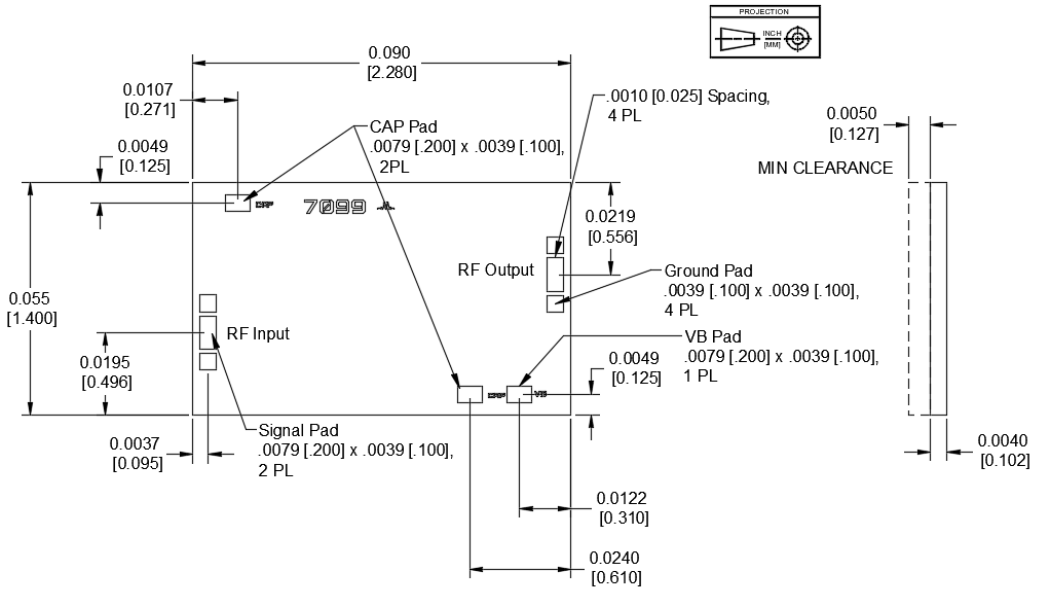


Designator	Description	Sample Part Number
A	Presidio 0.1 µF + 1800 pF Capacitor	MVB4080X104ZGH5R3
B	Tecdia 0.030"x0.030" 150 pF Capacitor	CMS151Z2NC-CK
C*	0402 4.7 nF SMT Capacitor	CL05B472KB5NNNC
D	0402 1.0 µF SMT Capacitor	CL05A105KO5NNNC
E	0402 20Ω SMT Resistor	CPF0402B20RE1
F	Marki Surface-Mount Bias Tee; 5 MHz – 34 GHz	BT-0034SMG

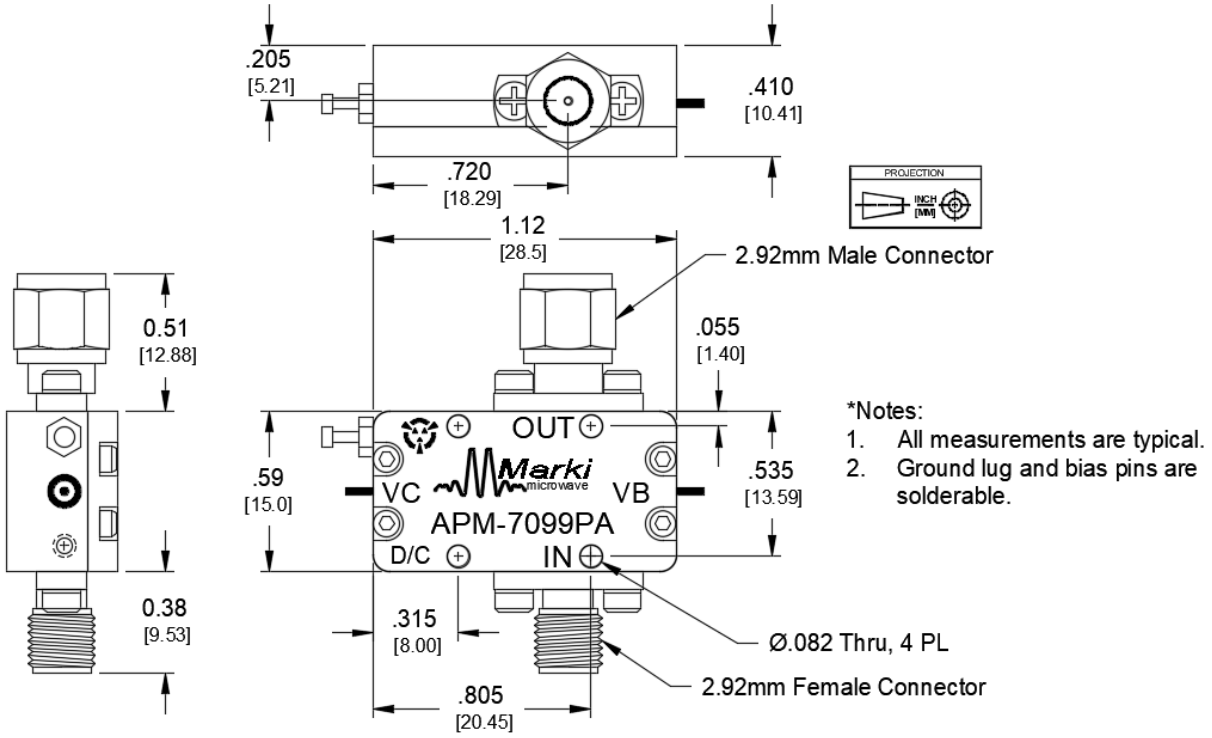
Note*: If the user intends to operate the APM-7099CH at less than 10 MHz input frequency, then the input DC blocking capacitor value must be no greater 4.7nF to avoid catastrophic damage.

5. Mechanical Data

5.1 APM-7099CH Outline Drawing



5.2 APM-7099PA Package Outline Drawing



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