

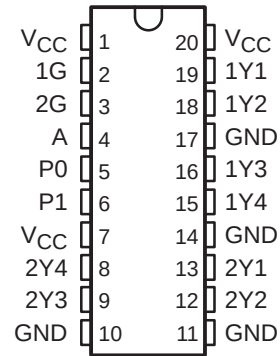
CDC341

1-LINE TO 8-LINE CLOCK DRIVER

SCAS333D – DECEMBER 1992 – REVISED OCTOBER 1998

- Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications
- TTL-Compatible Inputs and Outputs
- Distributes One Clock Input to Eight Outputs
- Distributed V_{CC} and Ground Pins Reduce Switching Noise
- High-Drive Outputs ($-48\text{-mA } I_{OH}$, $48\text{-mA } I_{OL}$)
- State-of-the-Art *EPIC-II B*[™] BiCMOS Design Significantly Reduces Power Dissipation
- Packaging Options Include Plastic Small-Outline (DW) Packages

DW PACKAGE
(TOP VIEW)



description

The CDC341 is a high-performance clock-driver circuit that distributes one (A) input signal to eight (Y) outputs with minimum skew for clock distribution. Through the use of the control pins (1G and 2G), the outputs can be placed in a low state regardless of the A input.

The propagation delays are adjusted at the factory using the P0 and P1 pins. These pins are not intended for customer use and should be strapped to GND.

The CDC341 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
1G	2G	A	1Y1–1Y4	2Y1–2Y4
X	X	L	L	L
L	L	H	L	L
L	H	H	L	H
H	L	H	H	L
H	H	H	H	H



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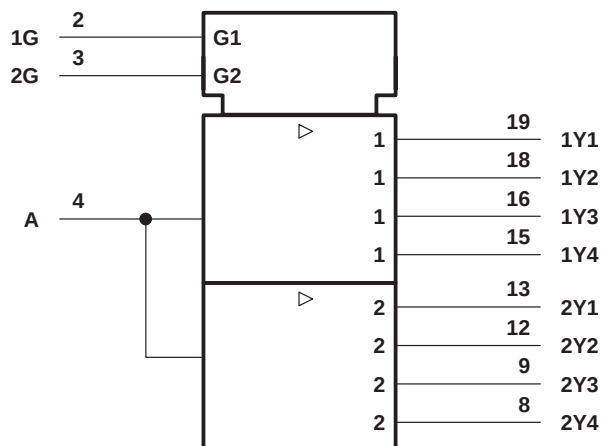
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1-LINE TO 8-LINE CLOCK DRIVER

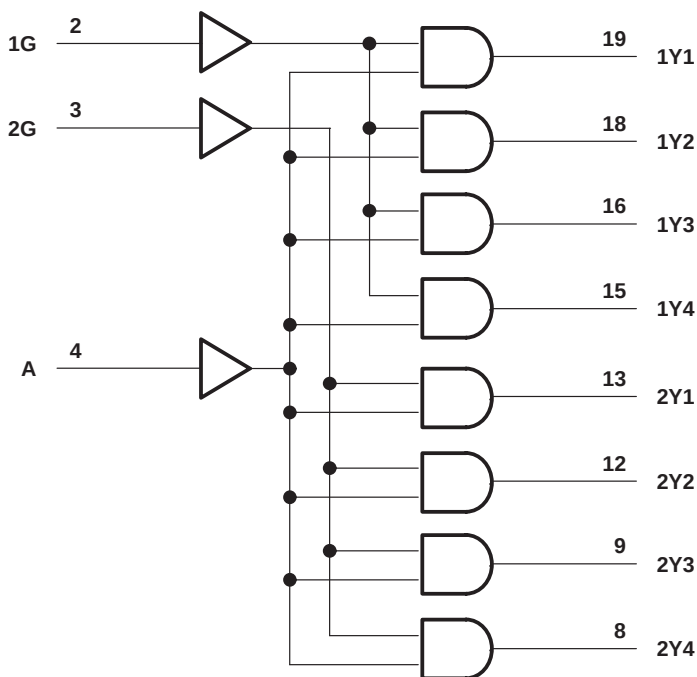
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O	96 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2)	1.6 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		–48	mA
I_{OL}	Low-level output current		48	mA
f_{clock}	Input clock frequency	One output bank loaded		80
		Both output banks loaded		40
T_A	Operating free-air temperature	0	70	°C

NOTE 3: Unused pins (input or I/O) must be held high or low.

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1-LINE TO 8-LINE CLOCK DRIVER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = 25°C			MIN	MAX	UNIT	
			MIN	TYP†	MAX				
V _{IK}	V _{CC} = 4.75 V,	I _I = −18 mA	−1.2			−1.2		V	
V _{OH}	V _{CC} = 4.75 V,	I _{OH} = − 3 mA	2.5			2.5		V	
	V _{CC} = 5 V,	I _{OH} = − 3 mA	3			3			
	V _{CC} = 4.75 V,	I _{OH} = − 48 mA	2			2			
V _{OL}	V _{CC} = 4.75 V,	I _{OL} = 48 mA				0.5		V	
I _I	V _{CC} = 5.25 V,	V _I = V _{CC} or GND		±1			±1		μA
I _O [‡]	V _{CC} = 5.25 V,	V _O = 2.5 V		−50	−100	−200	−50	−200	mA
I _{CC}	V _{CC} = 5.25 V, V _I = V _{CC} or GND	Outputs high	2			3.5		mA	
		Outputs low	24			33			
C _i	V _I = 2.5 V or 0.5 V		3					pF	

† All typical values are at V_{CC} = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics, C_L = 50 pF (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			V _{CC} = 4.75 V to 5.25 V, T _A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	A	Y	3.5		4.5	3.1	4.9	ns
t _{PHL}			3.5		4.3	3.1	4.9	
t _{PLH}	G	Y	2		3.8	2	4	ns
t _{PHL}			2		3.8	2	4	
t _{sk(o)}	A	Y		0.3	0.5		0.6	ns
t _{sk(p)}				0.6	0.8		0.9	
t _{sk(pr)}					1		1	
t _r	A	Y					1.5	ns
t _f	A	Y					1.5	ns

t_{pd} performance information relative to V_{CC} and temperature variation (see Note 4)

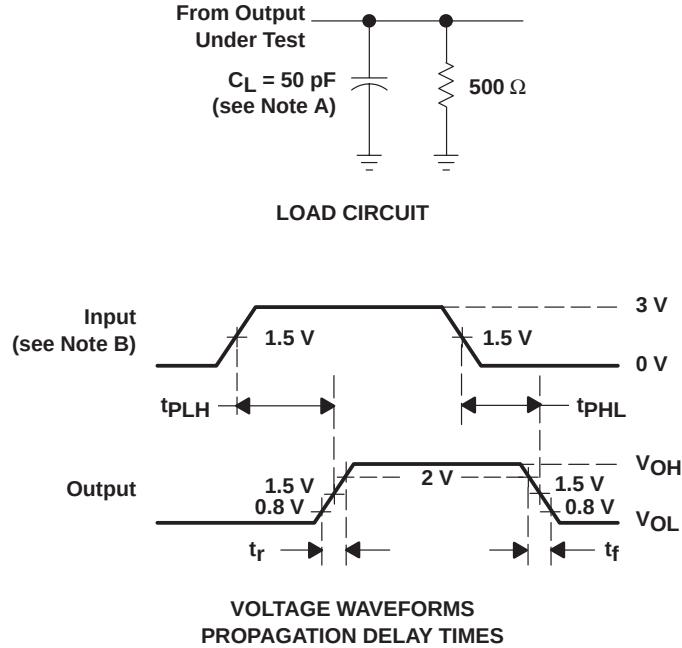
Dt _{PLH} (T _A)†	Temperature drift of t _{PLH} from 0°C to 70°C	–41 ps/10°C
Dt _{PHL} (T _A)†	Temperature drift of t _{PHL} from 0°C to 70°C	–52 ps/10°C
Dt _{PLH} (V _{CC})‡	V _{CC} drift of t _{PLH} from 4.75 V to 5.25 V	28 ps/100 mV
Dt _{PHL} (V _{CC})‡§	V _{CC} drift of t _{PHL} from 4.75 V to 5.25 V	20 ps/100 mV

† Virtually independent of V_{CC}

‡ Virtually independent of temperature

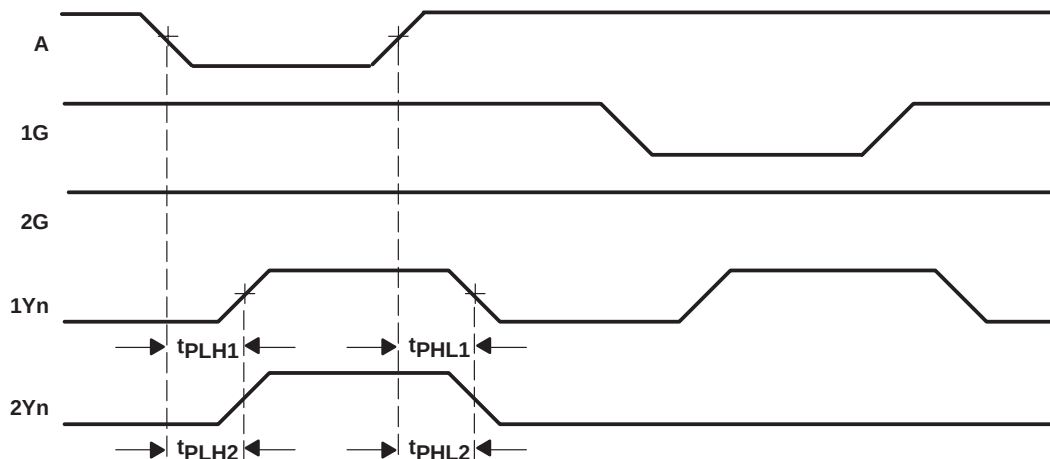
NOTE 4: The data extracted is from a wide range of characterization material.

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.

Figure 1. Load Circuit and Voltage Waveforms



- NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
– The difference between the fastest and slowest of t_{PLHn} ($n = 1, 2$)
– The difference between the fastest and slowest of t_{PHLn} ($n = 1, 2$)
B. Pulse skew, $t_{sk(p)}$, is calculated as the greater of $|t_{PLHn} - t_{PHLn}|$ ($n = 1, 2$).
C. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
– The difference between the fastest and slowest of t_{PLHn} ($n = 1, 2$) across multiple devices under identical operating conditions
– The difference between the fastest and slowest of t_{PHLn} ($n = 1, 2$) across multiple devices under identical operating conditions

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$, $t_{sk(pr)}$

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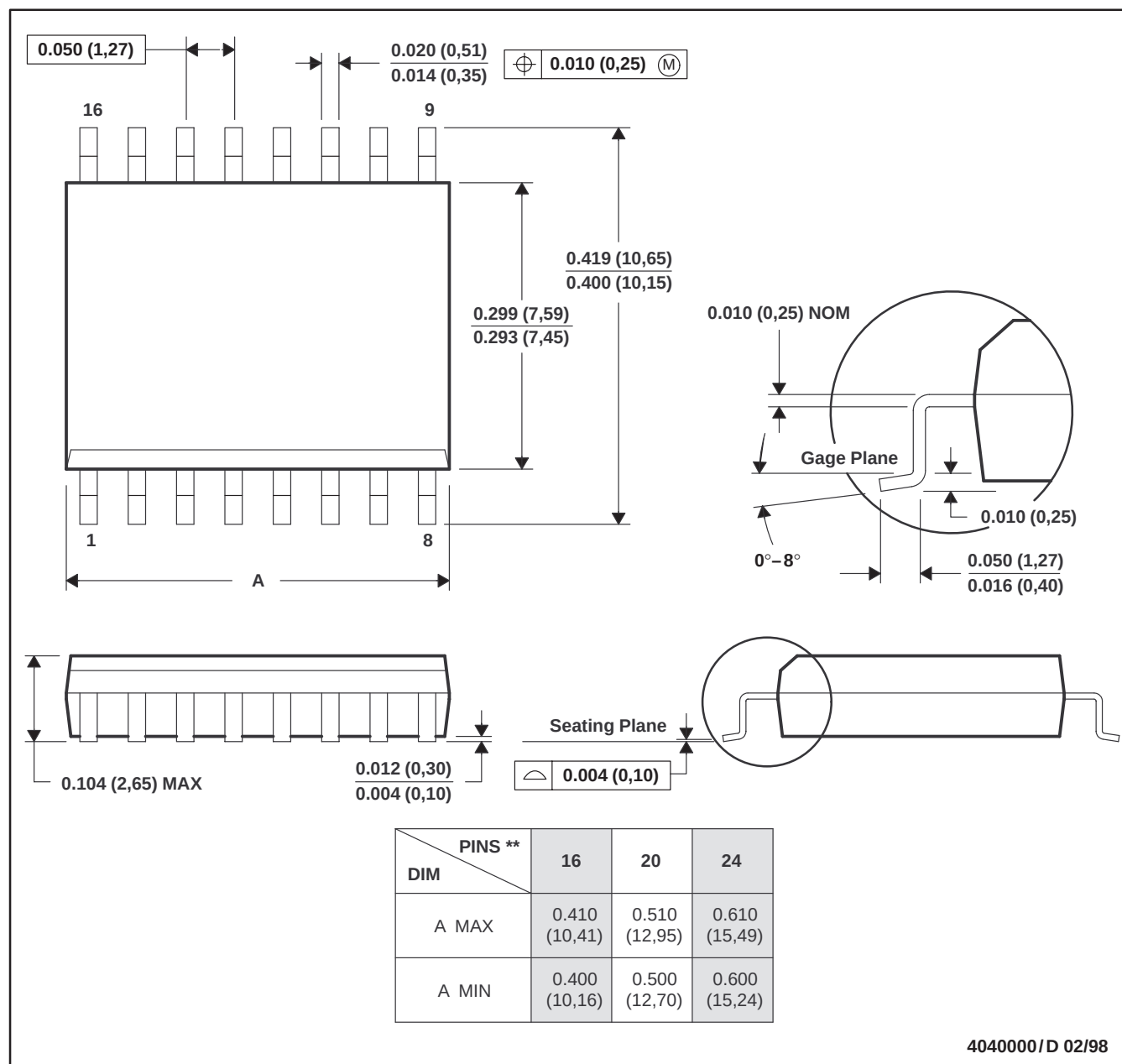
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MECHANICAL INFORMATION

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CDC341DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
CDC341DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC341DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC341DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC341DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC341NSR	OBSOLETE	SO	NS	20		TBD	Call TI	Call TI
CDC341NSRG4	OBSOLETE	SO	NS	20		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

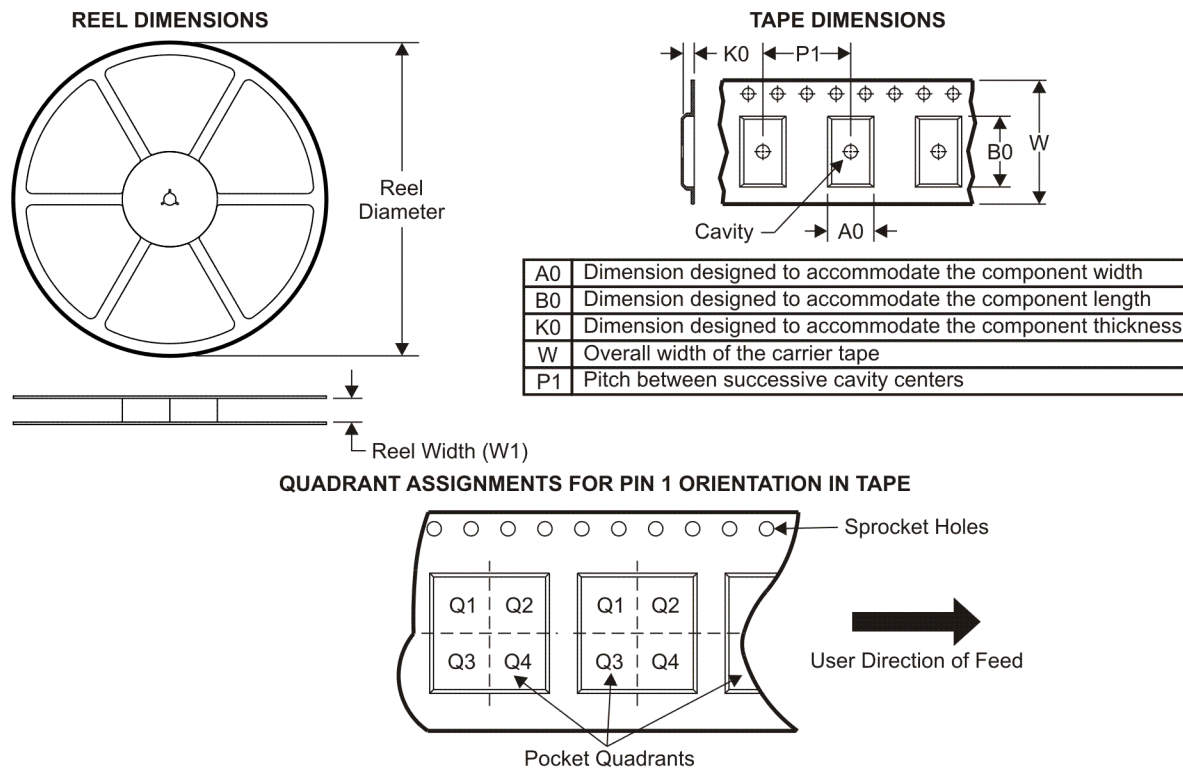
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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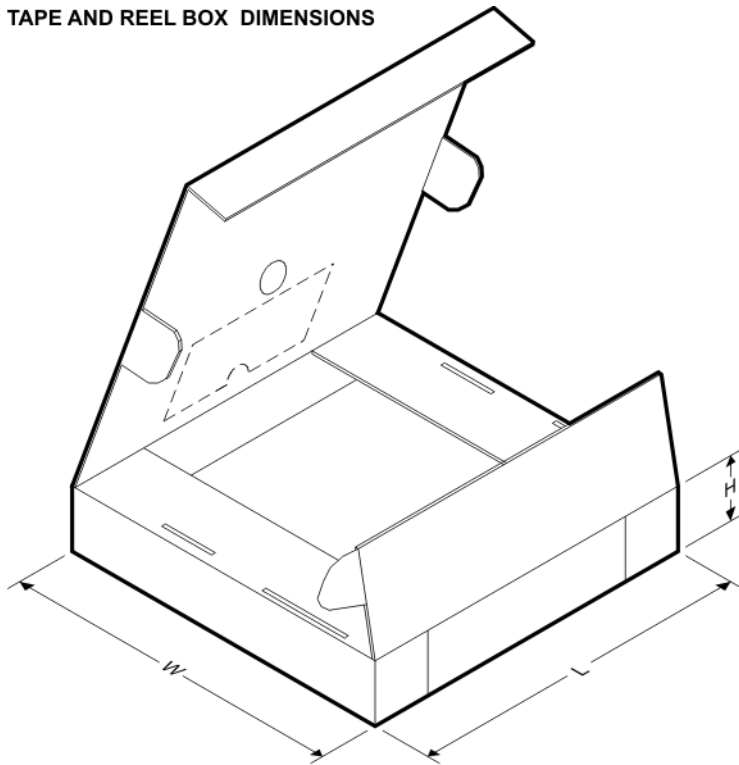
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC341DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC341DWR	SOIC	DW	20	2000	346.0	346.0	41.0

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