Panasonic

NN30310AA

VIN = 6 V to 30 V, 3 A
Synchronous DC-DC Step down Regulator
comprising of Controller IC and Power MOSFET

FEATURES

- High-Speed Response DC-DC Step Down Regulator Circuit that employs Hysteretic Control System
- Two 25 mΩ (Typ.) MOSFETs for High Efficiency at 3 A
- SKIP (discontinuous) Mode for Light Load Efficiency
- Up to 3 A Output Current
- Input VoltageRange : AVIN : 6 V to 30 V,
  PVIN : 6 V to 30 V,
  Output Voltage Range : 0.75 V to 5.5 V
  Selectable Switching Frequency 250 kHz , 750 kHz , 1250 kHz
- Adjustable Soft Start
- Low Operating and Standby Quiescent Current
- Open Drain Power Good Indication for Output Over , Under Voltage
- Built-in Under Voltage Lockout (UVLO),
  Thermal Shut Down (TSD),
  Over Voltage Detection (OVD),
  Under Voltage Detection (UVD),
  Over Current Protection (OCP),
  Short Circuit Protection (SCP)
- HQFN024-A3-0404 (Size : 4 mm X 4 mm, 0.5 mm pitch), 24pin Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN Type)

DESCRIPTION

NN30310AA is a synchronous DC-DC Step down Regulator (1-ch) comprising of a Controller IC and two power MOSFETs and employs the hysteretic control system.

By this system, when load current changes suddenly, it responds at high speed and minimizes the changes of output voltage.

Since it is possible to use capacitors with small capacitance and it is unnecessary to add external parts for system phase compensation, this IC realizes downsizing of set and reducing in the number of external parts. Output voltage is adjustable by user.

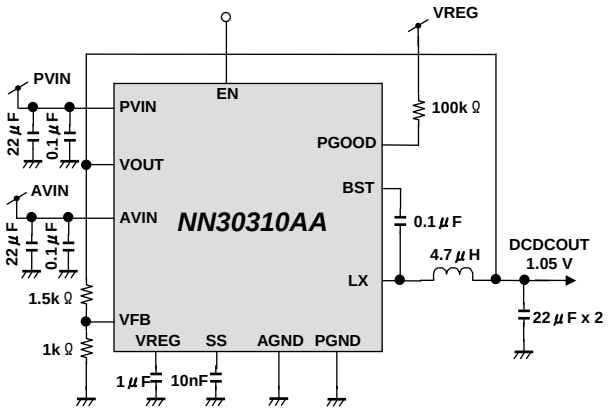
Maximum current is 3 A.

APPLICATIONS

High Current Distributed Power Systems such as

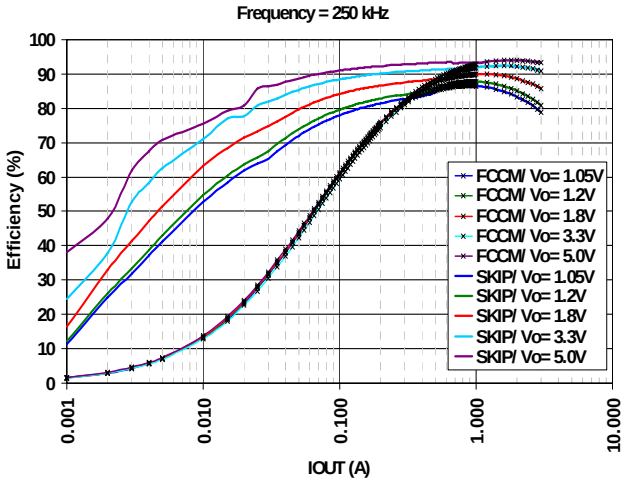
- HDDs (Hard Disk Drives)
- SSDs (Solid State Drives)
- PCs
- Game consoles
- Servers
- Security Cameras
- Network TVs
- Home Appliances
- OA Equipment etc.

SIMPLIFIED APPLICATION



Notes) This application circuit is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

EFFICIENCY CURVE



Condition)

V_{IN} = 12.5 V, Vout = 1.05 V , 1.2 V , 1.8 V , 3.3 V , 5.0 V,
Lo = 4.7 µH, Co = 44 µF (22 µF x 2), Frequency = 250 kHz

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Notes
Supply voltage	V_{IN}	33	V	*1
Operating free-air temperature	T_{opr}	– 40 to + 85	°C	*2
Operating junction temperature	T_j	– 40 to + 150	°C	*2
Storage temperature	T_{stg}	– 55 to + 150	°C	*2
Input Voltage Range	MODE,FSEL,VOUT,VFB,	– 0.3 to (VREG + 0.3)	V	*1 *3
	EN	-0.3 to 6.0	V	*1
Output Voltage Range	PGOOD	– 0.3 to (VREG + 0.3)	V	*1 *3
	LX	– 0.3 to (V_{IN} + 0.3)	V	*1 *4
ESD	HBM (Human Body Model)	1.4	kV	—

Notes) Do not apply external currents and voltages to any pin not specifically mentioned.
This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected. V_{IN} is voltage for AVIN, PVIN. AVIN = PVIN.

*1:The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2:Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25 °C.
*3:(VREG + 0.3) V must not be exceeded 6 V.
*4:(V_{IN} + 0.3) V must not be exceeded 33 V.

POWER DISSIPATION RATING

PACKAGE	θ_{JA}	PD (Ta = 25 °C)	PD (Ta = 85 °C)	Notes
24pin Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN Type)	61.6 °C /W	2.03 W	1.06 W	*1

Note). For the actual usage, please refer to the PD-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.
*1:Glass Epoxy Substrate (4 Layers) [Glass-Epoxy: 50 X 50 X 0.8 t (mm)]
Die Pad Exposed , Soldered.



CAUTION

Although this has limited built-in ESD protection circuit, but permanent damage may occur on it.
Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Min.	Typ.	Max.	Unit	Notes
Supply voltage range	AVIN	6	12	30	V	—
	PVIN	6	12	30	V	—
Input Voltage Range	MODE	– 0.3	—	VREG + 0.3	V	*1
	FSEL	– 0.3	—	VREG + 0.3	V	*1
	EN	– 0.3	—	6.0	V	—
Output Voltage Range	PGOOD	– 0.3	—	VREG + 0.3	V	*1
	LX	– 0.3	—	V_{IN} + 0.3	V	*2

Note) Do not apply external currents and voltages to any pin not specifically mentioned.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for AGND, PGND. AGND = PGND
V_{IN} is voltage for AVIN, PVIN. AVIN = PVIN.
The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*1 : (VREG + 0.3) V must not be exceeded 6 V.
*2 : (V_{IN} + 0.3) V must not be exceeded 33 V.

ELECRTRICAL CHARACTERISTICS

Co = 22 µF X 2 (Murata), Lo= 1 µH (Panasonic), VOUT Setting = 3.3 V, V_{IN} = AV_{IN} = PV_{IN} = 12 V,
Switching Frequency = 750 kHz, MODE = VREG (FCCM), T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current Consumption							
Consumption current at active	I_{VDDACT}	EN= 5 V, I_{OUT} = 0 A RFB1 = 4.5 kΩ RFB2 = 1.0 kΩ MODE=GND (Skip MODE)	—	650	1000	µA	—
Consumption current at standby	I_{VDDSTB}	EN = 0 V	—	—	2	µA	—
Logic Pin							
EN pin Low-level input voltage	V_{ENL}	—	—	—	0.3	V	—
EN pin High-level input voltage	V_{ENH}	—	1.5	—	5.0	V	—
EN pin leak current	I_{LEAKEN}	EN = 5 V	—	5.0	10.0	µA	—
MODE pin Low-level input voltage	V_{MODEL}	—	—	—	VREG X 0.3	V	—
MODE pin High-level input voltage	V_{MODEH}	—	VREG X 0.7	—	VREG	V	—
MODE pin leak current	$I_{LEAKMODE}$	MODE = 5 V	—	5.0	10.0	µA	—
FSEL pin Low-level input voltage	V_{MODEL}	—	—	—	0.3	V	—
FSEL pin High-level input voltage	V_{MODEH}	—	VREG – 0.3	—	VREG	V	—
FSEL pin leak current	I_{LEAKMD}	FSEL = 5 V	—	15.0	25.0	µA	—
VREG							
VREG output voltage	V_{REGOUT}	IVREG = – 6 mA	5.1	5.5	5.9	V	
VREG drop out voltage	$V_{REGLINE}$	V_{IN} = 6.0 V IVREG = – 6 mA	—	—	200	mV	—

ELECRTRICAL CHARACTERISTICS (Continued)

Co = 22 µF X 2 (Murata), Lo= 1 µH (Panasonic), VOUT Setting = 3.3 V, V_{IN} = AV_{IN} = PV_{IN} = 12 V,
Switching Frequency = 750 kHz, MODE = VREG (FCCM), T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
VFB Characteristics							
VFB comparator threshold	V_{FBTS}	—	0.594	0.600	0.606	V	—
Under Voltage Lock Out							
UVLO start voltage 1	$V_{UVLODET}$	V_{IN} = 5 V to 0 V	3.5	3.8	4.1	V	—
UVLO recover voltage 1	$V_{UVLORMV}$	V_{IN} = 0 V to 5 V	3.9	4.2	4.5	V	—
PGOOD							
PGOOD Threshold 1 (VFB ratio for UVD detect)	V_{THPG1}	PGOOD : High to Low	78	85	92	%	—
PGOOD Hysteresis 1 (VFB ratio for UVD release)	V_{HYSPG1}	PGOOD : Low to High	2	5	8	%	—
PGOOD Threshold 2 (VFB ratio for OVD detect)	V_{THPG2}	PGOOD : High to Low	108	115	122	%	—
PGOOD Hysteresis 2 (VFB ratio for OVD release)	V_{HYSPG2}	PGOOD : Low to High	2	5	8	%	—
PGOOD ON resistance	RPG	—	—	8	12	Ω	—

ELECRTRICAL CHARACTERISTICS (Continued)

Co = 22 µF X 2 (Murata), Lo= 1 µH (Panasonic), VOUT Setting = 3.3 V, V_{IN} = AV_{IN} = PV_{IN} = 12 V,
Switching Frequency = 750 kHz, MODE = VREG (FCCM), T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
DC-DC							
DC-DC line regulation	DDREGIN	PVIN = 6 V to 30 V I_{OUT} = – 0.5 A	—	0.25	0.75	%/V	—
DC-DC load regulation	DDREGLD	I_{OUT} = – 10 mA to – 3 A	—	3.5	—	%	*1
DC-DC efficiency 1	DDEFF1	I_{OUT} = – 10 mA MODE=GND (Skip MODE)	—	70	—	%	*1
DC-DC efficiency 2	DDEFF2	I_{OUT} = – 3 A	—	90	—	%	*1
DC-DC output ripple voltage 1	DDVRPL1	I_{OUT} = – 10 mA	—	20	—	mV [p-p]	*1
DC-DC output ripple voltage 2	DDVRPL2	I_{OUT} = – 3A	—	20	—	mV [p-p]	*1
DC-DC load transient response	DDDVAC	I_{OUT} = – 100 mA ↔ – 1.5 A Vout = 1 V Δt = 0.5 A / µs	—	20	—	mV	*1
DC-DC High Side MOS ON resistance	DDRONH	VGS = 5.5 V	—	25	50	mΩ	—
DC-DC Low Side MOS ON resistance	DDRONL	VGS = 5.5 V	—	25	50	mΩ	—
MIN Input and output voltage difference	DV	DV = PVIN – VOUT	—	2.5	—	V	*1
VFB Characteristics							
VFB pin leak current 1	ILEAKFB1	VFB = 0 V	– 1	—	1	µA	—
VFB pin leak current 2	ILEAKFB2	VFB = 6 V	– 1	—	1	µA	—

*1 : Typical Value checked by design.

ELECRTRICAL CHARACTERISTICS (Continued)

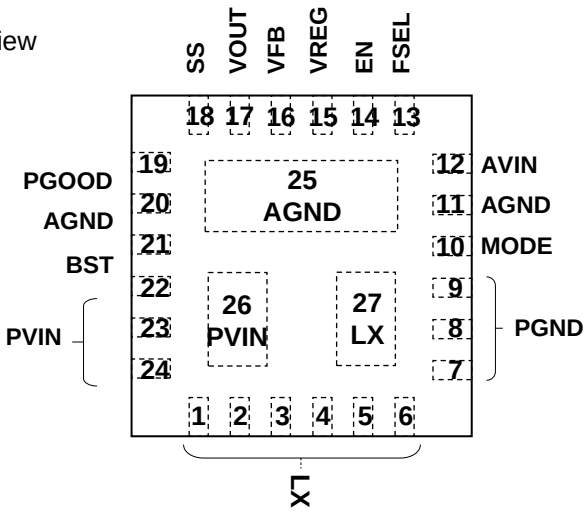
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Switching Frequency = 750 kHz, MODE = VREG (FCCM), T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
PROTECTION							
DC-DC output current limit	DDILMT	Vout = 1.0 V	—	4.7	—	A	*1
DC-DC Output GND Short Protection Threshold	DDSHPTH	FB = 0.6 V to 0.0 V	50	60	70	%	—
Soft-Start Timing							
SS Charge Current	ISSCHG	V_{SS} = 0.3 V	– 4	– 2	—	µA	—
SS Discharge Resistance (Shut-down)	RSSDIS	EN = 0 V	—	5	10	kΩ	—
Switching Frequency Adjustment							
DC-DC Switching Frequency 1	DDFSW1	Vout = 0.75 V I_{OUT} = – 3 A	—	250	—	kHz	*1
DC-DC Switching Frequency 2	DDFSW2	Vout = 0.75 V I_{OUT} = – 3 A	—	750	—	kHz	*1
DC-DC Switching Frequency 3	DDFSW3	Vout = 0.75 V I_{OUT} = – 3 A	—	1250	—	kHz	*1

*1 : Typical Value checked by design.

PIN CONFIGURATION

Top View

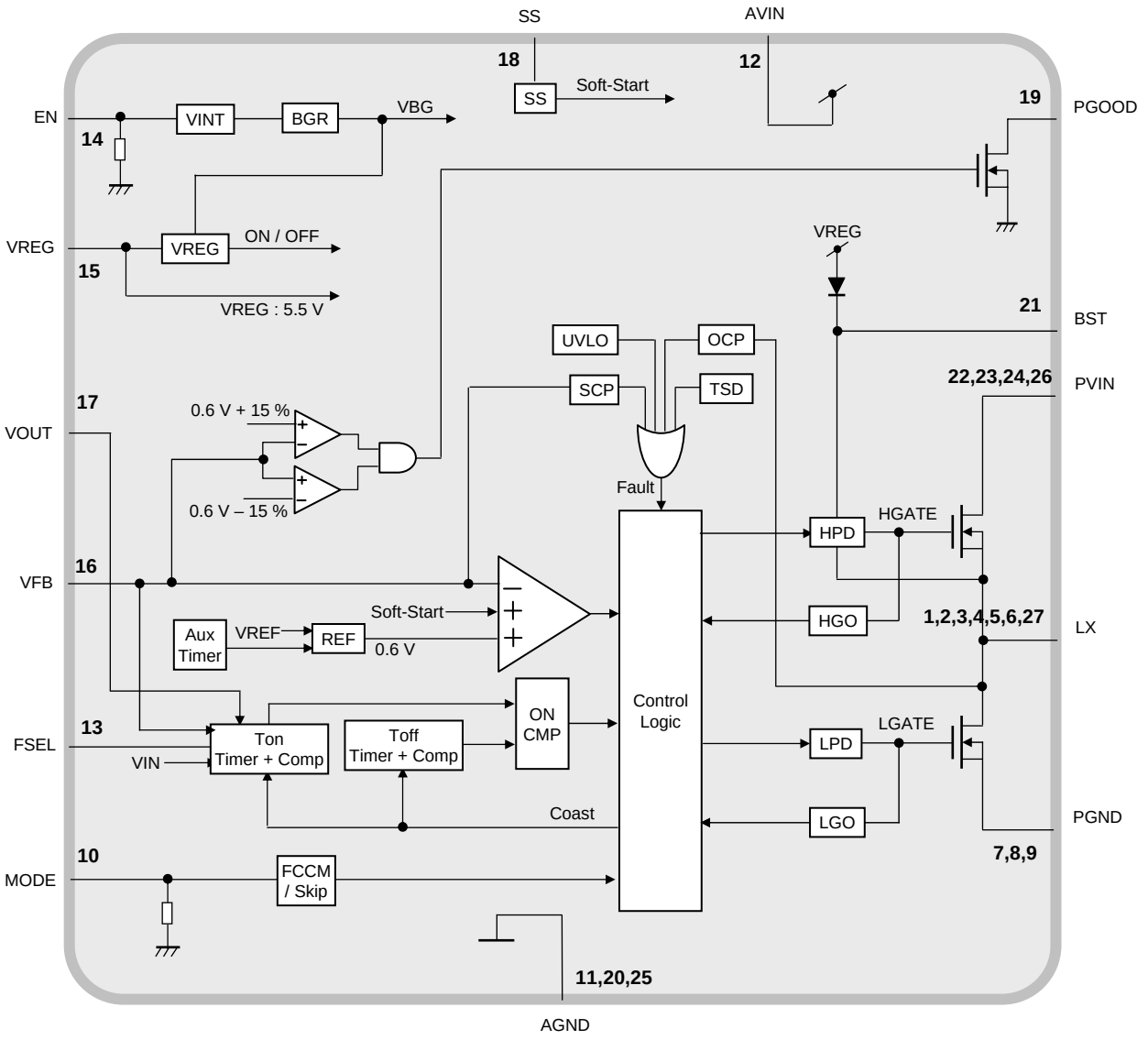


PIN FUNCTIONS

Pin No.	Pin name	Type	Description
1	LX	Output	Power MOSFET output pin
2			
3			
4			
5			
6			
7	PGND	Ground	Ground pin for Power MOSFET
8			
9			
10	MODE	Input	Skip / FCCM mode select pin
11	AGND	Ground	Ground pin
12	AVIN	Power supply	Power supply pin
13	FSEL	Input	Frequency selection pin
14	EN	Input	ON/OFF control pin
15	VREG	Output	LDO output pin (Power supply for internal control circuit)
16	VFB	Input	Comparator negative input pin
17	VOUT	Input	Output voltage sense pin
18	SS	Output	Soft start capacitor connect pin
19	PGOOD	Output	Power good open drain pin
20	AGND	Ground	Ground pin
21	BST	Output	Supply input pin for high side FET gate driver
22	PVIN	Power supply	Power supply pin for Power MOSFET
23			
24			
25	AGND	Ground	Ground pin for radiation of heat
26	PVIN	Power supply	Power supply pin for radiation of heat
27	LX	Output	Power MOSFET output pin for radiation of heat

Notes) Concerning detail about pin description, please refer to OPERATION and APPLICATION INFORMATION section.

FUNCTIONAL BLOCK DIAGRAM



Notes) This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

OPERATION

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

1. Protection

(1).Output Over-Current Protection (OCP) function And Short-Circuit Protection (SCP) function

1) The Over Current Protection is activated at about 4.7 A (Typ.) During the OCP, the output voltage continues to drop at the specified current.
2) The Short-Circuit Protection function is implemented when the output voltage decreases and the VFB pin reaches to about 60 % of the set voltage of 0.6 V.
3) The SCP operates intermittently at 2 ms-ON, 16 ms OFF intervals.

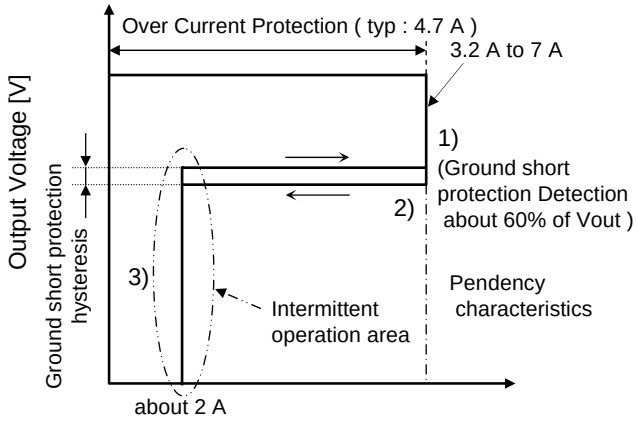


Figure : OCP and SCP Operation

(2).Over Voltage Detection (OVD) and Under Voltage Detection (UVD)

1).The NMOS connected to the PGOOD pin turns ON when the output voltage rises and the VFB pin voltage reaches 115 % of its set voltage (0.6 V).
2).After (1) above, the NMOS connected to the PGOOD pin is turned OFF after 1 ms when the output voltage drops and the VFB pin voltage reaches 110 % of its set voltage (0.6 V).
3).The NMOS connected to the PGOOD pin turns ON when the output voltage drops and the VFB pin voltage reaches 85 % of its set voltage (0.6 V).
4).After (3) above, the NMOS connected to the PGOOD pin is turned OFF after 1 ms when the output voltage drops and the VFB pin voltage reaches 90 % of its set voltage (0.6 V).

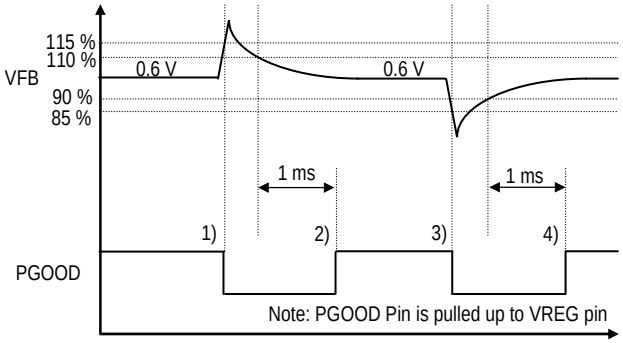


Figure : OVD and UVD Operation

(3).Thermal Shut Down (TSD)

When the IC internal temperature becomes more than about 130 °C, TSD operates and DCDC turns off.

2. Pin Setting

(1).Operating Mode Setting

The IC can operate at two different modes : Skip mode and Forced Continuous Conduction mode (FCCM).

In Skip mode, the IC is working under pulse skipping mechanism to improve efficiency at light load condition.

In FCCM mode, the IC is working at fixed frequency to avoid EMI issues.

The Operating Mode can be set by MODE pin as follows.

MODE pin	Mode
Low	Skip
High	FCCM

(2).Switching Frequency Setting

The IC can operate at three different frequency : 1250 kHz, 750 kHz and 250 kHz.

The Switching Frequency can be set by FSEL pin as follows.

FSEL pin	Frequency [kHz]
Low	1250
High	250
Open	750

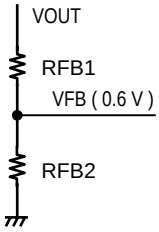
OPERATION (Continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

3. Output Voltage Setting

The Output Voltage can be set by external resistance of FB pin, and its calculation is as follows.
(VIN = 12 V, IOUT = 0 A, FCCM, Fsw = 750 kHz).

$$VOUT = \left(1 + \frac{RFB1}{RFB2}\right) \times 0.6$$



Below resistors are recommended for following popular output voltage.

VOUT [V]	RFB1 [Ω]	RFB2 [Ω]
5.0	11.0 k	1.5 k
3.3	4.5 k	1.0 k
1.8	2.0 k	1.0 k
1.0	1.0 k	1.5 k

Note: RFB2 can be set to a maximum value of 10 kΩ. A larger FBR2 value will be more susceptible to noise.

VFB comparator threshold is adjusted to ± 1 %, but the actual output voltage accuracy becomes more than ± 1 % due to the influence from the circuits other than VFB comparator.
In the case of VOUT setting = 3.3 V, the actual output voltage accuracy becomes ± 2.5 %.
(VIN = 12 V, IOUT = 0 A, FCCM, Fsw = 750 kHz).

4. Soft Start Setting

Soft Start function maintains the smooth control of the output voltage during start up by adjusting soft start time. When the EN pin becomes High, the current (2 µA) begin to charge toward the external capacitor (Css) of SS pin, and the voltage of SS pin increases straightly.

Because the voltage of FB pin is controlled by the voltage of SS pin during start up, the voltage of FB increase straightly to the regulation voltage (0.6 V) together with the voltage of SS pin and keep the regulation voltage after that. On the other hand, the voltage of SS pin increase to about 2.8 V and keep the voltage. The calculation of Soft Start Time is as follows.

$$Soft\ Start\ Time(\sec) = \frac{0.6}{2\mu} \times Css$$

When Css is set at 10 nF, soft-start time is approximately 3ms.

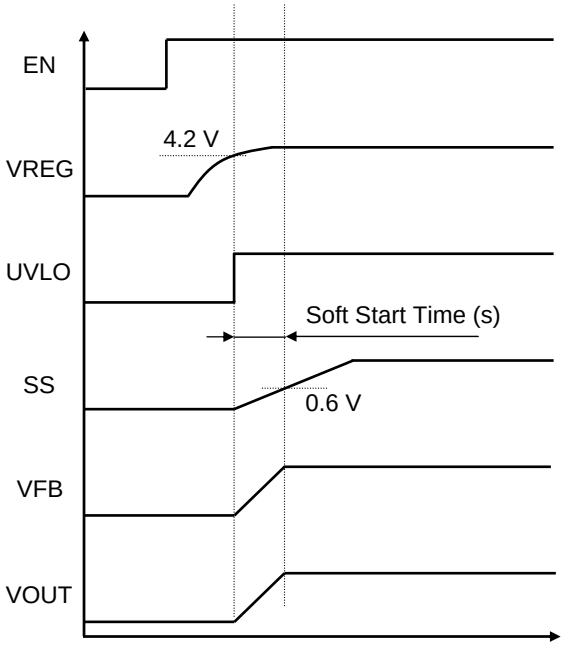


Figure : Soft Start Operation

OPERATION (Continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

5. Start-up / Shut-down Settings

The Start-up / Shut-down is enabled by the EN pin.
The EN pin can be set by either applying voltage from an external voltage source or through a resistor connected to the AVIN pin.

Case 1: Setting up the EN pin using an external voltage source. When an external voltage source is used, the EN pin input voltage (VENH, VENL) should satisfy the conditions as defined in the electrical characteristics

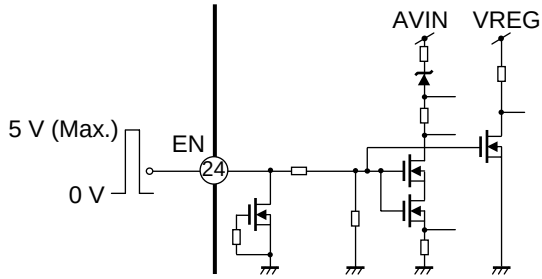


Figure : Internal circuit with EN pin

6. Power ON / OFF sequence

(1) When the EN pin is set to High after the VIN settles, the BGR and the VREG start-up.
(2) When the VREG pin exceeds its threshold value, the UVLO is released and the SOFT START sequence is enabled.
The capacitor connected to the SS pin begins to charge and the SS pin voltage increases linearly.
(3) The VOUT pin (DC-DC Output) voltage increases at the same rate as the SS pin.
Normal operation begins after the VOUT pin reaches the set voltage.
(4) When the EN pin is set to “Low”, the BGR, VREG and UVLO stop operation. The VOUT pin / SS pin Voltage starts to drop and the VOUT pin discharge time depends on the value of the Feedback resistors and the output load current.

Note: The SS pin capacitor should be discharged completely before restarting the startup sequence. An incomplete discharge process might result in an overshoot of the output voltage.

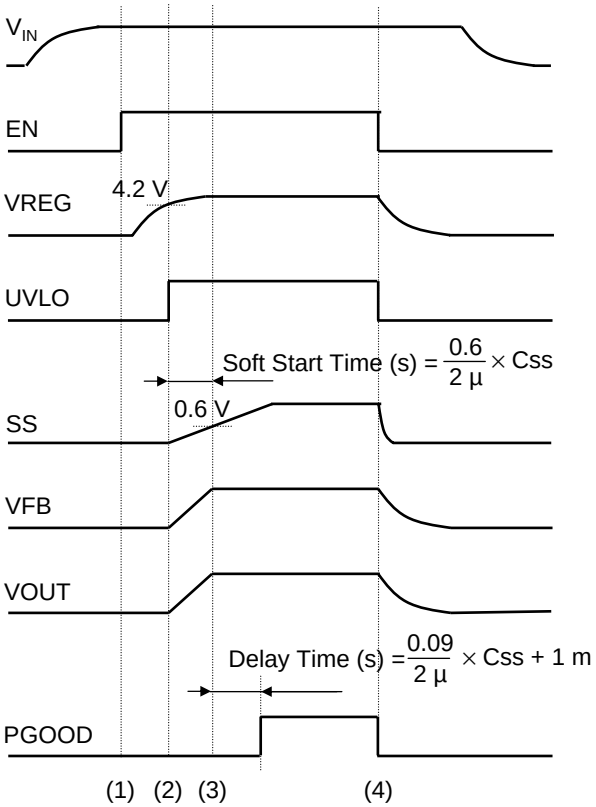
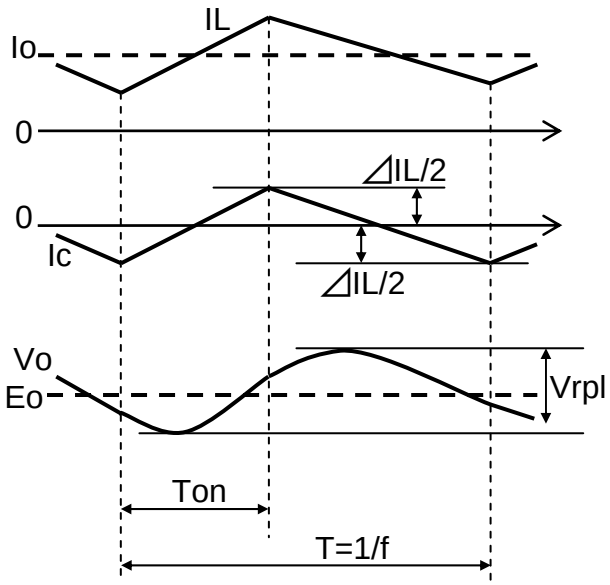


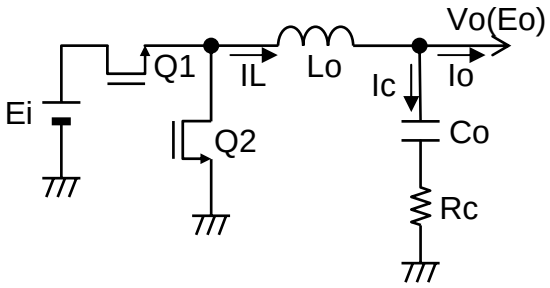
Figure : Power ON/OFF sequence

OPERATION (Continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

7. Inductor and Output Capacitor Setting





Given the desired input and output voltages, the inductor value and operating frequency determine the ripple Current.

$$\Delta IL = \frac{Eo \cdot (Ei - Eo)}{Ei \cdot Lo \cdot f}$$

$$Iox = \frac{\Delta IL}{2}$$

Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off among component size, efficiency and operating frequency. A reasonable starting point is to choose a ripple current that is about 40 % of IOUT(MAX). The largest ripple current occurs at the highest VIN. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$Lo \geq \frac{Eo \cdot (Ei - Eo)}{2Ei \cdot Iox \cdot f} \quad @\ \mathrm{Ei} = \mathrm{Ei_max}$$

And its maximum current rating is

$$IL_\max = \mathrm{Io_max} + \frac{\Delta IL}{2} \quad (@\ \mathrm{Ei} = \mathrm{Ei_max})$$

The selection of COUT is primarily determined by the ESR (Rc) required to minimize voltage ripple and load transients. The output ripple Vrpl is approximately bounded by:

$$Vrpl = Vop - Vob = Ei \cdot \frac{Co \cdot Rc^2}{2Lo} + \frac{\Delta IL}{8Co \cdot f}$$

$$= Ei \cdot \frac{Co \cdot Rc^2}{2Lo} + \frac{Eo \cdot (Ei - Eo)}{8Ei \cdot Lo \cdot Co \cdot f^2}$$

From the above equation, to achieve desired output ripple, low ESR ceramic capacitors are recommended, and its required RMS current rating is:

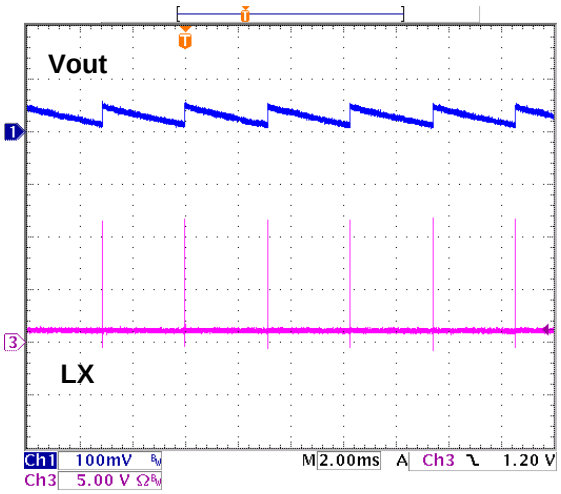
$$Ic(\mathrm{rms})_\max = \frac{\Delta IL}{2\sqrt{3}} \quad (@\ \mathrm{Ei} = \mathrm{Ei_max})$$

TYPICAL CHARACTERISTICS CURVES

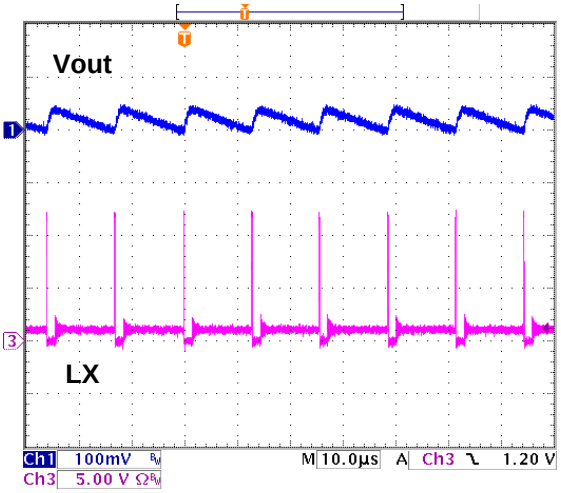
(1) Output Ripple Voltage

Condition : VIN=12V,Vout = 1.05V,Frequency = 750kHz,Skip Mode

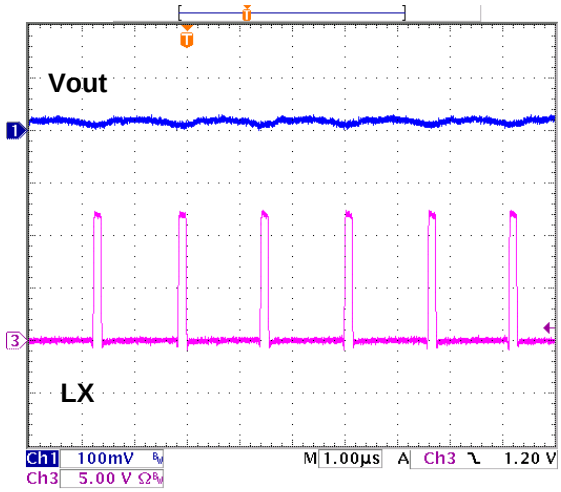
I Load = 0A



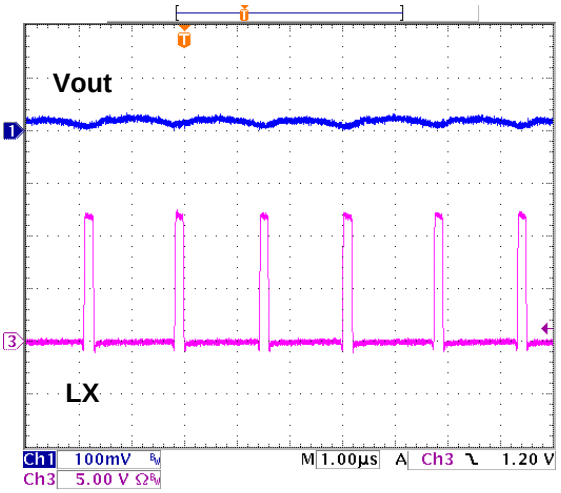
I Load = 0.1A



I Load = 1A



I Load = 3A

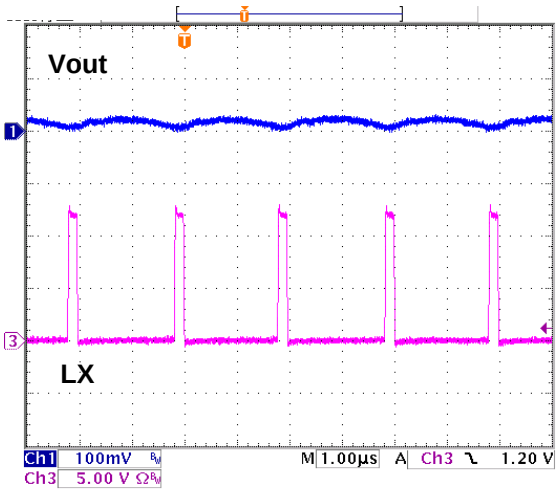


TYPICAL CHARACTERISTICS CURVES (Continued)

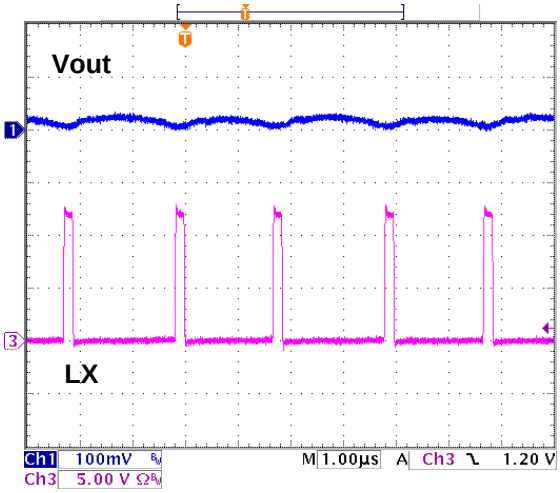
(1) Output Ripple Voltage

Condition : VIN=12V,Vout = 1.05V,Frequency = 750kHz,FCCM Mode

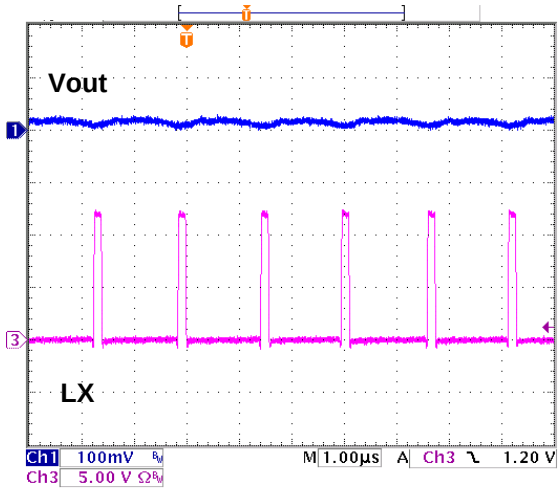
I Load = 0A



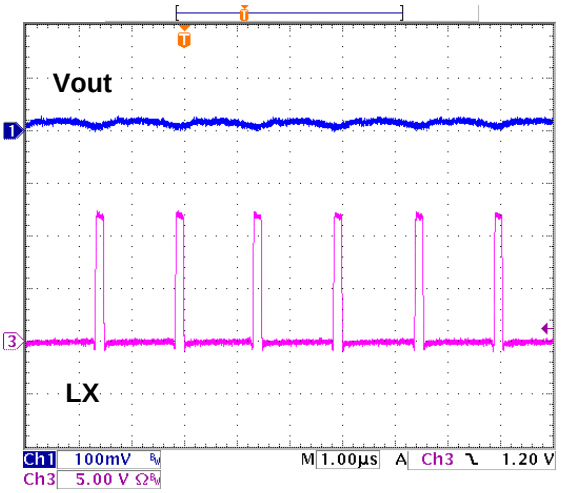
I Load = 0.1A



I Load = 1A



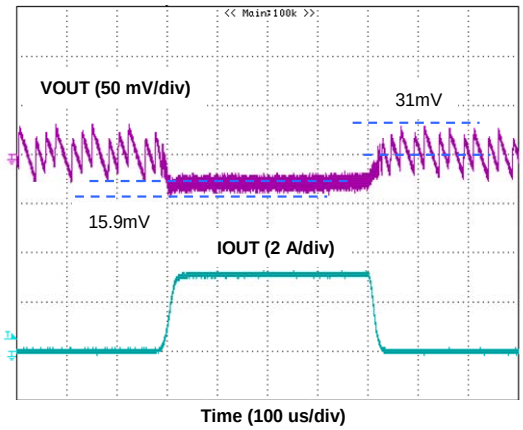
I Load = 3A

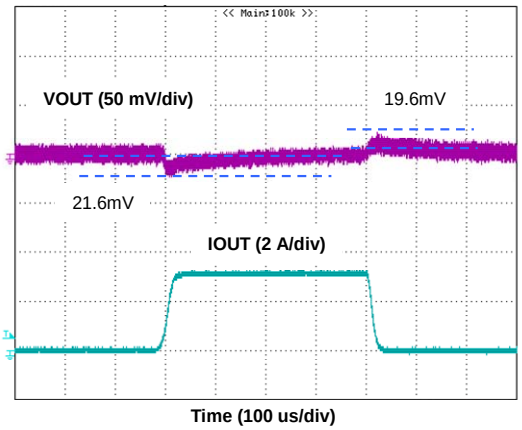


TYPICAL CHARACTERISTICS CURVES (Continued)

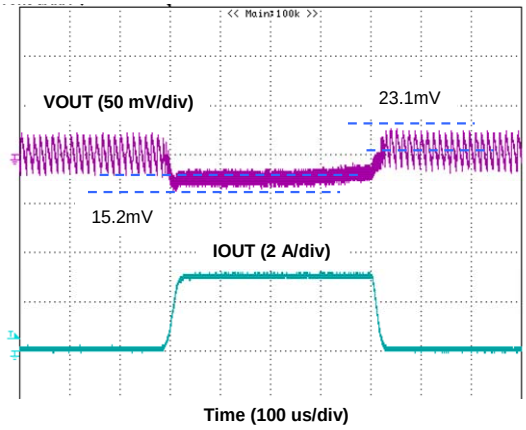
(2) Load transient

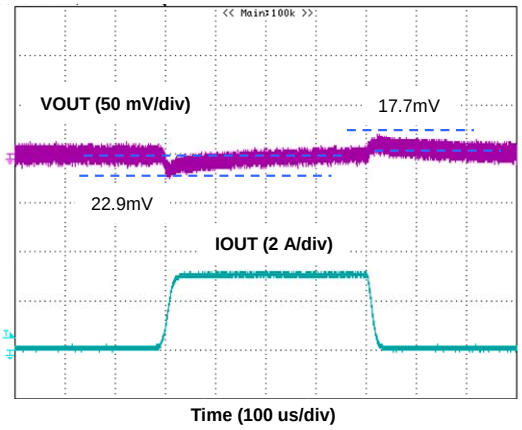
Condition : VIN = 12 V, Vout = 1.05 V, Frequency = 750 kHz, Iout = 50 mA ←→ 3 A (0.15 A / µs)





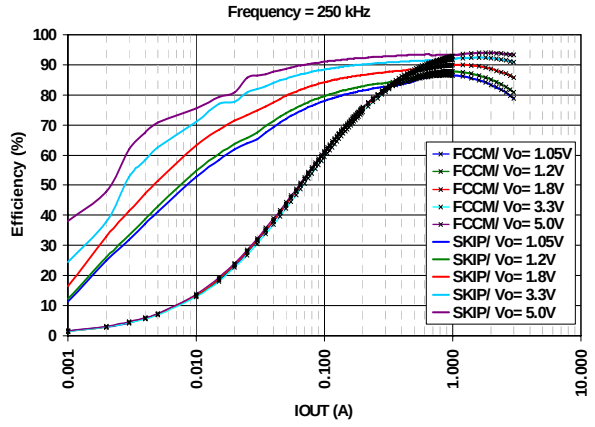
Condition : VIN = 12 V, Vout = 1.05 V, Frequency = 750 kHz, Iout = 0.1 A ←→ 3 A (0.15 A / µs)



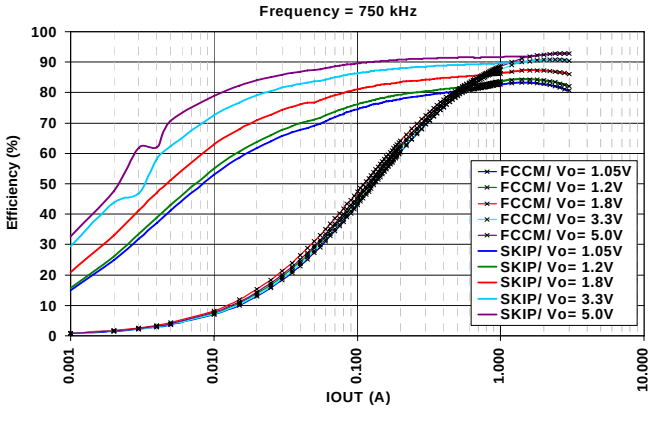


(3) Efficiency

Condition : Vin = 12 V, Vout = 1.05 V / 1.2 V / 1.8V / 3.3V / 5.0 V, L = 4.7 µH, Cout = 66 µF (22 µF x 3), Frequency = 250 kHz



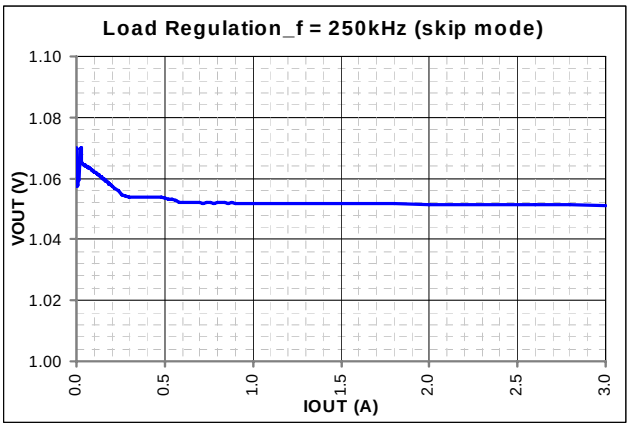
Condition : Vin = 12 V, Vout = 1.05 V / 1.2 V / 1.8V / 3.3V / 5.0 V, L = 1 µH, Cout = 66 µF (22 µF x 3), Frequency = 750kHz

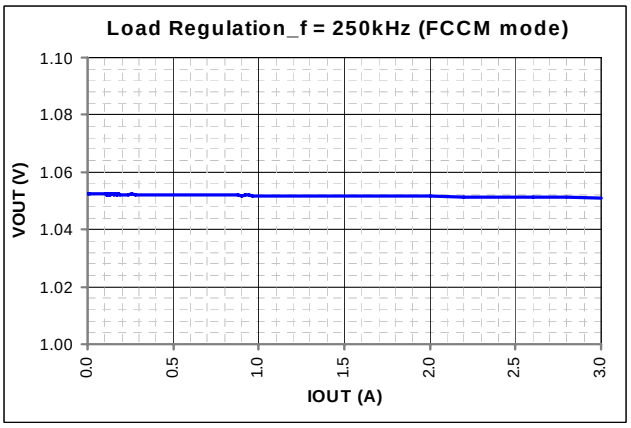


TYPICAL CHARACTERISTICS CURVES (Continued)

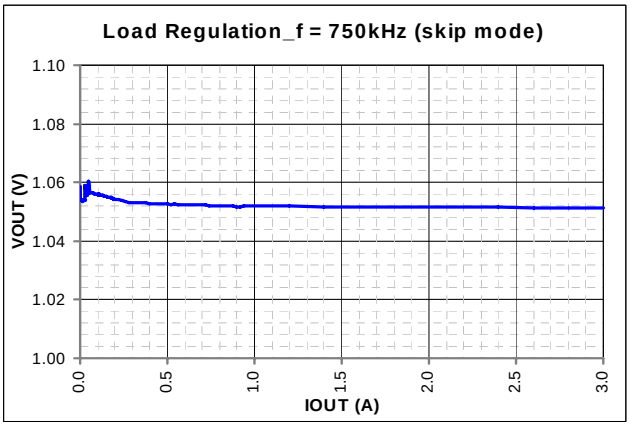
(4) Load regulation

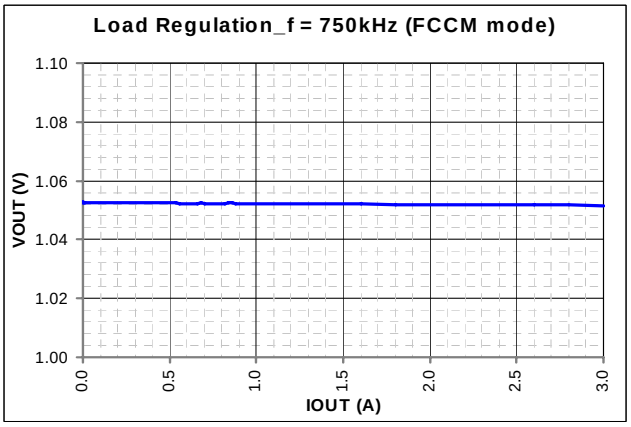
Condition : VIN = 12 V, Vout = 1.05 V, Frequency = 250 kHz





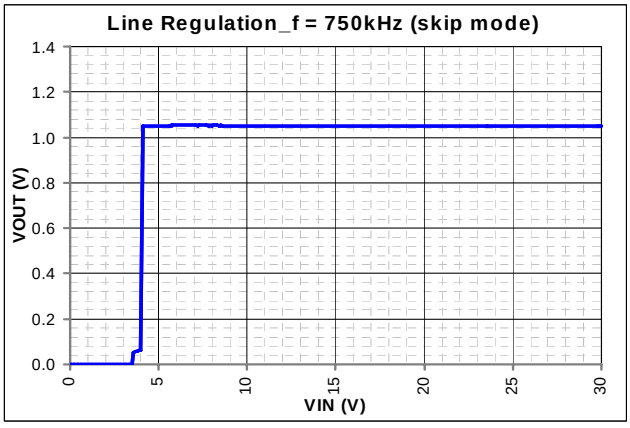
Condition : VIN = 12 V, Vout = 1.05 V, Frequency = 750 kHz

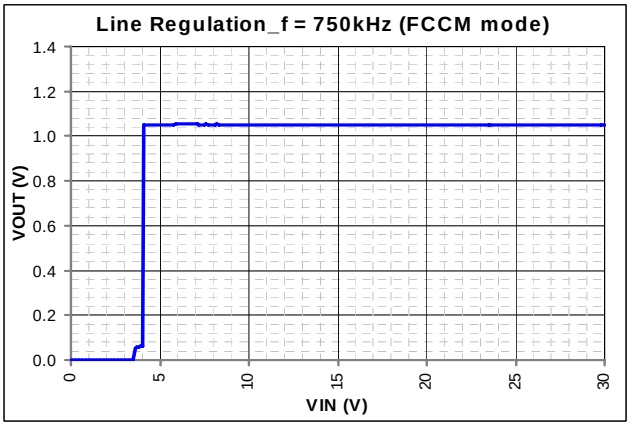




(5) Line regulation

Condition : VIN = 12 V, Vout = 1.05 V, Frequency = 750 kHz, Iout = 1.5 A

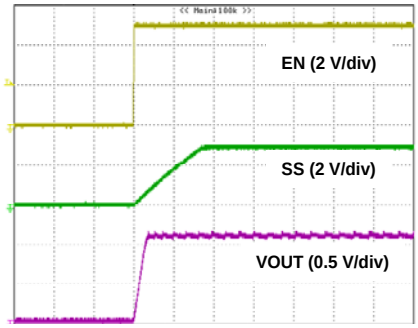




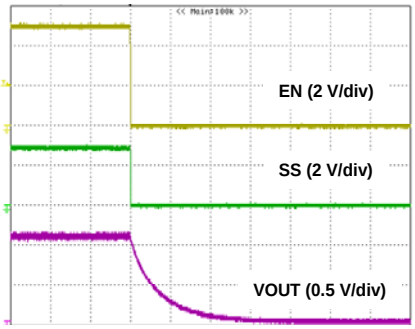
TYPICAL CHARACTERISTICS CURVES (Continued)

(6) start/shut down

Condition : VIN = 12 V, Vout = 1.05 V, Frequency = 750 kHz, SKIP mode, Iout = 0 A

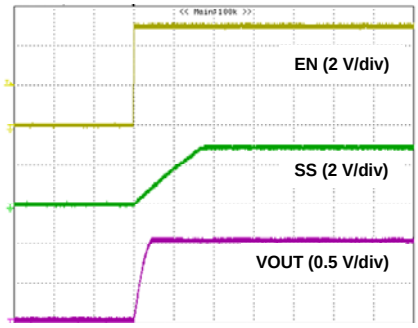


Time (10 ms/div)

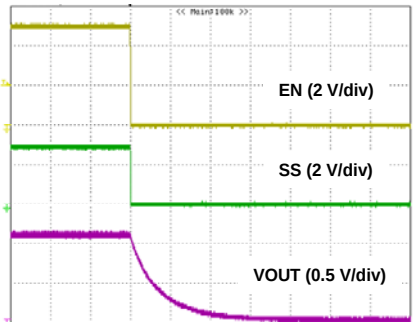


Time (200 ms/div)

Condition : VIN = 12 V, Vout = 1.05 V, Frequency = 750 kHz, FCCM mode, Iout = 0 A

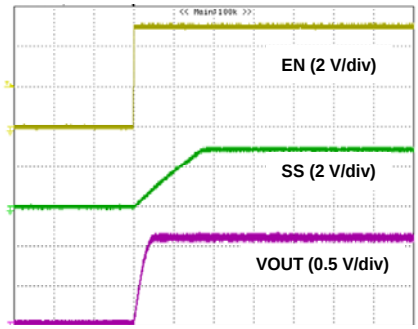


Time (10 ms/div)

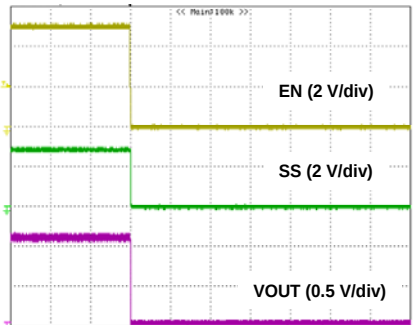


Time (200 ms/div)

Condition : VIN = 12 V, Vout = 1.05 V, Frequency = 750 kHz, SKIP mode, Rload = 0.5 Ω

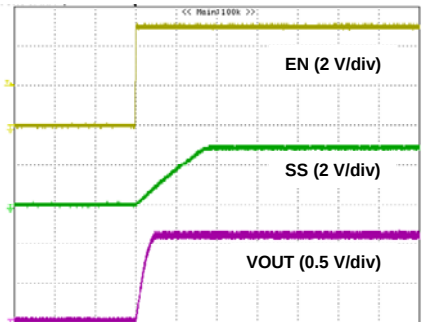


Time (10 ms/div)

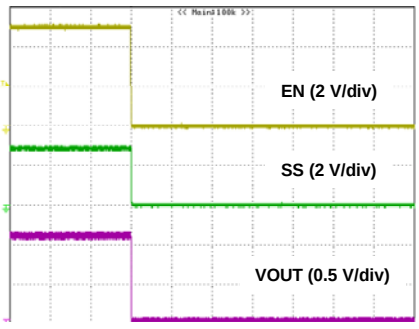


Time (10 ms/div)

Condition : VIN = 12 V, Vout = 1.05 V, Frequency = 750 kHz, FCCM mode, Rload = 0.5 Ω



Time (10 ms/div)



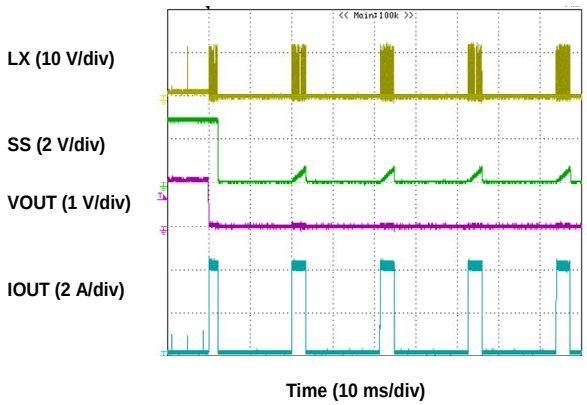
Time (10 ms/div)

TYPICAL CHARACTERISTICS CURVES (Continued)

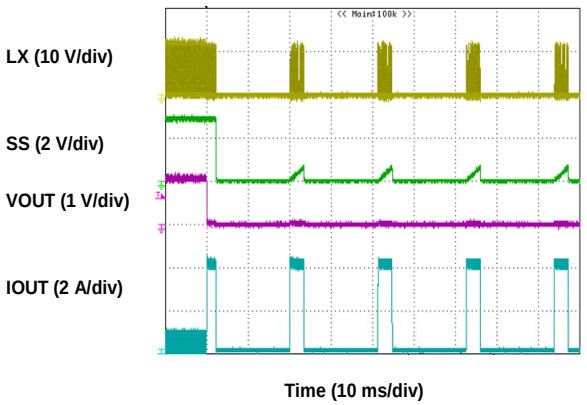
(7) Short Current Protection

Condition : VIN = 12 V, Vout = 1.05 V, Frequency = 750 kHz

Skip Mode

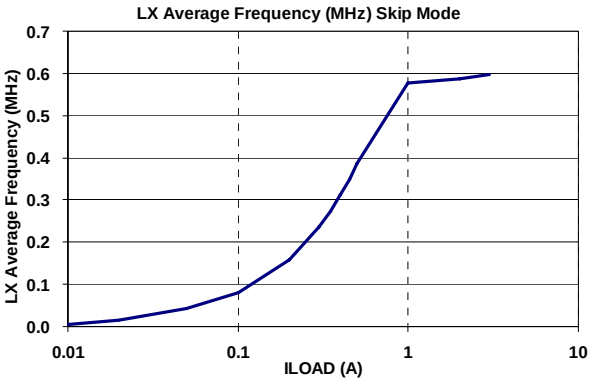


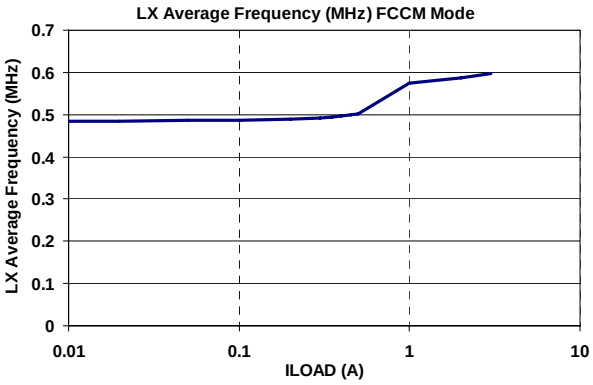
FCCM Mode



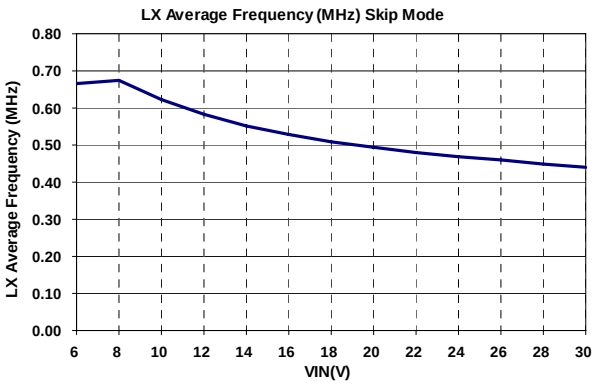
(8) Switching Frequency

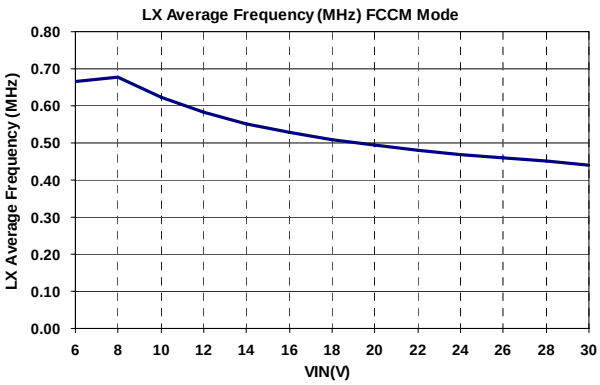
Condition : Vin = 12 V, Vout = 1.05 V, Frequency = 750 kHz, Iout = 10 mA ~ 3 A





Condition : Vout = 1.05 V, Frequency = 750 kHz, Iout = 1.5 A

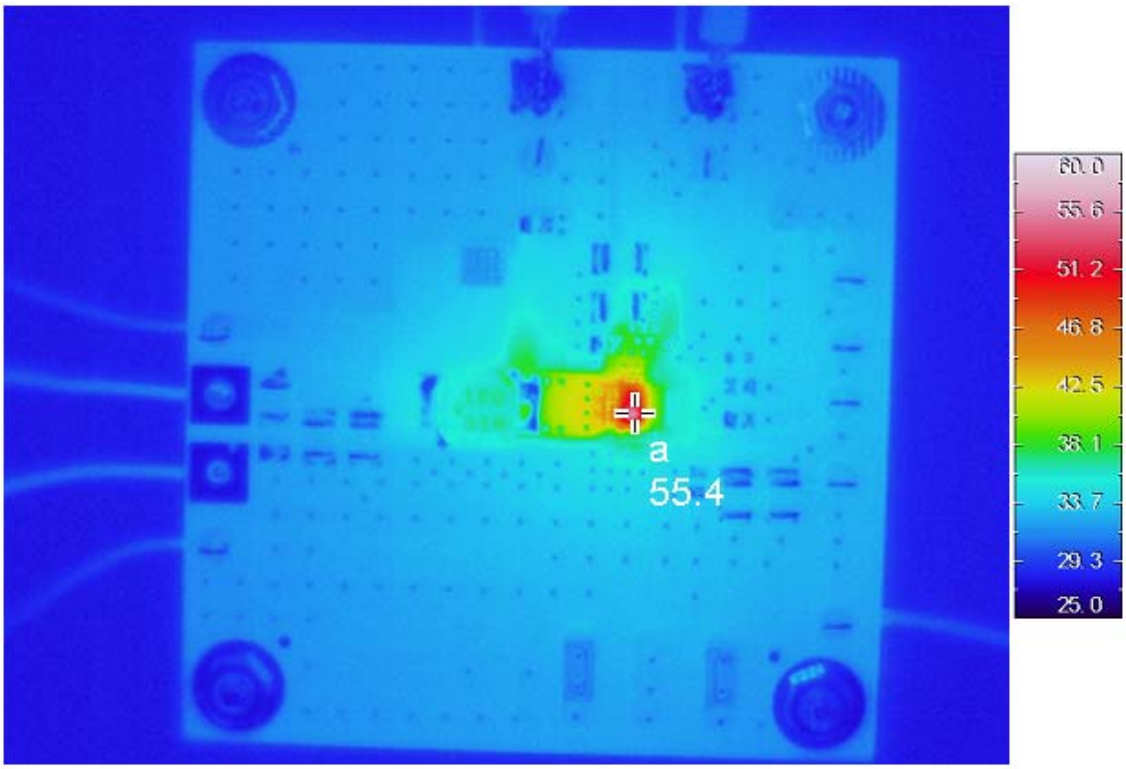




TYPICAL CHARACTERISTICS CURVES (Continued)

(9) Thermal Performance

Condition : VIN=12V , Vout = 1.05V , Frequency = 750kHz , ILoad = 3A , FCCM Mode



APPLICATIONS INFORMATION

Condition : Vout = 3.3 V, Frequency = 750 kHz, SKIP mode

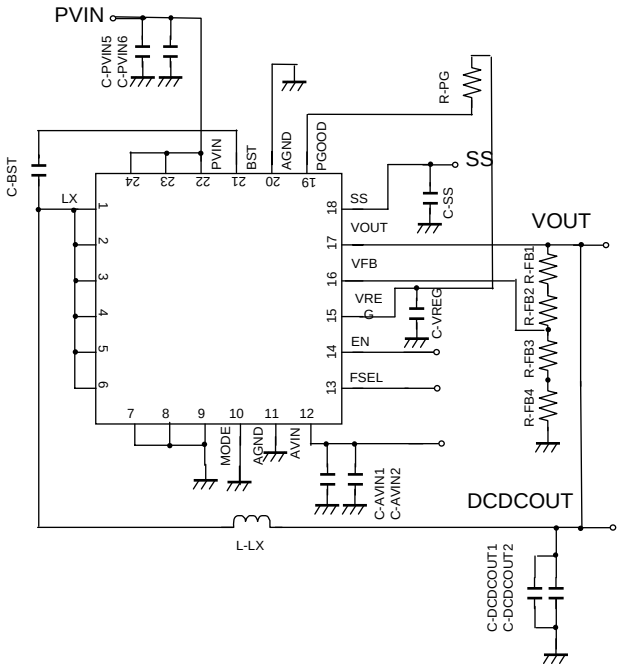


Figure : Application circuit

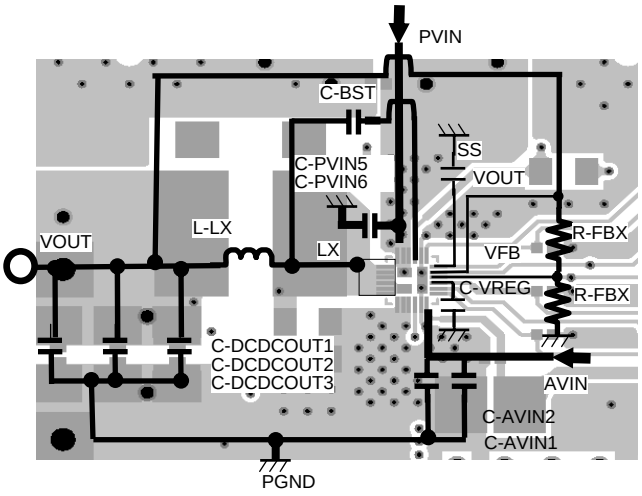


Figure : layout

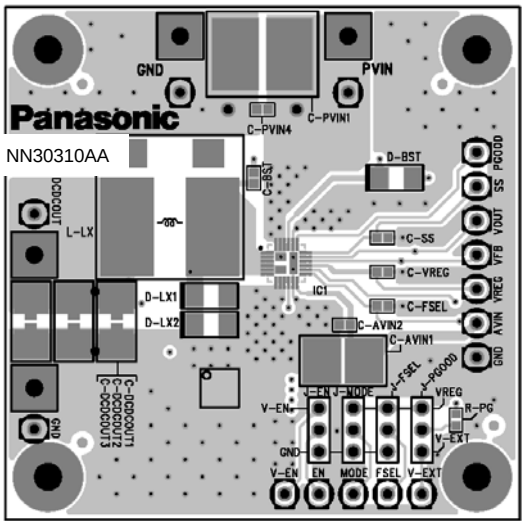


Figure Top Layer with silk screen
(Top View) with Evaluation board

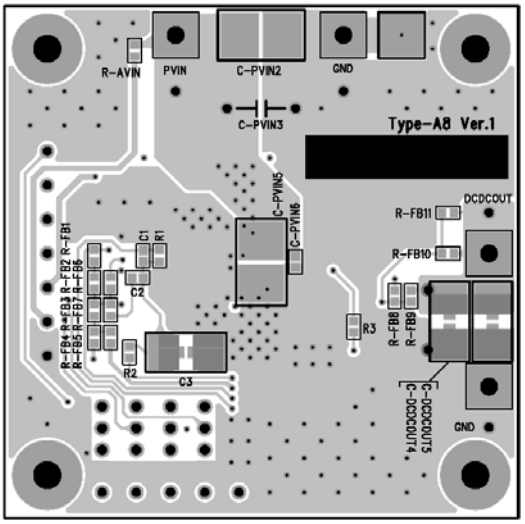


Figure Bottom Layer with silk screen
(Bottom View) with Evaluation board

Notes) This application circuit and layout is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

APPLICATIONS INFORMATION (Continued)

Reference Designator	QTY	Value	Manufacturer	Part Number	Note
C-AVIN1	2	10 µF	TAIYO YUDEN	UMK325AB7106MM-T	—
C-AVIN2	1	0.1 µF	Murata	GRM188R72A104KA35L	—
C-BST	1	0.1 µF	Murata	GRM188R72A104KA35L	—
C-DCDCOUT	2	22 µF	Murata	GRM32ER71E226KE15L	—
C-PVIN5	2	10 µF	TAIYO YUDEN	UMK325AB7106MM-T	—
C-PVIN6	1	0.1 µF	Murata	GRM188R72A104KA35L	—
C-SS	1	10 nF	Murata	GRM188R72A103KA01L	—
C-VREG	1	1.0 µF	Murata	GRM188R71E105KA12L	—
L-LX	1	1.0 µH	Panasonic	ETQP3W1R0WFN	FSEL GND (1250 kHz) OPEN (750 kHz)
		4.7 µH	Panasonic	ETQ3W4R7WFN	FSEL VREG (250 kHz)
R-FB1	1	3.3 kΩ	Panasonic	ERJ3EKF3301V	—
R-FB2	1	1.2 kΩ	Panasonic	ERJ3EKF1201V	—
R-RB3	1	1.0 kΩ	Panasonic	ERJ3EKF1001V	—
R-FB4	1	0	Panasonic	ERJ3GEY0R00V	—
R-PG	1	100 kΩ	Panasonic	ERJ3EKF1003V	—

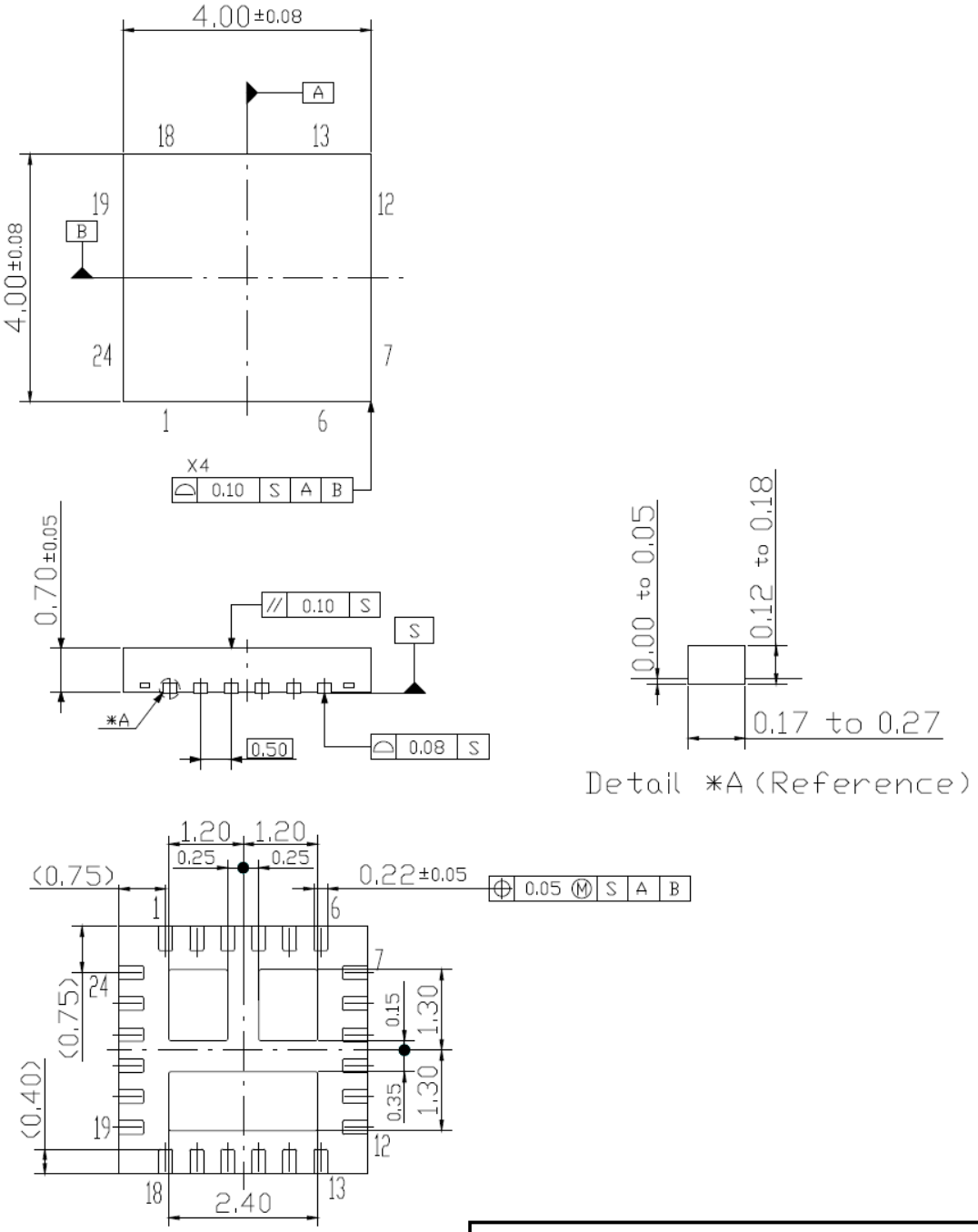
Figure : Recommended component

PACKAGE INFORMATION (Reference Data)

Outline Drawing

Package Code : HQFN024-A3-0404

Unit : mm



Body Material : Br/Sb Free Epoxy Resin
Lead Material : Cu Alloy
Lead Finish Method : Pd Plating

PACKAGE INFORMATION (Reference Data)

Power dissipation (Supplementary explanation)

[Experiment environment]

Power Dissipation (Technical Report) is a result in the experiment environment of SEMI standard conformity. (Ambient air temperature (Ta) is 25 degrees C)

[Supplementary information of PWB to be used for measurement]

The supplement of PWB information for Power Dissipation data (Technical Report) are shown below.

Indication	Total Layer	Resin Material
Glass-Epoxy	1-layer	FR-4
4-layer	4-layer	FR-4

[Notes about Power Dissipation (Thermal Resistance)]

Power Dissipation values (Thermal Resistance) depend on the conditions of the surroundings, such as specification of PWB and a mounting condition , and a ambient temperature. (Power Dissipation (Thermal Resistance) is not a fixed value.)

The Power Dissipation value (Technical Report) is the experiment result in specific conditions (evaluation environment of SEMI standard conformity) ,and keep in mind that Power Dissipation values (Thermal resistance) depend on circumference conditions and also change.

[Definition of each temperature and thermal resistance]

Ta : Ambient air temperature
※The temperature of the air is defined at the position where the convection, radiation, etc. don't affect the temperature value, and it's separated from the heating elements.

Tc : It's the temperature near the center of a package surface. The package surface is defined at the opposite side if the PWB.

Tj : Semiconductor element surface temperature (Junction temperature.)

Rth(j-c) : The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the package surface

Rth(c-a) : The thermal resistance (difference of temperature of per 1 Watts) between the package surface and the ambient air

Rth(j-a) : The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the ambient air

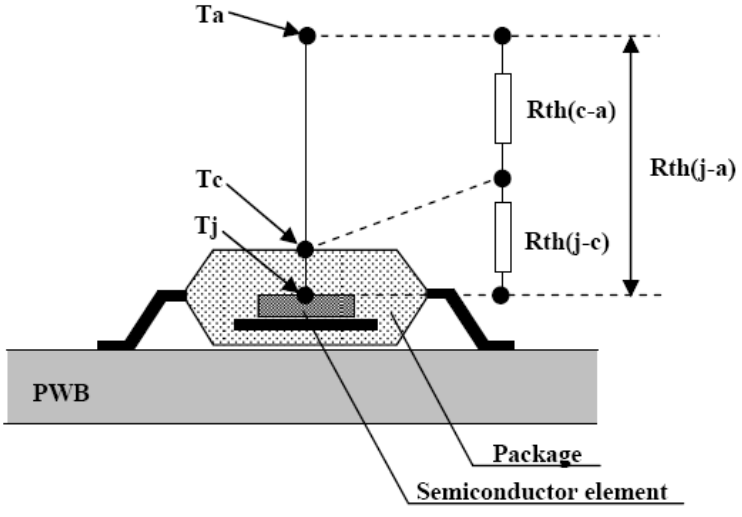


Fig1. Definition image

[Definition formula]

$$Tj = \{Rth(j\text{-}c) + Rth(c\text{-}a)\} \times P + Ta$$
$$= Rth(j\text{-}a) \times P + Ta$$

$$Rth(j\text{-}c) = \frac{Tj - Tc}{P} \quad (°C / W)$$

$$Rth(c\text{-}a) = \frac{Tc - Ta}{P} \quad (°C / W)$$

$$Rth(j\text{-}a) = \frac{Tj - Ta}{P} \quad (°C / W)$$

P : power (W)

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Be sure to read the notes to descriptions and the usage notes in the book.

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(4) Submarine transponder
(5) Control equipment for power plant
(6) Disaster prevention and security device
(7) Weapon
(8) Others : Applications of which reliability equivalent to (1) to (7) is required
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USAGE NOTES

1. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.

   Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

2. Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

3. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.

4. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

5. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.

6. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .

   And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.

7. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.

   Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.

8. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.

9. The product which has specified ASO (Area of Safe Operation) should be operated in ASO

10. Verify the risks which might be caused by the malfunctions of external components.

11. Connect the metallic plates on the back side of the LSI with their respective potentials (AGND, PVIN, LX). The thermal resistance and the electrical characteristics are guaranteed only when the metallic plates are connected with their respective potentials.

Request for your special attention and precautions in using the technical information and semiconductors described in this book

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