# R2A20169NP/SA/SP

8-bit 12ch D/A Converter with Buffer Amplifiers

R03DS0020EJ0300
Rev.3.00
Jul 25, 2013

## Description

The R2A20169 is an integrated circuit semiconductor of CMOS structure with 12 channels of built in D/A unnecessary and enabling configuration of a system with few component parts.
Serial data transfer type input can easily be used through a combination of three lines: DI, CLK, and LD.

Outputs incorporate buffer op-amps that have a drive capacity of 1 mA or above for both sink source, and can operate over the entire voltage range from almost ground to Vcc ( 0 to 5V ), making peripheral elements unnecessary and enabling configuration of a system with few component parts.
Very small QFN package is added to lineup. It is suitable for a small mounting and reduces the mounting area.

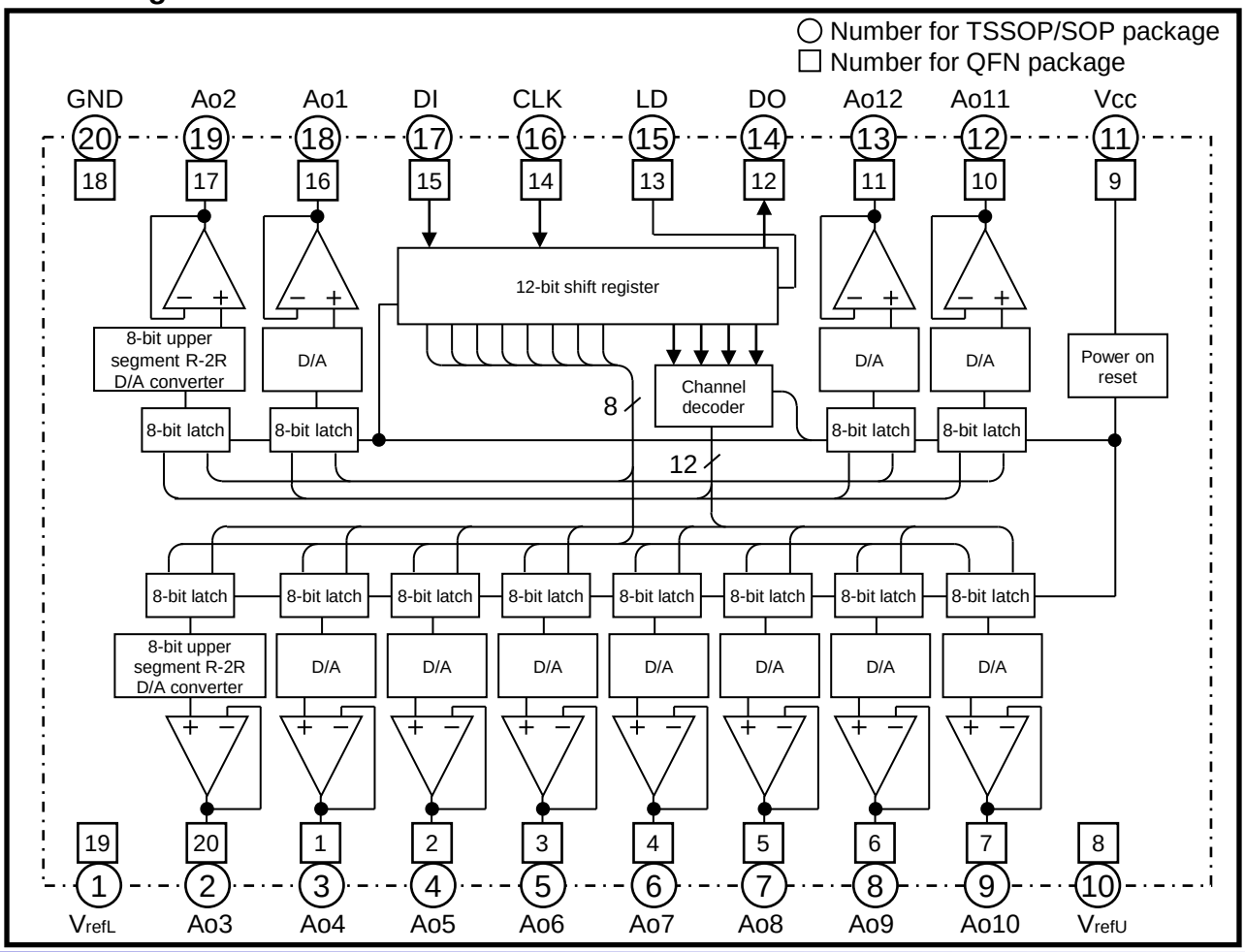
## Features

- Guarantee Nonlinearity error : +/-1.0LSB, Differential nonlinearity error : +/-0.7LSB
- Data transfer format: 12-bit serial data input type by 3 wire ( DI, SCK, LD )
- Output buffer op-amps: Operable over entire voltage range from almost ground to Vcc ( 0 to 5V )
- High output current capacity: +/-1mA or Higher
- Very small size package line-up: QFN-20 (pin pitch: 0.5mm), TSSOP-20 (pin pitch 0.65mm)

## Application

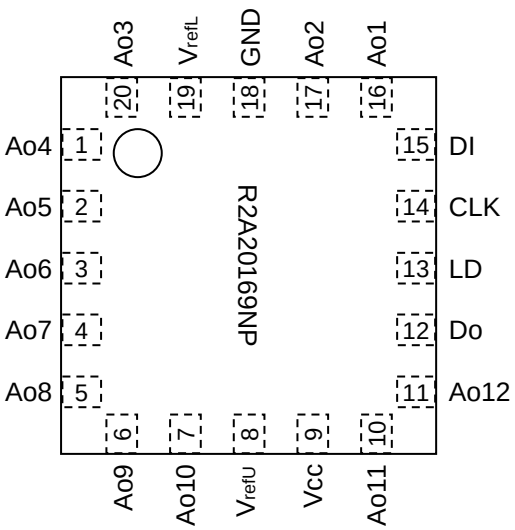
- Conversion from digital data to analog control data for home-use and industrial equipment.

## Block Diagram



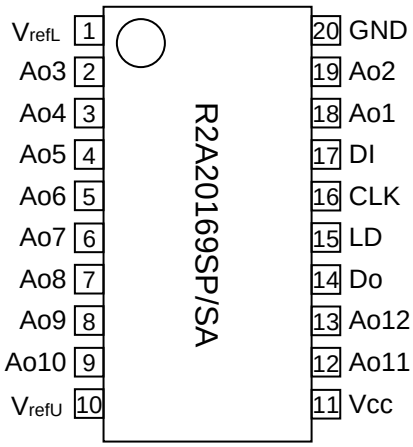
## Pin Arrangement

R2A20169NP (Top view)




Outline: PWQN0020KB-A [NP]

R2A20169SP/SA (Top view)




Outline: PRSP0020DD-B[SP]
PTSP0020JB-A [SA]

## Pin Description

| Pin No. | | Pin Name | Function |
|---|---|---|---|
| [QFN] | [TSSOP /SOP] | | |
| 15 | 17 | DI | Serial data input terminal.<br>(Input serial data with a 12-bit data length.) |
| 12 | 14 | Do | Serial data output terminal<br>(Data is sequentially output from the MSB bit.) |
| 14 | 16 | CLK | Serial clock input terminal<br>(Input signal from DI terminal is input to 12-bit shift register at rise of serial clock.) |
| 13 | 15 | LD | Load terminal<br>(When High level is input to LD terminal, value in 12-bit shift register is loaded into decoder and 8-bit latch.) |
| 16 | 18 | Ao1 | 8-bit resolution D/A converter output terminals<br>(After power-on, all channels are reset and DAC data 00h is output.) |
| 17 | 19 | Ao2 | |
| 20 | 2 | Ao3 | |
| 1 | 3 | Ao4 | |
| 2 | 4 | Ao5 | |
| 3 | 5 | Ao6 | |
| 4 | 6 | Ao7 | |
| 5 | 7 | Ao8 | |
| 6 | 8 | Ao9 | |
| 7 | 9 | Ao10 | |
| 10 | 12 | Ao11 | |
| 11 | 13 | Ao12 | |
| 9 | 11 | Vcc | Power supply terminal |
| 18 | 20 | GND | GND terminal |
| 8 | 10 | $V_{refU}$ | D/A converter upper reference voltage input terminal |
| 19 | 1 | $V_{refL}$ | D/A converter lower reference voltage input terminal |

## Absolute Maximum Ratings

(Ta= +25deg unless otherwise noted)

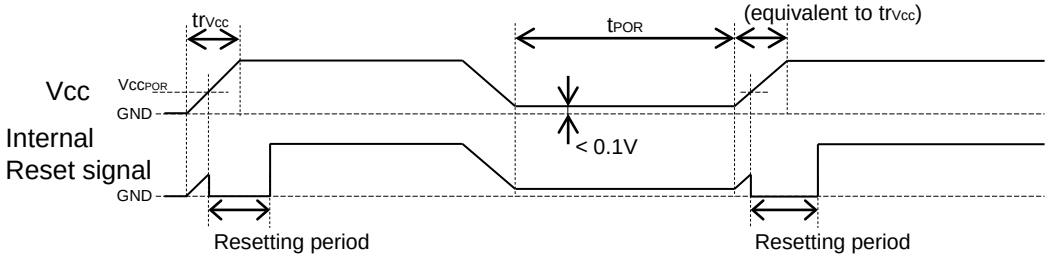
| Item | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | Vcc | | -0.3 to +6.5 | V |
| D/A converter upper reference voltage | $V_{refU}$ | | -0.3 to +6.5 | V |
| D/A converter lower reference voltage | $V_{refL}$ | | -0.3 to +6.5 | V |
| Buffer amplifier output current | $I_{AO}$ | Continuous | -2.0 to +2.0 | mA |
| Input voltage | Vin | | -0.3 to Vcc+0.3 <+6.5 | V |
| Output voltage | Vo | | -0.3 to Vcc+0.3 <+6.5 | V |
| Power dissipation | Pd | Ta= +85deg | 290(NP) / 150(SA) / 300(SP) | mW |
| Thermal derating factor | K theta | Ta> +25deg | 7.25(NP) / 3.75(SA) / 7.5(SP) | mW/deg |
| Operating temperature | Topr | | -30 to +85 | deg |
| Storage temperature | Tstg | | -40 to +125 | deg |

## Electrical Characteristics

**« Digital Part »** ( Vcc, $V_{refU}$ = +5V +/-10%, Vcc>$V_{refU}$, GND,$V_{refL}$ =0V, Ta= -30 to +85deg, Unless otherwise noted )

| Item | Symbol | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Supply voltage | Vcc | | 2.7 | 5.0 | 5.5 | V |
| Supply current | Icc | CLK = 1MHz, Vcc =5V, $I_{AO}$ =0µA | - | 0.6 | 1.8 | mA |
| Input leak current | $I_{ILK}$ | $V_{IN}$ = 0 to Vcc | -10 | - | 10 | µA |
| Input low voltage | $V_{IL}$ | | - | - | 0.2Vcc | V |
| Input high voltage | $V_{IH}$ | 4.0V < Vcc | 0.5Vcc | - | - | V |
| | | Vcc < 4.0V | 0.8Vcc | - | - | V |
| Output low voltage | $V_{OL}$ | 4.0V < Vcc, $I_{OL}$ =2.0 mA | - | - | 0.4 | V |
| | | Vcc < 4.0V, $I_{OL}$ =1.5 mA | - | - | 0.4 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = -400 µA | Vcc – 0.4 | - | - | V |
| Supply voltage rise time *1 | $tr_{Vcc}$ | Vcc = 0 ® 2.7V | 100 | - | - | µs |
| Internal reset operating voltage *1 | $Vcc_{POR}$ | Vcc = 0 ® 2.7V | - | 1.5 | 1.9 | V |
| Power supply restart interval (Power supply OFF à ON) *1 | $t_{POR}$ | Vcc < 0.1V | 1 | - | - | ms |

*1 : When power supply is turned on, internal circuit is initialized by power on reset circuit. But, if re-powered on quickly, initialize is not operate. So, keep the time period of re-powered on ($t_{POR}$).



**« Analog Part »** ( Vcc,$V_{refU}$ = +5V +/-10%, Vcc>$V_{refU}$, GND,$V_{refL}$=0V, Ta= -30 to +85deg, unless otherwise noted )

| Item | Symbol | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Current dissipation | $I_{refU}$ | $V_{refU}$=5V, $V_{refL}$=0V, $I_{AO}$=0µA, Data condition: at maximum current | - | 1.5 | 3.0 | mA |
| D/A converter upper reference voltage range *2 | $V_{refU}$ | Vcc ³ 4.5V | 3.5 | - | Vcc | V |
| | | Vcc < 4.5V | 0.7Vcc | - | Vcc | |
| D/A converter lower reference voltage range *2 | $V_{refL}$ | Vcc ³ 4.5V | GND | - | Vcc-3.5 | V |
| | | Vcc < 4.5V | GND | - | 0.3Vcc | |
| Buffer amplifier output voltage range | $V_{AO}$ | $I_{AO}$ = +/- 100 µA | 0.1 | - | Vcc – 0.1 | V |
| | | $I_{AO}$ = +/- 500 µA | 0.2 | - | Vcc – 0.2 | V |
| Buffer amplifier output drive range | $I_{AO}$ | Upper side saturation voltage = 0.3V, Lower side saturation voltage = 0.2V | -1.0 | - | 1.0 | mA |
| Differential nonlinearity | $S_{DL}$ | $V_{refU}$ = 4.79V, $V_{refL}$ = 0.95V, Vcc = 5.5V (15mV/LSB), Without load ($I_{AO}$ =0µA) | -0.7 | - | 0.7 | LSB |
| Nonlinearity | $S_L$ | | -1.0 | - | 1.0 | LSB |
| Zero code error | $S_{ZERO}$ | | -2.0 | - | 2.0 | LSB |
| Full scale error | $S_{FULL}$ | | -2.0 | - | 2.0 | LSB |
| Output capacitive load | Co | | - | - | 0.1 | µF |
| Buffer amplifier output impedance | Ro | | - | 5.0 | - | ohm |

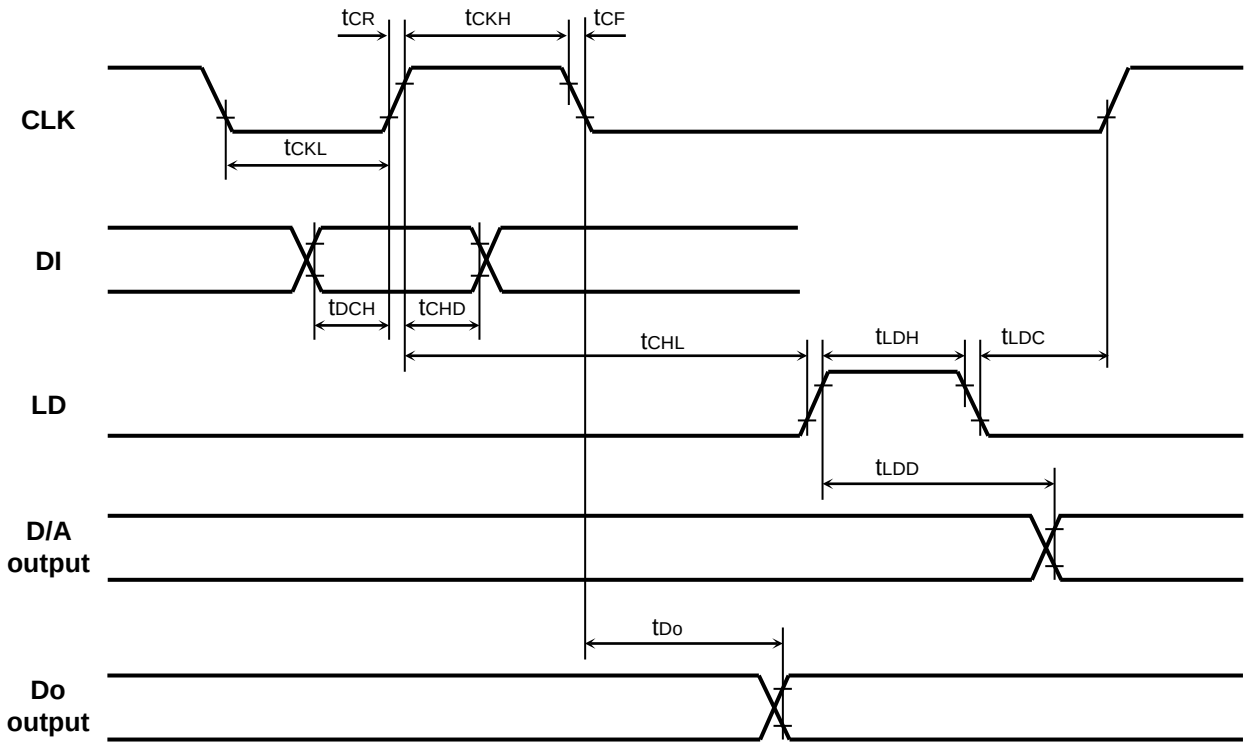
*2 : The output does not necessary be the value with the reference voltage setting range.
The output value is determined by the buffer amplifier output voltage range ($V_{AO}$).

## AC Characteristics

( Vcc, $V_{refU}$ = +5V +/-10%, Vcc >$V_{refU}$, GND=$V_{refL}$ = 0V, Ta = -30 to +85deg, unless otherwise noted )

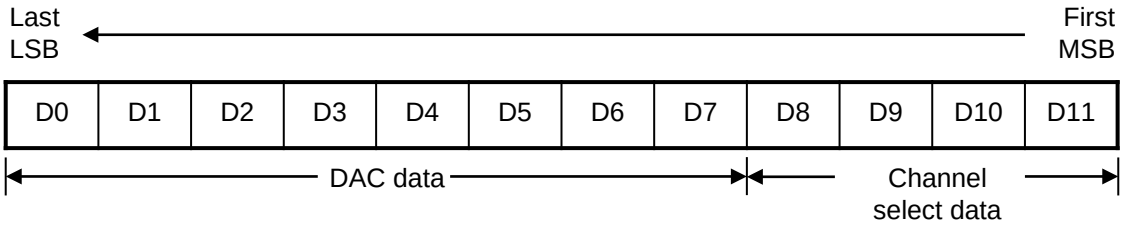
| Item | Symbol | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Clock frequency | $f_{CLK}$ | | - | 1.0 | 10 | MHz |
| Clock low pulse width | $t_{CKL}$ | | 40 | - | - | ns |
| Clock high pulse width | $t_{CKH}$ | | 40 | - | - | ns |
| Clock rise time | $t_{CR}$ | | - | - | 200 | ns |
| Clock fall time | $t_{CF}$ | | - | - | 200 | ns |
| Data setup time | $t_{DCH}$ | | 4 | - | - | ns |
| Data hold time | $t_{CHD}$ | | 30 | - | - | ns |
| LD setup time | $t_{CHL}$ | | 40 | - | - | ns |
| LD hold time | $t_{LDC}$ | | 40 | - | - | ns |
| LD high pulse width | $t_{LDH}$ | | 40 | - | - | ns |
| Data output delay time | $t_{DO}$ | $C_L$ < 100 pF | -10 | - | 50 | ns |
| D/A output settling time | $t_{LDD}$ | Ta=25deg, $C_L$<100pF, $V_{AO}$: 0.5¬ ® 4.5V, The time until the output becomes the final value of 1/2 LSB. | - | - | 150 | µs |

## Timing Chart




(Note) Timing chart above is a schematic representation of the timing of each signal type.
CLK signal input is High or Low regardless, LD signal High input is enabled.

## Digital Data Format



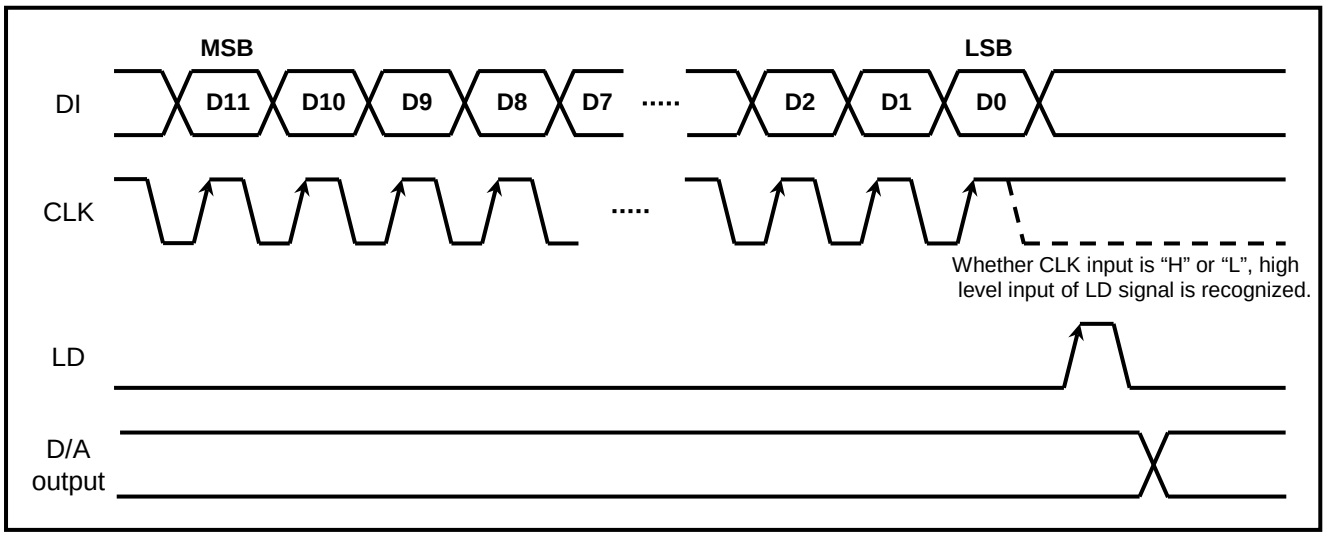

**Channel select data**

| D8 | D9 | D10 | D11 | Chanel Selection |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Don't care |
| 0 | 0 | 0 | 1 | Ao1 select |
| 0 | 0 | 1 | 0 | Ao2 select |
| 0 | 0 | 1 | 1 | Ao3 select |
| 0 | 1 | 0 | 0 | Ao4 select |
| 0 | 1 | 0 | 1 | Ao5 select |
| 0 | 1 | 1 | 0 | Ao6 select |
| 0 | 1 | 1 | 1 | Ao7 select |
| 1 | 0 | 0 | 0 | Ao8 select |
| 1 | 0 | 0 | 1 | Ao9 select |
| 1 | 0 | 1 | 0 | Ao10 select |
| 1 | 0 | 1 | 1 | Ao11 select |
| 1 | 1 | 0 | 0 | Ao12 select |
| 1 | 1 | 0 | 1 | Don't care |
| 1 | 1 | 1 | 0 | Don't care |
| 1 | 1 | 1 | 1 | Don't care |

**DAC data**

| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D/A Output |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $(V_{refU} – V_{refL}) / 256 \times 1 + V_{refL}$ |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $(V_{refU} – V_{refL}) / 256 \times 2 + V_{refL}$ |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | $(V_{refU} – V_{refL}) / 256 \times 3 + V_{refL}$ |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | $(V_{refU} – V_{refL}) / 256 \times 4 + V_{refL}$ |
| : | : | : | : | : | : | : | : | : |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | $(V_{refU} – V_{refL}) / 256 \times 255 + V_{refL}$ |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | $V_{refU}$ |

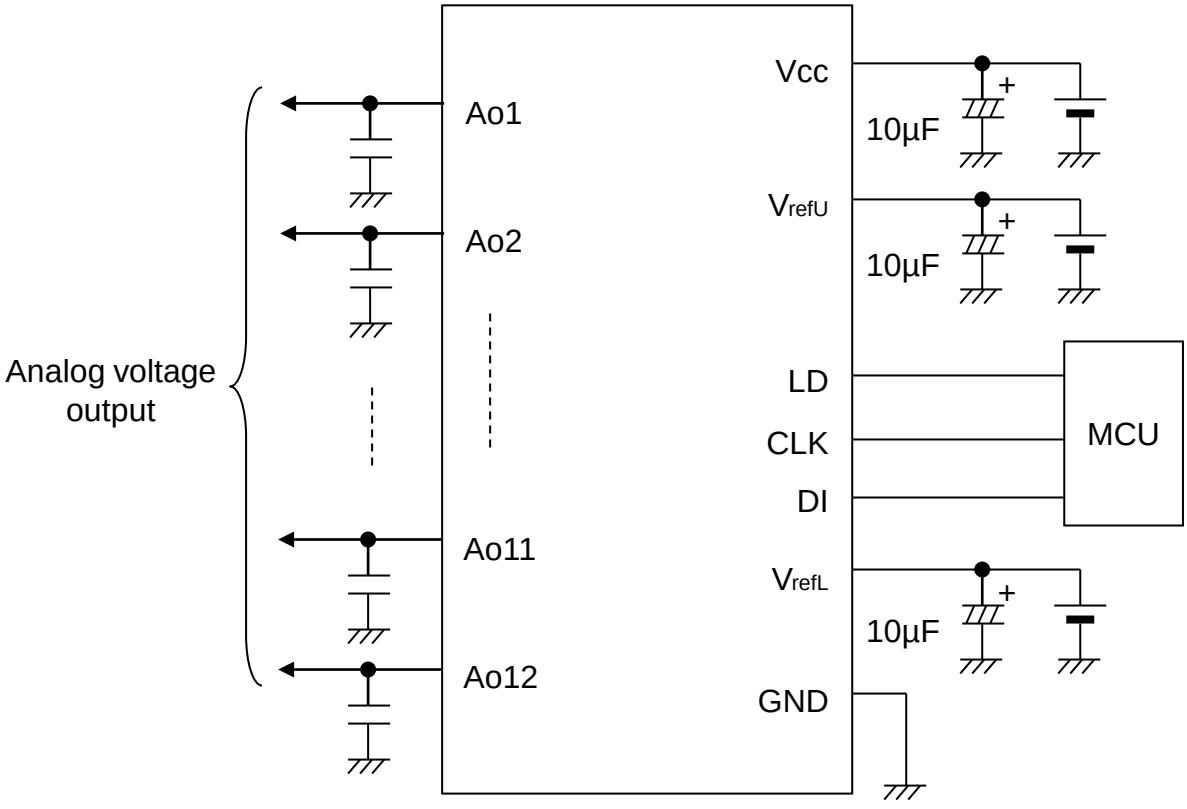
## Data Timing Chart ( Model )




## Precaution For use

- There are three terminals (Vcc, $V_{refU}$, $V_{refL}$) that should be impressed a constant voltage. When ripple or spike noise is input to this terminal, there is fear that the accuracy of D/A conversion becomes lower and this IC malfunction. So, when use this IC, please connect capacitor between these terminals (Vcc, $V_{refU}$, $V_{refL}$) and GND for stable D/A conversion.
- This IC’s output amplifier has an advantage to capacitive load, So, it’s no problem at device action when connect capacitor ( 0.1µF Max ) among output to GND for every noise elimination.

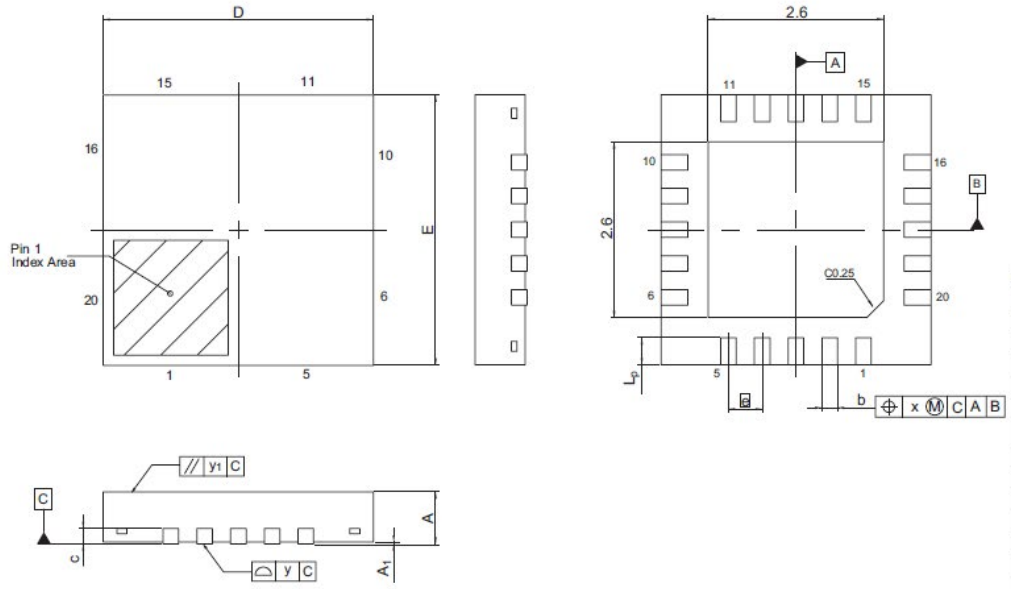
## Standard Application Circuit



## Package Dimensions

### PWQN0020KB-A [NP]

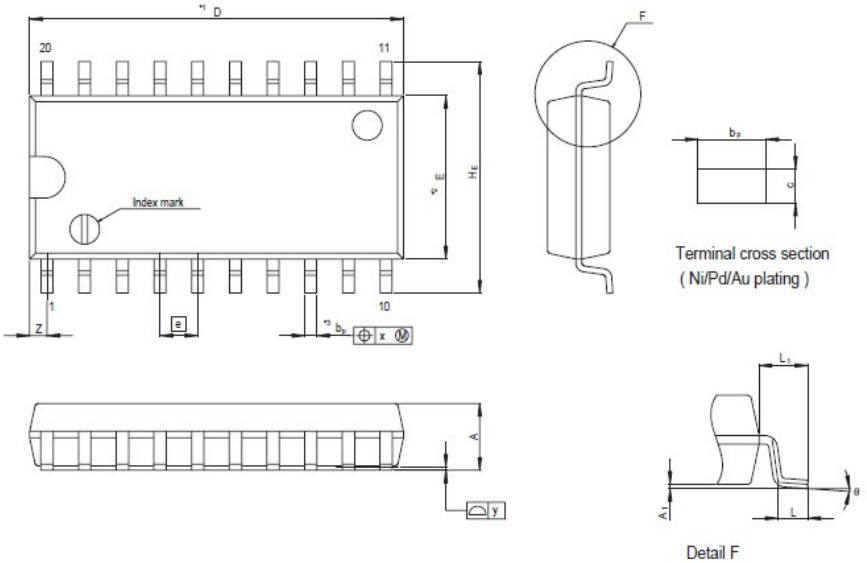
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-HWQFN20-4x4-0.50 | PWQN0020KB-A | — | 0.037g |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 3.90 | 4.00 | 4.10 |
| E | 3.90 | 4.00 | 4.10 |
| $A_2$ | — | — | — |
| A | — | — | 0.80 |
| $A_1$ | 0 | — | 0.05 |
| b | 0.18 | 0.23 | 0.28 |
| $b_1$ | — | — | — |
| e | — | 0.5 | — |
| $L_p$ | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| $y_1$ | — | — | 0.1 |
| t | — | — | — |
| $H_D$ | — | — | — |
| $H_E$ | — | — | — |
| $Z_D$ | — | — | — |
| $Z_E$ | — | — | — |
| c | — | 0.20 | — |
| $c_1$ | — | — | — |

### PRSP0020DD-B [SP]

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-SOP20-5.5x12.6-1.27 | PRSP0020DD-B | FP-20DAV | 0.31g |

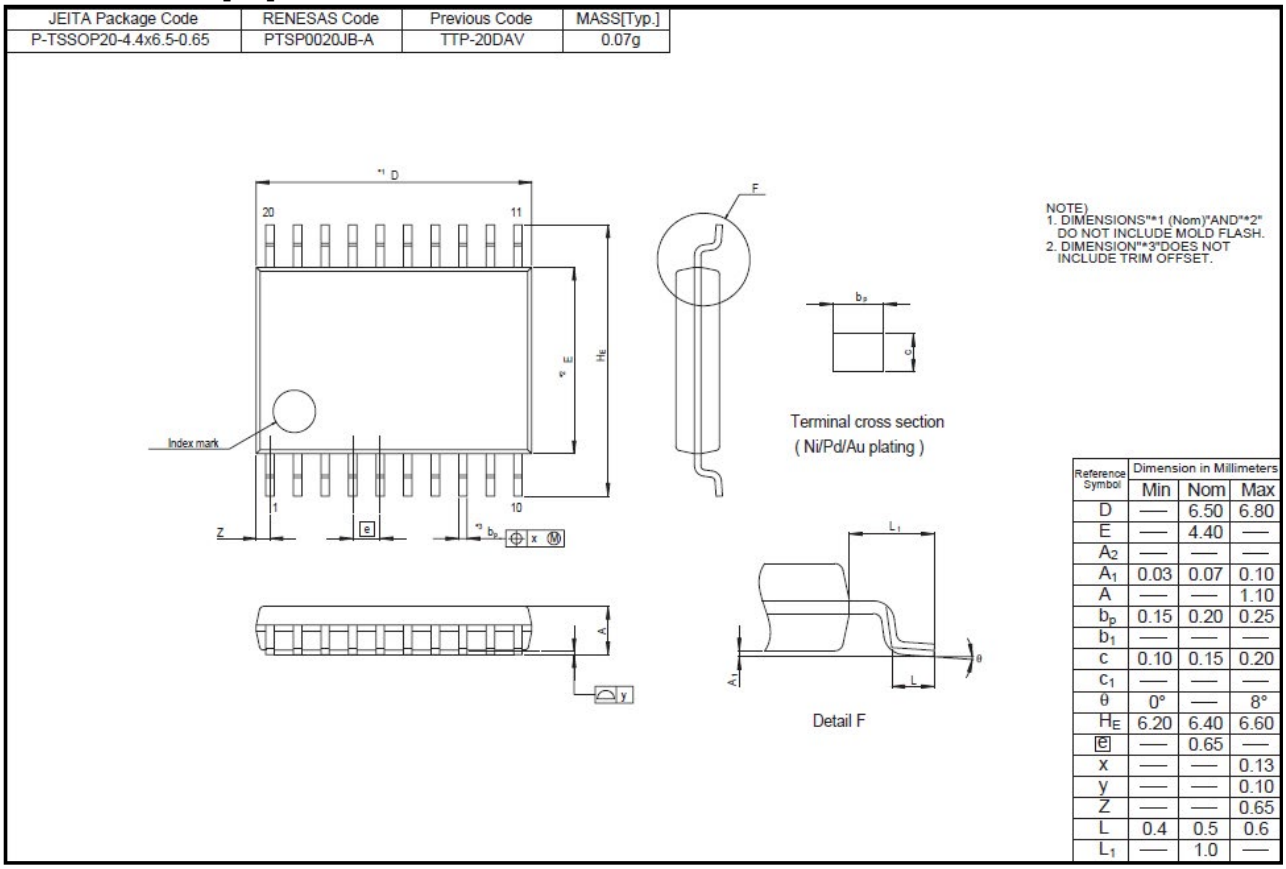



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 12.60 | 13.0 |
| E | — | 5.50 | — |
| $A_2$ | — | — | — |
| $A_1$ | 0.00 | 0.10 | 0.20 |
| A | — | — | 2.20 |
| $b_p$ | 0.34 | 0.40 | 0.46 |
| $b_1$ | — | — | — |
| c | 0.15 | 0.20 | 0.25 |
| $c_1$ | — | — | — |
| θ | 0° | — | 8° |
| $H_E$ | 7.50 | 7.80 | 8.00 |
| e | — | 1.27 | — |
| x | — | — | 0.12 |
| y | — | — | 0.15 |
| Z | — | — | 0.80 |
| L | 0.50 | 0.70 | 0.90 |
| $L_1$ | — | 1.15 | — |

**PTSP0020JB-A [SA]**

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-TSSOP20-4.4x6.5-0.65 | PTSP0020JB-A | TTP-20DAV | 0.07g |




NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 6.50 | 6.80 |
| E | — | 4.40 | — |
| $A_2$ | — | — | — |
| $A_1$ | 0.03 | 0.07 | 0.10 |
| A | — | — | 1.10 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | — | — |
| c | 0.10 | 0.15 | 0.20 |
| $c_1$ | — | — | — |
| θ | 0° | — | 8° |
| $H_E$ | 6.20 | 6.40 | 6.60 |
| e | — | 0.65 | — |
| x | — | — | 0.13 |
| y | — | — | 0.10 |
| Z | — | — | 0.65 |
| L | 0.4 | 0.5 | 0.6 |
| $L_1$ | — | 1.0 | — |

## Ordering Information

| Order part No. | Package Name | Package Code | Package type No. | Packing/Quantity |
|---|---|---|---|---|
| R2A20169SP#W5 | SOP-20 | PRSP0020DD-B | SP | Embossed Taping/2,000 pcs. |
| R2A20169SA#W5 | TSSOP-20 | RTSP0020JB-A | SA | Embossed Taping/2,000 pcs. |
| R2A20169NP#W5 | QFN-20 | PWQN0020KB-A | NP | Embossed Taping/2,500 pcs. |

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