# LM2759 1A Switched Capacitor Flash LED Driver with I²C Compatible Interface

**Check for Samples: LM2759**

## FEATURES

- **Up to 1A Output Current**
- **Solution Area < 22 mm²**
- **No Inductor Required**
- **90% Peak Efficiency**
- **Adaptive 1x, 1.5x and 2x Gains for Maximum Efficiency**
- **Load Disconnect in Shutdown**
- **Accurate Input Current Control During Gain Transitions**
- **Flash Time-Out**
- **TX Input Pin Ensures Synchronization with RF Power Amplifier Pulse**
- **Torch, Flash, and Indicator Modes**
- **External Flash Enable via Strobe Input Pin**
- **Strobe Input Disable via I²C**
- **Programmable Flash Pulse Duration, and Torch and Flash Currents via I²C-Compatible Interface**
- **1MHz Constant Frequency Operation**
- **Low Profile 12–Pin WSON (3mm x 3mm x 0.8mm)**

## APPLICATIONS

- **Camera Flash in Cellular Phones**

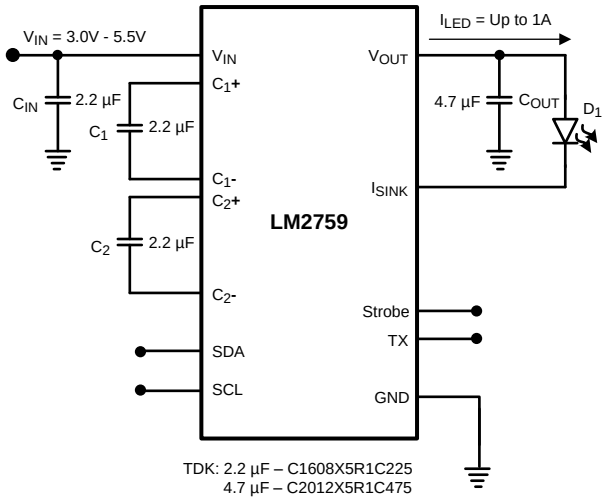
## DESCRIPTION

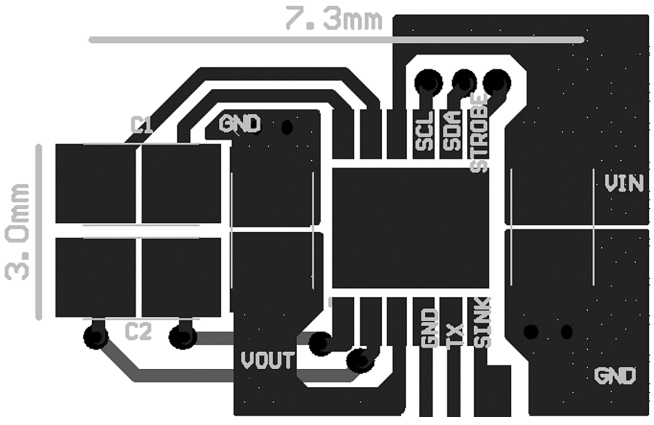
LM2759 is an integrated low-noise, high-current switched capacitor DC/DC converter with a regulated current source. The device requires only four small ceramic capacitors making the total solution area less than 22 mm² and the height less than 1 mm. The LM2759 is capable of driving loads up to 1A from a single-cell Li-Ion battery. Maximum efficiency is achieved over the input voltage range by actively selecting the proper gain based on the LED forward voltage and current requirements.

The LED current can be programmed up to 1A via an I²C-compatible interface, along with eight selectable Flash Time-Out durations. One high-current Flash LED can be driven either in a high-power Flash mode or a low-power Torch mode. The Strobe pin allows the flash to be toggled via a Flash enable signal from a camera module. The TX input pin limits the Flash LED current to the Torch current level during a RF PA pulse, to reduce high loads on the battery. Internal soft-start circuitry limits the amount of inrush current during start-up.

LM2759 is offered in a small 12-pin thermally enhanced WSON package.

### Typical Application Circuit




Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2008–2013, Texas Instruments Incorporated

## Connection Diagram

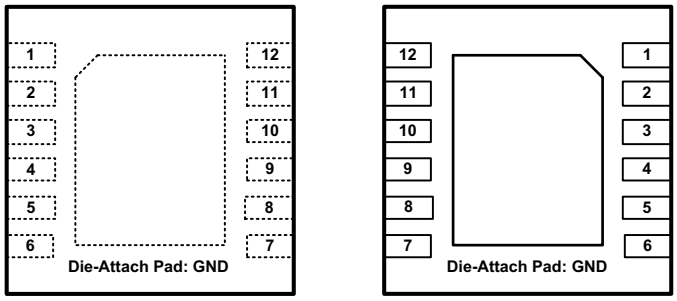



**Figure 1. 12-Pin WSON Package**
**3mm x 3mm x 0.8mm**
**Package Number DQB0012A**

### PIN DESCRIPTIONS

| Pin | Name | Description |
|---|---|---|
| 10 | $V_{IN}$ | Input voltage connection. |
| 3 | $V_{OUT}$ | Charge pump regulated output. |
| 12 | C1− | Flying capacitor connections. |
| 11 | C1+ | |
| 2 | C2+ | |
| 1 | C2− | |
| 4 | GND | Ground connection. |
| 6 | $I_{SINK}$ | Regulated current sink input. |
| 8 | SDA | Serial data I/O pin. |
| 7 | Strobe | Manual flash enable pin. Flash will remain on for the duration that the Strobe pin is held high or when the Flash Timeout occurs, whichever comes first. |
| 5 | TX | Transmission pulse Flash interrupt pin. High = RF PA pulse active, LED current reduced to Torch level, Low = RF PA pulse off, LED at full programmed current level. |
| 9 | SCL | Serial clock pin. |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.


Copyright © 2008–2013, Texas Instruments Incorporated

## Absolute Maximum Ratings[1][2][3]

| | | |
|---|---|---|
| $V_{IN}$ pin: Voltage to GND | | -0.3V to 6.0V |
| Strobe, TX, SDA, SCL, $I_{SINK}$ pins: Voltage to GND | | -0.3V to ($V_{IN}$ + 0.3V) w/ 6.0V max |
| Continuous Power Dissipation[4] | | Internally Limited |
| Junction Temperature ($T_{J-MAX}$) | | 150°C |
| Storage Temperature Range | | -65°C to 150°C |
| Maximum Lead Temp. (Soldering) | | [5] |
| ESD Rating | Human Body Model[6] | 2.5KV |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential to the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at $T_J$=150°C (typ.) and disengages at $T_J$ = 120°C (typ.).
(5) For detailed soldering specifications and information, please refer to Texas Instruments Application Note AN-1187 (SNOA401).
(6) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. (MIL-STD-883 3015.7)

## Operating Ratings[1][2]

| | |
|---|---|
| Input Voltage Range | 2.7V to 5.5V |
| LED Voltage Range | 2.0V to 4.0V |
| Junction Temperature Range ($T_J$) | -30°C to +125°C |
| Ambient Temperature Range ($T_A$)[3] | -30°C to +85°C |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential to the GND pin.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A-MAX}$) is dependent on the maximum operation junction temperature ($T_{J-MAX-OP}$ = 125ºC), the maximum power dissipation of the device in the application ($P_{D-MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($\theta_{JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

## Thermal Information

| | |
|---|---|
| Junction-to-Ambient Thermal Resistance, ($\theta_{JA}$), [1] | 36.7°C/W |

(1) Junction-to-ambient thermal resistance ($\theta_{JA}$) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4–layer FR-4 board measuring 102 mm x 76 mm x 1.6 mm with a 2x1 array of thermal vias. The ground plane on the board is 50 mm x 50 mm. Thickness of copper layers are 53µm/35µm/35µm/53µm (1.5oz/1oz/1oz/1.5oz). Ambient temperature in simulation is 22°C, still air. Power dissipation is 1W.The value of $\theta_{JA}$ of this product in the WSON package could fall in a range as wide as 30ºC/W to 150ºC/W (if not wider), depending on PWB material, layout, and environmental conditions. In applications where high maximum power dissipation exists (high $V_{IN}$, high $I_{OUT}$), special care must be paid to thermal dissipation issues. For more information on these topics, please refer to Application Note AN-1187 (SNOA401): and the *Power Efficiency and Power Dissipation* section of this datasheet.

Copyright © 2008–2013, Texas Instruments Incorporated

## Electrical Characteristics[1][2]

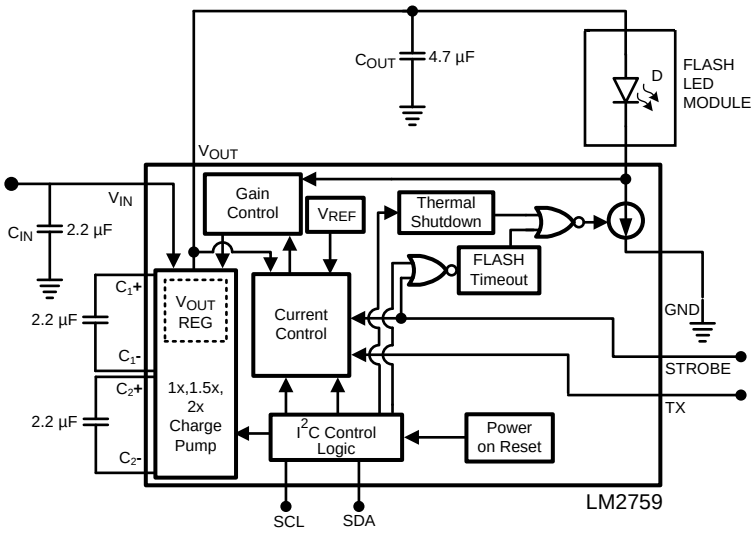
Limits in standard typeface are for $T_J$ = 25°C. Limits in **boldface** type apply over the full operating junction temperature range (-30°C ≤ $T_J$ ≤ +125 °C). Unless otherwise noted, specifications apply to the LM2759 Typical Application Circuit (pg.1) with $V_{IN}$ = 3.6V, $V_{TX}$ = 0V, $V_{STROBE}$ = 0V, $C_{IN}$ = $C_1$ = $C_2$ = 2.2 µF, $C_{OUT}$ = 4.7 µF.[3]

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LED}$ | LED Current Sink Accuracy | Flash Mode<br>ADDR xB0 = 0x02 | **198<br>−10%** | 220 | **242<br>+10%** | mA |
| $I_{FLASH}$ | Max Flash Output Current | Flash Mode<br>ADDR xB0 = 0x0F | | 1 | | A |
| $V_{GDX}$ | Gain Transition Voltage Threshold on $I_{SINK}$ | $I_{LED}$ = 500mA<br>($V_{ISINK}$ falling) | | 350 | | mV |
| $V_{OUT}$ | Output Voltage | 1x Mode, $I_{OUT}$ = 0 mA ($V_{IN}$ >$V_{OUT}$)[4] | | 4.7 | **4.9** | V |
| | | 1.5x Mode, $I_{OUT}$ = 0 mA | | 4.7 | **4.9** | |
| | | 2x Mode, $I_{OUT}$ = 0 mA | | 5.1 | **5.4** | |
| $R_{OUT}$ | x1 Mode Output Impedance | $I_{OUT}$ = 200mA, $V_{IN}$ = 3.3V | | 0.33 | | Ω |
| | 1.5x Mode Output Impedance | $I_{OUT}$ = 500mA, $V_{IN}$ = 3.3V | | 1.9 | | |
| | x2 Mode Output Impedance | | | 2.25 | | |
| $F_{SW}$ | Switching Frequency | 2.7V ≤ $V_{IN}$ ≤ 5.5V | **0.7** | 1 | **1.3** | MHz |
| $V_{IH}$ | Input Logic High | Pins: TX, Strobe | **1.26** | | | V |
| $V_{IL}$ | Input Logic Low | Pins: TX, Strobe | | | **0.7** | V |
| $I_Q$ | Quiescent Current | $I_{OUT}$ = 0 mA, 1x Mode | | 0.6 | **0.9** | mA |
| | | $I_{OUT}$ = 0 mA, 1.5x Mode | | 3.4 | **4.0** | |
| | | $I_{OUT}$ = 0 mA, 2x Mode | | 5.9 | **7.0** | |
| $I_{SD}$ | Shutdown Current | Device Disabled<br>2.7V ≤ $V_{IN}$ ≤ 5.5V | | 5.8 | **9.7** | µA |
| **$I^2C$ Compatible Interface Voltage Specifications (SCL, SDA)** | | | | | | |
| $V_{IL}$ | Input Logic Low “0” | 2.7V ≤ $V_{IN}$ ≤ 5.5V | | | **0.72** | V |
| $V_{IH}$ | Input Logic High “1' | 2.7V ≤ $V_{IN}$ ≤ 5.5V | **1.25** | | | V |
| $V_{OL}$ | Output Logic Low “0” | $I_{LOAD}$ = 3 mA | | | **300** | mV |
| **$I^2C$ Compatible Interface Timing Voltage Specifications (SCL, SDA)[5]** | | | | | | |
| $t_1$ | SCL (Clock Period) | | **2.5** | | | µs |
| $t_2$ | Data in Setup Time to SCL High | | **100** | | | ns |
| $t_3$ | Data Out Stable After SCL Low | | **0** | | | ns |
| $t_4$ | SDA Low Setup Time to SCL Low (Start) | | **100** | | | ns |
| $t_5$ | SDA High Hold Time After SCL High (Stop) | | **100** | | | ns |

(1) All voltages are with respect to the potential to the GND pin.
(2) Min and Max limits are specified by design, test, or statistical analysis. Typical (Typ) numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: $V_{IN}$ = 3.6V and $T_A$ = 25°C.
(3) $C_{IN}$, $C_{OUT}$, $C_1$, $C_2$: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.
(4) For input voltage below the regulation target during the gain of 1x, the output voltage will typically be equal to the input voltage.
(5) SCL and SDA should be glitch-free in order for proper brightness control to be realized.


Copyright © 2008–2013, Texas Instruments Incorporated

## Block Diagram



## Typical Performance Characteristics

Unless otherwise specified: $T_A$ = 25°C, $V_{IN}$ = 3.6V, $C_{IN}$ = $C_1$ = $C_2$ = 2.2µF, $C_{OUT}$ = 4.7µF. Capacitors are low-ESR multi-layer ceramic capacitors (MLCC's). Luxeon PWF3 Flash LED.

**Efficiency vs $V_{IN}$**

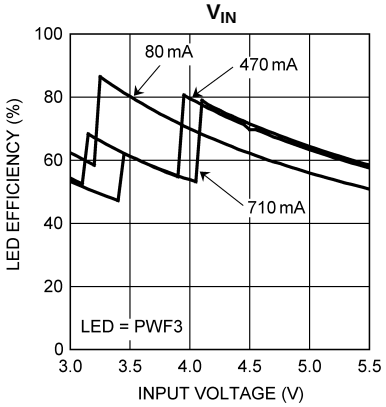



Figure 2.

**Input Current vs $V_{IN}$**

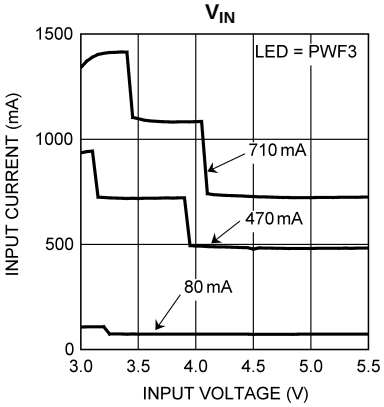



Figure 3.

**Quiescent Current vs $V_{IN}$, Gain = 1X**

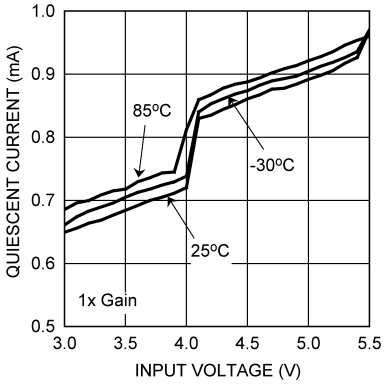



Figure 4.

**Quiescent Current vs $V_{IN}$, Gain = 2X**

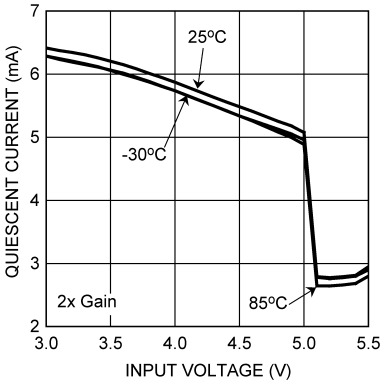



Figure 5.

**$I_{LED}$ vs $V_{ISINK}$**

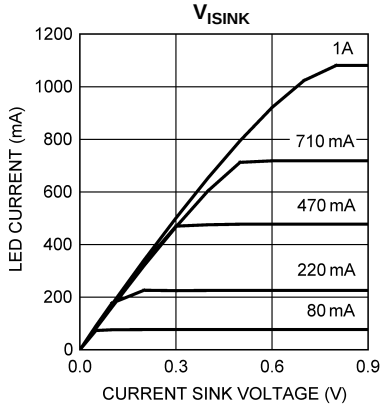



Figure 6.

**Shutdown Current vs $V_{IN}$**

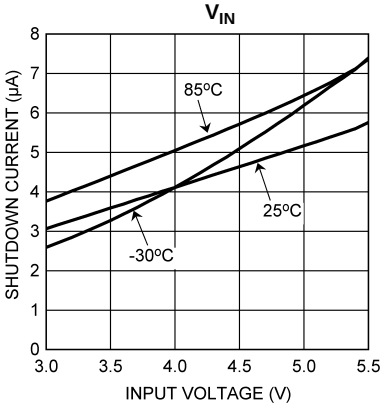



Figure 7.


Copyright © 2008–2013, Texas Instruments Incorporated

## Typical Performance Characteristics (continued)

Unless otherwise specified: $T_A$ = 25°C, $V_{IN}$ = 3.6V, $C_{IN}$ = $C_1$ = $C_2$ = 2.2µF, $C_{OUT}$ = 4.7µF. Capacitors are low-ESR multi-layer ceramic capacitors (MLCC's). Luxeon PWF3 Flash LED.

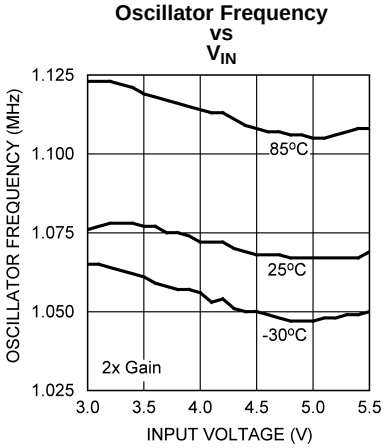



**Figure 8.**

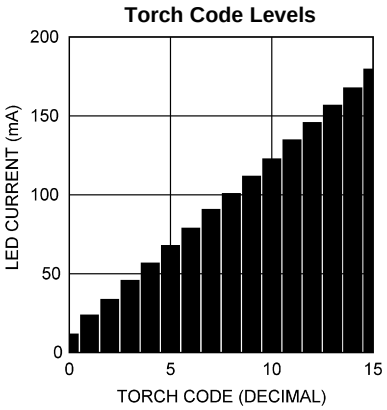



**Figure 9.**

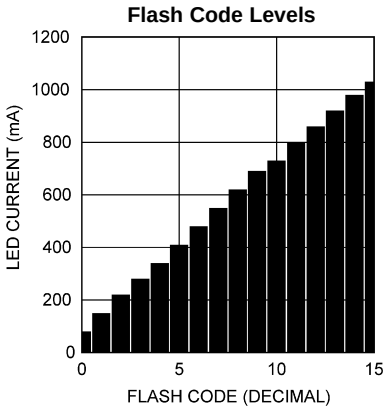
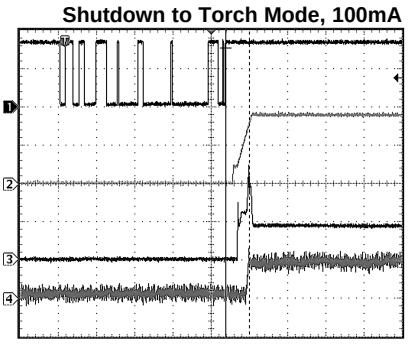
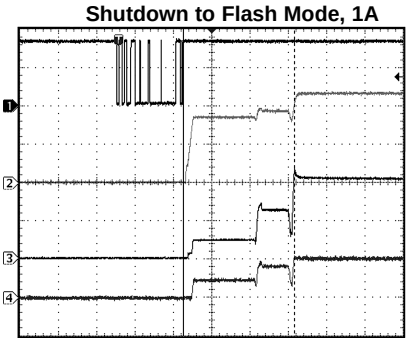



**Figure 10.**



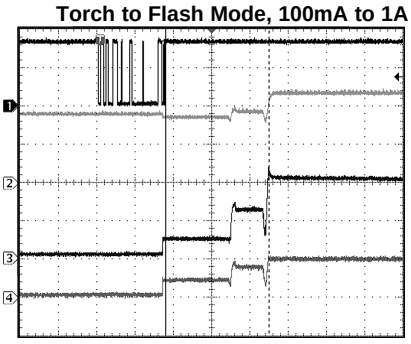

CH1: SDA; Scale: 2V/Div, DC Coupled
CH2: $V_{OUT}$; Scale: 2V/Div, DC Coupled
CH3: $I_{IN}$; Scale: 100mA/Div, DC Coupled
CH4: $I_{LED}$; Scale: 100mA/Div, DC Coupled
Time scale: 400µs/Div

**Figure 11.**




CH1: SDA; Scale: 2V/Div, DC Coupled
CH2: $V_{OUT}$; Scale: 2V/Div, DC Coupled
CH3: $I_{IN}$; Scale: 1A/Div, DC Coupled
CH4: $I_{LED}$; Scale: 1A/Div, DC Coupled
Time scale: 1ms/Div

**Figure 12.**




CH1: SDA; Scale: 2V/Div, DC Coupled
CH2: $V_{OUT}$; Scale: 2V/Div, DC Coupled
CH3: $I_{IN}$; Scale: 1A/Div, DC Coupled
CH4: $I_{LED}$; Scale: 1A/Div, DC Coupled
Time scale: 1ms/Div

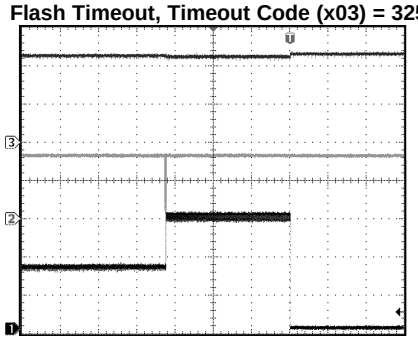
**Figure 13.**

Copyright © 2008–2013, Texas Instruments Incorporated

## Typical Performance Characteristics (continued)

Unless otherwise specified: $T_A$ = 25°C, $V_{IN}$ = 3.6V, $C_{IN}$ = $C_1$ = $C_2$ = 2.2µF, $C_{OUT}$ = 4.7µF. Capacitors are low-ESR multi-layer ceramic capacitors (MLCC's). Luxeon PWF3 Flash LED.

**Flash Timeout, Timeout Code (x03) = 325ms**



**Torch Level (x0F) = 180mA, Flash Level (x05) = 410mA**
**CH1(bottom): $I_{IN}$; Scale: 200mA/Div, DC Coupled**
**CH2(middle): SDA; Scale: 2V/Div, DC Coupled**
**CH3(top): $V_{OUT}$; Scale: 2V/Div, DC Coupled**
**Time scale: 100ms/Div**

**Figure 14.**


Copyright © 2008–2013, Texas Instruments Incorporated

# APPLICATION INFORMATION

## CIRCUIT DESCRIPTION

The LM2759 is an adaptive CMOS charge pump with gains of 1x, 1.5x, and 2x, optimized for driving Flash LEDs in camera phones and other portable applications. It provides a constant current of up to 1A (typ.) for Flash mode and 180 mA (typ.) for Torch mode.

The LM2759 has selectable modes including Flash, Torch, Indicator and Shutdown. Flash mode for the LM2759 can also be enabled via the Strobe input pin. The LED is driven from $V_{OUT}$ and connected to the current sink. The LED drive current and operating modes are programmed via an $I^2C$ compatible interface. The LM2759 adaptively selects the next highest gain mode when needed to maintain the programmed LED current level.

To prevent a high battery load condition during a simultaneous RF PA transmission and Flash event, LM2759 has a Flash interrupt pin (TX) to reduce the LED current to the programmed Torch current level for the duration of the RF PA transmission pulse.

## CHARGE PUMP AND GAIN TRANSITIONS

The input to the 1x, 1.5x, 2x charge pump is connected to the $V_{IN}$ pin, and the loosely regulated output of the charge pump is connected to the $V_{OUT}$ pin. In 1x mode, as long as the input voltage is less than 4.7V (typ.), the output voltage is approximately equal to the input voltage. When the input voltage is over 4.7V (typ.) the output voltage is regulated to 4.7V (typ.). In 1.5x mode, the output voltage is regulated to 4.7V (typ.) over entire input voltage range. For the gain of 2x, the output voltage is regulated to 5.1V (typ.). When under load, the voltage at $V_{OUT}$ can be less than the target regulation voltage while the charge pump is still in closed loop operation. This is due to the load regulation topology of the LM2759.

The charge pump's gain is selected according to the headroom voltage across the current sink of LM2759. When the headroom voltage $V_{GDX}$ (at the LED cathode) drops below 350 mV (typ.) the charge pump gain transitions to the next available higher gain mode. Once the charge pump transitions to a higher gain, it will remain at that gain for as long as the device remains enabled. Shutting down and then re-enabling the device resets the gain mode to the minimum gain required to maintain the load.

### SOFT START

The LM2759 contains internal soft-start circuitry to limit inrush currents when the part is enabled. Soft start is implemented internally with a controlled turn-on of the internal voltage reference.

### CURRENT LIMIT PROTECTION

The LM2759 charge pump contains current limit protection circuitry that protects the device during $V_{OUT}$ fault conditions where excessive current is drawn. Output current is limited to 1.4A typically.

### LOGIC CONTROL PINS

LM2759 has two asynchronous logic pins, Strobe and TX. These logic inputs function according to the table below:

| TX | STROBE | FUNCTION |
|---|---|---|
| 0 | 0 | Current $I^2C$ programmed state (Off, Torch, Flash, Indicator) |
| 1 | 0 | Current $I^2C$ programmed state (Off, Torch, Flash, Indicator). If Flash is enabled via $I^2C$ and TX is logic High, the LED current will be at the programmed Torch level. |
| 0 | 1 | Flash Mode (Total LED "ON" Duration limited by Flash Timeout) |
| 1 | 1 | Torch Mode (Total LED "ON" Duration limited by Flash Timeout) |

Copyright © 2008–2013, Texas Instruments Incorporated

## I²C COMPATIBLE INTERFACE

### *START AND STOP CONDITIONS*

START and STOP conditions classify the beginning and the end of the I²C session. A START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP conditions. The I²C bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

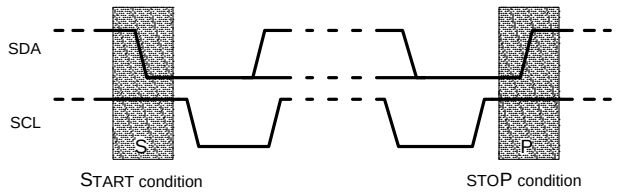



**Figure 15. Start and Stop Conditions**

### *DATA VALIDITY*

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when SCL is LOW.

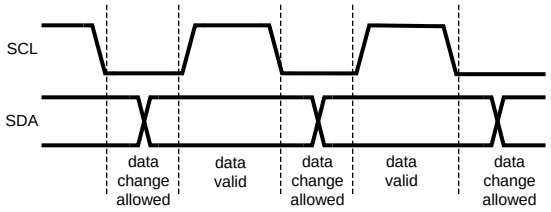



**Figure 16. Data Validity Diagram**

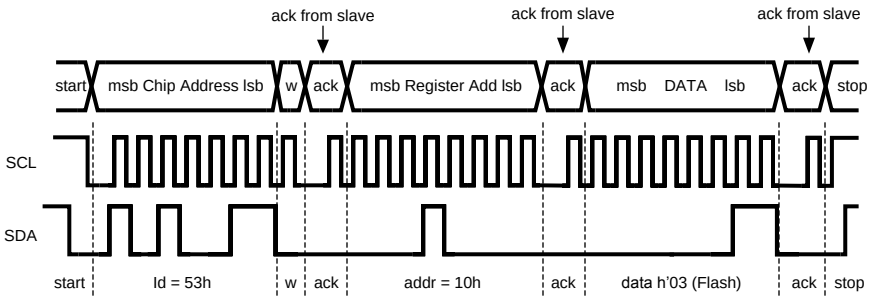
A pull-up resistor between the controller's VIO line and SDA must be greater than [**(VIO-$V_{OL}$) / 3.5mA**] to meet the $V_{OL}$ requirement on SDA. Using a larger pull-up resistor results in lower switching current with slower edges, while using a smaller pull-up results in higher switching currents with faster edges.

### *TRANSFERING DATA*

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LM2759 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LM2759 generates an acknowledge after each byte is received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM2759 address is 53h. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.


Copyright © 2008–2013, Texas Instruments Incorporated

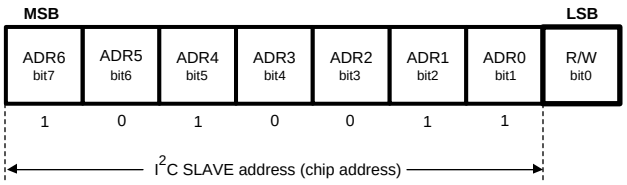



w = write (SDA = "0")
r = read (SDA = "1")
ack = acknowledge (SDA pulled down by either master or slave)
id = chip address, 53h for LM2759

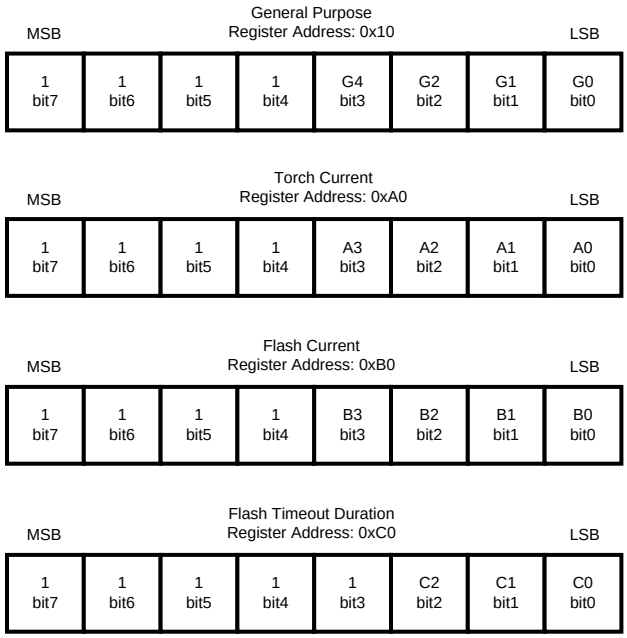
**Figure 17. Write Cycle**

## *I²C COMPATIBLE CHIP ADDRESS*

The chip address for LM2759 is 1010011, or 53h.




## *INTERNAL REGISTERS*




| Register | Internal Hex Address | Power On Value (lowest 4 bits) |
|---|---|---|
| General Purpose Register | 10h | 0000 |
| Flash Current Register | B0h | 1010 |
| Torch Current Register | A0h | 0111 |

Copyright © 2008–2013, Texas Instruments Incorporated

| Register | Internal Hex Address | Power On Value (lowest 4 bits) |
|---|---|---|
| Flash Timeout Duration Register | C0h | 1011 |

### GENERAL PURPOSE REGISTER AND STROBE INHIBIT FUNCTION

The general purpose register (x10) is used set the mode of operation for the LM2759. The selectable operating modes using the lower 4 bits in the general purpose register are listed in the table below.

The Strobe Input Pin can be disabled via $I^2C$ to ignore external signals into this pin when desired. This function is implemented through bit 3 of the General Purpose Register (See table below). In the default state, input signals on the Strobe Input are enabled. (Bit3 = “0”, inputs into the Strobe Pin are not inhibited).

**Table 1. General Purpose Register (Reg x10)**

| Bit3 | Bit2 | Bit1 | Bit0 | Mode |
|---|---|---|---|---|
| X | X | X | 0 | Shutdown |
| X | 0 | 0 | 1 | Torch |
| X | X | 1 | 1 | Flash |
| X | 1 | 0 | 1 | Indicator (Lowest Torch Level) |
| 1 | X | X | X | Inhibit Inputs into the Strobe Pin |

### SETTING LED CURRENT

The current through the LED is set by programming the appropriate register with the desired current level code for Flash and Torch. The time that Flash mode is active is dependent on the lesser of the duration that it is set to "ON" (via $I^2C$ or the Strobe pin), or the duration of the Flash Timeout. Use the tables below to select the desired current level.

Using the part in conditions where the junction temperature might rise above the rated maximum requires that the operating ranges and/or conditions be de-rated. The printed circuit board also must be carefully laid out to account for high thermal dissipation in the part.

**Table 2. Flash Current Table (Reg xB0)**

| CODE (Hex) | FLASH CURRENT (mA) |
|---|---|
| 00 | 80 |
| 01 | 150 |
| 02 | 220 |
| 03 | 280 |
| 04 | 350 |
| 05 | 410 |
| 06 | 470 |
| 07 | 530 |
| 08 | 590 |
| 09 | 650 |
| 0A | 710 |
| 0B | 770 |
| 0C | 830 |
| 0D | 890 |
| 0E | 950 |
| 0F | 1010 |


Copyright © 2008–2013, Texas Instruments Incorporated

**Table 3. Torch Current Table (Reg xA0)**

| CODE (Hex) | TORCH CURRENT (mA) |
|---|---|
| 00 | 15 |
| 01 | 30 |
| 02 | 40 |
| 03 | 50 |
| 04 | 65 |
| 05 | 80 |
| 06 | 90 |
| 07 | 100 |
| 08 | 110 |
| 09 | 120 |
| 0A | 130 |
| 0B | 140 |
| 0C | 150 |
| 0D | 160 |
| 0E | 170 |
| 0F | 180 |

### FLASH TIME-OUT FEATURE

Time-out Protection Circuitry disables the current sink when either the Strobe pin is held at logic high or the Flash mode is enabled via the $I^2C$ compatible interface longer than the programmed timeout duration. This prevents the device from self-heating due to the high power dissipation during Flash conditions. During the time-out condition, voltage will still be present on $V_{OUT}$ but the current sink will be shut off, resulting in no current through the Flash LED. When the device goes into a time-out condition, disabling and then re-enabling the device will reset the time-out. Use the table below to set the desired Flash timeout duration.

**Table 4. Flash Timeout Duration (Reg xC0)**

| CODE (Hex) | TIME (ms) |
|---|---|
| 00 | 60 |
| 01 | 125 |
| 02 | 250 |
| 03 | 375 |
| 04 | 500 |
| 05 | 625 |
| 06 | 750 |
| 07 | 1100 |

## CAPACITOR SELECTION

The LM2759 requires 4 external capacitors for proper operation. Surface-mount multi-layer ceramic capacitors are recommended. These capacitors are small, inexpensive and have very low equivalent series resistance (ESR <20 mΩ typ.). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors are not recommended for use with the LM2759 due to their high ESR, as compared to ceramic capacitors. For most applications, ceramic capacitors with X7R or X5R temperature characteristic are preferred for use with the LM2759. These capacitors have tight capacitance tolerance (as good as ±10%) and hold their value over temperature (X7R: ±15% over -55°C to 125°C; X5R: ±15% over -55°C to 85°C). Capacitors with Y5V or Z5U temperature characteristic are generally not recommended for use with the LM2759. Capacitors with these temperature characteristics typically have wide capacitance tolerance (+80%, -20%) and vary significantly over

Copyright © 2008–2013, Texas Instruments Incorporated

temperature (Y5V: +22%, -82% over -30°C to +85°C range; Z5U: +22%, -56% over +10°C to +85°C range). Under some conditions, a nominal 1 µF Y5V or Z5U capacitor could have a capacitance of only 0.1 µF. Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM2759. The voltage rating of the output capacitor should be 6.3V or more. For example, a 6.3V 0603 4.7 µF output capacitor (TDK C1608X5R0J475) is acceptable for use with the LM2759, as long as the capacitance on the output does not fall below a minimum of 3µF in the intended application. All other capacitors should have a voltage rating at or above the maximum input voltage of the application and should have a minimum capacitance of 1 µF.

**Table 5. Suggested Capacitors and Suppliers**

| MFG Part No. | Type | MFG | Voltage Rating | Case Size Inch (mm) |
|---|---|---|---|---|
| **4.7 µF for $C_{OUT}$** | | | | |
| C1608X5R0J475 | Ceramic X5R | TDK | 6.3V | 0603 (1608) |
| JMK107BJ475 | Ceramic X5R | Taiyo-Yuden | 6.3V | 0603 (1608) |
| **2.2 µF for C1, C2, $C_{IN}$** | | | | |
| C1608X5R0J225 | Ceramic X5R | TDK | 6.3V | 0603 (1608) |
| JMK107BJ225 | Ceramic X5R | Taiyo-Yuden | 6.3V | 0603 (1608) |

## POWER EFFICIENCY

Efficiency of LED drivers is commonly taken to be the ratio of power consumed by the LED ($P_{LED}$) to the power drawn at the input of the part ($P_{IN}$). With a 1x, 1.5x, 2x charge pump, the input current is equal to the charge pump gain times the output current (total LED current). The efficiency of the LM2759 can be predicted as follows:

$$P_{LED} = V_{LED} \times I_{LED} \quad (1)$$

$$P_{IN} = V_{IN} \times I_{IN} \quad (2)$$

$$P_{IN} = V_{IN} \times (Gain \times I_{LED} + I_Q) \quad (3)$$

$$E = (P_{LED} \div P_{IN}) \quad (4)$$

For a simple approximation, the current consumed by internal circuitry ($I_Q$) can be neglected, and the resulting efficiency will become:

$$E = V_{LED} \div (V_{IN} \times Gain) \quad (5)$$

Neglecting $I_Q$ will result in a slightly higher efficiency prediction, but this impact will be negligible due to the value of $I_Q$ being very low compared to the typical Torch and Flash current levels (100mA - 1A). It is also worth noting that efficiency as defined here is in part dependent on LED voltage. Variation in LED voltage does not affect power consumed by the circuit and typically does not relate to the brightness of the LED. For an advanced analysis, it is recommended that power consumed by the circuit ($V_{IN}$ x $I_{IN}$) be evaluated rather than power efficiency.

## THERMAL PROTECTION

Internal thermal protection circuitry disables the LM2759 when the junction temperature exceeds 150°C (typ.). This feature protects the device from being damaged by high die temperatures that might otherwise result from excessive power dissipation. The device will recover and operate normally when the junction temperature falls below 120°C (typ.). It is important that the board layout provide good thermal conduction to keep the junction temperature within the specified operating ratings.

## POWER DISSIPATION

The power dissipation ($P_{DISSIPATION}$) and junction temperature ($T_J$) can be approximated with the equations below. $P_{IN}$ is the power generated by the 1x, 1.5x, 2x charge pump, $P_{LED}$ is the power consumed by the LED, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance for the 12 pin WSON package. $V_{IN}$ is the input voltage to the LM2759, $V_{LED}$ is the nominal LED forward voltage, and $I_{LED}$ is the programmed LED current.

$$P_{DISSIPATION} = P_{IN} - P_{LED} \quad (6)$$

$$= (Gain \times V_{IN} \times I_{LED}) - (V_{LED} \times I_{LED}) \quad (7)$$

$$T_J = T_A + (P_{DISSIPATION} \times \theta_{JA}) \quad (8)$$


Copyright © 2008–2013, Texas Instruments Incorporated

The junction temperature rating takes precedence over the ambient temperature rating. The LM2759 may be operated outside the ambient temperature rating, so long as the junction temperature of the device does not exceed the maximum operating rating of 105°C. The maximum ambient temperature rating must be derated in applications where high power dissipation and/or poor thermal resistance causes the junction temperature to exceed 105°C.

## MAXIMUM OUTPUT CURRENT

The maximum LED current that can be used for a particular application depends on the rated forward voltage of the LED used, the input voltage range of the application, and the Gain mode of the LM2759's charge pump. The following equation can be used to approximate the relationship between the maximum LED current, the LED forward voltage, the minimum input voltage, and the charge pump gain:

$$(V_{IN_MIN} \times \text{Gain}) > (V_F + V_{HR}) + (I_{LED} \times R_{OUT_GAIN}) \quad (9)$$

$V_{HR}$ or the voltage required across the current sink to remain in regulation can be approximated by ($I_{LED}$ x $K_{HR}$), where $K_{HR}$ is 0.8 mV/mA (typ). $R_{OUT_GAIN}$ is the output impedance of the charge pump according to its gain mode. When using the equation above, keep in mind that the ($V_F$ + $V_{HR}$) portion of the equation can not be greater than the nominal output regulation voltage for a particular gain. In other words, when making calculations for an application where the term ($V_F$ + $V_{HR}$) is higher than a particular gain's regulation voltage, the next higher gain level must be used for the calculation.

Example: $V_F$ = 4V @ 1A, Charge Pump in the Gain of 2x with a $R_{OUT}$ of 2.25Ω (typ.)

$V_{IN_MIN}$ > [(4V + 0.8V) + (1A x 2.25Ω) ] ÷ 2

$V_{IN_MIN}$ > 3.53V (typ.)

The maximum power dissipation in the LM2759 must also be taken into account when selecting the conditions for an application, such that the junction temperature of the device never exceeds its rated maximum. The input voltage range, operating temperature range, and/or current level of the application may have to be adjusted to keep the LM2759 within normal operating ratings.

## BOARD LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the WSON package and board pads. Poor solder joints can result in erratic or degraded performance.

Copyright © 2008–2013, Texas Instruments Incorporated

## REVISION HISTORY

| Changes from Revision C (May 2013) to Revision D | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 15 |


Copyright © 2008–2013, Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM2759SD/NOPB | ACTIVE | WSON | DQB | 12 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -30 to 85 | L2759 | Samples |
| LM2759SDEV | ACTIVE | | | 0 | 1 | TBD | Call TI | Call TI | | | Samples |
| LM2759SDX/NOPB | ACTIVE | WSON | DQB | 12 | 4500 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -30 to 85 | L2759 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

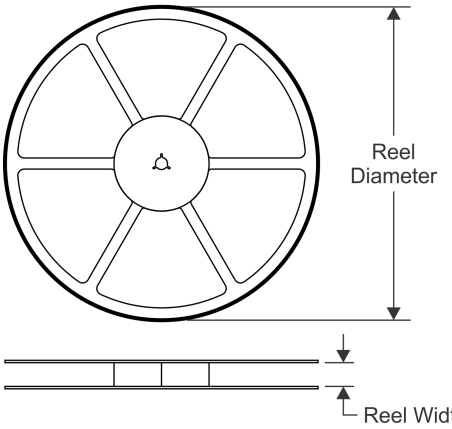
**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

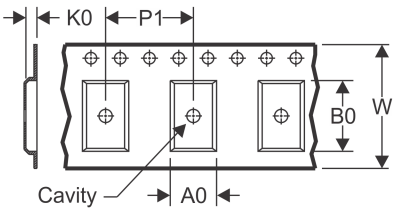
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

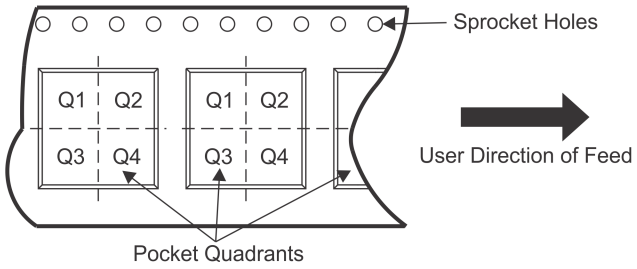



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

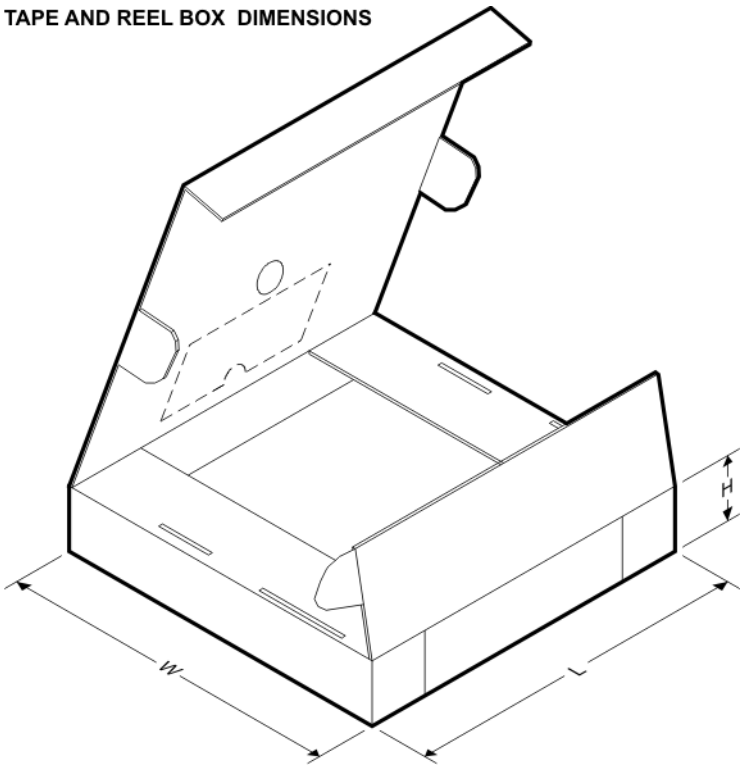
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM2759SD/NOPB | WSON | DQB | 12 | 1000 | 178.0 | 12.4 | 3.3 | 3.3 | 1.0 | 8.0 | 12.0 | Q1 |
| LM2759SDX/NOPB | WSON | DQB | 12 | 4500 | 330.0 | 12.4 | 3.3 | 3.3 | 1.0 | 8.0 | 12.0 | Q1 |

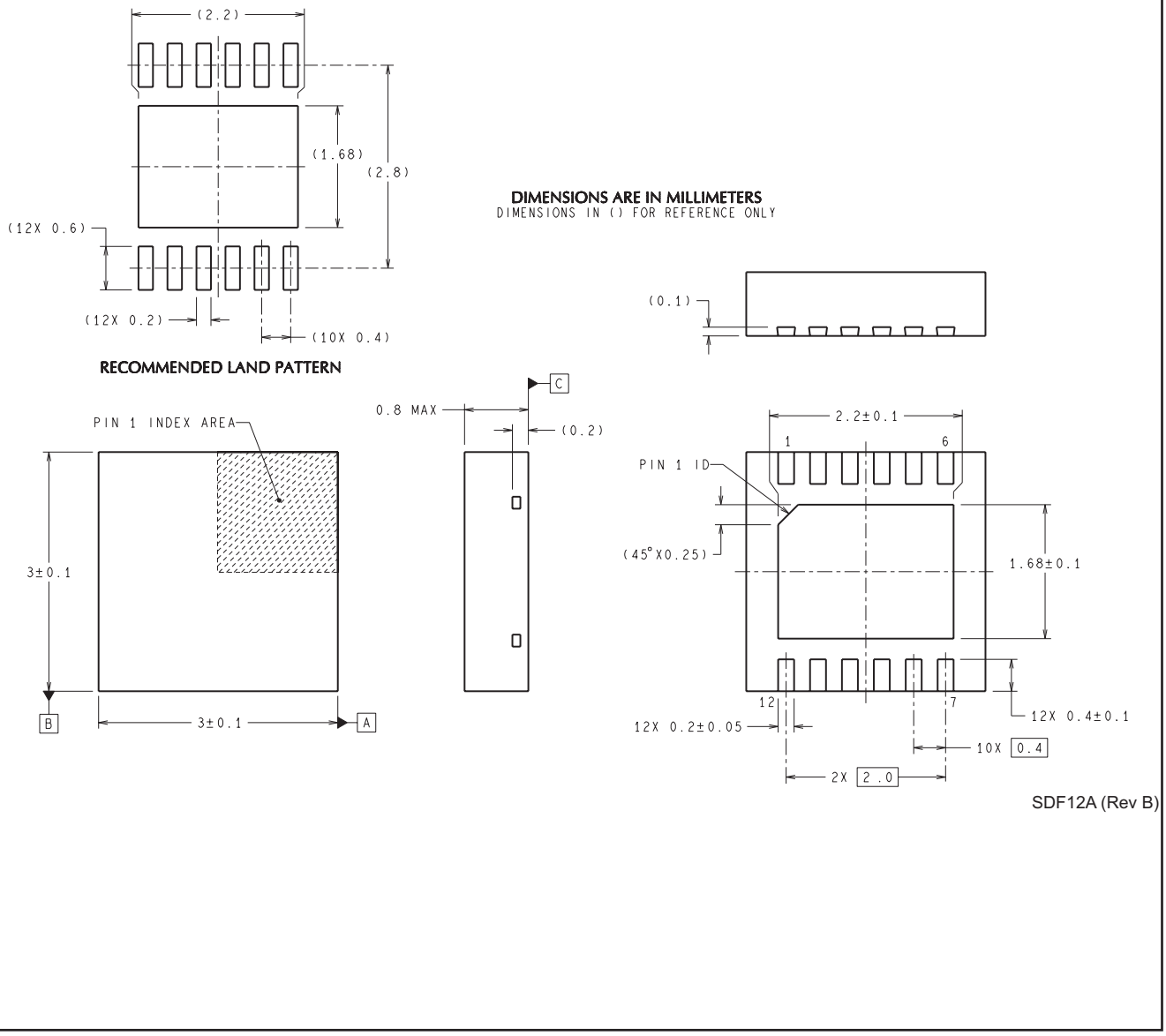
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM2759SD/NOPB | WSON | DQB | 12 | 1000 | 210.0 | 185.0 | 35.0 |
| LM2759SDX/NOPB | WSON | DQB | 12 | 4500 | 367.0 | 367.0 | 35.0 |

# DQB0012A




SDF12A (Rev B)

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated