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RF6100-1

3V 900MHZ LINEAR POWER AMPLIFIER MODULE

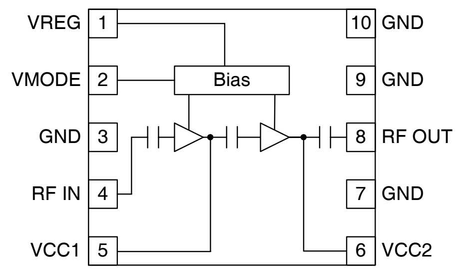
RoHS Compliant & Pb-Free Product
Package Style: Module (4 mm x 4 mm)

Features

- Input/Output Internally Matched@50Ω
- 28dBm Linear Output Power
- 40% Peak Linear Efficiency
- -50dBc ACPR @ 885kHz
- 29dB Linear Gain
- 53% AMPS Efficiency

Applications

- 3V CDMA/AMPS Cellular Handset
- 3V CDMA20001/X Cellular Handset
- Spread-Spectrum System



Functional Block Diagram

Product Description

The RF6100-1 is a high-power, high-efficiency linear amplifier module specifically designed for 3V handheld systems. The device is manufactured on an advanced third generation GaAs HBT process, and was designed for use as the final RF amplifier in 3V IS-95/CDMA 2000 1X/AMPS handheld digital cellular equipment, spread-spectrum systems, and other applications in the 824MHz to 849MHz band. The RF6100-1 has a digital control line for low power applications to lower quiescent current. The device is self-contained with 50Ω input and output that is matched to obtain optimum power, efficiency and linearity. The module is a 4mmx4mm land grid array with backside ground. The RF6100-1 is footprint compatible with industry standard 4mmx4mm CDMA modules, and requires only one decoupling capacitor.

Ordering Information

RF6100-1	3V 900MHz Linear Power Amplifier Module
RF6100-1PCBA-41X	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☑ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V
Supply Voltage ($P_{OUT} \leq 31$dBm)	+5.2	V
Control Voltage (V_{REG})	+4.2	V
Input RF Power	+10	dBm
Mode Voltage (V_{MODE})	+3.5	V
Operating Temperature	-30 to +110	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
High Power Mode (V_{MODE} Low)					T=25°C Ambient, V_{CC}=3.4V, V_{REG}=2.8V, V_{MODE}=0V, and P_{OUT}=28dBm for all parameters (unless otherwise specified).
Operating Frequency Range	824		849	MHz	
Linear Gain	27	29		dB	
Second Harmonics		-35		dBc	
Third Harmonics		-40		dBc	
Maximum Linear Output	28				
Linear Efficiency	35	40		%	
Maximum I_{CC}		465	530	mA	
ACPR @ 885kHz		-50	-46	dBc	
ACPR @ 1.98MHz		-58	-55	dBc	
Input VSWR		2:1			
Stability in Band			6:1		No oscillation>-70dBc
Stability out of Band			10:1		No damage
Noise Power		-133		dBm/Hz	At 45MHz offset.
Low Power Mode (V_{MODE} High)					T=25°C Ambient, V_{CC}=3.4V, V_{REG}=2.8V, V_{MODE}=2.8V, and P_{OUT}=18dBm for all parameters (unless otherwise specified).
Operating Frequency Range	824		849	MHz	
Linear Gain	24	26		dB	
Second Harmonics		-35		dBc	
Third Harmonics		-40		dBc	
Maximum Linear Output	18				
Maximum I_{CC}		135		mA	P_{OUT}=16dBm
ACPR @885kHz		-50	-46	dBc	
ACPR @1.98MHz		-60	-56	dBc	
Input VSWR		2:1			
Output VSWR Stability			6:1		No oscillation>-70dBc
			10:1		No damage

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
FM Mode					T=25°C Ambient, V_{CC}=3.4V, V_{REG}=2.8V, V_{MODE}=0V, and P_{OUT}=31dBm for all parameters (unless otherwise specified).
Operating Frequency Range	824		849	MHz	
AMPS Maximum Output Power		31		dBm	
AMPS Efficiency	47	53		%	
AMPS Gain	24	28			
AMPS Second Harmonics		-35	-30	dBc	
AMPS Third Harmonics		-40	-30	dBc	
Power Supply					
Supply Voltage	3.2	3.4	4.2	V	
High Gain Idle Current		65	100	mA	V_{MODE}=low and V_{REG}=2.8V
Low Gain Idle Current		55	70	mA	V_{MODE}=high and V_{REG}=2.8V
V_{REG} Current		4.7	5.5	mA	V_{MODE}=high
V_{MODE} Current		250	1000	uA	
RF Turn On/Off Time			6	uS	
DC Turn On/Off Time			40	uS	
Total Current (Power Down)		0.2	5.0	uA	
V_{REG} Low Voltage	0		0.5	V	
V_{REG} High Voltage (Recommended)	2.75	2.8	2.95	V	
V_{REG} High Voltage (Operational)	2.7		3.0	V	
V_{MODE} Voltage	0		0.5	V	High Gain Mode
	2.0		2.8	V	Low Gain Mode

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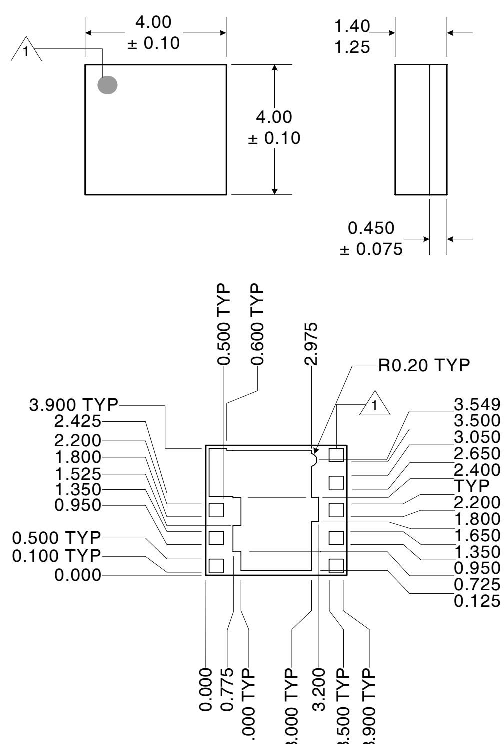
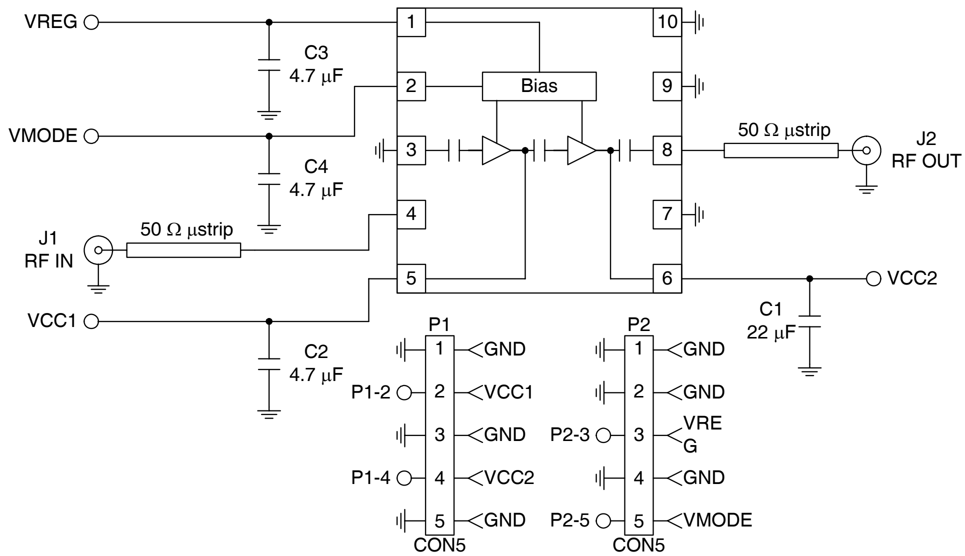
Pin	Function	Description	Interface Schematic
1	VREG	Regulated voltage supply for amplifier bias. In Power Down mode, both V_{REG} and V_{MODE} need to be LOW (<0.5V).	
2	VMODE	For nominal operation (High Power Mode), V_{MODE} is set LOW. When set HIGH, devices are biased lower to improve efficiency.	
3	GND	Ground connection. Connect to package base ground. For best performance, keep traces physically short and connect immediately to ground plane.	
4	RF IN	RF input internally matched to 50Ω. This input is internally AC-coupled.	
5	VCC1	First stage collector supply. A low frequency decoupling capacitor (e.g., 4.7μF) may be required.	
6	VCC2	Output stage collector supply. A low frequency decoupling capacitor (e.g., 4.7μF) is required.	
7	GND	Ground connection. Connect to package base ground. For best performance, keep traces physically short and connect immediately to ground plane.	
8	RF OUT	RF output internally matched to 50Ω. This output is internally AC-coupled.	
9	GND	Ground connection. Connect to package base ground. For best performance, keep traces physically short and connect immediately to ground plane.	
10	GND	Ground connection. Connect to package base ground. For best performance, keep traces physically short and connect immediately to ground plane.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

Package Drawing



Evaluation Board Schematic



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PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land and Solder Mask Pattern

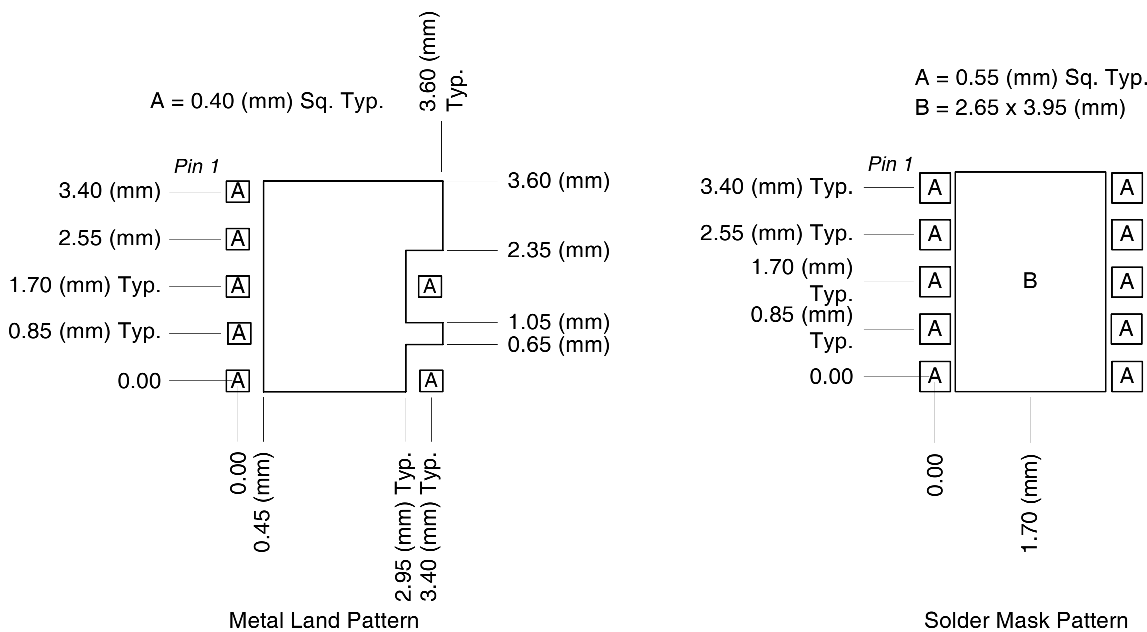

Figure 1. PCB Metal Land and Solder Mask Pattern (Top View)

Thermal Pad and Via Design

The PCB metal land pattern has been designed with a thermal pad that matches the exposed die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

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