

M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 4-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

Self or extended refresh current is low enough for battery back-up application.

FEATURES

Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V4405CXX-6, -6S	60	15	30	15	110	264
M5M4V4405CXX-7, -7S	70	20	35	20	130	231

XX=J, TP

- Standard 26 pin SOJ, 26 pin TSOP(II)
- Single 3.3V±0.3V supply
- Low stand-by power dissipation
 - CMOS Input level1.8mW(Max)*
 - CMOS Input level180µW(Max)
- Low operating power dissipation
 - M5M4V4405Cxx-6, -6S288.0mW (Max)
 - M5M4V4405Cxx-7, -7S252.0mW (Max)
- Self refresh capability*
 - Self refresh current100µA(max)
- Extended refresh capability*
 - Extended refresh current100µA(max)
- Hyper-page mode (1024-bit random access), Read-modify- write, RAS-only refresh CAS before RAS refresh, Hidden refresh, CBR self refresh(-6S,-7S) capabilities.
- Early-write mode and OE and W to control output buffer impedance
- 1024 refresh cycles every 16.4ms (A₀~A₉)*
- 1024 refresh cycle every 128ms (A₀~A₉)*

*: Applicable to self refresh version (M5M4V4405Cxx-6S,-7S: option) only

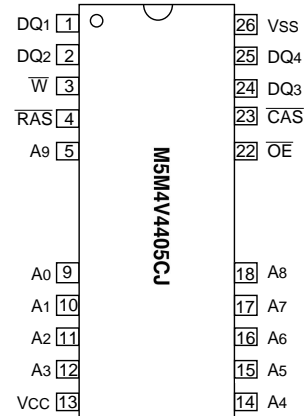
APPLICATION

Lap top personal computer, Solid state disc, Microcomputer memory, Refresh memory for CRT

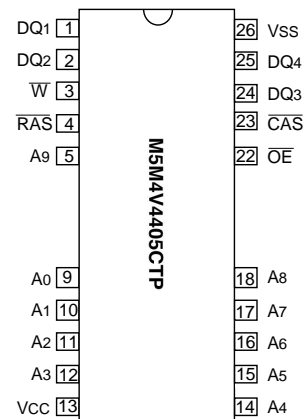
PIN DESCRIPTION

Pin name	Function
A ₀ ~A ₉	Address inputs
DQ ₁ ~DQ ₄	Data inputs / outputs
RAS	Row address strobe input
CAS	Column address strobe input
W	Write control input
OE	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 26P0J (300mil SOJ)



Outline 26P3Z-E (300mil TSOP)

M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

FUNCTION

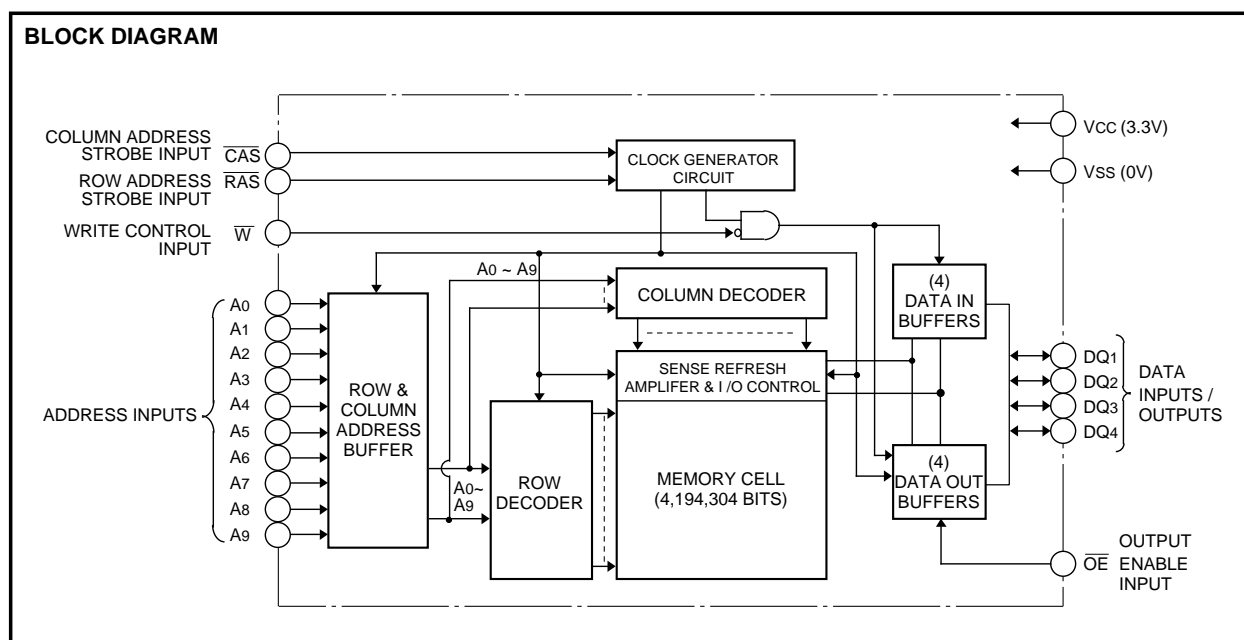
In addition to normal read, write, and read-modify-write operations the M5M4V4405CJ,TP provide, a number of other functions, e.g.,

Hyper Page mode, $\overline{\text{RAS}}$ -only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Hyper Page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	APD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	NAC	APD	APD	APD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	APD	VLD	YES	
$\overline{\text{RAS}}$ -only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	DNC	DNC	OPN	VLD	YES	
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Self refresh*	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open



M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS}	-0.5 ~ 4.6	V
V _I	Input voltage		-0.5 ~ 4.6	V
V _O	Output voltage		-0.5 ~ 4.6	V
I _O	Output current		50	mA
P _d	Power dissipation	T _a =25°C	1000	mW
T _{opr}	Operating temperature		0 ~ 70	°C
T _{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (T_a=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{CC}	Supply voltage	3.0	3.3	3.6	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.0		V _{CC} +0.3	V
V _{IL}	Low-level input voltage	DQ ₁ ~DQ ₄	-0.3	0.8	V
		others	-0.3	0.8	V

Note 1 : All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=3.3V±0.3V, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
V _{OH}	High-level output voltage	I _{OH} =-2mA	2.4		V _{CC}	V	
V _{OL}	Low-level output voltage	I _{OL} =2mA	0		0.4	V	
I _{OZ}	Off-state output current	Q floating, 0V V _{OUT} V _{CC}	-5		5	μA	
I _I	Input current	0V V _{IN} V _{CC} +0.3V, Other inputs pins=0V	-5		5	μA	
I _{CC1} (AV)	Average supply current from V _{CC} operating (Note 3,4,5)	M5M4V4405C-6,-6S	R _{AS} , C _{AS} cycling trc=twc=min. output open		80	mA	
		M5M4V4405C-7,-7S			70		
I _{CC2} (AV)	Supply current from V _{CC} , stand-by (Note 6)	R _{AS} =C _{AS} =V _{IH} , output open		2	mA		
		M5M4V4405C	R _{AS} =C _{AS} V _{CC} -0.2V output open	0.5			
M5M4V4405C(S)			0.05				
I _{CC3} (AV)	Average supply current from V _{CC} refreshing (Note 3,5)	M5M4V4405C-6,-6S	R _{AS} cycling, C _{AS} =V _{IH} trc=min. output open		80	mA	
		M5M4V4405C-7,-7S			70		
I _{CC4} (AV)	Average supply current from V _{CC} Hyper-Page-Mode (Note 3,4,5)	M5M4V4405C-6,-6S	R _{AS} =V _{IL} , C _{AS} cycling tpc=min. output open		80	mA	
		M5M4V4405C-7,-7S			70		
I _{CC6} (AV)	Average supply current from V _{CC} , CAS before RAS refresh mode (Note 3)	M5M4V4405C-6,-6S	C _{AS} before R _{AS} refresh cycling trc=min. output open		70	mA	
		M5M4V4405C-7,-7S			60		
I _{CC8} (AV)*	Average supply current from V _{CC} Extended-Refresh cycle (Note 6)	R _{AS} cycling C _{AS} 0.2V or C _{AS} before R _{AS} refresh cycling R _{AS} 0.2V or V _{CC} -0.2V C _{AS} 0.2V or V _{CC} -0.2V W 0.2V (Except for R _{AS} falling edge) or V _{CC} -0.2V OE 0.2V or V _{CC} -0.2V A ₀ ~A ₉ 0.2V or V _{CC} -0.2V DQ=open trc=125μs, t _{RAS} =t _{RAS} min ~1μs			100	μA	
I _{CC9} (AV)*	Average supply current from V _{CC} Self-Refresh cycle (Note 6)	M5M4V4405C(S)	R _{AS} =C _{AS} 0.2V output open			100	μA

Note 2: Current flowing into an IC is positive, out is negative.

3: I_{CC1}(AV), I_{CC3}(AV), I_{CC4}(AV) and I_{CC6}(AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: I_{CC1}(AV) and I_{CC4}(AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while R_{AS}=V_{IL} and C_{AS}=V_{IH}.

M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

CAPACITANCE (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test condition:	Limits			Unit
			Min	Typ	Max	
C _{I(A)}	Input capacitance, address inputs	V _I =V _{SS}			5	pF
C _{I(CLK)}	Input capacitance, clock inputs	f=1MHz			7	pF
C _{I/O}	Input/Output capacitance, data ports	V _I =25mVrms			7	pF

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
t _{CAC}	Access time from $\overline{\text{CAS}}$ (Note 7,8)		15		20	ns
t _{TRAC}	Access time from RAS (Note 7,9)		60		70	ns
t _{TAA}	Column address access time (Note 7,10)		30		35	ns
t _{CPA}	Access time from $\overline{\text{CAS}}$ precharge (Note 7,11)		33		38	ns
t _{OE A}	Access time from $\overline{\text{OE}}$ (Note 7)		15		20	ns
t _{OHC}	Output hold time from $\overline{\text{CAS}}$	5		5		ns
t _{OHR}	Output hold time from RAS (Note 13)	5		5		ns
t _{CLZ}	Output low impedance time from $\overline{\text{CAS}}$ low (Note 7)	5		5		ns
t _{OEZ}	Output disable time after $\overline{\text{OE}}$ high (Note 12)		15		20	ns
t _{WEZ}	Output disable time after $\overline{\text{WE}}$ low (Note 12)		15		20	ns
t _{OFF}	Output disable time after $\overline{\text{CAS}}$ high (Note 12,13)		15		20	ns
t _{TREZ}	Output disable time after RAS high (Note 12,13)		15		20	ns

Note 6: An initial pause of 200µs is required after power-up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles).

Note the $\overline{\text{RAS}}$ may be cycled during the initial pause. And eight initialization cycles are required after prolonged periods (greater than t_{REF(max)}) of $\overline{\text{RAS}}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to 100pF, V_{OH}=2.4V(I_{OH}=-2mA) and V_{OL}=0.4V(I_{OL}=2mA). The reference levels for measuring of output signals are 2.0V(V_{OH}) and 0.8V(V_{OL}).

8: Assumes that t_{TRCD} t_{TRCD(max)} and t_{TASC} t_{TASC(max)} and t_{CP} t_{CP(max)}.

9: Assumes that t_{TRCD} t_{TRCD(max)} and t_{TRAD} t_{TRAD(max)}. If t_{TRCD} or t_{TRAD} is greater than the maximum recommended value shown in this table, t_{TRAC} will increase by amount that t_{TRCD} exceeds the value shown.

10: Assumes that t_{TRAD} t_{TRAD(max)} and t_{TASC} t_{TASC(max)}.

11: Assumes that t_{CP} t_{CP(max)} and t_{TASC} t_{TASC(max)}.

12: t_{OEZ} (max), t_{WEZ} (max), t_{OFF} (max) and t_{TREZ} (max) defines the time at which the output achieves the high impedance state (I_{OUT} | ±10µA) and is not reference to V_{OH}(min) or V_{OL}(max).

13: Output is disabled after both RAS and CAS go to high.

M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Hyper-Page Mode Cycles)

(Ta=0~70°C, Vcc = 3.3V±0.3V, Vss =0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
tREF	Refresh cycle time		16.4		16.4	ms
tREF	Refresh cycle time*		128		128	ms
tRP	RAS high pulse width	40		50		ns
tRCD	Delay time, RAS low to CAS low (Note 16)	20	45	20	50	ns
tCRP	Delay time, CAS high to RAS low	5		5		ns
tRPC	Delay time, RAS high to CAS low	0		0		ns
tCPN	CAS high pulse width	10		13		ns
tRAD	Column address delay time from RAS low (Note 17)	15	30	15	35	ns
tASR	Row address setup time before RAS low	0		0		ns
tASC	Column address setup time before CAS low (Note 18)	0	13	0	13	ns
tRAH	Row address hold time after RAS low	10		10		ns
tCAH	Column address hold time after CAS low	10		10		ns
tDZC	Delay time, data to CAS low (Note 19)	0		0		ns
tDZO	Delay time, data to OE low (Note 19)	0		0		ns
tRDD	Delay time, RAS high to data (Note 20)	15		20		ns
tCDD	Delay time, CAS high to data (Note 20)	15		20		ns
tODD	Delay time, OE high to data (Note 20)	15		20		ns
tT	Transition time (Note 21)	1	50	1	50	ns

Note 14: The timing requirements are assumed $t_T = 2ns$.

Note 15: $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals.

Note 16: $t_{RCD}(max)$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD}(max)$, access time is t_{RAC} . If t_{RCD} is greater than $t_{RCD}(max)$, access time is controlled exclusively by t_{CAC} or t_{AA} .

Note 17: $t_{RAD}(max)$ is specified as a reference point only. If t_{RAD} , $t_{RAD}(max)$ and t_{ASC} , $t_{ASC}(max)$, access time is controlled exclusively by t_{AA} .

Note 18: $t_{ASC}(max)$ is specified as a reference point only. If t_{RCD} , $t_{RCD}(max)$ and t_{ASC} , $t_{ASC}(max)$, access time is controlled exclusively by t_{CAC} .

Note 19: Either t_{DZC} or t_{DZO} must be satisfied.

Note 20: Either t_{RDD} or t_{CDD} or t_{ODD} must be satisfied.

Note 21: t_T is measured between $V_{IH}(min)$ and $V_{IL}(max)$.

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
tRC	Read cycle time	110		130		ns
tRAS	RAS low pulse width	60	10000	70	10000	ns
tCAS	CAS low pulse width	10	10000	13	10000	ns
tCSH	CAS hold time after RAS low	48		55		ns
tRSH	RAS hold time after CAS low	15		20		ns
tRCS	Read Setup time before CAS low	0		0		ns
tRCH	Read hold time after CAS high (Note 22)	0		0		ns
tRRH	Read hold time after RAS high (Note 22)	0		0		ns
tRAL	Column address to RAS hold time	30		35		ns
tCAL	Column address to CAS hold time	18		23		ns
tORH	RAS hold time after OE low	15		20		ns
tOCH	CAS hold time after OE low	15		20		ns

Note 22: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
tWC	Write cycle time	110		130		ns
tRAS	RAS low pulse width	60	10000	70	10000	ns
tCAS	CAS low pulse width	10	10000	13	10000	ns
tCSH	CAS hold time after RAS low	48		55		ns
tRSH	RAS hold time after CAS low	10		13		ns
tWCS	Write setup time before CAS low (Note 24)	0		0		ns
tWCH	Write hold time after CAS low	10		13		ns
tcWL	CAS hold time after \bar{W} low	10		13		ns
trWL	RAS hold time after \bar{W} low	10		13		ns
tWP	Write pulse width	10		13		ns
tDS	Data setup time before $\bar{C}AS$ low or \bar{W} low	0		0		ns
tDH	Data hold time after $\bar{C}AS$ low or \bar{W} low	10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
trWC	Read write/read modify write cycle time (Note 23)	133		161		ns
tRAS	RAS low pulse width	89	10000	107	10000	ns
tCAS	CAS low pulse width	44	10000	57	10000	ns
tCSH	CAS hold time after RAS low	89		107		ns
tRSH	RAS hold time after CAS low	44		57		ns
trCS	Read setup time before $\bar{C}AS$ low	0		0		ns
tcWD	Delay time, $\bar{C}AS$ low to \bar{W} low (Note 24)	32		42		ns
trWD	Delay time, RAS low to \bar{W} low (Note 24)	77		92		ns
tAWD	Delay time, address to \bar{W} low (Note 24)	47		57		ns
toEH	OE hold time after \bar{W} low	15		20		ns

Note 23: trWC is specified as $trWC(\min) = trAC(\max) + tODD(\min) + trWL(\min) + trP(\min) + 4tT$.

Note 24: tWCS, tcWD, trWD, tAWD, and tCPWD are specified as reference points only. If tWCS tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tcWD tcWD(min), trWD trWD(min), tAWD tAWD(min) and tCPWD tCPWD (min) (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until CAS or OE goes back to VIH) is indeterminate.

MITSUBISHI LSIs
M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

Hyper page Mode Cycle

(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by \overline{OE} or \overline{W}) (Note 25)

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
tHPC	Hyper page mode read/write cycle time (Note 26)	25		30		ns
tHPRWC	Hyper Page Mode read write / read modify write cycle time	66		79		ns
tDOH	Output hold time from CAS low	5		5		ns
tRAS	RAS low pulse width for read or write cycle (Note 27)	77	100000	92	100000	ns
tCP	CAS high pulse width (Note 28)	10	16	13	16	ns
tCPRH	RAS hold time after CAS precharge	33		38		ns
tCPWD	Delay time, CAS precharge to W low (Note 24)	50		60		ns
tCHOL	Hold time to maintain the data Hi-Z until CAS access	7		7		ns
tOEPE	OE Pulse Width (Hi-Z control)	7		7		ns
tWPE	W Pulse Width (Hi-Z control)	7		7		ns
tHCWD	Delay time, \overline{CAS} low to W low after read	32		42		ns
tHAWD	Delay time, Address to W low after read	47		57		ns
tHPWD	Delay time, CAS precharge to W low after read	50		60		ns
tHCOD	Delay time, CAS low to \overline{OE} high after read	15		20		ns
tHAOD	Delay time, Address to \overline{OE} high after read	30		35		ns
tHPOD	Delay time, \overline{CAS} precharge to \overline{OE} high after read	33		38		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.

26: tHPC(min) is specified in the case of read-only and early write-only in Hyper page Mode.

27: tRAS(min) is specified as two cycles of CAS input are performed.

28: tCP(max) is specified as a reference point only.

CAS before RAS Refresh Cycle (Note 29)

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
tCSR	CAS setup time before RAS low	5		5		ns
tCHR	CAS hold time after RAS low	10		15		ns
tRSR	Read setup time before RAS low	10		10		ns
tRHP	Read hold time after RAS low	10		15		ns
tCAS	CAS low pulse width	17		22		ns

Note 29: Eight or more CAS before RAS cycles instead of eight RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

Self Refresh Cycle* (Note 30)

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
tRASS	CBR self refresh RAS low pulse width	100		100		μs
tRPS	CBR self refresh RAS high precharge time	110		130		ns
tCHS	CBR self refresh CAS hold time	-50		-50		ns
tRSR	Read setup time before RAS low	10		10		ns
tRHR	Read hold time after RAS low	10		15		ns

M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

Test Mode Specification (Note 31)

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
ICC1 (AV)	Average supply current from Vcc operating (Note 3,4,5)	M5M4V4405C-6,-6S	RAS, CAS cycling		85	mA
		M5M4V4405C-7,-7S	trc=twc=min. output open		75	
ICC3 (AV)	Average supply current from Vcc refreshing (Note 3,5)	M5M4V4405C-6,-6S	RAS cycling, CAS= VIH		85	mA
		M5M4V4405C-7,-7S	trc=min. output open		75	
ICC4(AV)	Average supply current from Vcc Hyper-Page-Mode (Note 3,4,5)	M5M4V4405C-6,-6S	RAS=VIL, CAS cycling		85	mA
		M5M4V4405C-7,-7S	tpc=min. output open		75	
ICC6(AV)	Average supply current from Vcc CAS before RAS refresh mode (Note 3)	M5M4V4405C-6,-6S	CAS before RAS refresh cycling		75	mA
		M5M4V4405C-7,-7S	trc=min. output open		65	

Note 31: All previously specified electrical characteristics, switing characteristics, and timing requirements are applicable to that of test mode.

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
tCAC	Access time from CAS (Note 7,8)		20		25	ns
tRAC	Access time from RAS (Note 7,9)		65		75	ns
tAA	Column address access time (Note 7,10)		35		40	ns
tCPA	Access time from CAS precharge (Note 7,11)		38		43	ns
tOEA	Access time from OE (Note 7)		20		25	ns

TIMING REQUIREMENTS (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 14,15)

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
tRC	Read cycle time	115		135		ns
tRAS	RAS low pulse width	65	10000	75	10000	ns
tCAS	CAS low pulse width	15	10000	18	10000	ns
tCSH	CAS hold time after RAS low	53		60		ns
tRSH	RAS hold time after CAS low	20		25		ns
tRAL	Column address to RAS hold time	35		40		ns
tCAL	Column address to CAS hold time	23		28		ns
tORH	RAS hold time after OE low	20		25		ns
tOCH	CAS hold time after OE low	20		25		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time (Note 23)	138		166		ns
tRAS	RAS low pulse width	94	1000C	112	1000C	ns
tCAS	CAS low pulse width	49	10000	62	1000C	ns
tCSH	CAS hold time after RAS low	94		112		ns
tRSH	RAS hold time after CAS low	49		62		ns
tCWD	Delay time, CAS low to W low (Note 24)	37		47		ns
tRWD	Delay time, RAS low to W low (Note 24)	82		97		ns
tAWD	Delay time, address to W low (Note 24)	52		62		ns

M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

Hyper page Mode Cycle

(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by \overline{OE} or \overline{W}) (Note 25)

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
tHPC	Hyper page mode read/write cycle time (Note 26)	30		35		ns
tHPRWC	Hyper Page Mode read write / read modify write cycle time	71		84		ns
tRAS	RAS low pulse width for read or write cycle (Note 27)	82	100000	97	100000	ns
tCPRH	RAS hold time after CAS precharge	38		43		ns
tCPWD	Delay time, \overline{CAS} precharge to \overline{W} low (Note 24)	55		65		ns
tHCWD	Delay time, \overline{CAS} low to \overline{W} low after read	37		47		ns
tHAWD	Delay time, Address to \overline{W} low after read	52		62		ns
tHPWD	Delay time, \overline{CAS} precharge to \overline{W} low after read	55		65		ns
tHCOD	Delay time, \overline{CAS} low to \overline{OE} high after read	20		25		ns
tHAOD	Delay time, Address to \overline{OE} high after read	35		40		ns
tHPOD	Delay time, \overline{CAS} precharge to \overline{OE} high after read	38		43		ns

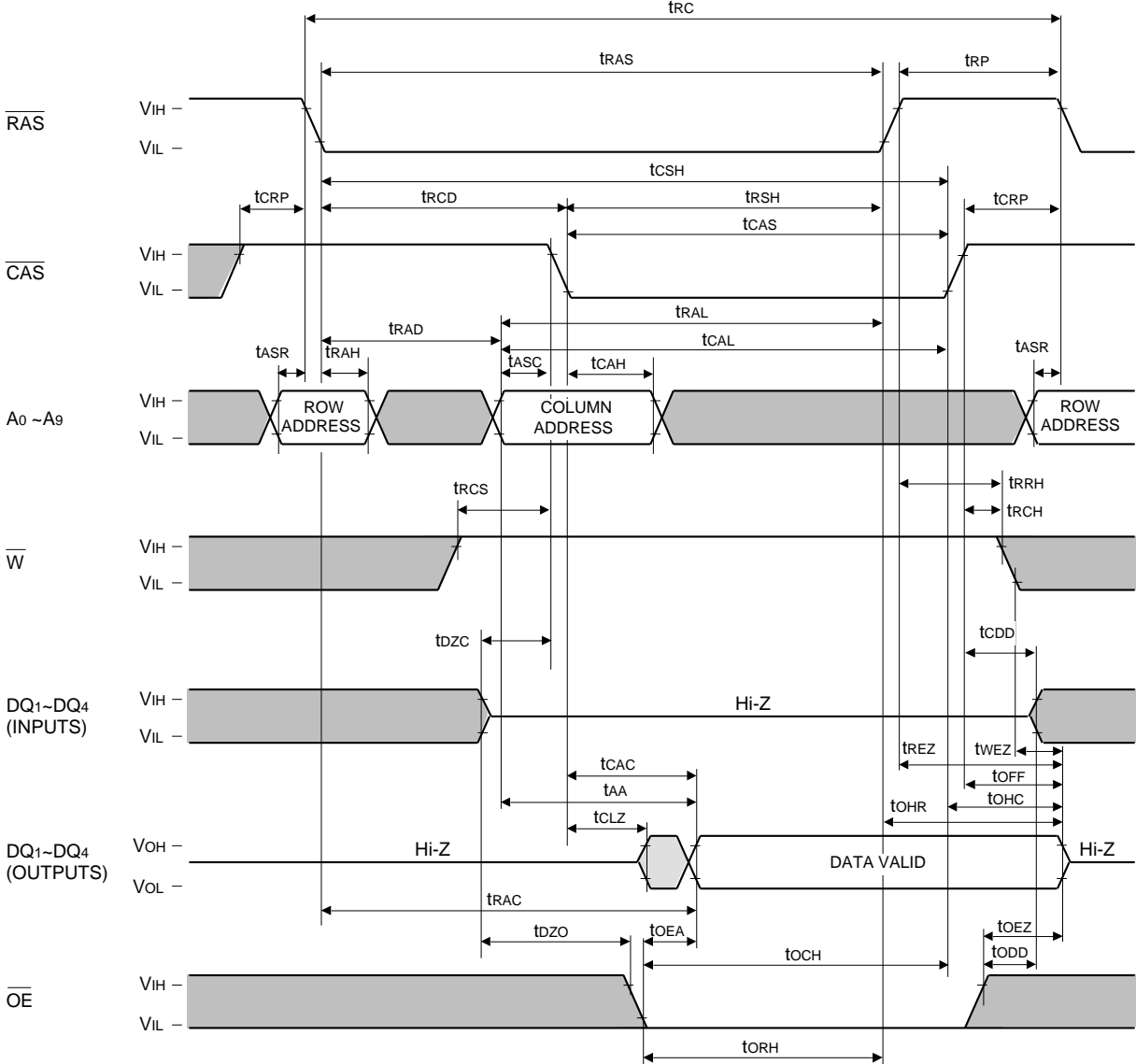
Test Mode Set Cycle


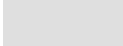
Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
tWSR	Write setup time before \overline{RAS} low	10		10		ns
tWHR	Write hold time after \overline{RAS} low	10		15		ns

M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

Timing Diagrams (Note 32)
Read Cycle

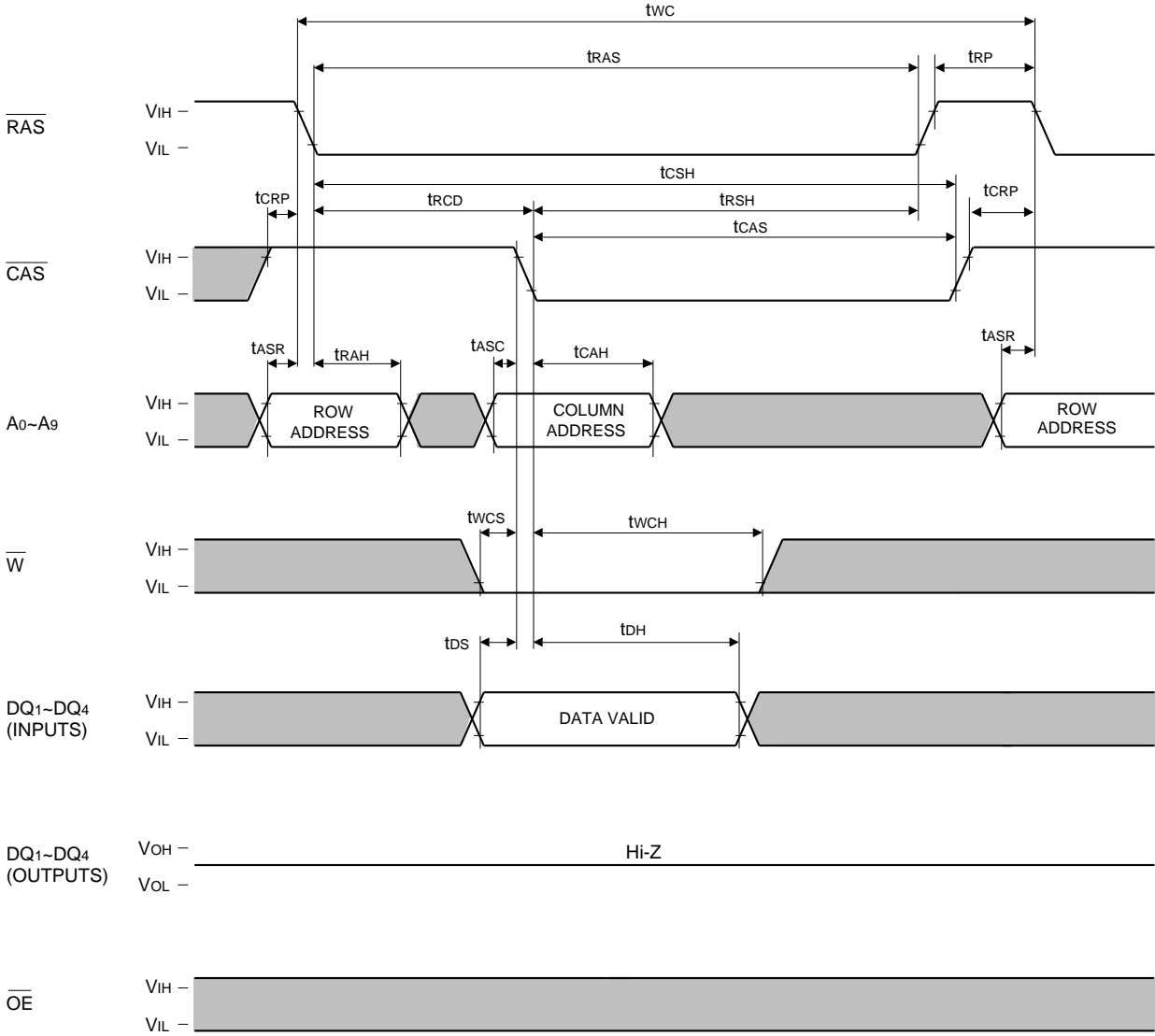


Note 32  Indicates the don't care input.
 $V_{IH(min)}$ V_{IN} $V_{IH(max)}$ or $V_{IL(min)}$ V_{IN} $V_{IL(max)}$
 Indicates the invalid output.

M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

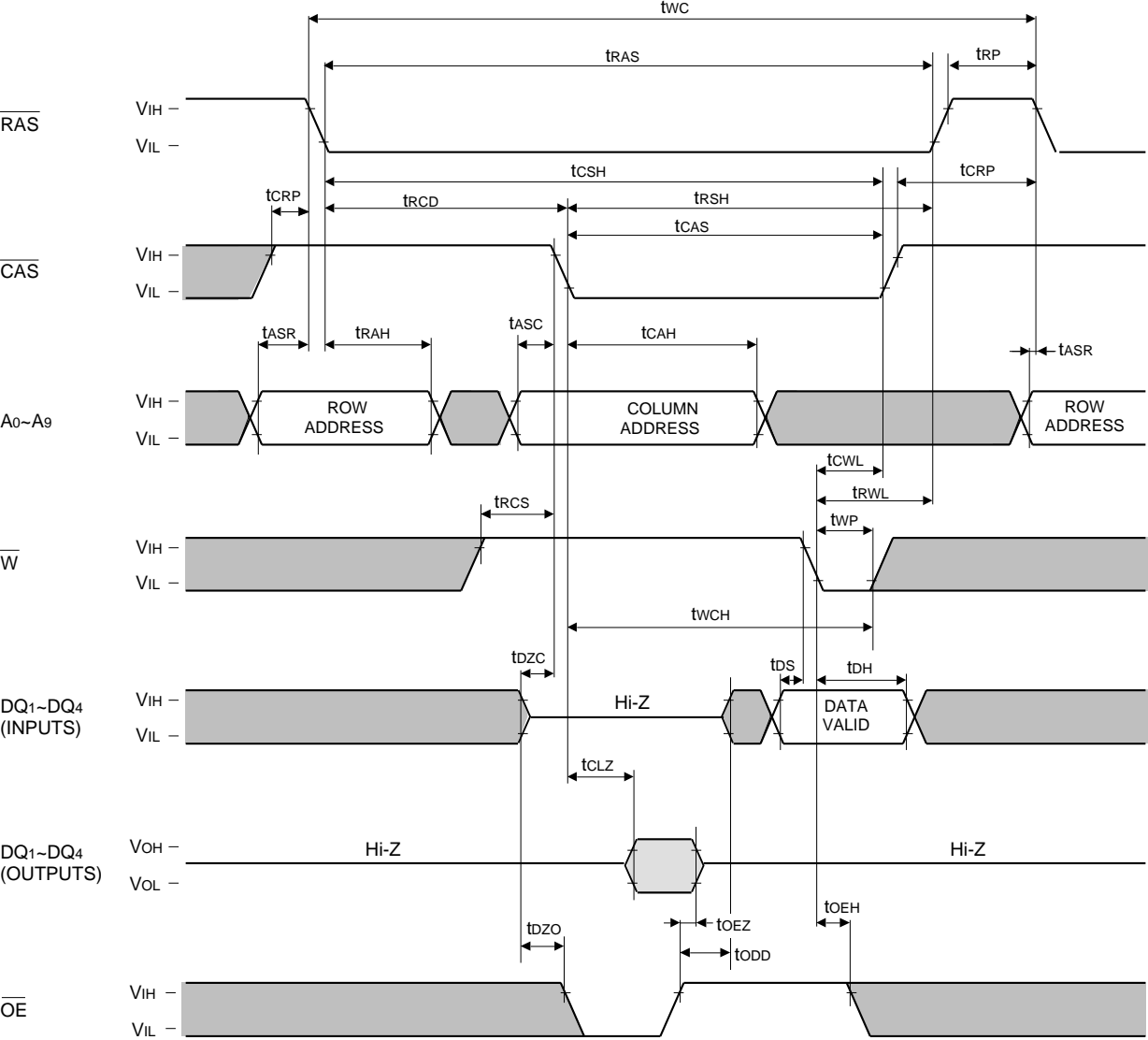
Early Write Cycle



M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

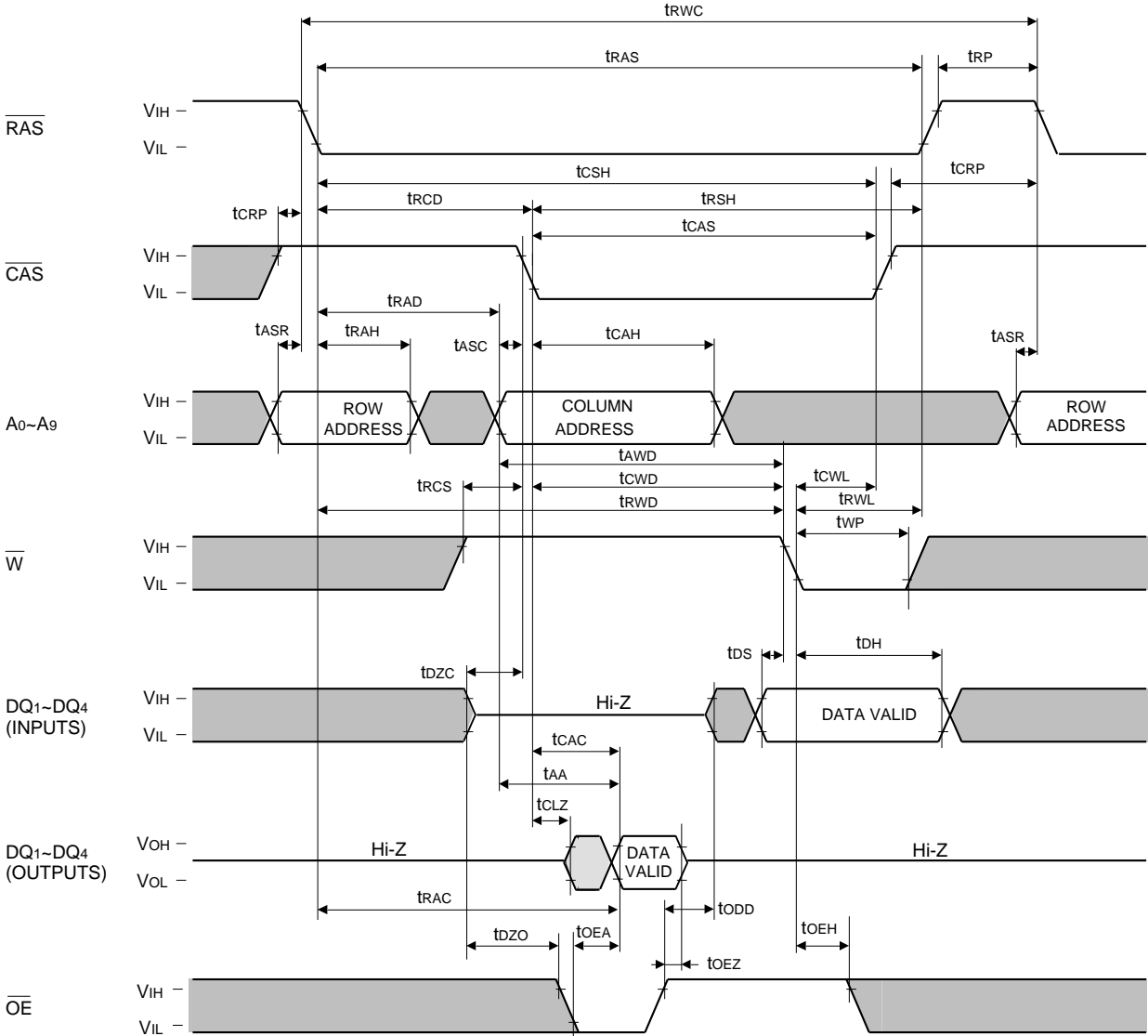
Delayed Write Cycle



M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

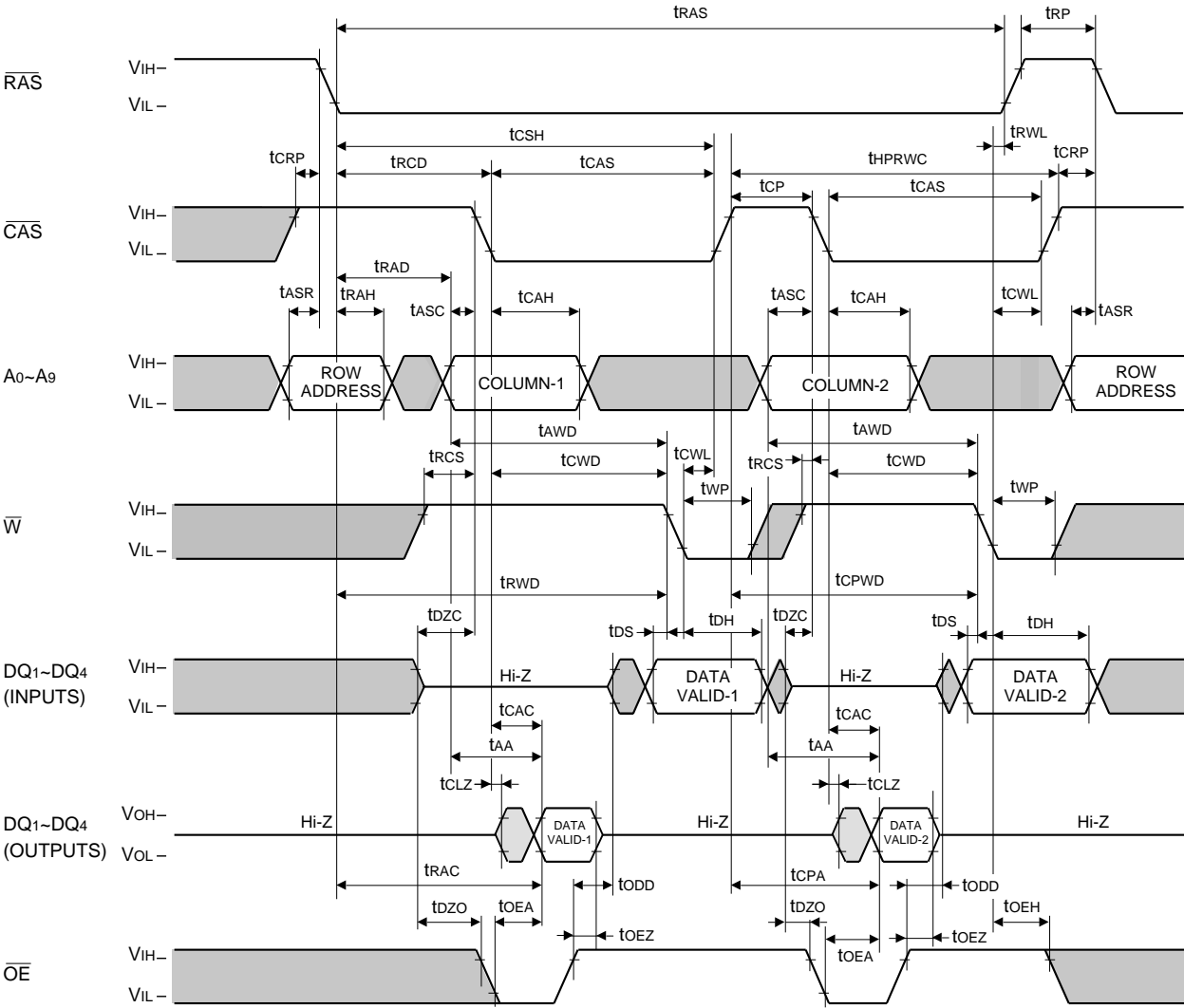
Read-Write, Read-Modify-Write Cycle



M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

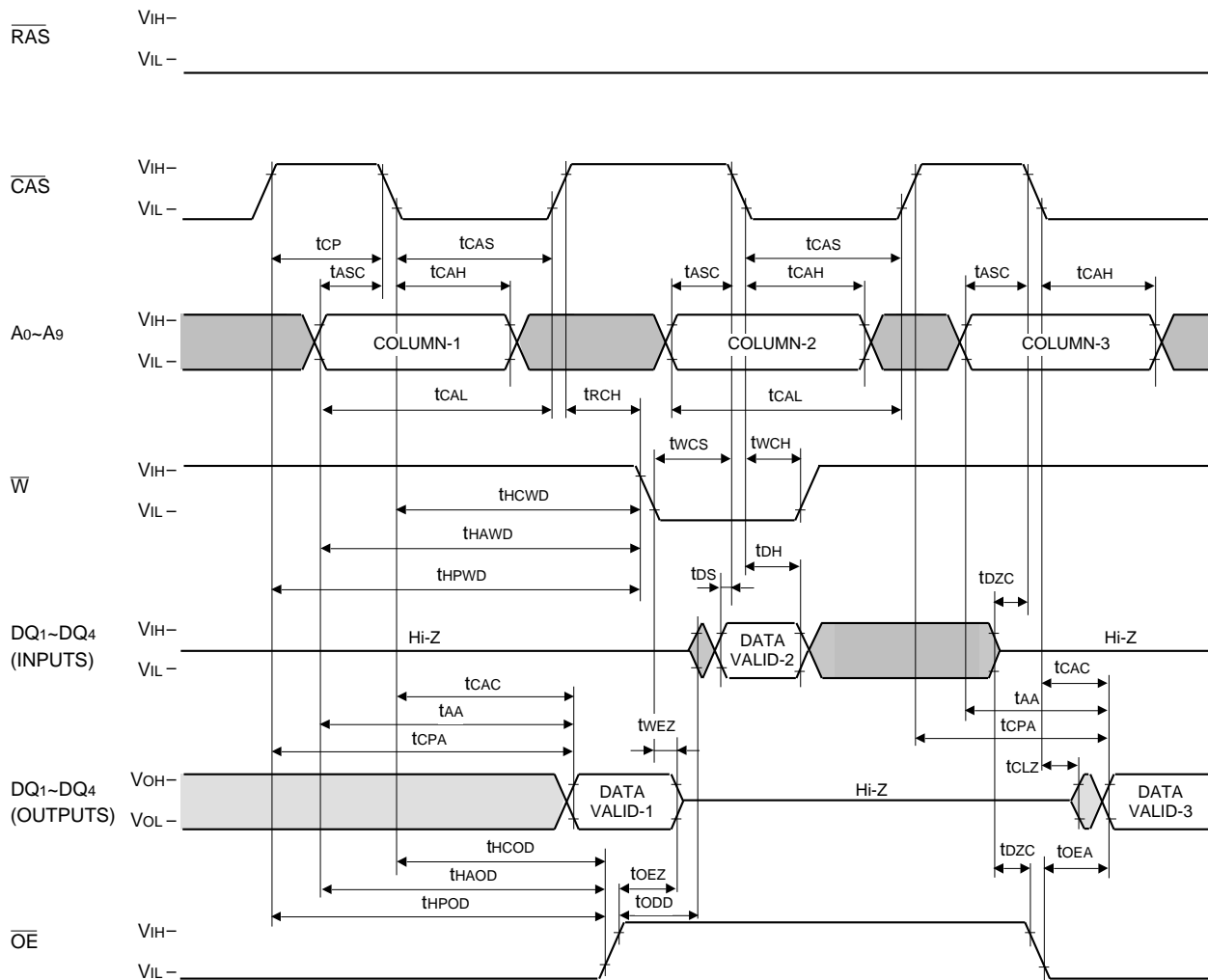
Hyper Page Mode Read-Write, Read-Modify-Write Cycle



M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

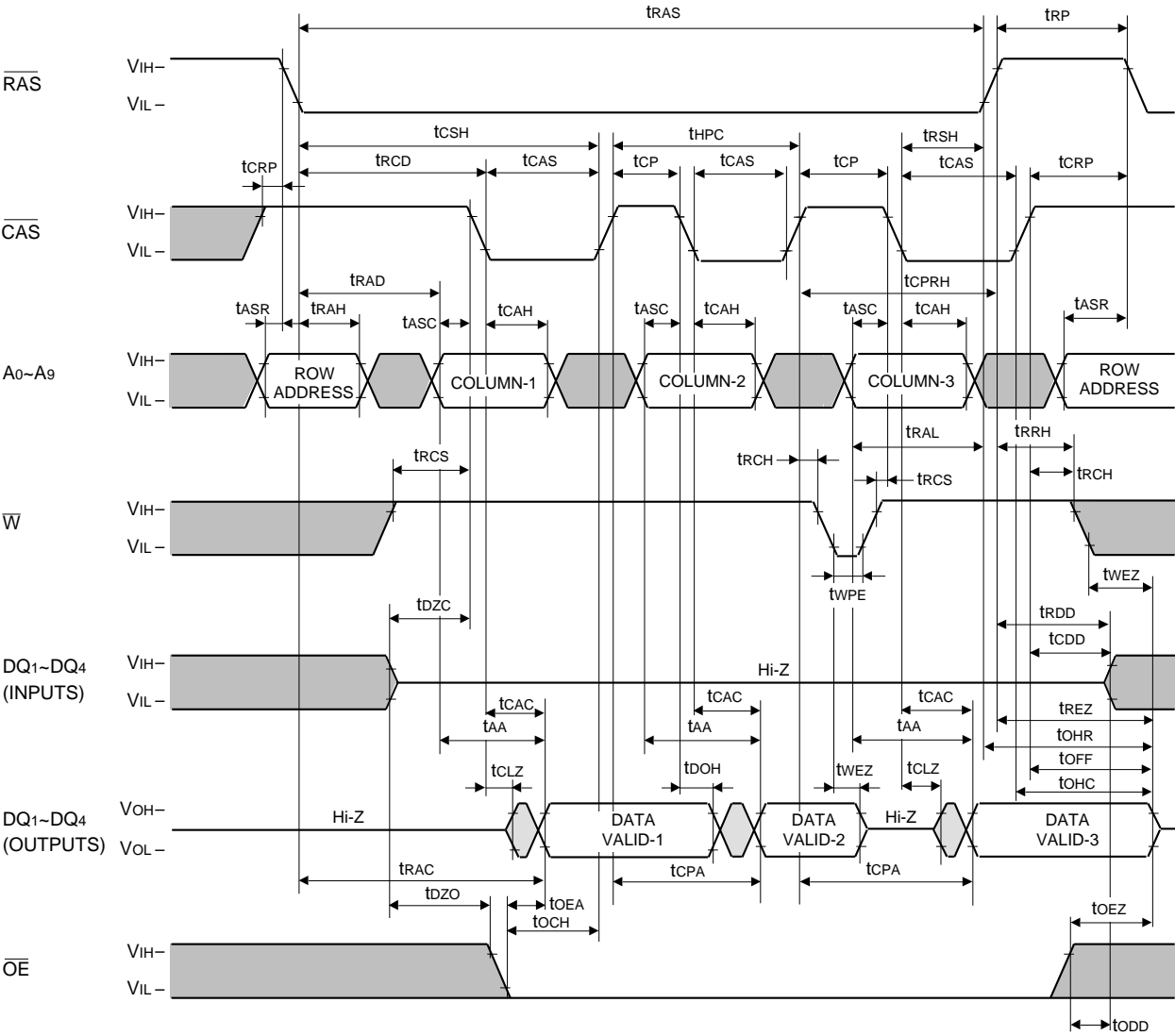
Hyper Page Mode Mix Cycle (2)



M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

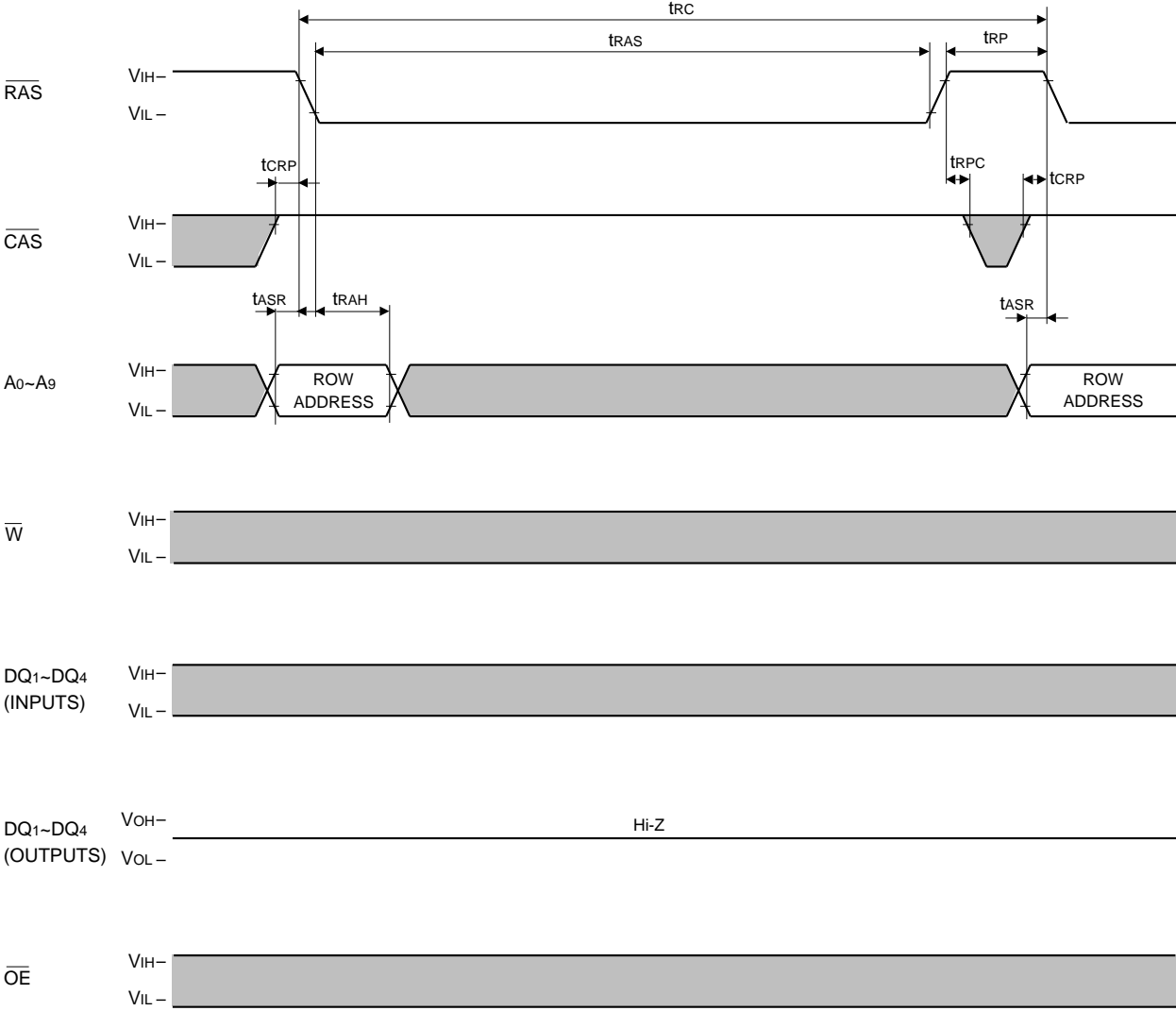
Hyper Page Mode Read Cycle (Hi-Z control by \overline{W})



M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

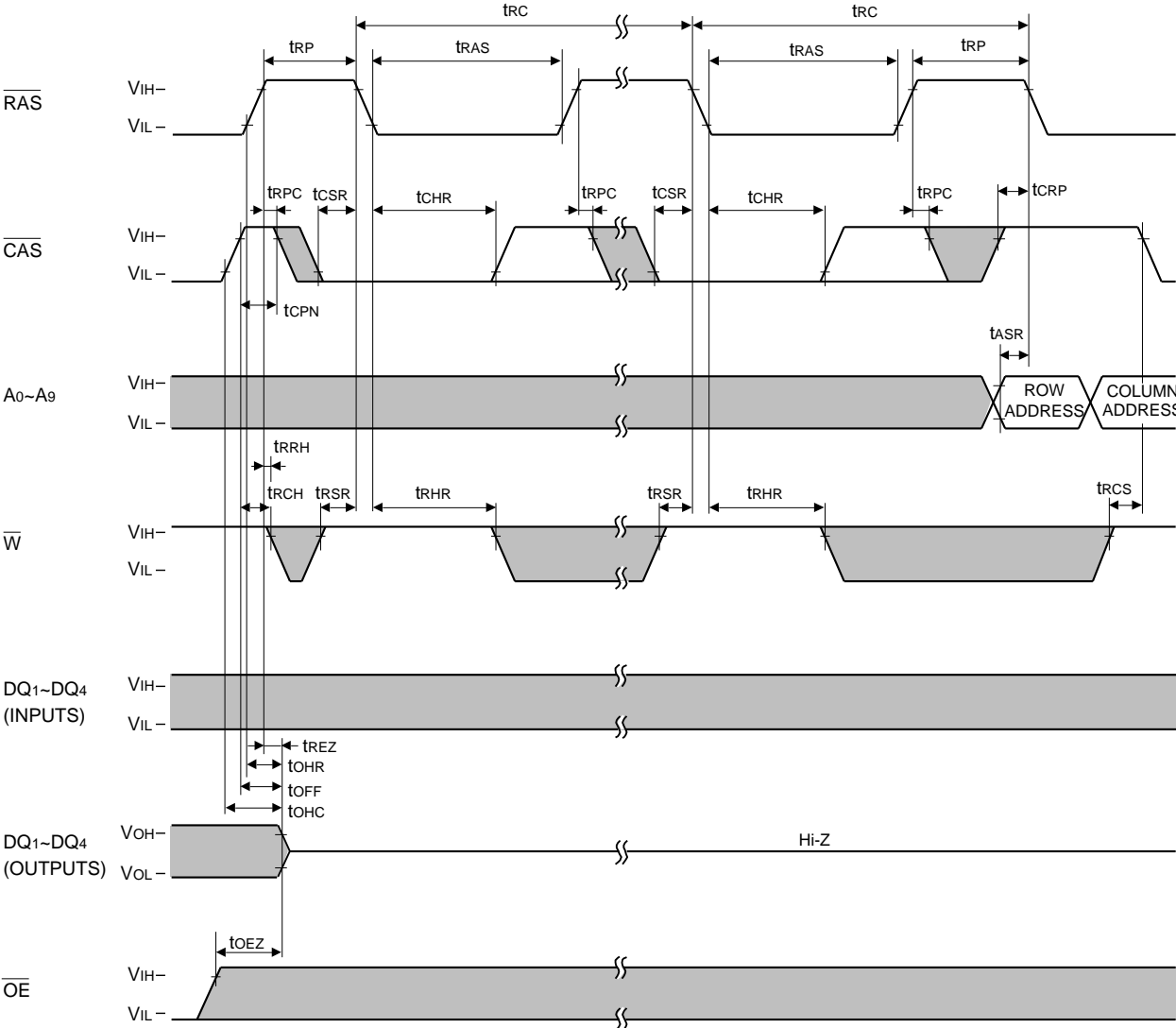
RAS-only Refresh Cycle



M5M4V4405CJ,TP-6,-7,-6S,-7S

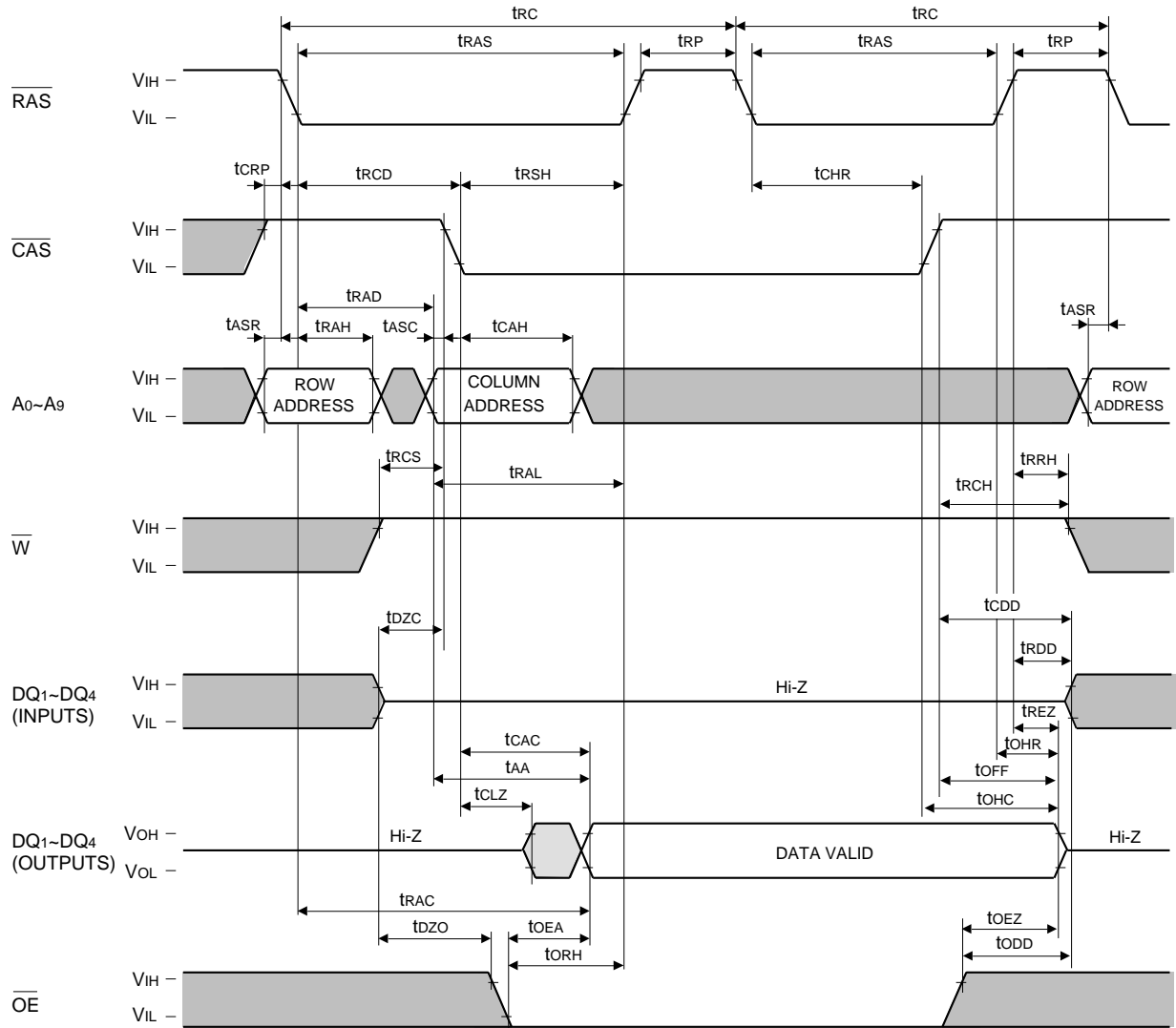
EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

CAS before RAS Refresh Cycle, Extended Refresh Cycle*



EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

Hidden Refresh Cycle (Read) (Note 33)

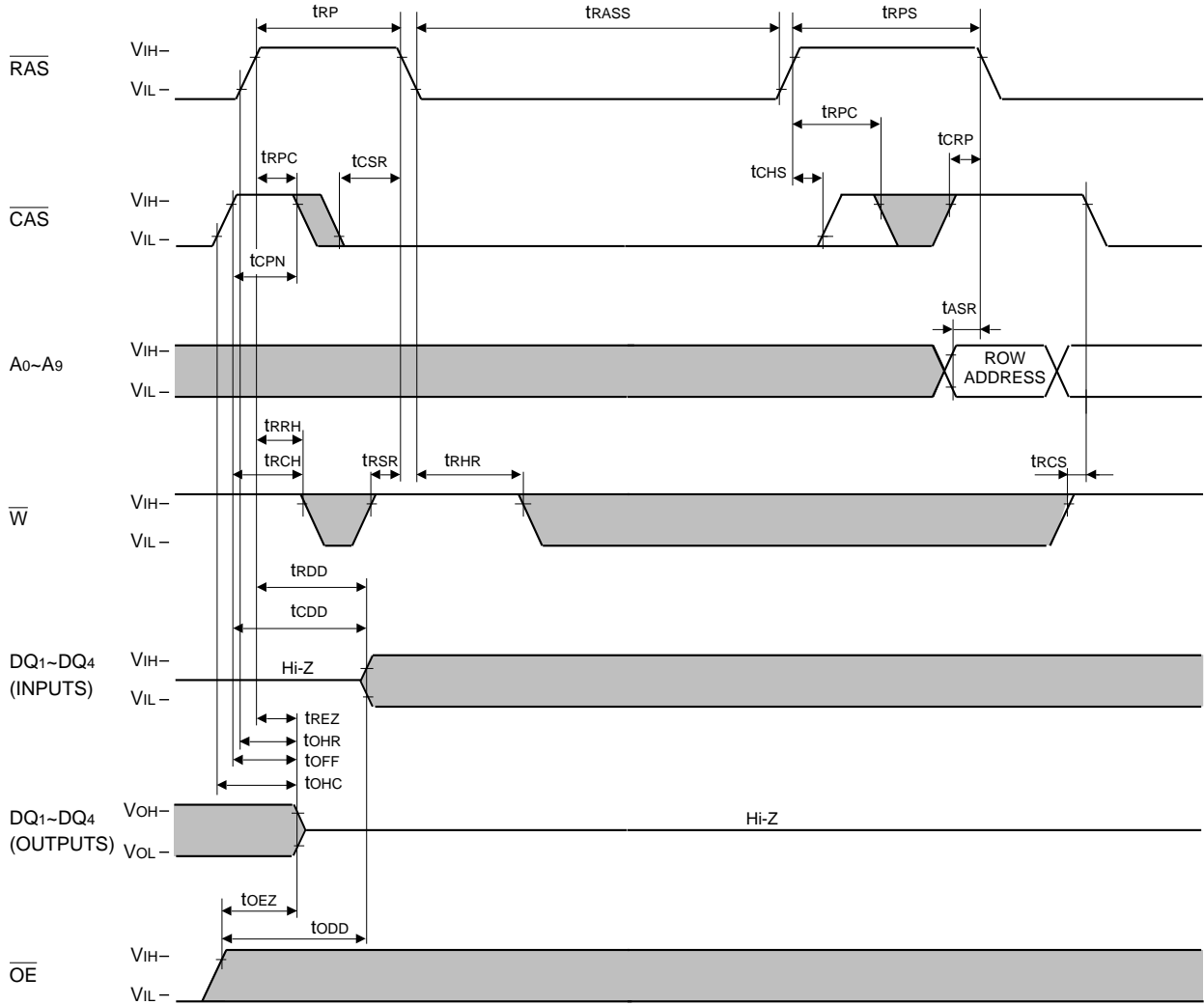


Note 33: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
 Timing requirements and output state are the same as that of each cycle shown above.

M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

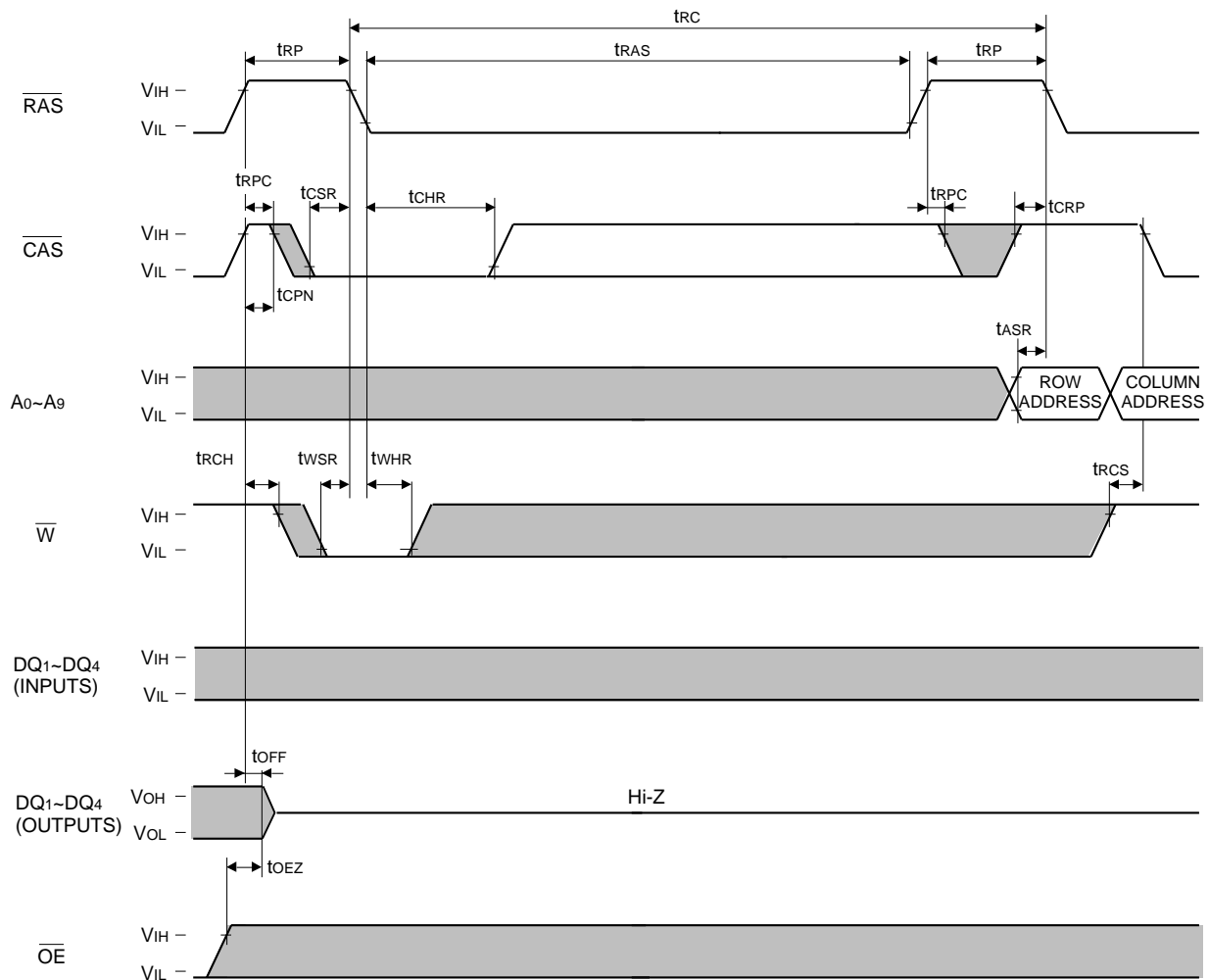
Self Refresh Cycle* (Note 30)



M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

Test Mode Set Cycle (Note 34)



Note 34: The cycle is also available for initialization cycle, but in this case device enters test mode. The test mode function is initiated with a $\overline{\text{W}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycle(WCBB cycle) as specified above timing diagram. The test mode function is terminated by either a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ (CBB) refresh or a $\overline{\text{RAS}}$ only refresh cycle. During the test mode, the device is internally organized as 4-bits wide (256 kilobytes deep) for each DQ (input / output) port. No addressing of A_0 , A_1 (column only) is required. During a write cycle, data on the each DQ (input) pin is written in parallel into all 4-bits for each DQ port and can be written independently for each DQ port. During a read cycle, the each DQ (output) pin indicates independently a HIGH state if all 4-bits are equal, and a LOW state if any bits differ. During the test mode operation, a WCBB cycle is used to perform refresh.

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

Note 30 : Self refresh sequence

Two refreshing methods should be used properly depending on the low pulse width(t_{RASS}) of \overline{RAS} signal during self refresh period.

1. Distributed refresh during Read / Write operation

(A) Timing Diagram

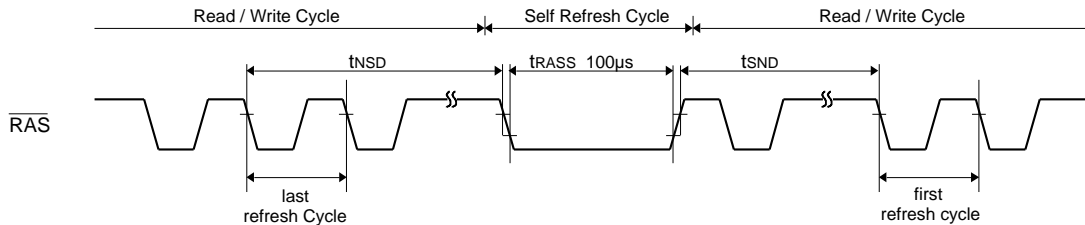
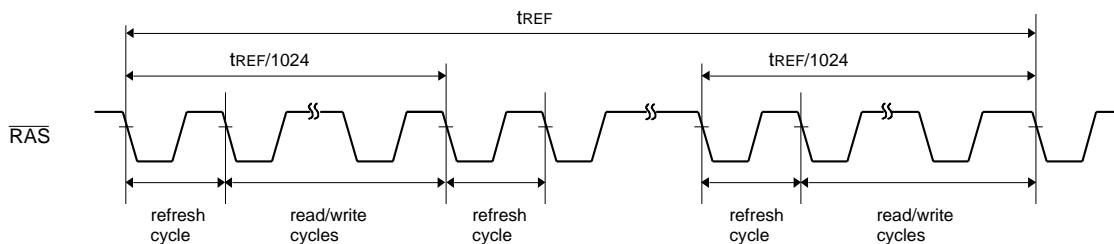


Table 2

Read / Write Cycle	Read / Write → Self Refresh	Self Refresh → Read / Write
CBR distributed refresh	t_{NSD} 125µs	t_{NSD} 125µs
\overline{RAS} only distributed refresh	t_{NSD} 16µs	t_{NSD} 16µs

(B) Definition of distributed refresh



Definition of CBR distributed refresh
(Including extended refresh)

The CBR distributed refresh performs more than 1024 constant period(125µs max.) CBR cycles within 128 ms.

Definition of \overline{RAS} only distributed refresh

All combinations of nine row address signals (A_0 ~ A_9) are selected during 1024 constant period(16µs max.) \overline{RAS} only refresh cycles within 16.4 ms.

Note:

Hidden refresh may be used instead of CBR refresh.

$\overline{RAS}/\overline{CAS}$ refresh may be used instead of \overline{RAS} only refresh.

1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of \overline{RAS} signal in the last CBR refresh cycle during read/write operation period to the falling edge of \overline{RAS} signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).

- Switching from self refresh operation to read/write operation. The time interval from the rising edge of \overline{RAS} signal at the end of self refresh operation to the falling edge of \overline{RAS} signal in the first CBR refresh cycle during read/write operation period should be set within t_{NSD} (shown in table 2).

1.2 \overline{RAS} only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of \overline{RAS} signal in the last \overline{RAS} only refresh cycle during read/write operation period to the falling edge of \overline{RAS} signal at the start of self refresh operation should be set within 16µs.
- Switching from self refresh operation to read/write operation. The time interval t_{NSD} from the rising edge of \overline{RAS} signal at the end of self refresh operation to the falling edge of \overline{RAS} signal in the first CBR refresh cycle during read/write operation period should be set within 16µs.

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

2. Burst refresh during Read/Write operation
(A) Timing diagram

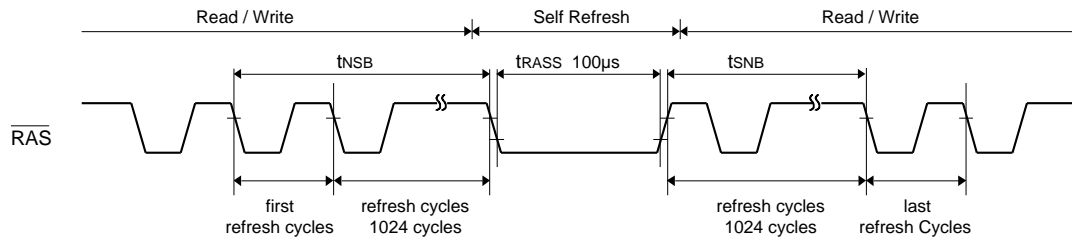
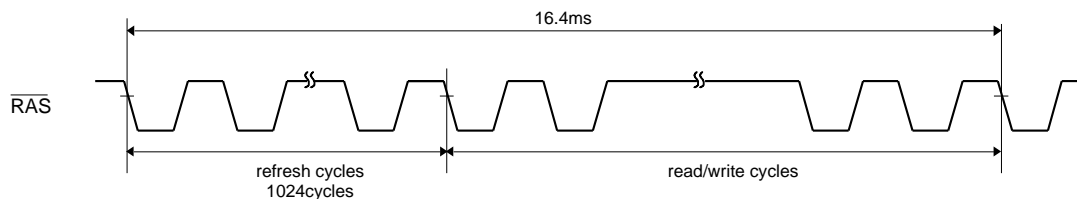


Table 3

Read / Write Cycle	Read / Write → Self Refresh	Self Refresh → Read / Write
CBR burst refresh	tNSB 16.4ms	tSNB 16.4ms
$\overline{\text{RAS}}$ only burst refresh	tNSB+tSNB 16.4ms	

(B) Definition of burst refresh



Definition of CBR burst refresh

The CBR burst refresh performs more than 1024 continuous CBR cycles within 16.4 ms.

Definition of $\overline{\text{RAS}}$ only burst refresh

All combination of nine row address signals ($A_0 \sim A_9$) are selected during 1024 continuous $\overline{\text{RAS}}$ only refresh cycles within 16.4 ms.

2.1 CBR burst refresh

- Switching from read/write operation to self refresh operation. The time interval ns from the falling edge of $\overline{\text{RAS}}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{\text{RAS}}$ signal at the start of self refresh operation should be set within 16.4 ms.
- Switching from self refresh operation to read/write operation. The time interval snob from the rising edge of $\overline{\text{RAS}}$ signal at the end of self refresh operation to the falling edge of $\overline{\text{RAS}}$ signal in the last CBR refresh cycle during read/write operation period should be set within 16.4 ms.

2.2 $\overline{\text{RAS}}$ only burst refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{\text{RAS}}$ signal in the first $\overline{\text{RAS}}$ only refresh cycle during read/write operation period to the falling edge of $\overline{\text{RAS}}$ signal at the start of self refresh operation should be set within tNSB(Shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{\text{RAS}}$ signal at the end of self refresh operation to the falling edge of $\overline{\text{RAS}}$ signal in the last $\overline{\text{RAS}}$ only refresh cycle during read/write operation period should be set within tSNB(shown in table 3).