Description

The GM76C88AL is a 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology and operated from a single 5V supply. Advanced circuit techniques provide low power feature with a maximum operating current of 40mA and standby current of max 100μA. Its very low standby power requirement makes it ideal for applications requiring nonvolatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuits.

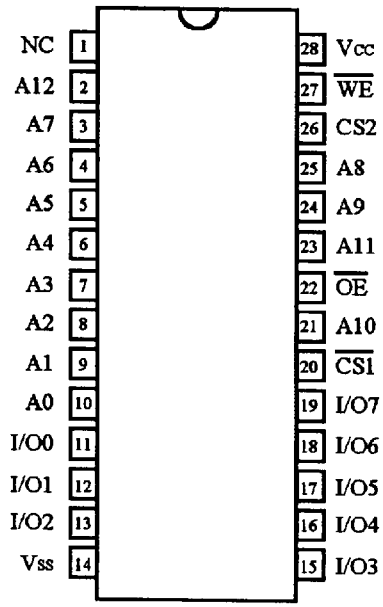
Features

- Fast Access Time : 120/150ns
- Low Power Operation
  Standby : 2μA (Typ)
  Operation : 25mA (Typ)
- Completely Static RAM : No Clock or Timing Strobe Required
- Non-Volatile Storage with Back-up Batteries
- 3-State Output with Wired-OR Capability
- Directly TTL Compatible : All Inputs and Outputs
- Single Power Supply (5V $\pm$ 10%)
- Standard 28 DIP, SOP and S-DIP

Pin Description

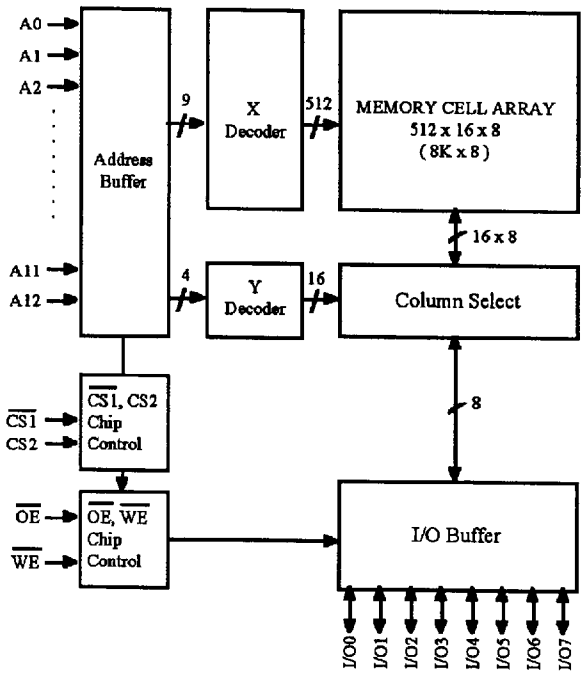
Pin	Function
A0-A12	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS1}$, CS2	Chip Select
$\overline{OE}$	Output Enable
I/O0-I/O7	Data Input/Output
Vcc	Power Supply (+5V)
Vss	Ground
NC	No Connection

Pin Configuration



(Top View)

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	℃
T_{STG}	Storage Temperature	-65 ~ 150	℃
T_{SOL}	Soldering Temperature and Time	260, 10 (at lead)	℃, S
V_{CC}	Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-0.5 ~ 7.0	V
P_D	Power Dissipation	1.0	W

Recommended Operating Conditions ($T_A = 0 \sim 70℃$)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	-0.5	-	0.8	V

Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	A0 to A12	DATA I/O	MODE
H	X	X	X	-	Hi-Z	Standby
X	L	X	X	-	Hi-Z	
L	H	X	L	Stable	Input Data	Write
L	H	L	H	Stable	Output Data	Read
L	H	H	H	Stable	Hi-Z	Output Disable

*Note: X means don't care.

DC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$, $T_A = 0 \sim 70℃$)

Symbol	Parameter	Conditions		Min	*Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = -1.0mA		2.4	V_{CC}-0.1	-	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0mA		-	0.2	0.4	V
$I_{I(L)}$	Input Leakage Current	V_I = 0 to V_{CC}		-	-	1	uA
$I_{O(L)}$	Output Leakage Current	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{CC}		-	-	1	uA
I_{CC1}	Operating Supply Current	V_I = V_{IL}, V_{IH} $I_{I/O}$ = 0mA	t_{RC} = 1us	-	6	10	mA
I_{CC2}			t_{PC} = Min	-	25	40	
		V_I = 0.2V/V_{CC}-0.2V $I_{I/O}$ = 0mA	t_{RC} = 1us	-	3	5	mA
			t_{PC} = Min	-	20	35	
I_{CCS1}	Standby Power Supply Current	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL}		-	1.5	3	mA
I_{CCS2}		$\overline{CS1}$ = CS2 ≥ V_{CC}-0.2V or CS2 ≤ 0.2V		-	2	100	uA

*TYP. Values are measured at 25℃, V_{CC} = 5V

AC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$, $T_A = 0 \sim 70℃$)

Read Cycle

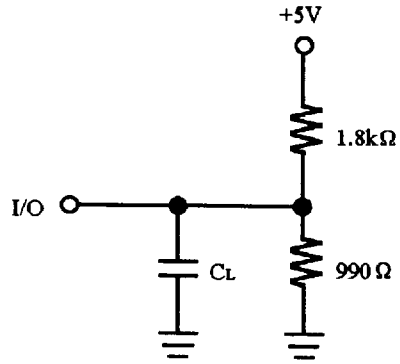
Symbol	Parameter	Conditions	GM76C88AL-12		GM76C88AL-15		Unit
			Min	Max	Min	Max	
t_{RC}	Read Cycle Time	*1	120	-	150	-	ns
t_{AA}	Address Access Time		-	120	-	150	ns
t_{ACS1}	Chip Select 1 Access Time		-	120	-	150	ns
t_{ACS2}	Chip Select 2 Access Time		-	120	-	150	ns
t_{OE}	Output Enable Access Time		-	60	-	70	ns
t_{OH}	Output Hold Time		30	-	30	-	ns
t_{CLZ1}	Chip Select 1 Output Setup Time	*2	10	-	10	-	ns
t_{CHZ1}	Chip Select 1 Output Floating		-	60	-	70	ns
t_{CLZ2}	Chip Select 2 Output Setup Time		10	-	10	-	ns
t_{CHZ2}	Chip Select 2 Output Floating		-	60	-	70	ns
t_{OLZ}	Output Enable Output Setup Time		5	-	5	-	ns
t_{OHZ}	Output Enable Output Floating		-	55	-	60	ns

Write Cycle

Symbol	Parameter	Conditions	GM76C88AL-12		GM76C88AL-15		Unit
			Min	Max	Min	Max	
t_{WC}	Write Cycle Time	*1	120	-	150	-	ns
t_{CW1}	Chip select Time 1		100	-	120	-	ns
t_{CW2}	Chip Select Time 2		100	-	120	-	ns
t_{AW}	Address Enable Time		100	-	120	-	ns
t_{AS}	Address Setup Time		0	-	0	-	ns
t_{WP}	Write Pulse Width		85	-	100	-	ns
t_{WR}	Address Hold Time		0	-	0	-	ns
t_{DW}	Input Data Setup Time		50	-	60	-	ns
t_{DH}	Input Data Hold Time		0	-	0	-	ns
t_{WHZ}	R/W Output Floating	*2	-	60	-	70	ns
t_{OW}	R/W Output Setup Time		10	-	10	-	ns

*1 Test Conditions.

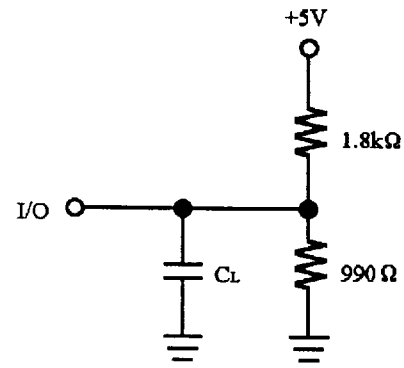
1. Input pulse level : 0.8V to 2.2V
2. $t_r = t_f = 5ns$
3. Input/output timing reference level : 1.5V
4. Output load : 1TTL + 100pF



C_L = 100pF (Includes Jig Capacitance)

*2 Test Conditions.

1. Input pulse level : 0.8V to 2.2V
2. $t_r = t_f = 10ns$
3. Input timing reference level : 1.5V
4. Output timing reference levels : ±200mV (the level displace from stable output voltage level)
5. Output load : 1TTL + 5pF



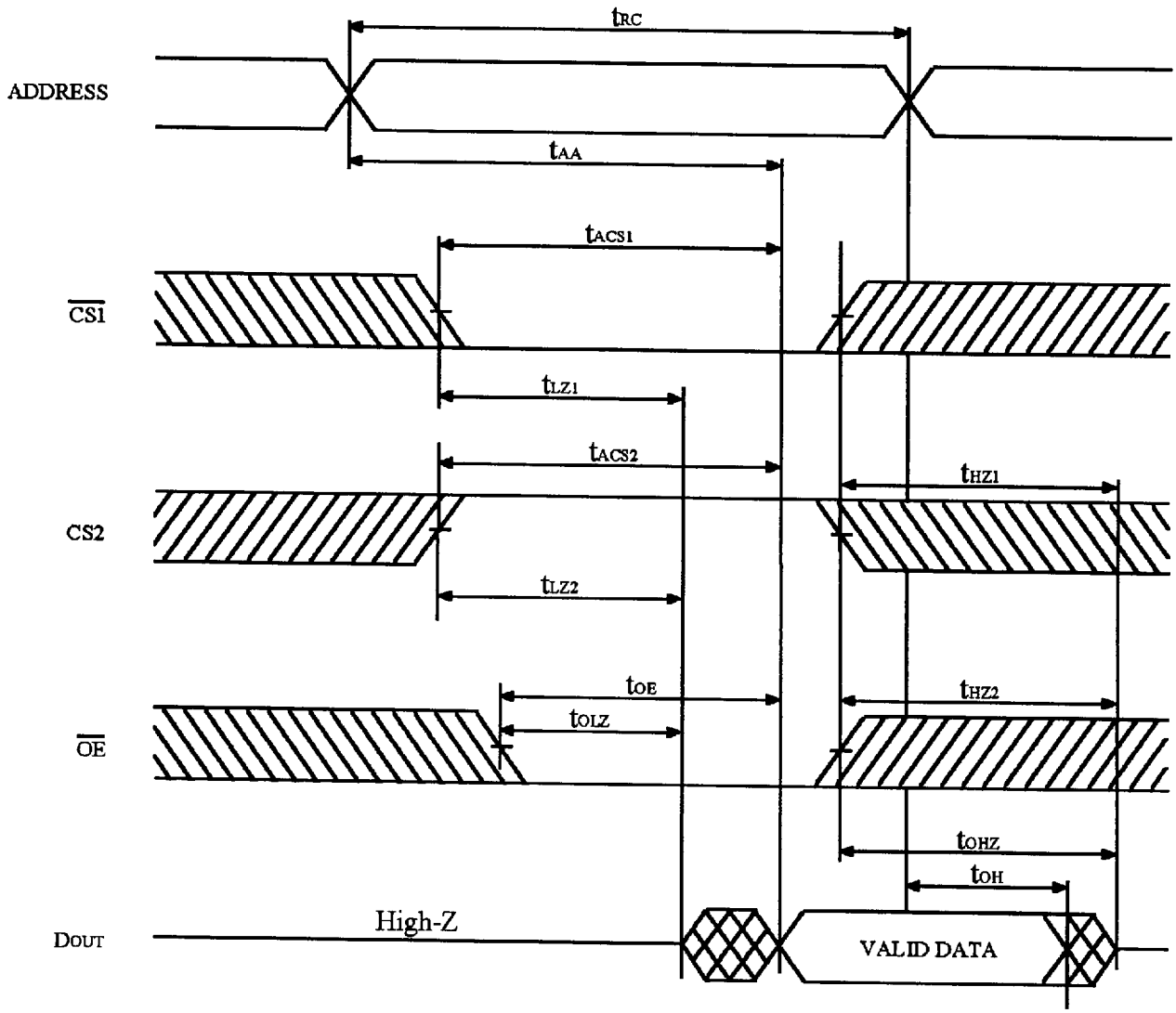
C_L = 5pF (Includes Jig Capacitance)

Capacitance ($f = 1MHz$, $T_A = 25℃$)

Symbol	Parameter	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	$V_I = 0V$	-	6	pF
C_{OUT}	Output Capacitance	$V_O = 0V$	-	8	pF

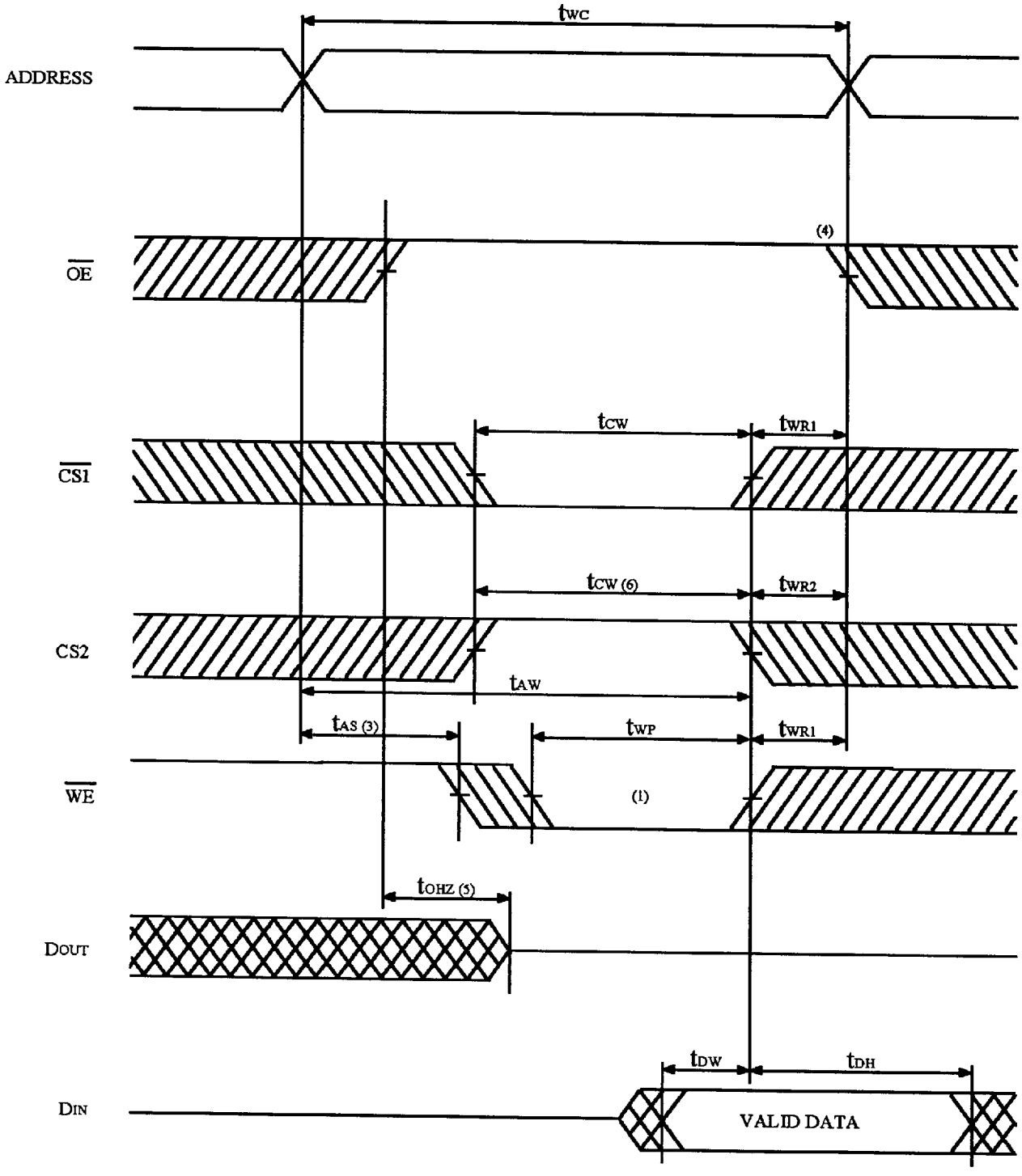
Timing Waveforms

Read Cycle

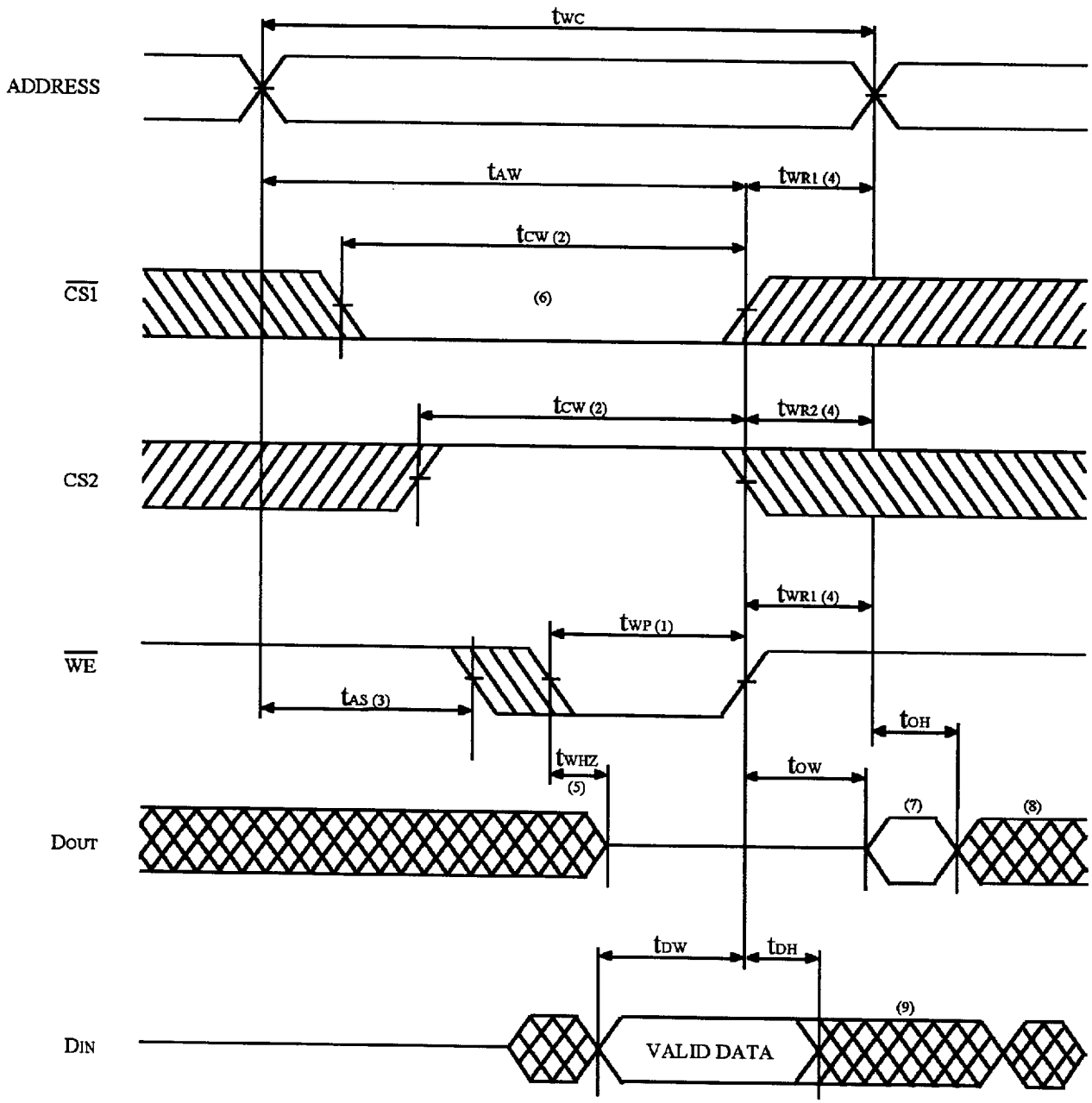


Note : 1) $\overline{WE}$ is High for Read Cycle

Write Cycle (1) ($\overline{OE}$ Controlled)



Write Cycle (2) ($\overline{OE}$ Low Fix)



Notes:

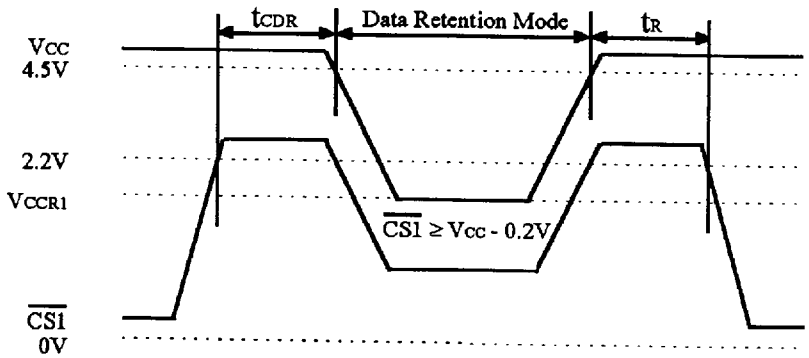
1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earlist transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high, twp is measured from the beginning of write to the end of wirte.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high. t_{WR2} applies in case a write ends at CS2 going low.
5. During this period, I/O pins are in the output state, therfore the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the same phase of the latest written data in this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

Data Retention Characteristics ($T_A = 0 \sim 70℃$)

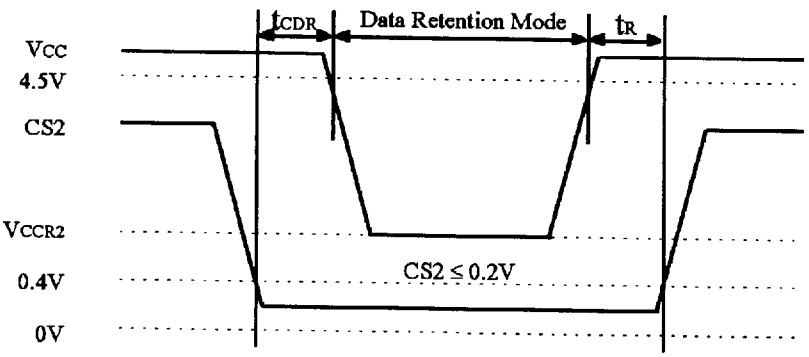
Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
V_{CCR}	Data Retention Supply Voltage	V_{CCR1}	$\overline{CS1} \geq V_{CC}-0.2V$, $CS2 \geq V_{CC}-0.2V$ or $CS2 \leq 0.2V$	2.0	-	5.5	V
		V_{CCR2}	$CS2 \leq 0.2V$	2.0	-	-	V
I_{CCR}	Data Retention Current	I_{CCR1}	$V_{CC} = 3.0V$, $\overline{CS1} \geq V_{CC}-0.2V$ $CS2 \geq V_{CC}-0.2V$ or $CS2 \leq 0.2V$	-	1	50*	uA
		I_{CCR2}	$V_{CC} = 3.0V$, $CS2 \leq 0.2V$	-	1	50*	uA
t_{CDR}	Chip Select to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time	t_R		t_{RC}**	-	-	ns

* V_{IL} min = -3V, 1uA max at $T_A = 0 \sim 40℃$
** t_{RC} = Read Cycle Time

• Low Vcc Data Retention Mode: (1) $\overline{CS1}$ Controlled



• Low Vcc Data Retention Mode: (2) CS2 Controlled

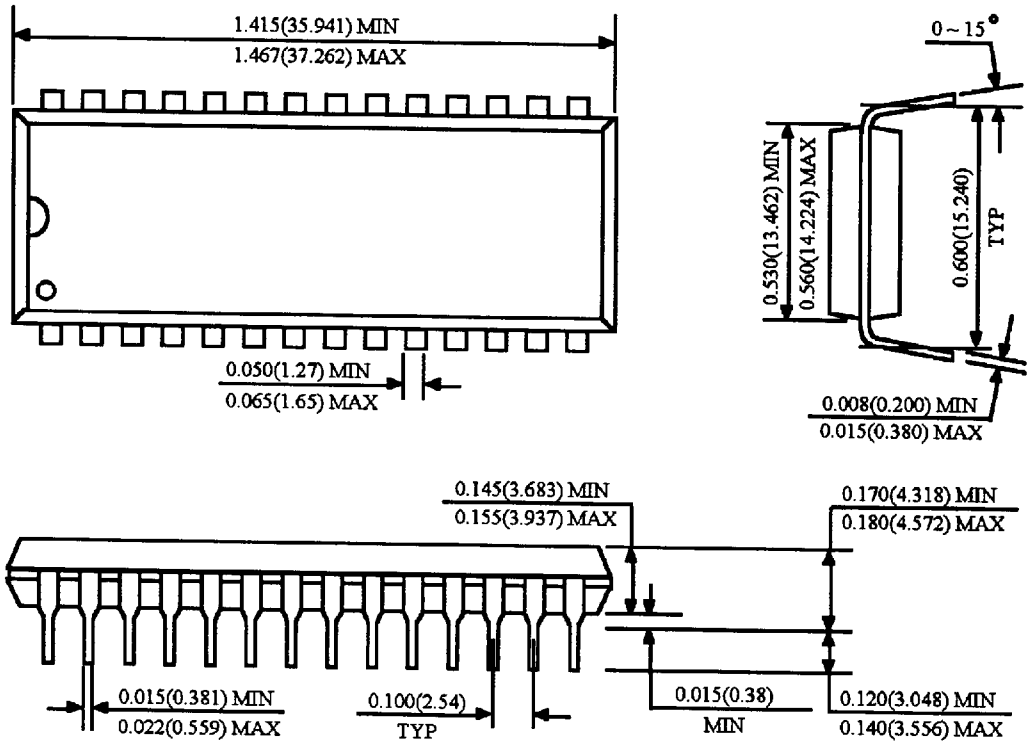


Notes: In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and D_{IN} buffer. If CS2 controls data retention mode, V_{IN} for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$. The other input levels (Address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

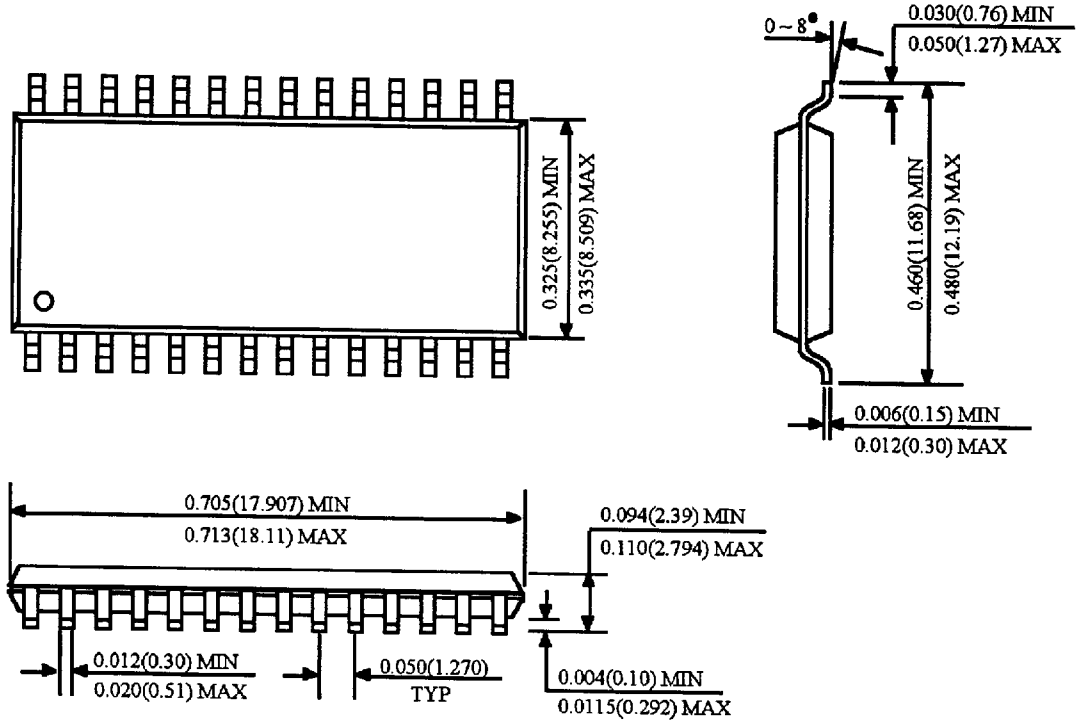
Package Dimensions

Unit: Inches (mm)

28 DIP - A



28 SOP - A



28 SKINNY DIP

Unit: Inches (mm)