

Complementary N- and P-Channel 20 V (D-S) MOSFET

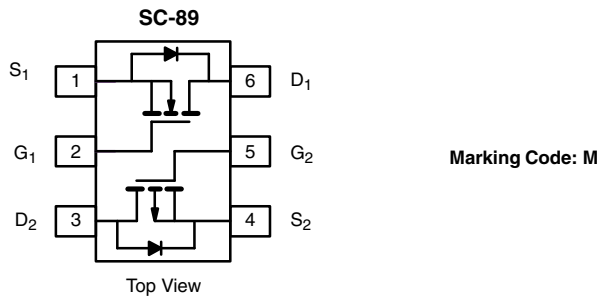
PRODUCT SUMMARY			
	V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (mA)
N-Channel	20	5 at $V_{GS} = 4.5$ V	200
		7 at $V_{GS} = 2.5$ V	175
		9 at $V_{GS} = 1.8$ V	150
		10 at $V_{GS} = 1.5$ V	50
P-Channel	- 20	8 at $V_{GS} = - 4.5$ V	- 150
		12 at $V_{GS} = - 2.5$ V	- 125
		15 at $V_{GS} = - 1.8$ V	- 100
		20 at $V_{GS} = - 1.5$ V	- 30

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET: 1.5 V Rated
- Very Small Footprint
- High-Side Switching
- Low On-Resistance:
N-Channel, 5 Ω
P-Channel, 8 Ω
- Low Threshold: ± 0.9 V (typ.)
- Fast Switching Speed: 45 ns (typ.)
- 1.5 V Operation
- Gate-Source ESD Protected: 2000 V
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE



Ordering Information: Si1035X-T1-GE3 (Lead (Pb)-free and Halogen-free)

BENEFITS

- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Battery Voltage Operation

APPLICATIONS

- Replace Digital Transistor, Level-Shifter
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones, Pagers

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		5 s	Steady State	5 s	Steady State		
Drain-Source Voltage	V_{DS}	20		- 20		V	
Gate-Source Voltage	V_{GS}	± 5					
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D	$T_A = 25$ °C	190	180	- 155	- 145	mA
		$T_A = 85$ °C	140	130	- 110	- 105	
Pulsed Drain Current ^b	I_{DM}	650		- 650			
Continuous Source Current (Diode Conduction)	I_S	450	380	- 450	- 380		
Maximum Power Dissipation ^a	P_D	$T_A = 25$ °C	280	250	280	250	mW
		$T_A = 85$ °C	145	130	145	130	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150				°C	
Gate-Source ESD Rating (HBM, Method 3015)	ESD	2000				V	

Notes:

a. Surface mounted on FR4 board.

b. Pulse width limited by maximum junction temperature.

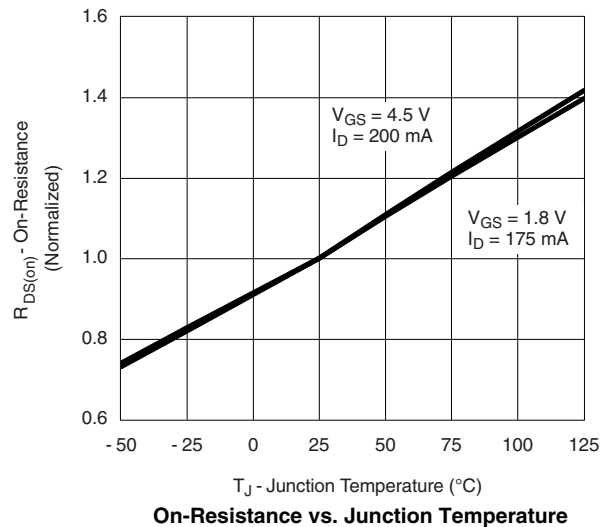
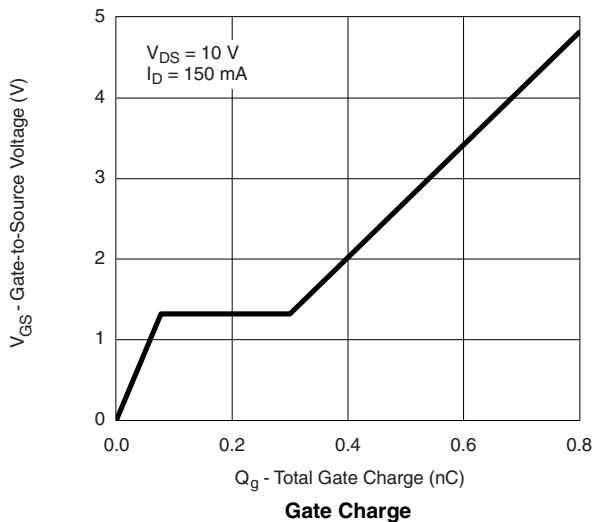
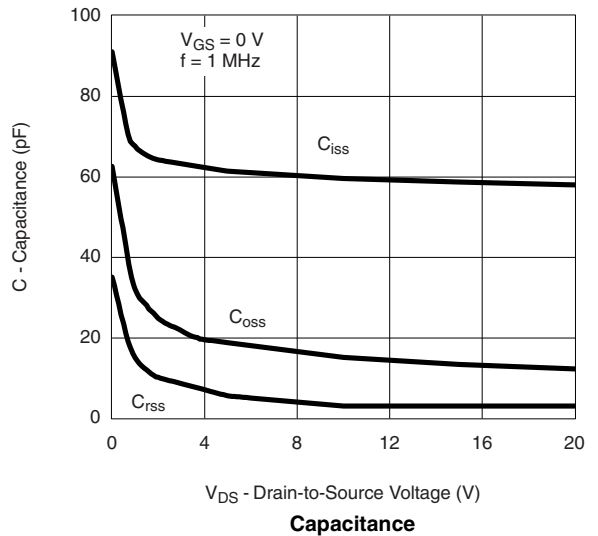
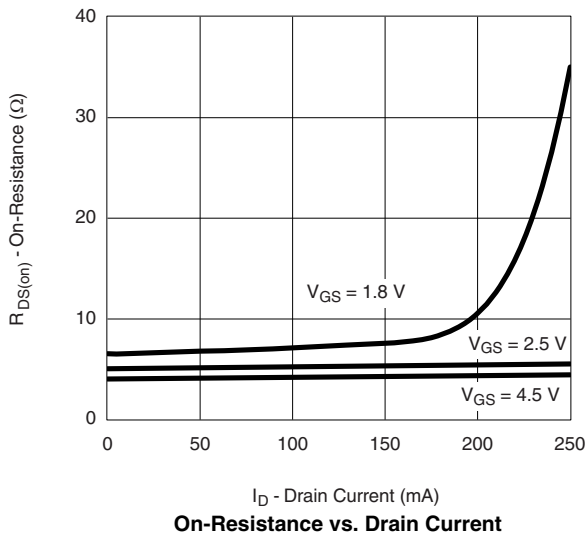
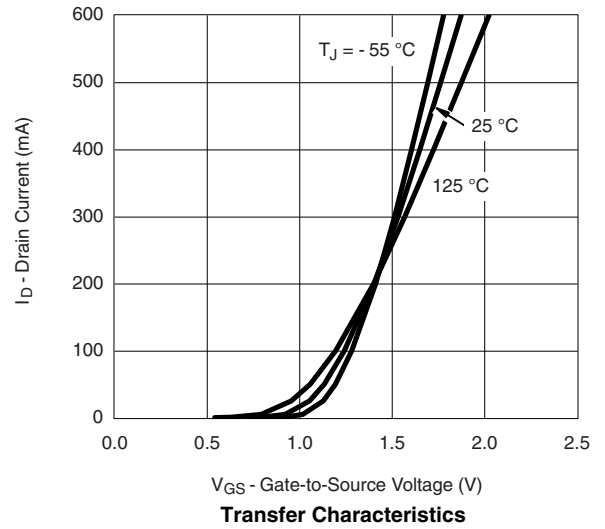
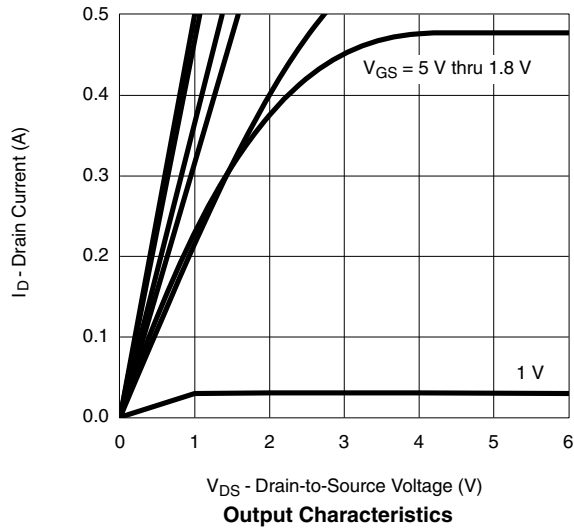
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	0.40		V	
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.40			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 2.8\text{ V}$	N-Ch	± 0.5	± 1.0	μA	
			P-Ch	± 0.5	± 1.0		
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$	N-Ch	± 1.5	± 3.0		
			P-Ch	± 1.0	± 3.0		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$	N-Ch	1	500	nA	
		$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$	P-Ch	-1	-500		
		$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$	N-Ch			10	μA
		$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$	P-Ch			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 4.5\text{ V}$	N-Ch	250		mA	
		$V_{DS} = -5\text{ V}, V_{GS} = -4.5\text{ V}$	P-Ch	-200			
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 200\text{ mA}$	N-Ch		5	Ω	
		$V_{GS} = -4.5\text{ V}, I_D = -150\text{ mA}$	P-Ch		8		
		$V_{GS} = 2.5\text{ V}, I_D = 175\text{ mA}$	N-Ch		7		
		$V_{GS} = -2.5\text{ V}, I_D = 125\text{ mA}$	P-Ch		12		
		$V_{GS} = 1.8\text{ V}, I_D = 150\text{ mA}$	N-Ch		9		
		$V_{GS} = -1.8\text{ V}, I_D = -100\text{ mA}$	P-Ch		15		
		$V_{DS} = 1.5\text{ V}, I_D = 40\text{ mA}$	N-Ch		10		
		$V_{DS} = -1.5\text{ V}, I_D = -30\text{ mA}$	P-Ch		20		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 200\text{ mA}$	N-Ch		0.5	S	
		$V_{DS} = -10\text{ V}, I_D = -150\text{ mA}$	P-Ch		0.4		
Diode Forward Voltage ^a	V_{SD}	$I_S = 150\text{ mA}, V_{GS} = 0\text{ V}$	N-Ch		1.2	V	
		$I_S = -150\text{ mA}, V_{GS} = 0\text{ V}$	P-Ch		-1.2		
Dynamic^b							
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 150\text{ mA}$ $V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -150\text{ mA}$	N-Ch		750	pC	
Gate-Source Charge	Q_{gs}		P-Ch		1500		
			N-Ch		75		
Gate-Drain Charge	Q_{gd}		P-Ch		150		
		N-Ch		225			
Turn-On Time	t_{ON}	$V_{DD} = 10\text{ V}, R_L = 47\text{ }\Omega$ $I_D \cong 250\text{ mA}, V_{GEN} = 4.5\text{ V}, R_g = 10\text{ }\Omega$	N-Ch		75	ns	
			P-Ch		80		
Turn-Off Time	t_{OFF}		$V_{DD} = -10\text{ V}, R_L = 65\text{ }\Omega$ $I_D \cong -150\text{ mA}, V_{GEN} = -4.5\text{ V}, R_g = 10\text{ }\Omega$	N-Ch			75
				P-Ch			90

Notes:

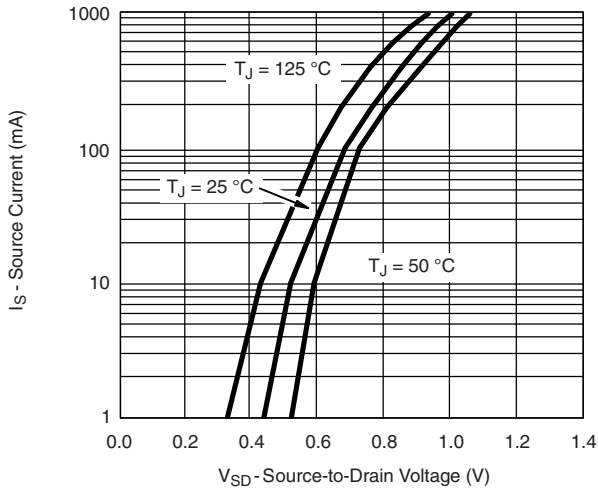
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

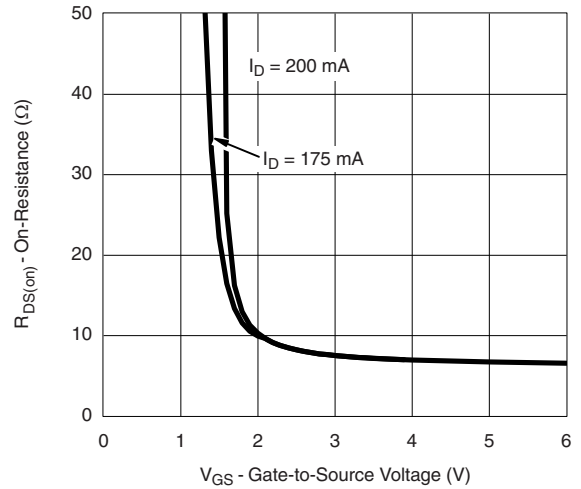
N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



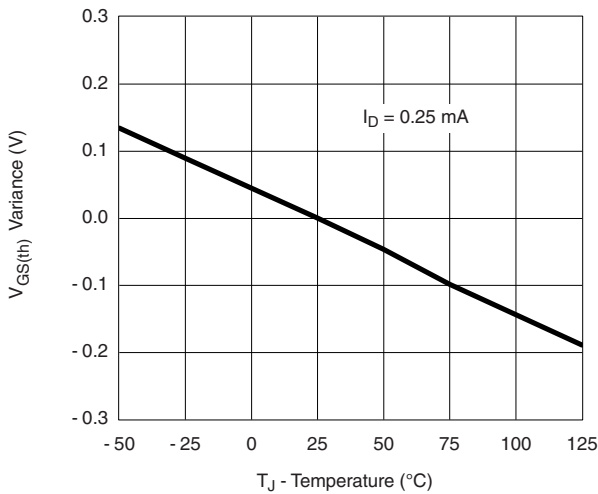
N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



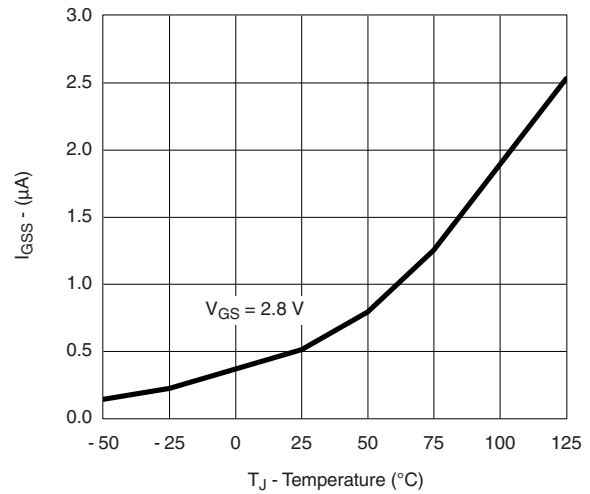
Source-Drain Diode Forward Voltage



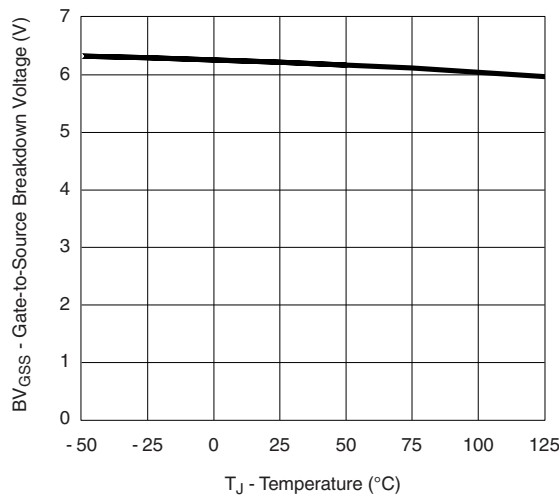
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage Variance vs. Temperature

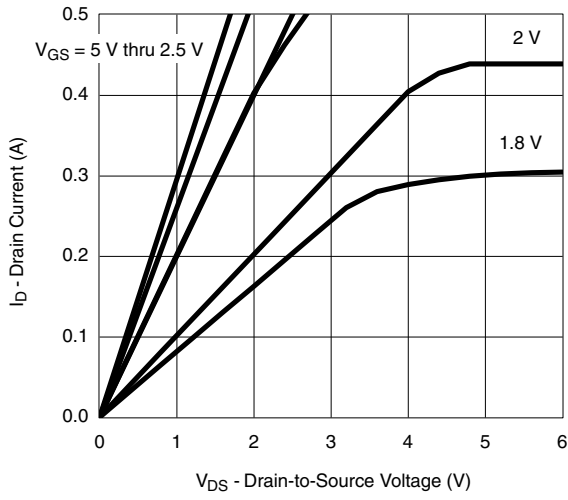


I_{GSS} vs. Temperature

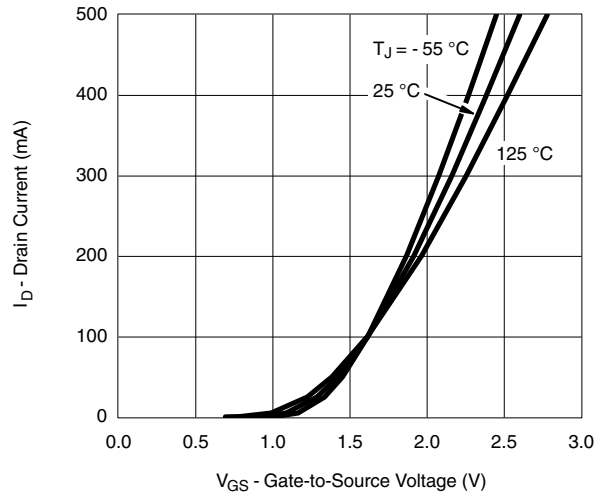


BV_{GSS} vs. Temperature

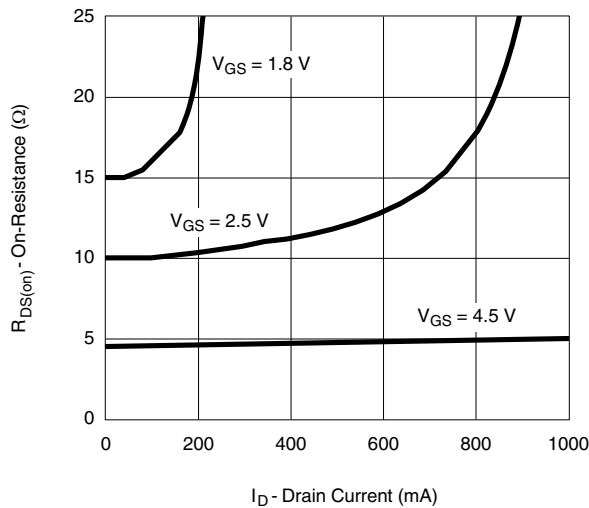
P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



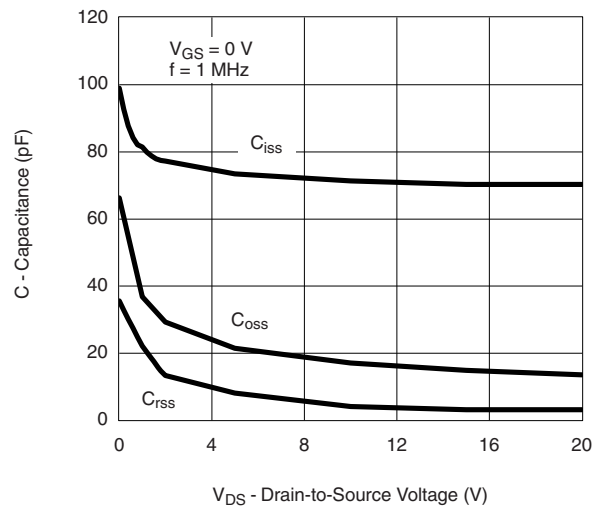
Output Characteristics



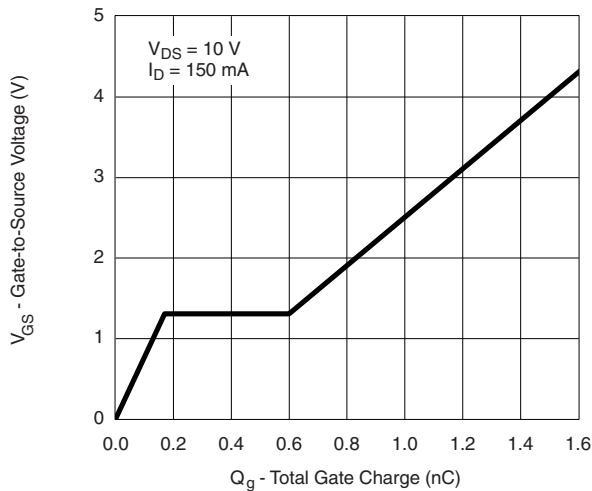
Transfer Characteristics



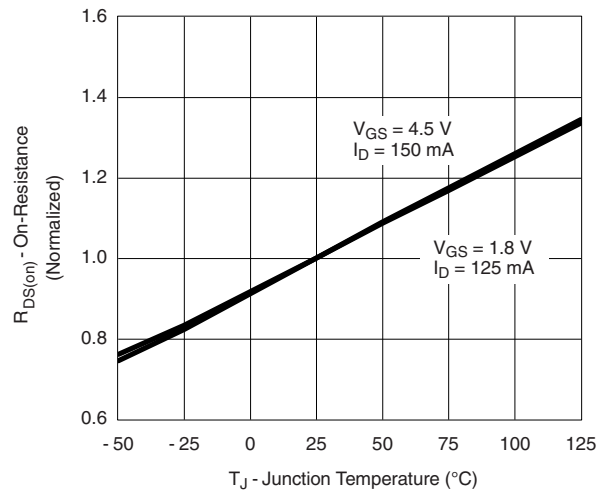
On-Resistance vs. Drain Current



Capacitance

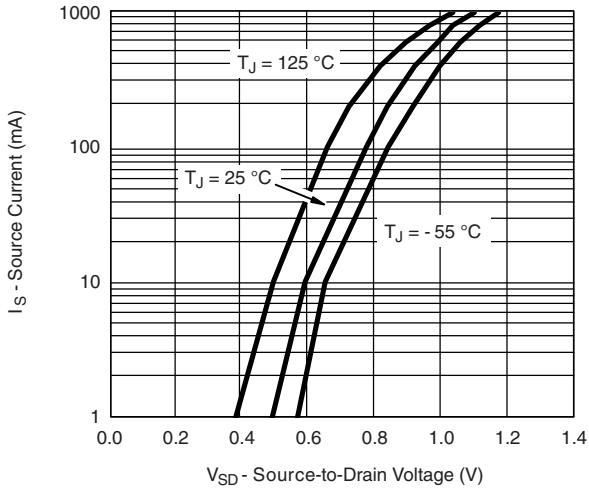


Gate Charge

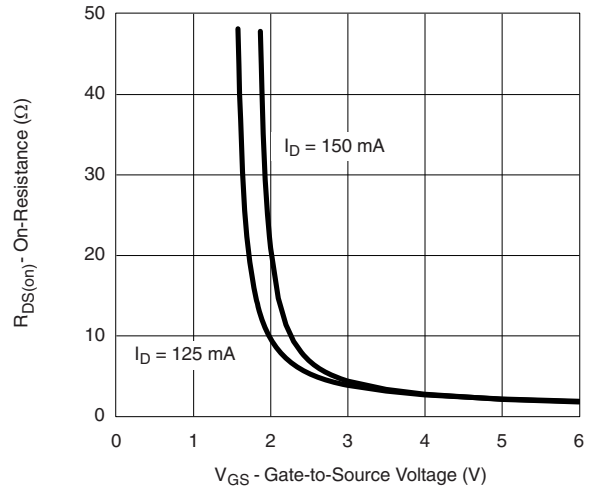


On-Resistance vs. Junction Temperature

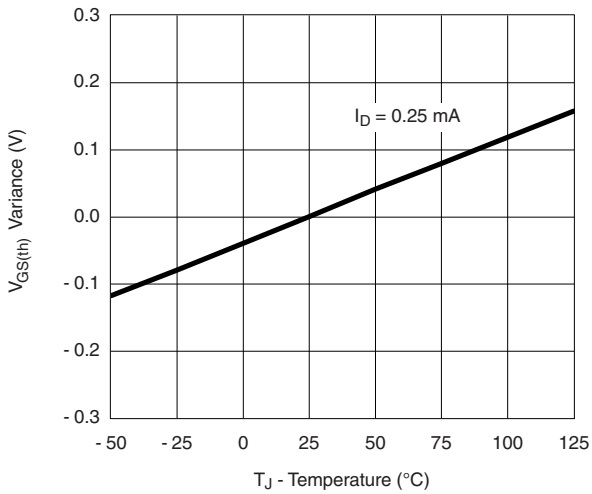
P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



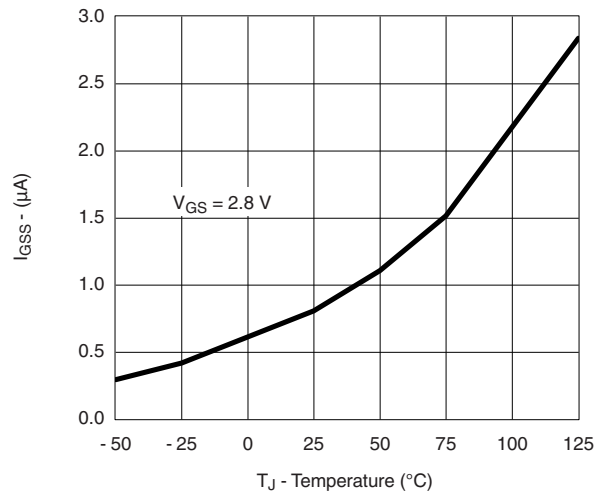
Source-Drain Diode Forward Voltage



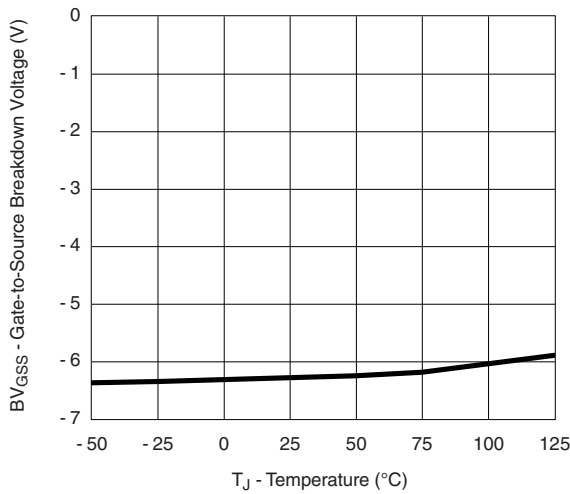
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage Variance vs. Temperature

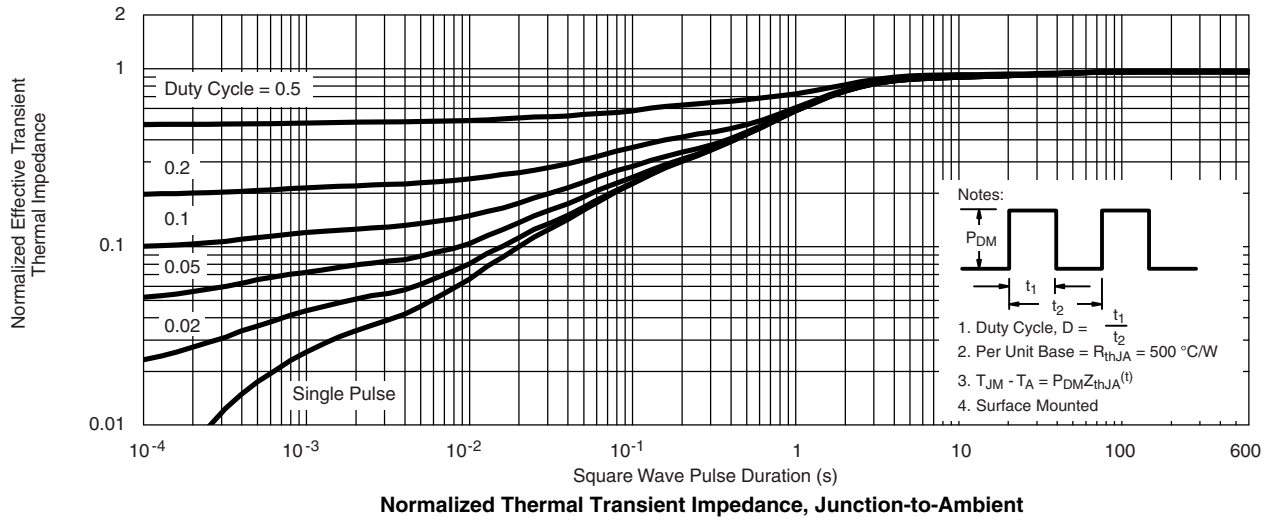


I_{GSS} vs. Temperature



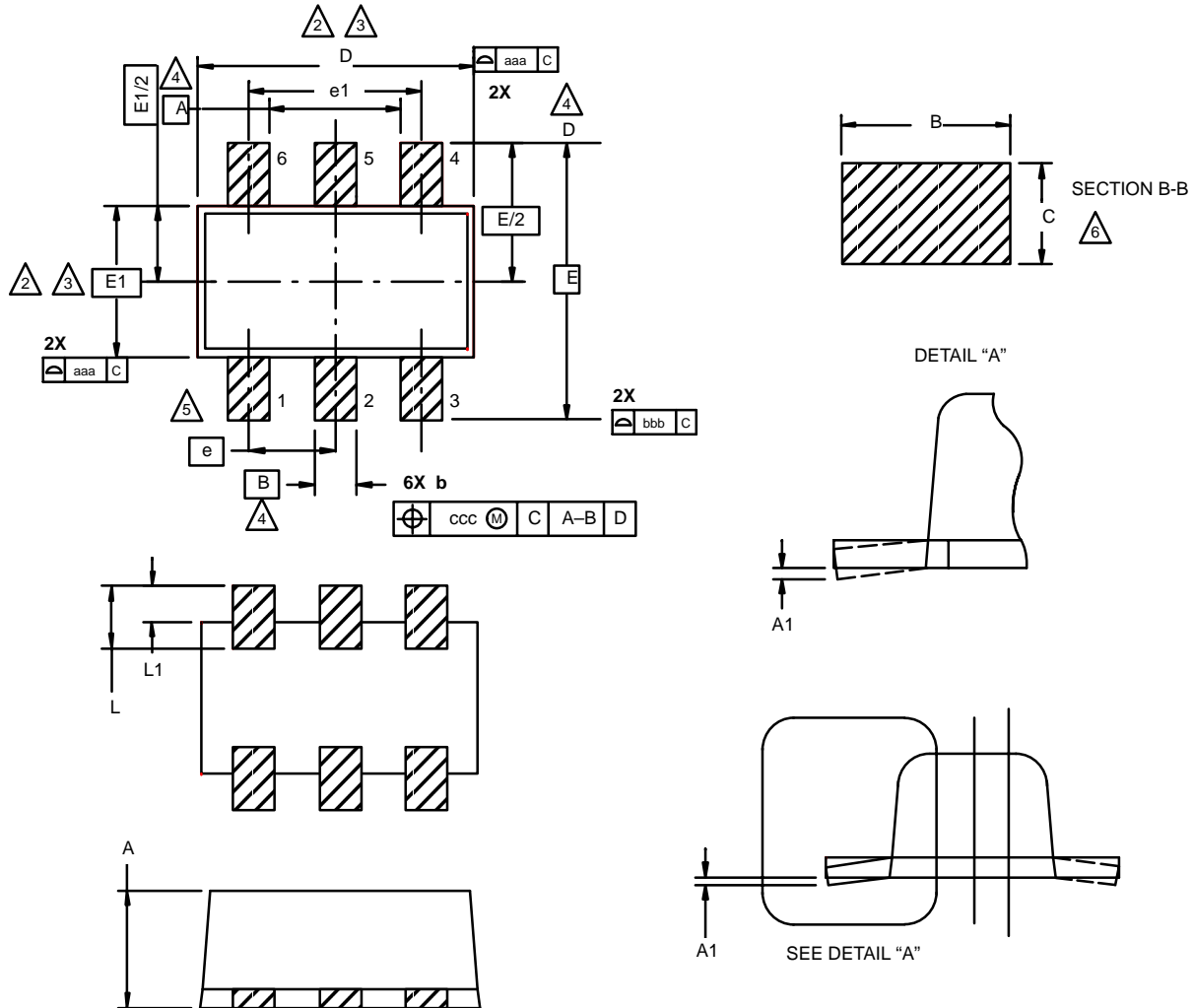
BV_{GSS} vs. Temperature

N- OR P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



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SC89: 6- LEADS (SOT-563F)



NOTES:

1. Dimensions in millimeters.

2 Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.

3 Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.

4 Datums A, B and D to be determined 0.10 mm from the lead tip.

5 Terminal numbers are shown for reference only.

6 These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

Dim	MILLIMETERS		Note	Symbol	Tolerances Of Form And Position
	Min	Max			
A	0.56	0.60		aaa	0.10
A1	0.00	0.10		bbb	0.10
b	0.15	0.30		ccc	0.10
c	0.10	0.18			
D	1.50	1.70	2, 3		
E	1.55	1.70			
E1	1.20 BSC		2, 3		
e	0.50 BSC				
e1	1.00 BSC				
L	0.35 BSC				
L1	0.20 BSC				

ECN: E-00499—Rev. B, 02-Jul-01
DWG: 5880

RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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