5-Port 10/100/1000 Smart Ethernet Switch

Features

- Stand Alone Switch On A Chip
- 5 Ethernet 10/100/1000 ports
- I Ethernet 10/100 port
- MII/GMII interface for 5 ports
- I extra MII interface for 6th port
- Four Classes of Service (CoS) selectable for each port and/or checked via IP Header and 802.1Q VLAN Tag
- Five port-based VLANs
- Maximum throughput, non head-of-line blocking architecture
- Embedded SSRAM packet buffer/address table
- 8K MAC address table
- Each port is configurable to 10 full/half duplex, 100 full/half duplex and 1000 full duplex mode
- Flow-control ability is able to set for both full and half duplex mode
- Broadcast throttling
- Port Mirroring
- Serial EEPROM Interface, EEPROM is optional
- MDIO master for PHY configuration / polling
- 0.18 micron technology
- 2V and 3.3V dual voltage power supply
- Packaged in PBGA 292
- 25MHz crystal input only

General Description

TC9205M is a fully integrated 5 Port 10/100/1000 smart Ethernet switch controller designed for low cost and high performance solutions. The chip embeds necessary SSRAM for packet buffering and MAC address table. It provides MII / GMII / interface for all ports.

A store-and-forward switching method using a non-blocking architecture is implemented within TC9205M to improve the availability and bandwidth. The chip embeds packet buffer, which it supports normal and priority queues for each transmission port.

TC9205M provides evolved CoS with four levels of priority. The priority can be checked via layer 2 (802.1Q VLAN Tagging) and/or layer 3 (IP Header TOS bits) packets. Port based priority is also provided to ensure transmission with precedence for all packets incoming from selected port(s). This feature allows improved support for multimedia applications.

The chip embeds IEEE 802.3 MAC functions for each port and these functions support full and half duplex modes for both 10 and 100 Mbits/s data rates and full duplex for 1000 Mbit/s. Each port includes dedicated receive and transmit FIFOs with necessary logic to implement flow control for both full and half duplex modes. TC9205M uses IEEE 802.3x frame based flow control for full duplex and backpressure for half duplex.

TC9205M handles an 8K address-lookup table with searching, self-learning, and automatic aging, at very high speed and excellent address space coverage. Forwarding rules are implemented according to IEEE 802.1D specifications. Filtering capabilities for bad packets and packets with Reserved Group Address DA are also provided.

The pin configuration interface comprises 40 configurations, which are shared with GMII output pins by latching the configuration data during reset. An external EEPROM device can also be used to configure the TC9205M at power-up. With reference to pin configuration interface, the EEPROM extends the chip's configuration capability with new features and enables a jumper-less configuration mode using a parallel interface for reprogramming. A virtual internal EEPROM mode is also provided to enable the use of the programming interface in the absence of external EEPROM. TC9205M can make effective use by most of its features using only the pin configuration interface.

TC9205M includes a physical layer configuration / polling entity, which it is use to configure the phy functions and to monitor the physical layer transceiver's speed, duplex mode, link status and full duplex flow control ability for each port. The chip provides four modes for phy configurations, which these modes include auto-negotiation disable procedure for 10/100 speed modes. The phy configuration information is stored in EEPROM setting.

The chip requires a 25 MHz system clock, dual 2V and 3.3V power supply and is packaged in PBGA 292.

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Block Diagram

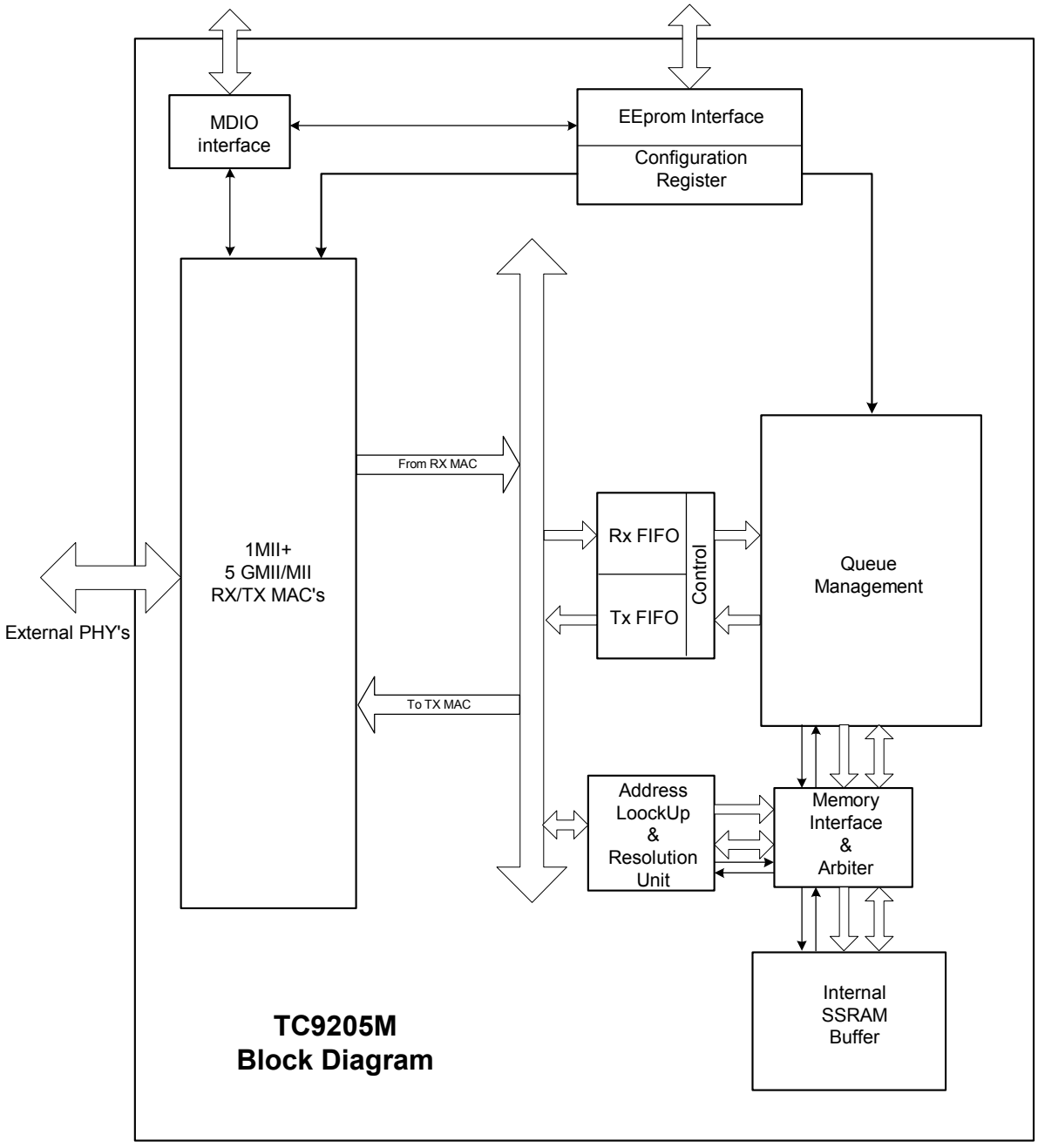


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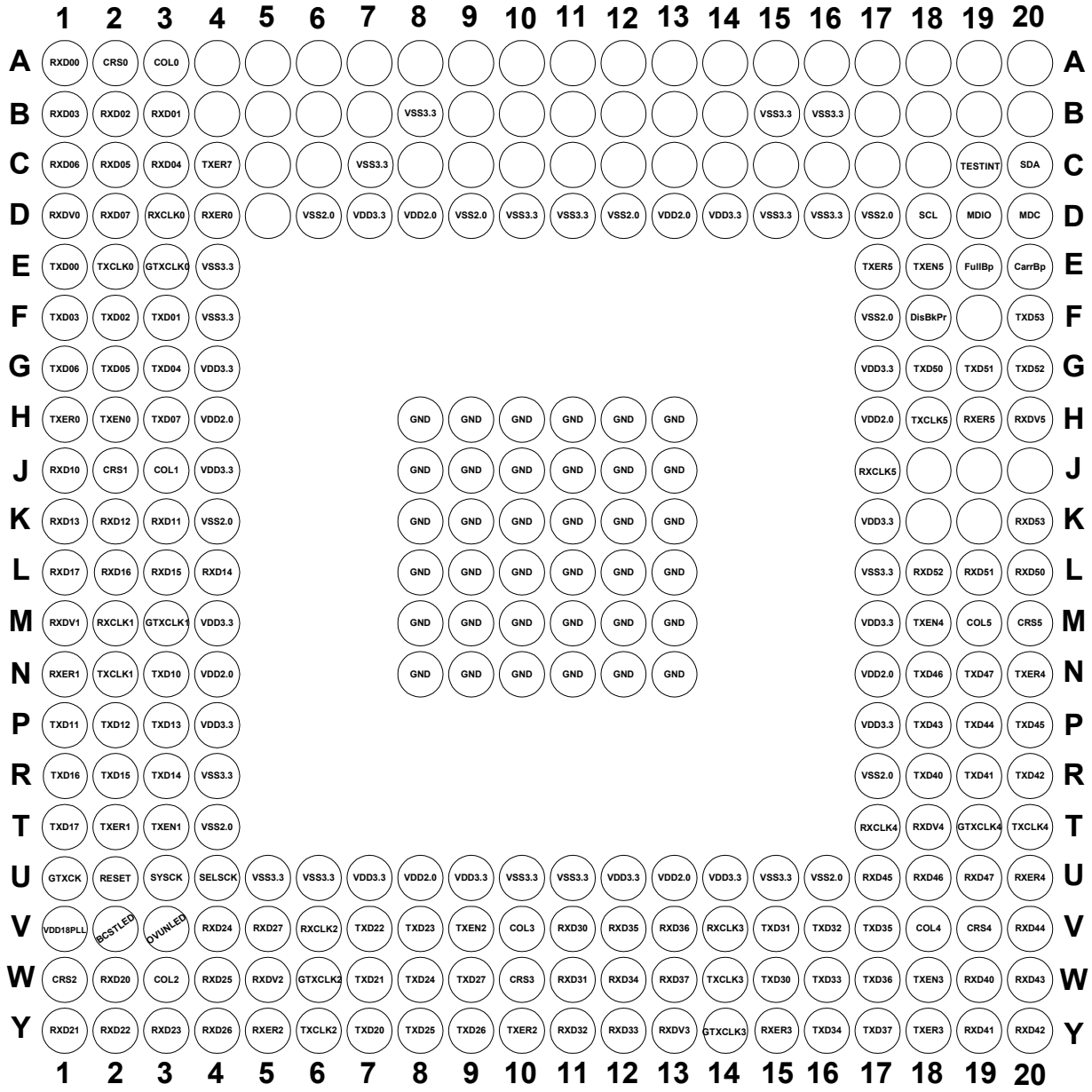
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Revision History

Revision #	Change Description
TC9205-DS-R02	
TC9205-DS-R03	1. Modify “Pin Latched” field in Class of Service section. 2. Correct the register map of “Broadcast Configuration Register” 3. Correct the junction temperature limit.

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Pins Placement



Top View

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1 Pin Listing (PBGA 292)

I ⇒ digital input
I_s ⇒ schmitt trigger digital input
I_{pd} ⇒ digital input with internal pull down
I/O ⇒ digital bi-directional
I/O_{pd} ⇒ digital bi-directional with internal pull down
I/O_{pu} ⇒ digital bi-directional with internal pull up
O ⇒ digital output
P ⇒ power
G ⇒ ground

No.	Pin label	Type	Description
G4	Vdd 3.3	P	Digital +3.3V power supply for I/O
E4	Vss 3.3	G	Digital ground for I/O
J4	Vdd 3.3	P	Digital +3.3V power supply for I/O
F4	Vss 3.3	G	Digital ground for I/O
B15	Vss 3.3	P	
H4	Vdd 2.0	P	Digital +2.0V power supply for core
B16	Vss 3.3	P	
K4	Vss 2.0	G	Digital ground for core
M4	Vdd 3.3	P	Digital +3.3V power supply for I/O
R4	Vss 3.3	G	Digital ground for I/O
N4	Vdd 2.0	P	Digital +2.0V power supply for core
T4	Vss 2.0	G	Digital ground for core
P4	Vdd 3.3	P	Digital +3.3V power supply for I/O
C7	Vss 3.3	P	
U5	Vss 3.3	G	Digital ground for I/O
B8	Vss 3.3	P	
U7	Vdd 3.3	P	Digital +3.3V power supply for I/O
U6	Vss 3.3	G	Digital ground for I/O
U9	Vdd 3.3	P	Digital +3.3V power supply for I/O
H3	TxData0_7	O	GMII transmit data - bits 7
G1	TxData0_6	O	GMII transmit data - bits 6
G2	TxData0_5	O	GMII transmit data - bits 5
U10	Vss 3.3	G	Digital ground for I/O
G3	TxData0_4	O	GMII transmit data - bits 4
F1	TxData0_3	O	GMII/MII transmit data - bits 3
F2	TxData0_2	O	GMII/MII transmit data - bits 2
U12	Vdd 3.3	P	Digital +3.3V power supply for I/O
F3	TxData0_1	I/O_{pd}	GMII/MII transmit data - bit 1
	PriClass0_1		Priority class - most significant bit.
E1	TxData0_0	I/O_{pu}	GMII/MII transmit data - least significant bit
	PriClass0_0		Priority class - least significant bit. Sets priority level per port basis. PriClass[0] - '00' - port 0 has low priority PriClass[0] - '01' - port 0 has normal priority PriClass[0] - '10' - port 0 has high priority PriClass[0] - '11' - port 0 has very high priority PriClass[0] is latched on reset
H2	TxEn0	O	GMII/MII transmit enable

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Pin Listing (continued)

No.	Pin label	Type	Description
E3	GTxClk0	O	GMII transmit clock
U11	Vss 3.3	G	Digital ground for I/O
H1	TxEr0	I/O_{pd}	Transmit Error
E2	TxClk0	I	MII transmit clock
A2	Crs0	I_s	MII carrier sense indication
A3	Col0	I_s	MII collision indication
D4	RxEr0	I_s	Receive Error
U8	Vdd 2.0	P	Digital +2.0V power supply for core
D3	RxClk0	I	MII receive clock
D1	RxDv0	I_s	GMII/MII data valid
A1	RxData0_0	I_s	GMII receive data - least significant nibble. MII receive data
B3	RxData0_1	I_s	GMII receive data - least significant nibble. MII receive data
B2	RxData0_2	I_s	GMII receive data - least significant nibble. MII receive data
U16	Vss 2.0	G	Digital ground for core
B1	RxData0_3	I_s	GMII receive data - least significant nibble. MII receive data
C3	RxData0_4	I_s	GMII receive data - most significant nibble
C2	RxData0_5	I_s	GMII receive data - most significant nibble
C1	RxData0_6	I_s	GMII receive data - most significant nibble
D2	RxData0_7	I_s	GMII receive data - most significant nibble
U14	Vdd 3.3	P	Digital +3.3V power supply for I/O
U15	Vss 3.3	G	Digital ground for I/O
T1	TxData1_7	O	GMII transmit data - bits 7
R1	TxData1_6	O	GMII transmit data - bits 6
R2	TxData1_5	O	GMII transmit data - bits 5
U13	Vdd 2.0	P	Digital +2.0V power supply for core
R3	TxData1_4	O	GMII transmit data - bits 4
P3	TxData1_3	O	GMII/MII transmit data - bits 3
P2	TxData1_2	O	GMII/MII transmit data - bits 2
R17	Vss 2.0	G	Digital ground for core
P1	TxData1_1	I/O_{pd}	GMII/MII transmit data - bit 1
	Priclass1_1		Priority class - most significant bit. PriClass[1] is latched on reset
N3	TxData1_0	I/O_{pu}	GMII/MII transmit data - least significant bit
	PriClass1_0		Priority class - least significant bit. Sets priority level per port basis. PriClass[1] - '00' - port 1 low priority PriClass[1] - '01' - port 1 has normal priority PriClass[1] - '10' - port 1 has high priority PriClass[1] - '11' - port 1 has very high priority PriClass[1] is latched on reset
T3	TxEn1	O	GMII/MII transmit enable
M3	GTxClk1	O	GMII transmit clock

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Pin Listing (continued)

No.	Pin label	Type	Description
P17	Vdd 3.3	P	Digital +3.3V power supply for I/O
T2	TxEr1	I/O_{pd}	Transmit Error
N2	TxClk1	I	MII transmit clock
J2	Crs1	I_s	MII carrier sense indication
J3	Col1	I_s	MII collision indication
N1	RxEr1	I_s	Receive Error
L17	Vss 3.3	G	Digital ground for I/O
M2	RxClk1	I	MII receive clock
M1	RxDv1	I_s	GMII/MII data valid
J1	RxData1_0	I_s	GMII receive data - least significant nibble. MII receive data
K3	RxData1_1	I_s	GMII receive data - least significant nibble. MII receive data
K2	RxData1_2	I_s	GMII receive data - least significant nibble. MII receive data
M17	Vdd 3.3	P	Digital +3.3V power supply for I/O
K1	RxData1_3	I_s	GMII receive data - least significant nibble. MII receive data
L4	RxData1_4	I_s	GMII receive data - most significant nibble
L3	RxData1_5	I_s	GMII receive data - most significant nibble
L2	RxData1_6	I_s	GMII receive data - most significant nibble
L1	RxData1_7	I_s	GMII receive data - most significant nibble
U4	selsck	I_s	Selects the source for the system clock. selsck - '1' - sysck is driven by a 25MHz external clock.
U1	gtxck	I	The 125Mhz reference clock for 1000Mbps operating mode. This clock is used as a reference clock for the GMII transmission clock for every port.
V1	Vdd 2.0	P	Digital +2.0V power supply for core
V2	BcstLED	I/O_{pd}	The led can signal filtering of broadcast frames Also the led remains lit if the POST test fails, which indicates a faulty chip.
V3	OvUnLED	O	The led is lit whenever a unicast packets overflow condition is reached and some frames are dropped by the buffer management engine.
D9	Vss 2.0	G	Digital ground for core
U3	sysck	I	The 25MHz system clock.
U2	reset	I_{pus}	General reset.
W9	TxData2_7	I/O_{pd}	GMII transmit data - most significant bit
Y9	TxData2_6	I/O_{pd}	GMII transmit data - bit 6
Y8	TxData2_5	I/O_{pd}	GMII transmit data - bit 5
W8	TxData2_4	I/O_{pd}	GMII transmit data - bit 4
V8	TxData2_3	I/O_{pd}	GMII/MII transmit data - bit 3
	PriBndw1		Priority bandwidth configuration pins. PriBndw(1)is latched on reset
N17	Vdd 2.0	P	Digital +2.0V power supply for core

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Pin Listing (continued)

No.	Pin label	Type	Description
V7	TxData2_2	I/O_{pu}	GMII/MII transmit data - bit 2
	PriBndw0		Priority bandwidth configuration pins. These configuration pins allow the bandwidth percentage assigned to a priority packet queue to be modified to certain hardwired levels. PriBndw chooses between 4 hardwired spreading percentage schemes among the 4 priority queues of each port. PriBndw(0)is latched on reset
W7	TxData2_1	I/O_{pd}	GMII/MII transmit data - bit 1 PriClass[2] is latched on reset
	PriClass2_1		Priority class - most significant bit.
Y7	TxData2_0	I/O_{pu}	GMII/MII transmit data - least significant bit
	PriClass0_0		Priority class - least significant bit. Sets priority level per port basis. PriClass[2] - '00' - port 2 low priority PriClass[2] - '01' - port 2 has normal priority PriClass[2] - '10' - port 2 has high priority PriClass[2] - '11' - port 2 has very high priority PriClass[2] is latched on reset
V9	TxEn2	O	GMII/MII transmit enable
W6	GTxClk2	O	GMII transmit clock
F17	Vss 2.0	G	Digital ground for core
Y10	TxEr2	I/O_{pd}	Transmit Error
Y6	TxClk2	I	MII transmit clock
W1	Crs2	I_s	MII carrier sense indication
W3	Col2	I_s	MII collision indication
Y5	RxEr2	I_s	Receive Error
K17	Vdd 3.3	P	Digital +3.3V power supply for I/O
V6	RxClk2	I	MII receive clock
W5	RxDv2	I_s	GMII/MII data valid
W2	RxData2_0	I_s	GMII receive data - least significant nibble. MII receive data
Y1	RxData2_1	I_s	GMII receive data - least significant nibble. MII receive data
Y2	RxData2_2	I_s	GMII receive data - least significant nibble. MII receive data
D16	Vss 3.3	G	Digital ground for I/O
Y3	RxData2_3	I_s	GMII receive data - least significant nibble. MII receive data
V4	RxData2_4	I_s	GMII receive data - most significant nibble
W4	RxData2_5	I_s	GMII receive data - most significant nibble
Y4	RxData2_6	I_s	GMII receive data - most significant nibble
V5	RxData2_7	I_s	GMII receive data - most significant nibble

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Pin Listing (continued)

No.	Pin label	Type	Description
Y17	TxData3_7	I/O_{pd}	GMII transmit data - bit 7
	EnIPPr		Enables IP prioritization. CoS resolution will consider TOS Precedence bits from IP Header. '1' – IP priority will be taken into consideration '0' – IP priority will be neglected EnIPPr is latched on reset
W17	TxData3_6	I/O_{pd}	GMII transmit data - bit 6
	IPTosMap1		IP type of service mapping - the most significant bit IPTosMap(1) is latched on reset
V17	TxData3_5	I/O_{pu}	GMII transmit data - bit 5
	IPTosMap0		IP type of service mapping - the least significant bit. This configuration chooses between 4 hard-wired mapping schemes for the associations of IP priority within the received packet and one of the 4 priority levels set by PriClass. In case the receiving port already has a priority level assigned by PriClass configuration, or the VLAN prioritization is also active, a resolution function is used for the final priority class. IPTosMap(0) is latched on reset.
Y16	TxData3_4	I/O_{pu}	GMII/MII transmit data - bit 4
	EnVLANPr		Enables VLAN prioritization. CoS resolution will consider user priority bits (TCI field) from 802.1Q VLAN Tag Header. '1' – VLAN priority will be taken into consideration '0' – VLAN priority will be neglected EnVLANPr is latched on reset
W16	TxData3_3	I/O_{pd}	GMII/MII transmit data - bit 3
	VLANPrMap1		VLAN priority mapping VLANPrMap(1)is latched on reset.
G17	Vdd 3.3	P	Digital +3.3V power supply for I/O
V16	TxData3_2	I/O_{pu}	GMII/MII transmit data - bit 2
	VLANPrMap0		VLAN priority mapping This configuration chooses between 4 hard-wired mapping schemes for the associations of VLAN priority within the received packet and one of the 4 priority levels set by PriClass. In case the receiving port already has a priority level assigned by PriClass configuration, or the IP prioritization is also active, a resolution function is used for the final priority class. VLANPrMap(0)is latched on reset.
V15	TxData3_1	I/O_{pd}	GMII/MII transmit data - bit 1
	PriClass3_1		Priority class - most significant bit. PriClass[3] is latched on reset
W15	TxData3_0	I/O_{pu}	GMII/MII transmit data - least significant bit
	PriClass3_0		Priority class - least significant bit. Sets priority level per port basis. PriClass[3] - '00' - port 3 low priority PriClass[3] - '01' - port 3 has normal priority PriClass[3] - '10' - port 3 has high priority PriClass[3] - '11' - port 3 has very high priority PriClass[3] is latched on reset

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Pin Listing (continued)

No.	Pin label	Type	Description
W18	TxEn3	O	GMII/MII transmit enable
Y14	GTxClk3	O	GMII transmit clock
D15	Vss 3.3	G	Digital ground for I/O
Y18	TxEr3	I/O_{pd}	Transmit Error
W14	TxClk3	I	MII transmit clock
W10	Crs3	I_s	MII carrier sense indication
V10	Col3	I_s	MII collision indication
Y15	RxEr3	I_s	Receive Error
H17	Vdd 2.0	P	Digital +2.0V power supply for core
V14	RxClk3	I	MII receive clock
Y13	RxDv3	I_s	GMII/MII data valid
V11	RxData3_0	I_s	GMII receive data - least significant nibble. MII receive data
W11	RxData3_1	I_s	GMII receive data - least significant nibble. MII receive data
Y11	RxData3_2	I_s	GMII receive data - least significant nibble. MII receive data
Y12	RxData3_3	I_s	GMII receive data - least significant nibble. MII receive data
W12	RxData3_4	I_s	GMII receive data - most significant nibble
V12	RxData3_5	I_s	GMII receive data - most significant nibble
V13	RxData3_6	I_s	GMII receive data - most significant nibble
W13	RxData3_7	I_s	GMII receive data - most significant nibble
N19	TxData4_7	I/O_{pd}	GMII transmit data - bit 7
	BcstThrot		Enables broadcast throttling. '1' – Enable '0' – Disable BcstThrot is latched on reset.
N18	TxData4_6	I/O_{pd}	GMII transmit data - bit 6
	OBMTest		Sets the switch into a special test mode. This test mode require crossover loopbacks cables to be placed on the pair ports: 1 & 2,2 & 3, 3 & 4, 4 & 5,5 & 6 while ports 0 and 7 will be accessible to the test machine. '1' – enabled '0' – disabled OBMTest is latched on reset.
P20	TxData4_5	I/O_{pd}	GMII transmit data - bit 5
	FcBcstMode		Changes the way flow control threshold is handled while in broadcast situations. '1' – only the flow control threshold on the broadcast queue is considered '0' – flow control thresholds associated to each source port originating the broadcast frames are considered FCBcstMode is latched on reset.

Pin Listing (continued)

No.	Pin label	Type	Description
P19	TxData4_4	I/O_{pd}	GMII transmit data - bit 4
	FcBcstEn		Enables/disables flow control for broadcast packets. '1' – enabled '0' – disabled FcBcstEn is latched on reset.
P18	TxData4_3	I/O_{pd}	GMII/MII transmit data - bit 3
D17	Vss 2.0	G	Digital ground for core
R20	TxData4_2	I/O_{pd}	GMII/MII transmit data - bit 2
R19	TxData4_1	I/O_{pd}	GMII/MII transmit data - bit 1
	PriClass4_1		Priority class - most significant bit. PriClass[4] is latched on reset.
R18	TxData4_0	I/O_{pu}	GMII/MII transmit data - least significant bit
	PriClass4_0		Priority class - least significant bit. Sets priority level per port basis. PriClass[4] - '00' - port 4 low priority PriClass[4] - '01' - port 4 has normal priority PriClass[4] - '10' - port 4 has high priority PriClass[4] - '11' - port 4 has very high priority PriClass[4] is latched on reset
M18	TxEn4	I/O_{pd}	GMII/MII transmit enable
	RejRDA		If this pin is set to '1' then all frames with 802.1D Reserved Group Address or 802.3x Full Duplex PAUSE operation DA will be filtered out. This setting is provided for testing purposes only and it is recommended to set high in normal operation. RejRDA is latched on reset.
T19	GTxClk4	O	GMII transmit clock
D7	Vdd 3.3	P	Digital +3.3V power supply for I/O
N20	TxEr4	I/O_{pd}	Transmit Error
T20	TxClk4	I	MII transmit clock
V19	Crs4	I_s	MII carrier sense indication
V18	Col4	I_s	MII collision indication
U20	RxEr4	I_s	Receive Error
D11	Vss 3.3	G	Digital ground for I/O
T17	RxClk4	I	MII receive clock
T18	RxDv4	I_s	GMII/MII data valid
W19	RxData4_0	I_s	GMII receive data - least significant nibble. MII receive data
Y19	RxData4_1	I_s	GMII receive data - least significant nibble. MII receive data
Y20	RxData4_2	I_s	GMII receive data - least significant nibble. MII receive data
W20	RxData4_3	I_s	GMII receive data - least significant nibble. MII receive data
V20	RxData4_4	I_s	GMII receive data - most significant nibble
U17	RxData4_5	I_s	GMII receive data - most significant nibble

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Pin Listing (continued)

No.	Pin label	Type	Description
U18	RxData4_6	I_s	GMII receive data - most significant nibble
U19	RxData4_7	I_s	GMII receive data - most significant nibble
D14	Vdd 3.3	P	Digital +3.3V power supply for I/O
E19	FullBp	I_{pd}	In normal operation the backpressure process is executed until flow control condition disappears or until the time limit for backpressure is reached. This limit is based on EEPROM's **BPTimeValue** register. When this configuration is '0' the backpressure process will be also limited from exceeding 28 consecutive collisions. The default value (28) can be changed by EEPROM settings. FullBp is latched on reset
E20	CarrBp	I_{pu}	Enable / disable carrier based backpressure for half -duplex mode. '1' – Carrier based backpressure '0' – Collision based backpressure. CarrBp is latched on reset
F18	DisBkPr	I_{pd}	Setting this pin to '1' will disable backpressure procedure for all half duplex ports. DisBkPr is latched on reset.
E17	TxEr5	I/O_{pd}	Transmit Error
F20	TxData5_3	I/O_{pd}	MII transmit data - bit 3
	FrcFdFc		Setting this bit to '1' will force flow control execution for 10/100Mbps, no matter the auto negotiation result. FrcFdFc is latched on reset.
D10	Vss 3.3	G	Digital ground for I/O
G20	TxData5_2	I/O_{pd}	MII transmit data - bit 2
	DisFdFc		Setting this bit to '1' will disable flow-control for full-duplex mode (transmission of pause frames). DisFdFc is latched on reset.
G19	TxData5_1	$I/_{pd}$	MII transmit data - bit 1
G18	TxData5_0	$I/_{pd}$	MII transmit data - least significant bit
E18	TxEn5	I/O_{pd}	MII transmit enable
	DisBPBk		Enable / disable backoff during backpressure. '1' – No backoff executed. Another collision will be forced again after one minimum IFG time following previous collision if carrier sense is observed. '0' – The MAC randomly chooses between 0 and 1 slot times of backoff. DisBkBp is latched on reset.
H19	RxEr5	I_s	Receive Error
D13	Vdd 2.0	P	Digital +2.0V power supply for core
H18	Txclk5	I	MII transmit clock
D12	Vss 2.0	G	Digital ground for core
J17	RxClk5	I	MII receive clock
H20	RxDv5	I_s	MII/MII data valid
M20	Crs5	I_s	MII carrier sense indication
M19	Col5	I_s	MII collision indication
L20	RxData5_0	I_s	MII receive data - least significant nibble. MII receive data

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Pin Listing (continued)

No.	Pin label	Type	Description
L19	RxData5_1	I_s	MII receive data - least significant nibble. MII receive data
L18	RxData5_2	I_s	MII receive data - least significant nibble. MII receive data
K20	RxData5_3	I_s	Receive data - least significant nibble. MII receive data
D8	Vdd 2.0	P	Digital +2.0V power supply for core
D20	MDC	O	MDIO Clock.
D19	MDIO	I/O_{pu}	MDIO Data.
D6	Vss 2.0	G	Digital ground for core
D18	SCL	I/O_{pu}	EEPROM's serial clock.
C20	SDA	I/O_{pu}	EEPROM's serial data.
C19	TestInt	I_{pd}	TestInt - '0' - switch normal mode(default) TestInt -'1' - internal memory test mode.

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2 Ethernet Media Access Controller

The TC9205M's Ethernet Media Access Controller (MAC) contains IEEE 802.3 MAC functions for 5 ports. It is able to operate in 10/100/1000 full duplex and 10/100 half duplex modes for all ports. Each port has its dedicated receive and transmit FIFO with necessary logic to implement flow control for both duplex modes. The MAC functions are specially designed for high speed and flexible interfacing.

2.1 Receive MAC

When a frame is received from the Ethernet media through the MII interface, it is stored first in a dedicated receive FIFO. This FIFO acts as a temporary buffer between the Receive MAC section and switch core interface.

The Receive MAC layer extracts the valid ethernet information by stripping off the preamble sequence and SFD of the received frame, which the frame was acquired from the PHY layer via either GMII or MII interface. The Receive MAC then sends packets with valid information to the receive FIFO.

TC9205M determines the validity of each received packet by checking the CRC and packet length. The bad packets will be dropped either by the MAC or by the queue manager. Oversized packets are truncated to 1536 bytes and marked as erroneous packets. Undersized packets are removed from the receive FIFO without being reported to the switch interface. Therefore the FIFO space held by undersized packets will be removed automatically.

In Full Duplex mode the Receive MAC can identify any received frame as a flow control frame having a valid CRC. It will load its internal pause counter with the 'pause quanta' value extracted from the incoming frame. The flow control frame will be rejected after the pausing period has been acquired. After the pausing period has obtained from the flow control frame, the flow control mechanism inside TC9205M will set a decremental timer in the pause counter according to the value of the pausing period. A non-zero value sets in the pause counter will issue the Receive MAC to XOFF (Transmit Stop) the Transmit MAC. The pause counter will decrement the 'pause quanta' value after each slot time until it reaches zero. If the pause quanta value is equal to zero the flow control mechanism will XON (Transmit Enable) the Transmit MAC.

If a frame transmission is in progress when the PAUSE frame is received, the transmission is allowed to complete for the current transmitting frame but the transmission for the next frame(s) will hold until the Receive MAC generates an XON command. The pause time will begin at the end of current transmission or start immediately if no transmission is in the medium when the PAUSE frame is received. If a pause command is received while the transmitter is already in pause, the new pause time indicated by the new Flow Control frame will be loaded into the pause register.

The MAC is also able to reject frames containing IEEE 802.1D Reserved Group Destination Addresses and frames with Mac Control Type (Type 88-08) if selected through configuration settings.

When the receive FIFO is full and additional data are still incoming from the MAC, then the overrun condition occurs and the frame is dropped. If the system clock frequency is not lower than the recommended value this condition will never occur.

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2.2 Transmit MAC

The Transmit MAC section assembles the MAC frames stored in the transmit FIFO and controls their transmission onto the media via external PHY entities. It appends the standard preamble and start of frame delimiter to the transmitted packets. The MAC also controls the interframe gap time during transmission, maintaining for default the standard minimum interframe gap of 96-bit time. This value can be changed in the EEPROM register setting.

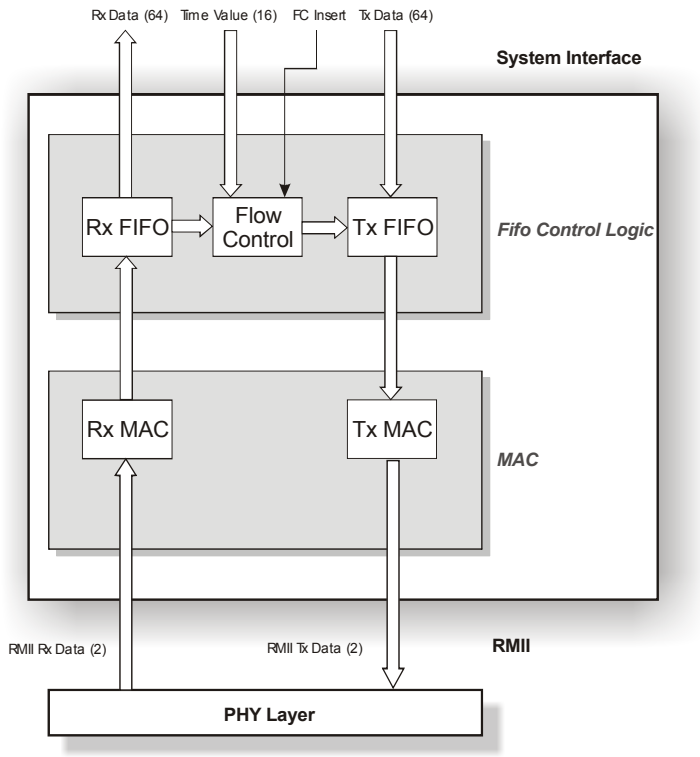
For Half Duplex mode the Transmit MAC meets CSMA/CD **IEEE 802.3** requirements. The FIFO logic manages frame retransmission for early collision conditions or discards the frame if late collision occurs. It also follows the truncated binary exponential backoff algorithm, collision and jamming procedures.

The transmit FIFO stores the packets which are ready for transmission in the main memory queues. If there is no packet ready in the transmit FIFO before the current packet completes its transmission, an underrun condition has occurred and the mechanism will generate a signal to indicate FIFO underrun event, but if the switch core transfers the rest of the packet(s) into the FIFO, the Transmit MAC will safely discard it without affecting the next packet. Underrun conditions never occur if the system is operating at the recommended clock frequency or higher.

For full duplex mode TC9205M implements the flow control algorithm according to the **IEEE 802.3x** standard, using the XON/XOFF method. Full duplex flow control can be configured automatically, by auto-negotiation result, or manually, pin configuration and/or EEPROM settings, to enable/disable the function.

The TC9205M executes backpressure algorithm for half duplex flow control supporting both collision based and carrier based backpressure. Both modes are based on carrier sense forced collisions and an aggressive backoff algorithm. The forced consecutive collisions generated for flow control purposes can be limited to a maximum of–28 collisions if this option is selected. This feature helps to avoid HUB partitioning in heavy traffic. The number of collisions can be adjusted in EEPROM settings.

MAC Block Diagram



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3 MAC Address Handling

After the frames are recovered from MAC FIFOs they are transferred to the queue management entity. Prior to this transfer the DA and SA are extracted from each frame and passed to MAC Address Lookup Table and Resolution Engine (ALR). The Lookup engine uses a proprietary hashing algorithm to access its 8K address table.

The engine will update its table with each SA, if it is found to be unknown or migrated, Then it will update the source port and aging information along with the new address. This learning process will be executed for all addresses except for multicast SA frames (bit 40 is '1'). For stored addresses, aging function is executed according to the time intervals set in the EEPROM registers. Default aging time is 600 seconds. TC9025M also provide option to disable the aging mechanism, please refer to the EEPROM Register in section 14.3.15 for more details.

Destination address is also analyzed in order to make forwarding decisions. If the destination address is a broadcast or multicast address, the frame will flood to all ports except its originated port (source port). If only some ports are allow to send those frame(s) with broadcast or multicast address(es), the destination ports will search the for the port(s) with correct address(s) in the MAC address table. If the address is found to be unknown, the frame will be also flooded to every port otherwise frame(s) will be forwarded to the legitimate port(s) only.

TC9205M will filter following frames:

- erroneous frames. This includes :
  - frames with CRC error;
  - undersized frames;
  - oversized frames;
  - frames that presents alignment error (this doesn't include frames with dribble bits).
- 802.3x pause frames. These frames will be filtered after executing appropriate flow control actions;
- frames with 802.3x full duplex flow control PAUSE operation destination address. These frames are not recognized as pause frames if the MAC type and subtype does not match the "88080001"H value;
- frames with 802.1D Reserved Group Address destination address;
- frames with MAC Control Type (8808);
- Local frames. If the port found to correspond to destination address matches the source port, then the frame is considered to be local and discarded.

4 Queue Management

TC9205M operates in a store and forward mode implementing efficient switching method that minimizes the overall latency. The queue manager uses the first in first out forwarding mode, which guarantees to maintain frame order. Congestion control is implemented within TC9205M, which will eliminate head-of-line blocking conditions.

The switch embeds a 2 Mbit SSRAM as a central frame buffer pool, which is divided into 256 byte buffers to increase memory utilization efficiency. Normal and priority transmission queues are implemented within TC9205M for each port. All available frame buffers are shared between all transmission queues and each queue can fully extend to all buffers. Still memory resource utilization is limited on receive port basis.

Evolved flow control and frame filtering mechanisms are implemented based on source, transmit and global memory load to maximize performance and minimize packet loss.

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5 Classes of Service

TC9205M implements advanced Class of Service (CoS), supporting both traffic priority and delay bound features. It provides four classes of service: class 0 (low), class 1 (normal), class 2 (high) and class 3 (very high). Each class of service has its dedicated transmission queue for each port. The frames assign with higher service class will arrive sooner at the destination.

Frames in the class 0 priority queue get the lowest transmission bandwidth percentage, while frames in the class 3 priority queue get the highest bandwidth percentage. The bandwidth percentage depends on two elements:

- CoS bandwidth Weights;
- The corresponding class of all non-empty queues for the respective port.

The CoS Weights can be set by using **PriBndw[1:0]** shared configuration pins or by setting the EEPROM Registers. While the pins provide only four predefined hardwired combinations for the transmission bandwidth percentage allocation among the queues, the EEPROM gives more flexibility over this configuration.

When EEPROM is not present, transmission bandwidth percentage distribution among the queues for the case when all the queues are loaded can be seen in the table below:

EEPROM is not present				
PriBndw[1:0]	Transmission Bandwidth Percentage			
	Class 0 Priority (lowest)	Class 1 Priority	Class 2 Priority	Class 3 Priority (highest)
00	7%	13%	27%	53%
01	3%	14%	27%	56%
10	2%	8%	30%	60%
11	3%	5%	10%	82%

The percentage refers to the port's bandwidth, which is determined by the current operating speed. Those values are the guaranteed minimum ones and the transmission bandwidth percentage cannot drop below specified value under any circumstance. If EEPROM is used, the user has more flexible adjustment of bandwidth weights to choose from the EEPROM register.

A special early packet dropping mechanism is also implemented to offer more protection against overflow conditions for priority packets. If the global memory load exceeds an overflow threshold, then all class 0 priority packets will be dropped from the source port(s) in order to save space for the higher priority packets. This will minimize the probability of packet loss in priority flows for senders that are not flow control capable.

The CoS mechanism supports multiple prioritization sources: 802.1Q VLAN Tag Header (layer 2), IP Header TOS bits (layer 3) and/or port based CoS. For IP and VLAN sources a mapping is executed between the values of the fields extracted from each frame and one of the four CoS provided by TC9205M. This mapping can be adjusted by using **IPTosMap[1:0]** and **VLANPrMap[1:0]** shared configuration pins or the EEPROM settings. While the pins provide just four predefined hard-wired mapping schemes, the EEPROM gives a custom explicit mapping.

Under some circumstances, one or more mechanisms can be active (VLAN, IP and/or port based). In this case there is a resolution function that resolves the CoS for each incoming frame. When EEPROM is not present and IP and/or VLAN prioritizations are enabled the corresponding headers are parsed. The frame will be assigned the CoS corresponding to the first header of each incoming frames parsed and found valid. When both above prioritizations are enabled the search order is determined by EEPROM

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configuration (default is IP). If no header is found or corresponding prioritizations are disabled then port based prioritization is executed. When EEPROM is present an additional method of prioritization is available. This method consists of selecting the highest service class from all classes corresponding to the enabled prioritization sources (IP, VLAN and port based). For both methods, when no prioritization source is available the default CoS is used (default is normal priority – CoS1 but it can be also changed by EEPROM configuration).

The CoS feature can be configured by adjusting shared configuration pins and/or programming EEPROM Register settings. VLAN prioritization can be enabled by **EnVLPr** shared configuration pin or by EEPROM register settings,, while **EnIPPr** shared configuration pin or the EEPROM can enable IP prioritization. The shared configuration pins are sampled during reset.

The per port basis CoS can be set using **PriClass[x][1:0]** shared configuration pins or configuring EEPROM registers, where **x** stands for port number. The port based prioritization can be disabled from EEPROM settings only.

<table>
<tr><th>Configuration</th><th>Pins Latched</th><th>Description</th></tr>
<tr><td>PriClass[x][1:0]</td><td>TxDataX_[1:0]</td><td>Set the priority class per port basis
'00' – the port has class 0 priority(lowest priority)
'01' – the port has class 1 priority
'10' – the port has class 2 priority
'11' – the port has class 3 priority(highest priority)</td></tr>
<tr><td>EnIPPr</td><td>TxData3_7</td><td>Enable/disable IP prioritization
‘0’ – IP priority within the received packet (if exists) is ignored
‘1’ – IP priority within the received packet (if exists) is considered</td></tr>
<tr><td>EnVLPr</td><td>TxData3_4</td><td>Enable/disable VLAN prioritization
‘0’ – VLAN priority within the received packet (if exists) is ignored
‘1’ – VLAN priority within the received packet (if exists) is considered</td></tr>
<tr><td>IPTosMap[1:0]</td><td>TxData3_[6:5]</td><td>Selects one of four mappings for the 8 level precedence extracted from frame’s IP header to the 4 CoS offered by TC9205M
(C0, C1, C2, C3 – class 0, 1, 2, 3 of service)
<table>
<tr><th></th><th colspan="8">Designated priority class</th></tr>
<tr><th>IPTosMap[1:0]</th><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th></tr>
<tr><td>00</td><td>C0</td><td>C0</td><td>C1</td><td>C1</td><td>C2</td><td>C2</td><td>C3</td><td>C3</td></tr>
<tr><td>01</td><td>C1</td><td>C2</td><td>C2</td><td>C2</td><td>C3</td><td>C3</td><td>C3</td><td>C3</td></tr>
<tr><td>10</td><td>C1</td><td>C1</td><td>C2</td><td>C2</td><td>C2</td><td>C3</td><td>C3</td><td>C3</td></tr>
<tr><td>11</td><td>C0</td><td>C1</td><td>C1</td><td>C2</td><td>C2</td><td>C3</td><td>C3</td><td>C3</td></tr>
</table></td></tr>
<tr><td>VLANPrMap[1:0]</td><td>TxData3_[3:2]</td><td>Selects one of four mappings for the 8 level user_priority extracted from the frame’s VLAN Tag to the 4 level priority offered by TC9205M
(C0, C1, C2, C3 – class 0, 1, 2, 3 of service)
<table>
<tr><th></th><th colspan="8">Designated priority class</th></tr>
<tr><th>VLANPrMap[1:0]</th><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th></tr>
<tr><td>00</td><td>C0</td><td>C0</td><td>C1</td><td>C1</td><td>C2</td><td>C2</td><td>C3</td><td>C3</td></tr>
<tr><td>01</td><td>C1</td><td>C0</td><td>C0</td><td>C1</td><td>C2</td><td>C2</td><td>C3</td><td>C3</td></tr>
<tr><td>10</td><td>C0</td><td>C0</td><td>C0</td><td>C1</td><td>C1</td><td>C2</td><td>C3</td><td>C3</td></tr>
<tr><td>11</td><td>C2</td><td>C0</td><td>C1</td><td>C2</td><td>C3</td><td>C3</td><td>C3</td><td>C3</td></tr>
</table></td></tr>
</table>

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6 Flow Control

Whenever the memory load exceeds preset thresholds, flow control commands are issued by the traffic management entity to the transmit MACs to prevent overflow conditions occurred. The overrun conditions are either locally or globally triggered, depending on the traffic management entity configuration. Transmit MAC executed those flow control commands depending on the duplex mode status. TC9205M executes backpressure for half duplex operation mode and it is IEEE 802.3x compliant for full duplex operation mode. In special conditions forward-pressure is also executed to eliminate packet loss.

For full duplex operation mode, TC9205M applies the XON/XOFF method using IEEE 802.3x PAUSE frames. When a flow control command is internally generated, the transmit MAC inserts a pause frame immediately or after the current transmission ends. On the receiving side, if a flow control frame is received, the transmit MAC will stop transmission for a number of slot times, where the pausing time was extracted from the received pause frame. The flow control function of the receiving side is always operational unless is specifically disabled by EEPROM on a per port basis (if no EEPROM is present the receive side flow-control is always operational), while transmission of the pause frames obeys the auto negotiation result.

TC9205M recognizes flow control frames from the incoming frames and these frames should also have a valid CRC. The IEEE 802.3x PAUSE operation reserved destination address, MAC control type and PAUSE opcode (88-08-00-01). The chip filters all frames having PAUSE operation reserved DA disregarding the other fields. If enabled, direct flow control addressing can be executed. This implies inserting the port address as SA in each flow control frame generated by TC9205M and recognizing as flow control all received frames with the port's address as DA, MAC control type and PAUSE opcode. After recognizing and executing appropriate flow control actions these frames will be also filtered. The port address is obtained by adding the port's number to the base address contained within EEPROM.

When no EEPROM is present and **DisFdFC** shared configuration pin is configured to high state, the switch will inhibit its ability to send flow control packets on all ports while preserving its ability to receive and act upon the incoming flow control packets. If this pin is configured to low state the switch will execute symmetrical PAUSE operation as defined in 802.3x.

The function of enabling/disabling the flow control in the EEPROM is now available on a per port basis rather than setting flow control globally for all ports and separate enabling/disabling flow control ability can be performed on either receive or transmit side of a port.

TC9205M can be instructed to ignore the auto-negotiation result for full duplex flow control ability. When the **FrcFdFC** shared configuration pin or the equvalent register in the EEPROM is equal to 1, the link partner will be considered to have full duplex flow control capable no matter of auto-negotiation result. The **FrcFdFC** setting is effective only for ports configured in 10/100 Mbps speed modes. When the **FrcGbFC** and the equivalent register in the EEPROM is equal to 1, the link partner will be considered symmetric and asymmetric towards link partner full duplex flow control capable no matter of auto-negotiation result. The **FrcGbFC** setting is effective only for ports configured in 1000 Mbps speed mode.

The TC9205M executes backpressure algorithm for half duplex flow control, supporting both collision-based and carrier-based backpressure. For collision-based backpressure the switch will be forced to send collision signals to the terminal that sends packets to TC9205M. While TC9205M detects an incoming frame that it wishes to backpressure with carrier sense signals, the switch will start transmission to that port. If no packet is available at that moment for transmission then the MAC layer will generate short jamming frames. Additionally, an aggressive backoff will be executed on the switch side (by the transmit MAC) after each of the forced collisions. The transmit MAC will chose between 0 and 1 slot times to backoff. This will grant a fast recovery for the switch's congested port and will secure the channel for the congested port in case it wishes to transmit (empty its buffers). If desired, the backoff can

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be completely disabled using shared configuration pin **DisBPBk** or EEPROM. In this case the switch will start transmitting with minimum IFG after carrier sense is deasserted and followed after collision.

For carrier-based backpressure the switch will use the deferral mechanism rather than the collision backoff mechanism. The transmit MAC will jam the line by sending continuous preamble. The link partner will see the channel busy and thus it will defer transmission without imposing any additional backoff delay. The jamming procedure will have short break to avoid jabber condition and the break will also be short enough to prevent the other stations from starting transmission. Preamble can be sent this way as long as necessary. If valid packets became available for transmission during this period then jamming will be interrupted and the packets will be transmitted with standard IFG (Inter-Frame Gap). In this case backpressure is executed the same way as collision based mechanism. Carrier based backpressure can be selected using shared configuration pin **CrBP** or EEPROM.

Backpressure operation can be disabled globally using the shared configuration pin **DisBkPr** or per port basis using the EEPROM. By default forward pressure is also enabled whenever backpressure is enabled. Forward pressure is executed only in extreme congestion conditions that normally do not occur often. This flow control procedure is highly efficient in minimizing the packet loss. If desired, the forward pressure can be disabled by the EEPROM setting.

If a HUB is connected to many workstations, one of the ports may be partitioned in heavy traffic when the switch executes backpressure. TC9205M can prevent this by discontinuing the backpressure process after a predefined number of consecutive collisions has reached. This function can be enabled using the shared configuration pin **FullBP** or adjusting EEPROM setting. Unlike other settings, to enable this feature the pin/bit should be set to '0'. The respective number of collisions defaults to 28 and can be specified using the EEPROM. In addition, when this feature is enabled the MAC will either grant receiving the next packet without colliding it, after which, it will resume the backpressure, or will completely quit backpressure waiting for a new XOFF command from internal flow control management device.

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7 Broadcast Throttling

In case of excessive broadcast, TC9205M will throttle the broadcast traffic based on buffer memory loading. Both global buffer pool loading and source port loading are considered. The number of frame buffers that can be consumed by broadcast packets received from an individual source port is permanently limited to the EEPROM configurable value (contained by **SrcLoadTrsh** field from Broadcast Configuration Register). The default value is 32 when the EEPROM is not present. Additionally, regarding the global aspect, broadcast frames are always dropped by broadcast queues overflow. Two broadcast queues are implemented within TC9205M, one for low and normal priority (Classes 0 and 1) and another for higher priorities (Classes 2 and 3).

Both filtering mechanisms described above can be avoided by enabling the flow control for broadcast process. This mechanism can be enabled using the **FcBcstEn** pin shared configuration or by adjusting the EEPROM setting. In this case the loading thresholds will never be reached and as result no broadcast packet will be dropped although the filtering mechanism always remains active. If the broadcast flow control is disabled TC9205M is still capable of taking continuous broadcast frames from one port and deliver them to all the other ports at maximum speed without losing packets.

Independent of the throttling mechanisms, a bandwidth based broadcast throttling can be enabled using the **BcstThrot** pin or by EEPROM setting. When this process is active, the receive broadcast bandwidth per port will be limited to a value between 1% and 31% from the port's maximum bandwidth. This percentage is encoded within **ThrotTrsh** field from EEPROM's Broadcast Configuration Register. Default value is 5 (%). Whenever the broadcast traffic bandwidth exceeds the above limit some broadcast frames will be randomly dropped in order to precisely meet the enforced bandwidth.

TC9205M has the ability to give an indication about its status, from the broadcast packets handling issue perspective. Its **BcstLED** pin can signal either if the incoming broadcast packets are dropped or if broadcast packets overflow a certain threshold. During reset, this pin has the meaning of **BcstCfg** shared configuration pin. The BcstLED will behave as a broadcast packets dropping indicator, it lights periodically whenever a broadcast packet is dropped due to buffer overflow.

8 Port Mirroring

Although TC9205M is a smart switch, it has the ability to set a pair of mirroring ports. This feature is available only through EEPROM settings. The port mirroring feature can be enabled by setting a value of '1' in either **EnTxMirror** field from EEPROM's **PortMirrorConfig** register or **EnRxMirror** field from the same register, or both.

When port-mirroring feature has been enabled, the **SourcePort** field from EEPROM's **PortMirrorConfig** register selects the monitored port while **DestinationPort** field from EEPROM's **PortMirrorConfig** register selects the monitoring port. The traffic on the monitored (mirror source) port will be forwarded to the monitor port (mirror destination). Both ports can be any of the TC9205M's ports.

If **EnRxMirror** field is set to '1' then all the incoming traffic of the mirror source port will be simultaneously forwarded towards its due destination and to the monitoring port. The bad CRC / undersized frames will be filtered out.

If **EnTxMirror** field is set to '1' then all the outgoing traffic of the mirror source port will be also forwarded to the monitoring port.

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9 Physical Layer Configuration / Polling

TC9205M embeds a Physical Layer MII Management configuration / polling entity which provides speed, duplex, link status and link partner full duplex flow control ability information to the switch. This information is obtained by continuously polling the status of Physical Layer devices through the serial management interface. The entity is under control of EEPROM settings and it can operate in four different modes. The polling entity also performs Phy configuration procedure at two seconds after reset and each time EEPROM control information changes.

The following operating modes are available per port basis (selectable by **ANMode** field from EEPROM's **ConfigRegP[x]**):

- **00** – **Normal Mode** (assumed by default when EEPROM is not present):In this mode the Auto-Negotiation Enable bit from MII Control Register (0.12) is checked first. If it is found enabled then TC9205M will disable advertisement for 1000BASE-T half duplex technology (9.8) and will advertise the full duplex flow control ability (4.10:11) according with internal flow control enable settings. Auto-negotiation is restarted leaving unchanged the rest of technology advertisements. Then Auto-Negotiation Advertisement register (4), Link Partner Base Page Ability register (5) and GMII registers (9:10) are polled continuously at 2 seconds interval in order to execute highest common denominator resolution. If auto-negotiation is disabled as reported by 0.12 then the switch will configure itself using bits 0.13 and 0.8 of Control register, and will consider link partner full duplex flow control capable. Gigabit speed will be disabled.
- **01** – **Advertise one mode:** Auto-Negotiation Enable is checked and if found to be disabled TC9205M will attempt to enable it. If successful the switch will force the port's speed and duplex mode by advertising only the technology corresponding to the **Speed** and **Duplex** fields from EEPROM's **ConfigRegP[x]**, otherwise bits 0.8 and 0.13 will be read for configuration and gigabit speed will be disabled. Full duplex flow control ability is also advertised along with selected technology and then auto-negotiation is restarted. An auto-negotiation register polling is executed as in Normal Mode.
- **10** – **Advertise multiple modes:** This mode is similar with previous one except that it advertises the technology corresponding to the forced mode and all lower position technologies, down to 10BASE-T half duplex.
- **11** – **Disable Auto-Negotiation:** When this mode is selected then auto-negotiation is disabled by setting bit 0.12 to '0' and the forced speed and duplex mode will be written to Configuration Register, bits 0.13, 0.6 and 0.8. This mode is available only for 10/100 Mbps speed modes so bit 0.6 will always be written as '0'. Link partner will be considered full duplex flow control capable.

In addition to the force mode feature, the TC9205M internal speed and duplex can be chosen between enforced ones (**Speed** and **Duplex** fields from EEPROM's **ConfigRegP[x]**) and polling results by means of **ForceIntMode** configuration.

Independently of Phy configuration/polling operation mode the Link Status is also permanently monitored. If a Physical device reports link failure via 1.2 status bit then TC9205M disables transmission on associated port without holding any memory resources allocated for its transmission queues. The reported Link Status can be forced to '1' using **ForceLink** bit from the same **ConfigRegP[x]** register.

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10 EEPROM Interface

TC9205M can be configured using a serial EEPROM device type AT24C02A (2048 bits organized as 256 pages of 1 byte each). With this device the manufacturer can deliver a pre-configured system to their customers while the customers can reconfigure the system and retain their preferences. TC9205M also provides a virtual internal EEPROM mode, which enables the programming entity to write the configuration data directly into the chip, without using the external EEPROM. In this mode the configuration data is lost after reset procedures.

The TC9205M is able to operate without this device and can make effective use of its features using only the pin configuration interface. The EEPROM configuration provides additional features and it can override all pin interface settings offering a jumperless configuration mode. For this reason equivalent EEPROM settings can be found for every configuration pin.

A validation bit is provided for each one of the EEPROM Configuration Registers. A dedicated Validation Register is reserved for this purpose and corresponding bits from this register must be set in order to enable the desired EEPROM configurations.

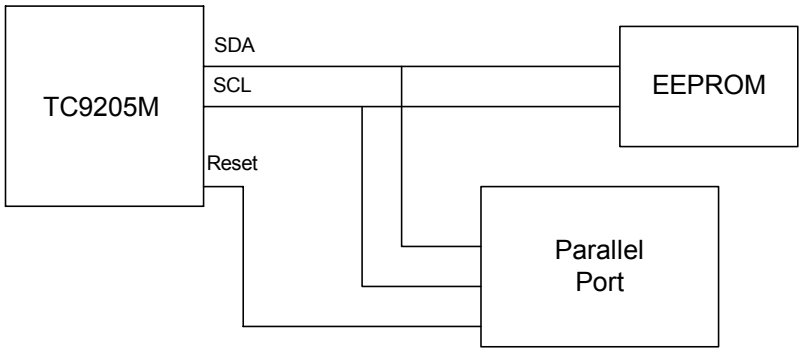
The EEPROM configuration information is accessed by the TC9205M after each reset procedure.

10.1 Reprogramming the EEPROM for reconfiguration

If the **'Reset'** pin is hold low the TC9205M's EEPROM interface will go into high impedance state. This feature enables easy reprogramming of the EEPROM during installation or reconfiguration.

The EEPROM can be reprogrammed using an external parallel port. A dedicated signal from this port can be used to hold the RESET pin low. Once the TC9205M interface pins have got to the high impedance state the EEPROM can be programmed by the parallel port trough the SDA and SCL pins.

To enable the AT24C02A device to be accessed by the TC9205M its page address input pins must be hardwired to '0'. For virtual EEPROM mode the programming can be done using the same AT24C02A byte write protocol but page address bits must be "100" (A2 downto A0).



10.2 EEPROM Address Map

Physical Address	Bits	Register Name	Validation Bit	DESCRIPTION
EEPROM				
00h	[7:0]	ValidReg [7 downto 0]	-	Validation Register
01h	[7:0]	ValidReg [15 downto 8]	-	Validation Register
02h	[7:0]	ValidReg [23 downto 16]	-	Validation Register
03h	[7:0]	ValidReg [24 downto 31]	-	Validation Register
04h	[7:0]	ValidReg [32 downto 39]	-	Validation Register
05h	[7:0]	ConfigRegP0 [7 downto 0]	ConfigRegP0	Port 0 Configuration Register
06h	[7:0]	ConfigRegP0 [15 downto 8]		
07h	[7:0]	ConfigRegP1 [7 downto 0]	ConfigRegP1	Port 1 Configuration Register
08h	[7:0]	ConfigRegP1 [15 downto 8]		
09h	[7:0]	ConfigRegP2 [7 downto 0]	ConfigRegP2	Port 2 Configuration Register
0ah	[7:0]	ConfigRegP2 [15 downto 8]		
0bh	[7:0]	ConfigRegP3 [7 downto 0]	ConfigRegP3	Port 3 Configuration Register
0ch	[7:0]	ConfigRegP3 [15 downto 8]		
0dh	[7:0]	ConfigRegP4 [7 downto 0]	ConfigRegP4	Port 4 Configuration Register
0eh	[7:0]	ConfigRegP4 [15 downto 8]		
0fh	[7:0]	ConfigRegP5 [7 downto 0]	ConfigRegP5	Port 5 Configuration Register
10h	[7:0]	ConfigRegP5 [15 downto 8]		
11h	Reserved			
12h	Reserved			
13h	Reserved			
14h	Reserved			
15h - 18h	Reserved			
19h	[7:0]	IFGConfigP0 [7 downto 0]	IFGConfigP0	Port 0 IFG Configuration
1ah	[7:0]	IFGConfigP1 [7 downto 0]	IFGConfigP1	Port 1 IFG Configuration
1bh	[7:0]	IFGConfigP2 [7 downto 0]	IFGConfigP2	Port 2 IFG Configuration
1ch	[7:0]	IFGConfigP3 [7 downto 0]	IFGConfigP3	Port 3 IFG Configuration
1dh	[7:0]	IFGConfigP4 [7 downto 0]	IFGConfigP4	Port 4 IFG Configuration
1eh	[7:0]	IFGConfigP5 [7 downto 0]	IFGConfigP5	Port 5 IFG Configuration
1fh	Reserved			
20h	Reserved			
21h – 2dh	Reserved			
2eh	[7:0]	FlowControlReg [7 downto 0]	FlowContrReg	Flow Control Register
2fh	[7:0]	FlowControlReg [15 downto 8]		
30h	[7:0]	BPTimeValue [7 downto 0]	BPTimeValue	Backpressure Time Value Register
31h	[7:0]	BPTimeValue [15 downto 8]		
32h	[7:0]	FCBaseAddress [47 downto 40]	FCBaseAddress	Flow Control Source Base Address Register
33h	[7:0]	FCBaseAddress [39 downto 32]		
34h	[7:0]	FCBaseAddress [31 downto 24]		
35h	[7:0]	FCBaseAddress [23 downto 16]		
36h	[7:0]	FCBaseAddress [15 downto 8]		
37h	[7:0]	FCBaseAddress [7 downto 0]		
38h – 3bh	Reserved			
3dh	[7:0]	BroadcastConfig [7 downto 0]	BroadcastConfig	Broadcast Configuration Register
3eh	[7:0]	BroadcastConfig [15 downto 8]		

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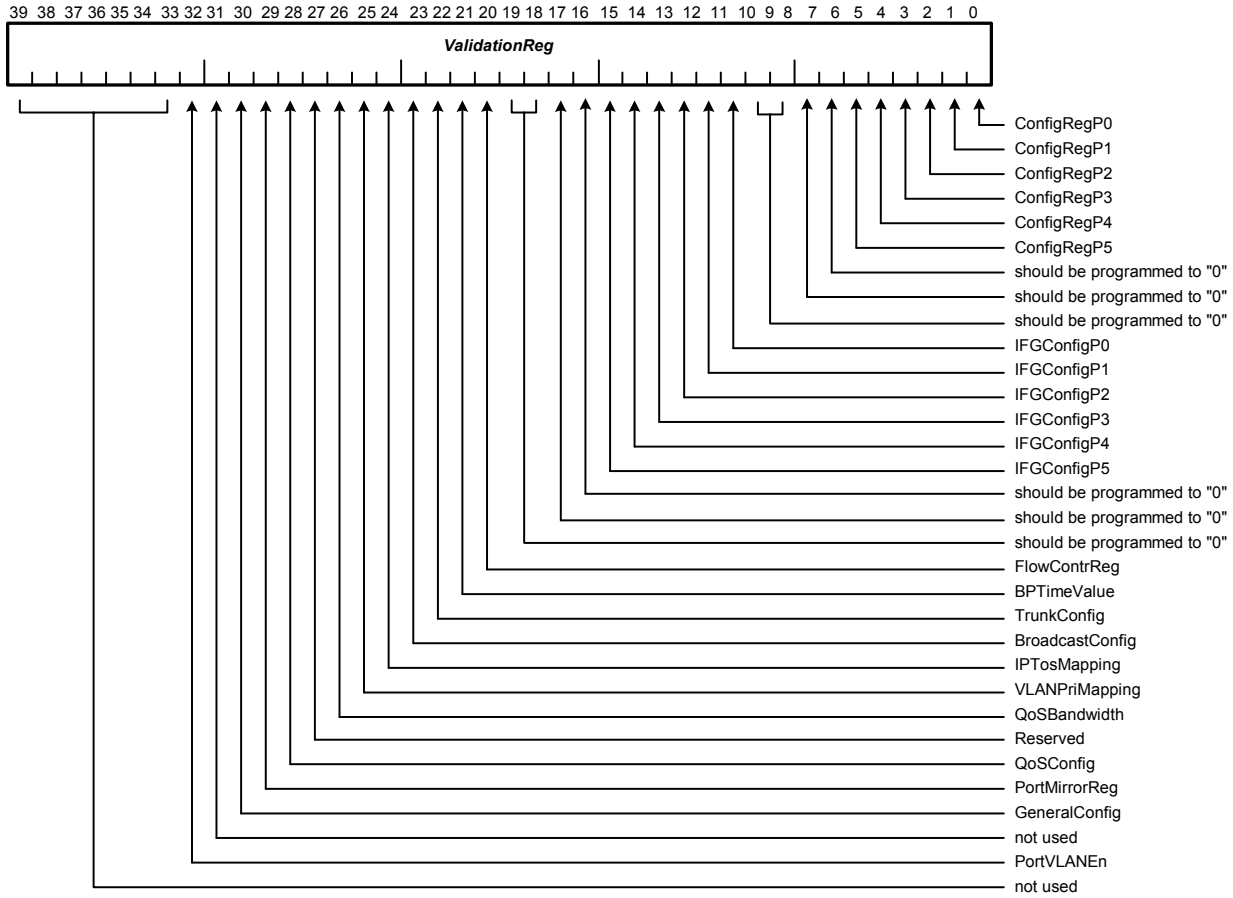
Physical Address	Bits	Register Name	Validation Bit	DESCRIPTION
EEPROM				
3fh	[7:0]	IPTosMapping [7 downto 0]	IPTosMapping	IP Priority Mapping Register
40h	[7:0]	IPTosMapping [15 downto 8]		
41h	[7:0]	VLANPriMapping [7 downto 0]	VLANPriMapping	VLAN Priority Mapping Register
42h	[7:0]	VLANPriMapping [15 downto 8]		
43h	[7:0]	CoSBandwidth [7 downto 0]	CoSBandwidth	CoS Bandwidth Register
44h	[7:0]	CoSBandwidth [15 downto 8]		
45h	[7:0]	[7 downto 0]		Reserved Register
46h	[7:0]	[15 downto 8]		
47h	[7:0]	CosConfig [7 downto 0]	CoSConfig	CoS Configuration Register
48h	[7:0]	PortMirrorReg [7 downto 0]	PortMirrorReg	Port Mirroring Configuration Register
49h	[7:0]	PortMirrorReg [15 downto 8]		
4ah	[7:0]	GeneralConfig [7 downto 0]	GeneralConfig	General Configuration Register
4bh – 4eh			Reserved	
4fh	[7:0]	PortVLANEn	PortVLANEn	Port VLAN Enable Register
50h	[7:0]	VLAN0Reg [7 downto 0]	PVIDEn	ID 0 virtual LAN Register
51h			Reserved	
52h	[7:0]	VLAN1Reg [7 downto 0]	PVIDEn	ID 1 virtual LAN Register
53h			Reserved	
54h	[7:0]	VLAN2Reg [7 downto 0]	PVIDEn	ID 2 virtual LAN Register
55h			Reserved	
56h	[7:0]	VLAN3Reg [7 downto 0]	PVIDEn	ID 3 virtual LAN Register
57h			Reserved	
58h	[7:0]	VLAN4Reg [7 downto 0]	PVIDEn	ID 4 virtual LAN Register
59h			Reserved	
5ah			Reserved	
5bh			Reserved	
5ch			Reserved	
5dh			Reserved	
5eh			Reserved	
5fh – 6fh			Reserved	
70h	[7:0]	DataWriteReg [15 downto 8]	-	Data Write Register
71h	[7:0]	DataWriteReg [7 downto 0]		
72h	[7:0]	PhyAddress [7 downto 0]	-	Phy Address Register
73h	[7:0]	RegAddress [7 downto 0]	-	Phy's Register Address Register
74h	[7:0]	IOControl [7 downto 0]	-	IO Control Register
75h	[7:0]	DataReadReg [7 downto 0]	-	Data Read Register
76h	[7:0]	DataReadReg [15 downto 8]		

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10.3 Register Description

10.3.1 Validation Register

- Address: 00h - 04h



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Bit(s)	Field	Description
39 – 0	ValidationReg	EEPROM's Configuration Registers Validation Register

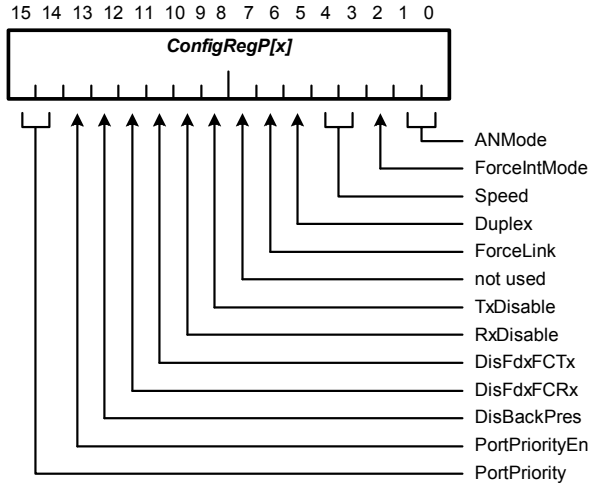
ValidationReg – each bit from this register corresponds to an EEPROM Configuration Register. To enable the use of a certain configuration register, a value of '1' shall be written to its corresponding bit from the validation register.

ConfigRegP0 – validation bit for Port 0 Configuration Register
ConfigRegP1 – validation bit for Port 1 Configuration Register
ConfigRegP2 – validation bit for Port 2 Configuration Register
ConfigRegP3 – validation bit for Port 3 Configuration Register
ConfigRegP4 – validation bit for Port 4 Configuration Register
ConfigRegP5 – validation bit for Port 5 Configuration Register (10/100 only)
IFGConfigP0 – validation bit for Port 0 IFG Configuration Register
IFGConfigP1 – validation bit for Port 1 IFG Configuration Register
IFGConfigP2 – validation bit for Port 2 IFG Configuration Register
IFGConfigP3 – validation bit for Port 3 IFG Configuration Register
IFGConfigP4 – validation bit for Port 4 IFG Configuration Register
IFGConfigP5 – validation bit for Port 5 IFG Configuration Register (10/100 only)
FlowContrReg – validation bit for Flow Control Register
BPTimeValue – validation bit for Back Pressure Time Value Register
BroadcastConfig – validation bit for Broadcast Configuration Register
IPTosMapping – validation bit for IP Priority Mapping Register
VLANPriMapping – validation bit for VLAN Priority Mapping Register
CoSBandwidth – validation bit for CoS Bandwidth Register
Reserved – Reserved Register
CoSConfig – validation bit for CoS Configuration Register
PortMirrorReg – validation bit for Port Mirroring Register
GeneralConfig – validation bit for General Configuration Register
PortVLANEn – validation bit for Port VLAN Enable Register

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10.3.2 Port [*X*] Configuration Register

- Addresses: 05h – 0eh
- Note: x is in range 0 to 4



Bit(s)	Field	Description
1 - 0	ANMode	Operating mode selection for the phy configuration/polling entity
2	ForceIntMode	Internal speed and duplex selection enforcement
4 - 3	Speed	Internal speed selection (10 Mbps/100Mbps/1000Mbps)
5	Duplex	Internal duplex selection (full/half)
6	ForceLnk	Force Link Status to 'ON'
7	not used	not used
8	TxDisable	Disable transmit MAC
9	RxDisable	Disable receive MAC
10	DisFdxFCTx	Disable flow control in full duplex on transmit side
11	DisFdxFCRx	Disable flow control in full duplex on receive side
12	DisBackPres	Disable backpressure
13	PortPriorityEn	Enable port priority
15 - 14	PortPriority	Sets the priority class(class 0, class 1, class 2, class 3)

ANMode This field selects the way auto-negotiation advertisements are configured by theTC9205M's physical layer management polling entity and the way Phy speed and duplex modes are extracted from management registers. It can enable EEPROM forced modes that also use **Duplex** and **Speed** bits below to configure the Phy mode.

- 00 – Normal Mode
- 01 – Advertise one mode
- 10 – Advertise multiple modes
- 11 – Disable auto-negotiation

Default is "00"(0).

ForceIntMode This bit selects the source of internal port mode configuration. When this bit is '0' the port's speed and duplex is configured according to Phy polling results, otherwise it is set as indicated by following **Speed** and **Duplex**. Default is '0'.

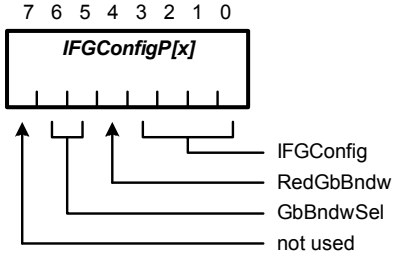
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Speed	Used by the physical layer management polling entity to configure physical layer's speed mode when EEPROM forced modes are selected. Additionally this bit can be used to directly force the internal speed mode. 00 – 10M 01 – 100M 10 – 1000M These bits should be programmed to 10M mode or 100M mode for port 5.
Duplex	Used by the physical layer management polling entity to configure physical layer's duplex mode when EEPROM forced modes are selected. Additionally this bit can be used to directly force the internal duplex mode.
ForceLnk	Setting this bit to '1' will force the internal polled link status of the corresponding port to *"ON"*. Default is '0'.
TxDisable	Setting this bit to '1' will disable the transmission MAC device, thus inhibiting transmission on the corresponding port. Default is '0'.
RxDisable	Setting this bit to '1' will disable the receiving MAC device, thus inhibiting receiving on the corresponding port. Default is '0'.
DisFdxFCTx	Setting this bit to '1' will disable flow control operation for full duplex mode on transmit side (transmission of pause frames). Default is '0'.
DisFdxFCRx	Setting this bit to '1' will disable flow control operation for full duplex mode on receive side (pausing frame transmission). Default is '0'.
DisBackPres	Setting this bit to '1' will disable flow control for half duplex mode (backpressure). Default value is its corresponding **DisBkPr** pin value.
PortPriorityEn	Setting this bit to '1' will force the corresponding port to the priority set within the **PortPriority** field, otherwise the pin configuration will be used.
PortPriority	This bit will set one of the four priority classes on the corresponding port.

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10.3.3 Port [*X*] IFG Configuration Register

- Addresses: 19h – 1dh



Bit(s)	Field	Description
3 - 0	IFGConfig	Interframe Gap Configuration
4	RedGbBndw	Reduced gigabit bandwidth
6 - 5	GbBndwSel	Gigabit bandwidth selection
7	not used	not used

IFGConfig These bits are used to set the minimum IFG with 32 bit time resolution. The default matches the standard minimum IFG of 96 bit time: '0011' (3).

IFGConfig	*IFG (bit time)*
0001	32
0010	64
0011	96 (default)
0100	128
…	…
1111	480
0000	512

RedGbBndw Setting this bit to '1', will enable a 1000Mbps port to reduce its transmission bandwidth to the percentage indicated by the **GbBndwSel** field. Setting this bit to '0', the **GbBndwSel** field will be meaningless and the port will make use of its full transmission bandwidth. This bit is in effect only when the port's speed mode is 1000Mbps. Default is '0'.

GbBndwSel Transmission bandwidth enforcement when in 1000 Mbps mode.

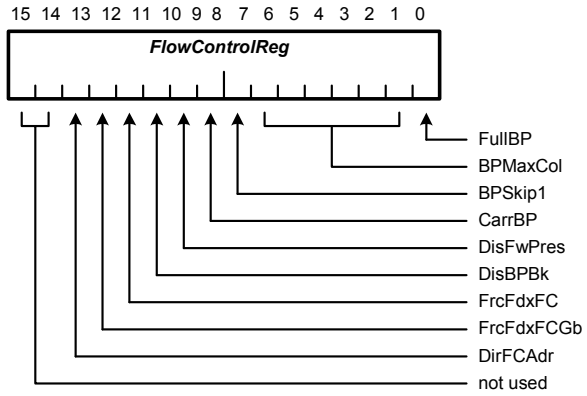
GbBndwSel	*Transmission bandwidth*
00	50%
01	66%
10	80%
11	90%

This feature can be used to avoid congestion in some LAN nodes without flow control capabilities or to avoid server overloads

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10.3.4 Flow Control Register

- Address: 2Eh, 2Fh



Bit(s)	Field	Description
0	FullBP	Full backpressure
6 - 1	BPMaxCol	Maximum number of collisions for backpressure
7	BPSkip1	Skip one packet for backpressure operation
8	CarrBp	Carrier backpressure
9	DisFwPres	Disable forwardpresure
10	DisBPBk	Disable backoff during backpressure
11	FrcFdxFC	Force full duplex flow control in 10/100 Mbps
12	FrcFdxFCGb	Force full duplex flow control in 1000 Mbps
13	DirFCAdr	Direct flow control addressing
15 - 14	not used	not used

FullBP In normal operation the backpressure process is executed until flow control condition disappears or until the time limit for backpressure is reached. This limit is based on EEPROM's **BPTimeValue** register. When this configuration is '0' the backpressure process will be also limited from exceeding the value contained in **BPMaxCol** field.
Default value is its corresponding **FullBP** pin value.

BPMaxCol Specifies the number of consecutive collisions that will determine TC9205M to quit backpressure (see the setting above). Default is '011100' (28).

BPSkip1 If **FullBP** setting is configured to '0' and a number of **BPMaxCol** collisions is reached, the MAC will ensure receiving the next packet without colliding it if this bit is set to '1', after which will resume the backpressure. Otherwise it will completely quit backpressure waiting for a new XOFF command from internal flow control entity.
Default is '0'.

CarrBp Setting this bit to '1' will enable carrier-based backpressure, otherwise only collision-based backpressure is executed. Default value is its corresponding **CarrBp** pin value.

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DisFwPres Whenever backpressure is enabled, in case of extreme congestion (memory overload) forward pressure is also executed unless deactivated by this bit. Forward pressure is never executed when backpressure is disabled. Setting this bit to '1' will disable forward pressure for all half duplex ports. Default is '0'.

DisBPBk Setting this bit to '1' will cause no backoff to be executed when a half duplex port is in backpressure mode. This means a new collision can be forced immediately after the previous one if carrier sense is observed. Setting this bit to '0' will enable a very aggressive backoff to be executed (recommended). Default value is its corresponding **DisBPBk** pin value.

FrcFdxFC Setting this bit to '1' will instruct TC9205M to disregard the auto-negotiation result for the full duplex flow control ability. Link partner will be considered full duplex flow control able. This setting is effective only for ports configured in 10/100 Mbps speed modes. Default is '0'.

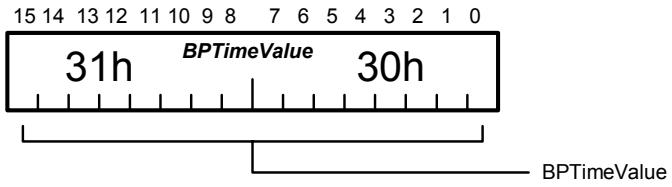
FrcFdxFCGb Setting this bit to '1' will instruct TC9205M to disregard the auto-negotiation result for the full duplex flow control ability. Link partner will be considered able to execute symmetric and asymmetric towards link partner full duplex flow control. This setting is effective only for ports configured in 1000 Mbps speed mode. Default is '0'.

DirFCAdr Setting this bit to '1' will enable direct flow control addressing mechanism, otherwise direct flow control addressing is disabled. Default is '0'.

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10.3.5 Backpressure Time Value Register

- Address: 31h, 30h

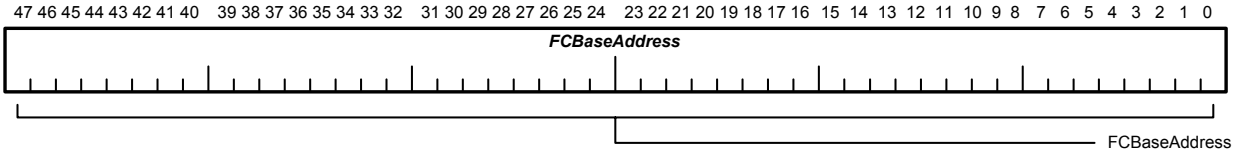


Bit(s)	Field	Description
15 – 0	BPTimeValue	Backpressure time value

BPTimeValue A 16 bit value used to compute internal time value for backpressure operation. Default value is '0000100000000000'(2048).

10.3.6 Flow Control Port Base Address Register

- Address: 32h, 33h, 34h, 35h, 36h, 37h



Bit(s)	Field	Description
47 – 0	FCBaseAddress	Source port base address for flow control packets

FCBaseAddress Contains a 48 bit MAC address used to generate the individual port address used in direct flow control addressing. The port addresses are obtained by incrementing this base address and assigning the result to the TC9205M's ports starting with port 0. The least significant 5 bits of this address will be ignored and replaced with '0', so these bits will encode the port number in the actual port address.

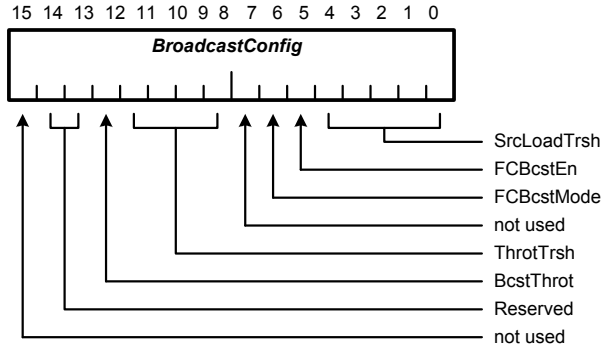
10.3.7 Reserved

- Address: 3Ch This register should be set to "0".

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10.3.8 Broadcast Configuration Register

- Address: 3Dh, 3Eh



Bit(s)	Field	Description
4 - 0	SrcLoadTrsh	Source port loading limit for broadcast
5	FCBcstEn	Flow control broadcast enable
6	FCBcstMode	Flow control broadcast mode
7	not used	not used
11 -8	ThrotTrsh	Global buffer pool loading threshold for broadcast
12	BcstThrot	Broadcast throttling (bandwidth)
14 - 13	Reserved	
15	not used	not used

SrcLoadTrsh The maximum number of frame buffers used on each receiving port for broadcast. Default is '11000' (24).

FCBcstEn Setting this bit to '1' will enable flow control mechanism for broadcast frames. Setting this bit to '0' will cause broadcast packets to be dropped on queue overflow condition. Default value is its corresponding **FcBcstEn** pin value.

FCBcstMode This bit selects the source of flow control for broadcast operation:
'0' – broadcast flow control is issued on source port basis
'1' – broadcast flow control is issued by any of the two broadcast queues
Default value is its corresponding **FcBcstMode** pin value.

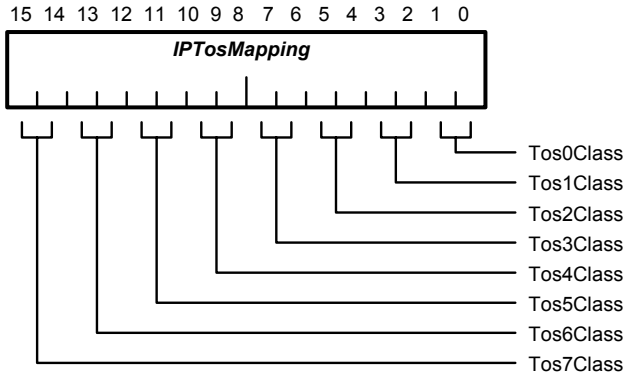
ThrotTrsh Setting this bit to '1' will enable bandwidth based broadcast throttling. The value represents the maximum percentage of the full receiving bandwidth than can be used for broadcast. Default is '00101'(5%).

BcstThrot Setting this bit to '1' will enable throttling for broadcast frames. Default value is its corresponding **BcstThrot** pin value.

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10.3.9 IP Priority Mapping Register

- Address: 3Fh, 40h



Bit(s)	Field	Description
1 - 0	Tos0Class	priority mapping for IP precedence 0
3 - 2	Tos1Class	priority mapping for IP precedence 1
5 - 4	Tos2Class	priority mapping for IP precedence 2
7 - 6	Tos3Class	priority mapping for IP precedence 3
9 - 8	Tos4Class	priority mapping for IP precedence 4
11 - 10	Tos5Class	priority mapping for IP precedence 5
13 - 12	Tos6Class	priority mapping for IP precedence 6
15 - 14	Tos7Class	priority mapping for IP precedence 7

Tos[x]Class This field maps the IP priority level **x** found in the incoming frame to one of the four priority classes. The table bellow shows the mapping.

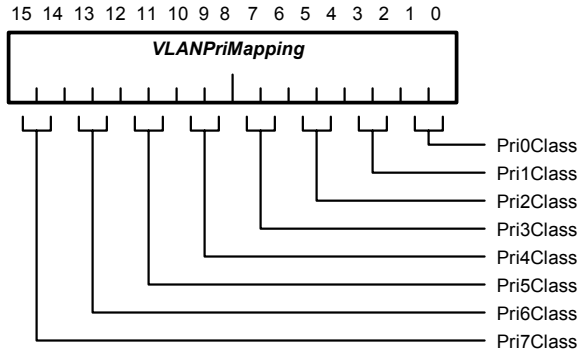
Tos[x]Class	CoS
00	Class 0 priority
01	Class 1 priority
10	Class 2 priority
11	Class 3 priority

x ranges in the field 0 to 7.

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10.3.10 VLAN Priority Mapping Register

- Address: 41h, 42h



Bit(s)	Field	Description
1 - 0	Pri0Class	priority mapping for VLAN user_priority 0
3 - 2	Pri1Class	priority mapping for VLAN user_priority 1
5 - 4	Pri2Class	priority mapping for VLAN user_priority 2
7 - 6	Pri3Class	priority mapping for VLAN user_priority 3
9 - 8	Pri4Class	priority mapping for VLAN user_priority 4
11 - 10	Pri5Class	priority mapping for VLAN user_priority 5
13 - 12	Pri6Class	priority mapping for VLAN user_priority 6
15 - 14	Pri7Class	priority mapping for VLAN user_priority 7

Pri[x]Class This field maps the VLAN priority level **x** found in the incoming frame to one of the four priority classes. The table bellow shows the mapping.

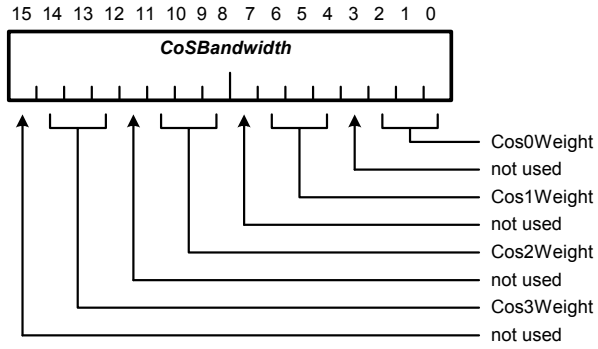
Pri[x]Class	CoS
00	Class 0 priority
01	Class 1 priority
10	Class 2 priority
11	Class 3 priority

x ranges in the field 0 to 7.

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10.3.11 CoS Bandwidth Register

- Address: 43h, 44h



Bit(s)	Field	Description
2 - 0	CoS0Weight	000
3	not used	not used
6 - 4	CoS1Weight	The weight for priority class 1 queue
7	not used	not used
10 - 8	CoS2Weight	The weight for priority class 2 queue
11	not used	not used
14 - 12	CoS3Weight	The weight for priority class 3 queue
15	not used	not used

CoS[y]Weight This field sets the weight for its associated priority queue. The transmission bandwidth percentage given to the associated queue is set by the formula below:

Queue **y**'s priority [%] = **F**(CoS[**y**]Weight) * $100 / \sum_{n=0}^{3} (\mathbf{F}(\text{CoS}[n]\text{Weight}))$

Note: **y** ranges in 0 to 3 and **F** is a tabled function described bellow:

f("000") = 1	f("100") = 16
f("001") = 2	f("101") = 32
f("010") = 4	f("110") = not used
f("011") = 8	f("111") = not used

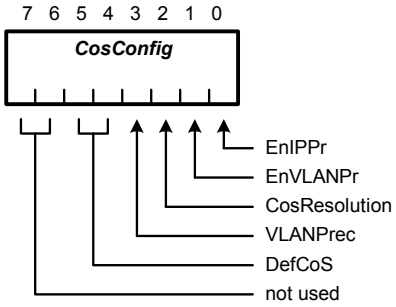
10.3.12 Reserved Register

- Address: 45h, 46h

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10.3.13 CoS Configuration Register

- Address: 47h



Bit(s)	Field	Description
0	EnIPPr	Enable IP priority
1	EnVLANPr	Enable VLAN priority
2	CoSResolution	CoS Resolution Mode
3	VLANPrec	VLAN Precedence
5 - 4	DefCoS	Default Class of Service
7 - 6	not used	not used

EnIPPr Setting this field to '1' will enable IP prioritization. CoS resolution function will consider TOS Precedence bits from IP Header. Default value is its corresponding **EnIPPr** pin value.

EnVLANPr Setting this field to '1' will enable VLAN prioritization. CoS resolution function will consider user-priority bits (TCI field) from 802.1Q VLAN Tag Header. Default value is its corresponding **EnVLANPr** pin value.

CoSResolution When this bit is set to '0' the CoS resolution function will assign to each frame the highest CoS obtained from all enabled prioritization sources.
Setting this field to '1', the resolution function will perform a prioritized parsing of CoS sources, depending of **VLANPrec** bit. The CoS will be assigned considering the first source that has been found within the frame (VLAN or IP). If none of the VLAN or IP prioritization sources have been found then the port based prioritization is considered if enabled, otherwise the frame will be assigned the default CoS. Default is '1'.

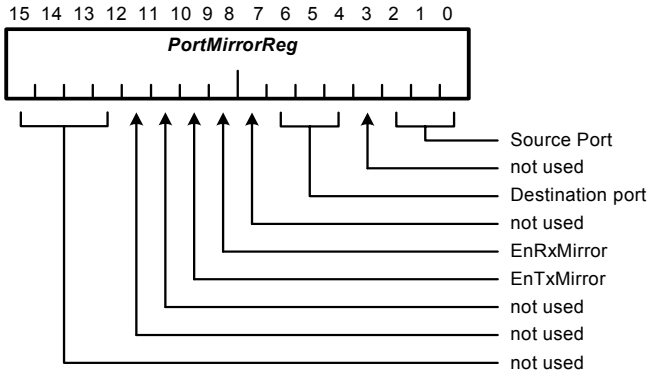
VLANPrec If **CoSResolution** field is set to '0', this field is meaningless. When **CoSResolution** field is set to '1', this field will set the prioritization sources precedence for the resolution function. A value of '1' will set the following precedence (from highest to lowest): **VLAN** priority, **IP** priority, **port** priority. A value of '0' will set the following precedence (from highest to lowest): **IP** priority, **VLAN** priority, **port** priority. Default is '0'.

DefCoS This is the CoS a frame will receive when port based prioritization is disabled and both VLAN and IP headers are not found (or the corresponding VLAN / IP prioritizations are also disabled). This configuration can be used especially when CoSResolution setting is '0'. Default is "01" (CoS 1).

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10.3.14 Port Mirroring Register

- Address: 48h, 49h



Bit(s)	Field	Description
2 - 0	SourcePort	Source port(monitored port)
3	not used	not used
6 - 4	DestinationPort	Destination port(monitoring port)
7	not used	not used
8	EnRxMirror	Enable mirroring on receiving packets
9	EnTxMirror	Enable mirroring on transmitting packets
10	not used	not used
11	not used	not used
15 - 12	not used	not used

SourcePort One of the eight ports of the switch that is intended for been monitored through port mirroring feature. If enabled, the traffic on this port can be additionally forwarded to the monitoring port. Only one port can be monitored at a time.

DestinationPort One of the eight ports address's of the switch that is intended to monitor one of the other ports through port mirroring feature. This port will receive all traffic on the mirror source port.

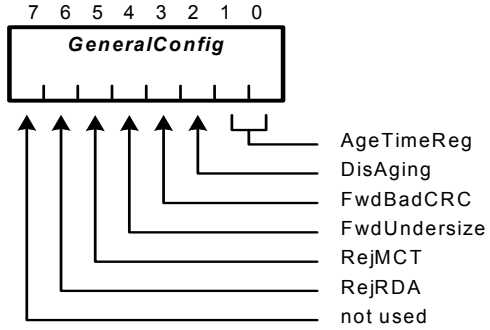
EnRxMirror Setting this bit to '1', the destination port will mirror all the source port's incoming traffic.

EnTxMirror Setting this bit to '1', the destination port will mirror all the source port's outgoing traffic.

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10.3.15 General Configuration Register

- Address: 4ah



Bit(s)	Field	Description
1 – 0	AgeTimeReg	Sets the aging time
2	DisAging	Disable aging
3	FwdBadCRC	Forward bad CRC packets
4	FwdUndersize	Forward undersized packets
5	RejMCT	Reject MAC Control Type frames
6	RejRDA	Reject 802.1D Reserved Group Addresses DA frames
7	not used	not used

AgeTimeReg Allows 4 values for the aging time to be chosen from.

- 00 – 300 seconds
- 01 – 600 seconds
- 10 – 900 seconds
- 11 – 1200 seconds

Default is ‘01’(600 seconds).

DisAging Setting this bit to '1' will cause TC9205M to disable its aging mechanism for the stored MAC addresses. Default is '0'.

FwdBadCRC Setting this bit to ‘1’ will enable forwarding of bad CRC packets. Default is '0'.

FwdUndersize Setting this bit to ‘1’ will enable forwarding of undersized packets. Default is '0'

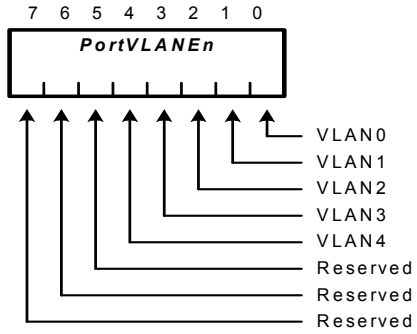
RejMCT Setting this bit to ‘1’ will configure the switch to filter all frames with MAC Control Type (type 8808). Default is ‘0’.

RejRDA Setting this bit to ‘1’ will configure the switch to filter all frames with 802.1D Reserved Group Destination Address except for Bridge Group Address (01-80-C2-00-00-00). Default value is its corresponding **RejRDA** pin value.

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10.3.16 Port VLAN Enable Register

- Address: 4fh



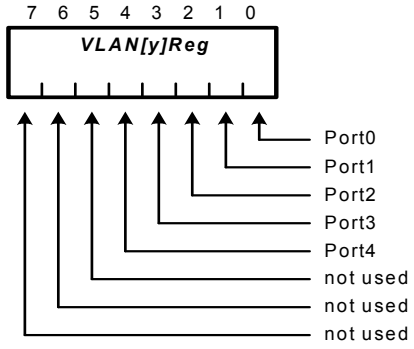
Bit(s)	Field	Description
0	VLAN0	VLAN 0 enable
1	VLAN1	VLAN 1 enable
2	VLAN2	VLAN 2 enable
3	VLAN3	VLAN 3 enable
4	VLAN4	VLAN 4 enable
5	Reserved	
6	Reserved	
7	Reserved	

VLAN[y] Enables/disables VLAN **y**. (**y** is in range 0 to 4)

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10.3.17 VLAN [Y] Register

- Address: 50h, 52h, 54h, 56h, 58h



Bit(s)	Field	Description
0	Port0	Port 0 membership to VLAN y
1	Port1	Port 1 membership to VLAN y
2	Port2	Port 2 membership to VLAN y
3	Port3	Port 3 membership to VLAN y
4	Port4	Port 4 membership to VLAN y
5	not used	If used, it should be a member of all VLANgroups.
6	not used	
7	not used	

Port[x] Port **x** membership to VLAN **y**.
'0' – Port **x** is not a member of VLAN **y**
'1' – Port **x** is a member of VLAN **y**

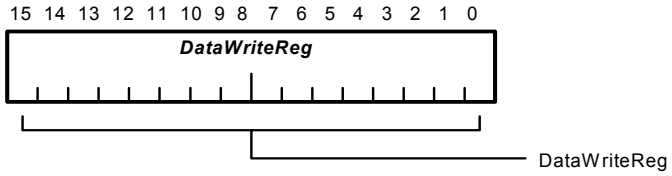
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10.4 Writing / Reading PHY management registers via EEPROM interface

The following set of registers allows read/write operations through MDIO interface for direct managing of physical layer devices. This feature is available through virtual EEPROM mode.

10.4.1 Data Write Register

- Address: 70h, 71h

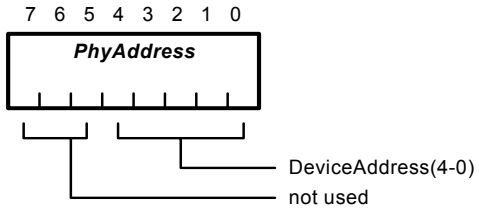


Bit(s)	Field	Description
15 - 0	DataWriteReg	MDIO Data Write Register

DataWriteReg – Contains a 16 bit data word used to write a PHY management register.

10.4.2 Physical Layer Device Address Register

- Address: 72h



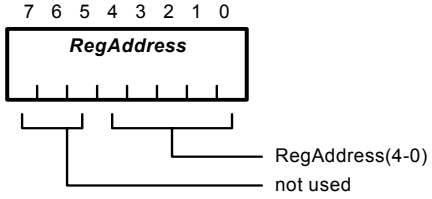
Bit(s)	Field	Description
4 – 0	DeviceAddress	Physical layer device address register
7 – 5	not used	not used

DeviceAddress – Contains a 5-bit word used as device address in MDIO operations.

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10.4.3 Physical Layer's Register Address Register

- Address: 73h

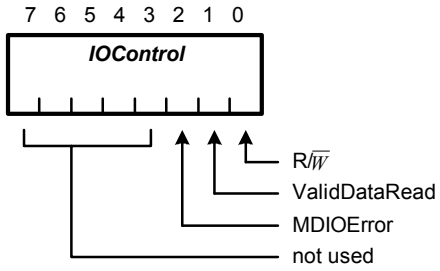


Bit(s)	Field	Description
4 – 0	RegAddress	Physical layer device's register address register
7 – 5	not used	not used

RegAddress – Contains a 5 bit word used as register address in MDIO operations.

10.4.4 IO Status Control Register

- Address: 74h



Bit(s)	Field	Description
0	R/$\overline{W}$	Operation code
1	ValidDataRead	Valid Data Read
2	MDIOError	MDIO Error
3 – 7	not used	not used

R/$\overline{W}$ – Operation Code. Setting this bit to '1' will select read operation otherwise will select write operation. MDIO Read / Write operation is started by performing a virtual EEPROM write to **IOControl** register.

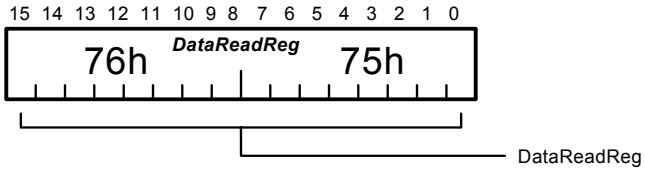
ValidDataRead – Indicates if **DataReadReg** register contains valid data.
'1'- data valid
'0'- read not performed yet

MDIOError – This bit signals errors on MDIO line.
'1'- MDIO error.
'0'- MDIO read successful.

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10.4.5 Data Read Register

- Address: 76h, 75h



Bit(s)	Field	Description
15 – 0	DataReadReg	MDIO Data Read Register

DataReadReg – Contains a 16 bit data word read from a PHY management register.

Write Operation.

Before starting a write operation the following registers need to be set :

- **PhyAddress** – written with MDIO device address
- **RegAddress** – written with MDIO register address
- **DataWriteReg** – data word to be write to selected register

The write operation is then started by performing a write to **IOControl** register with bit 0 cleared.

Read Operation.

Before starting a read operation the following registers need to be set :

- **PhyAddress** – written with MDIO device address
- **RegAddress** – written with MDIO register address

The write operation is then started by performing a write to **IOControl** register with bit 0 set.

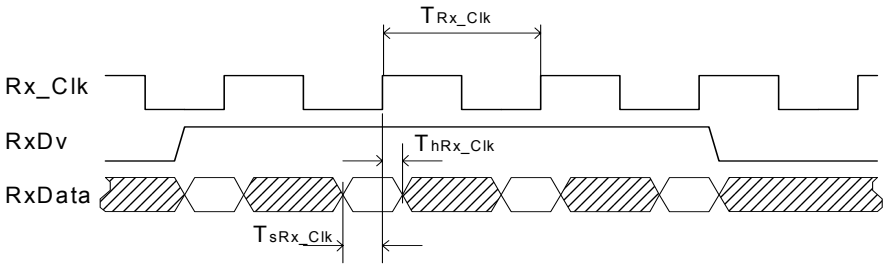
Subsequently, the **IOControl** register needs to be monitored in order to detect MDIO operation error reported via **IOControl's** bit 2. The **ValidDataRead** bit is always read as '1' unless the EEPROM line is driven at over 1MHz speed. If no error occurred then data can be read from **DataReadReg**.

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11 Timing Requirements

11.1 GMII / MII Receive Timing Requirements

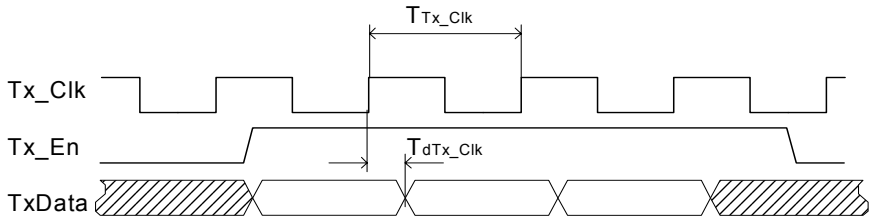
Symbol	Description	Min.	Typ.	Max.	Unit
$_{Rx_Clk}$	Receive clock period GMII	-	8	-	ns
$_{Rx_Clk}$	Receive clock period MII	-	40	-	ns
T_{sRx_Clk}	RxDv, RxData to Rx_Clk rising setup time	2	-	-	ns
T_{hRx_Clk}	RxDv, RxData to Rx_Clk rising hold time	0.5	-	-	ns



GMII / MII Receive

11.2 GMII / MII Transmit Timing

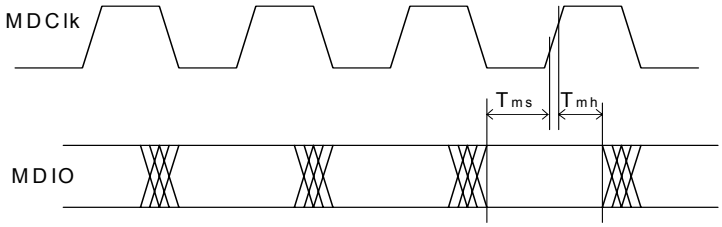
Symbol	Description	Min.	Typ.	Max.	Unit
T_{Tx_Clk}	Transmit clock period GMII	-	8	-	ns
T_{Tx_Clk}	Transmit clock period MII	-	40	-	ns
T_{dTx_Clk}	Tx_En, TxData to Tx_Clk rising delay	1	-	4	ns



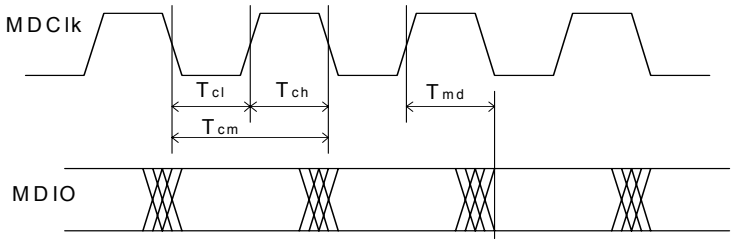
GMII / MII Transmit

11.3 PHY Management (MDIO) Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{ch}	MDCK High Time	-	300	-	ns
T_{cl}	MDCK Low Time	-	300	-	ns
T_{cm}	MDCK period	-	600	-	ns
T_{md}	MDIO output delay	-	-	50	ns
T_{mh}	MDIO hold time	10	-	-	ns



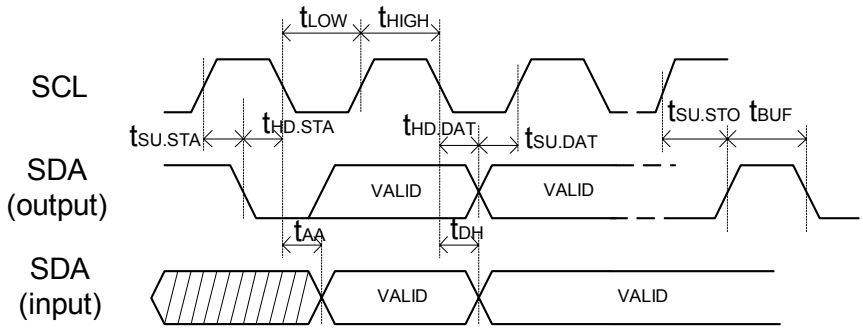
MDIO Write Cicle



MDIO Read Cicle

11.4 EEPROM Timing

Symbol	Description	Min.	Typ.	Max.	Unit
f_{SCL}	SCL frequency	-	66.6	-	KHz
t_{LOW}	Clock Pulse Width Low	10	-	-	us
t_{HIGH}	Clock Pulse Width High	10	-	-	us
t_{BUF}	Time the bus must be free before starting a new transmission	5	-	-	us
$t_{HD.STA}$	Start Hold Time	5	-	-	us
$t_{SU.STA}$	Start Setup Time	5	-	-	us
$t_{HD.DAT}$	Data Hold Time	5	-	-	us
$t_{SU.DAT}$	Data Setup Time	5	-	-	us
$t_{SU.STO}$	Stop Set-up Time	5	-	-	us
t_{AA}	Clock Low to Data Out Valid	-	-	4.9	us
t_{DH}	Data Out Hold Time	0	-	-	us



EEPROM Interface Timing

12 Electrical Specifications

12.1 ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the Recommended Operating Conditions section. Exposure to the Absolute Maximum Conditions for extended periods may affect device reliability.

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Supply Voltage	I/O	$V_{DDI/O}$	– 0.5	4.6	V
	Core	V_{DDCore}	– 0.5	2.5	V
Input Voltage		V_I	– 0.5	6	V
Output Voltage		V_O	– 0.5	6	V
Storage Temperature		T_{STG}	-65	+150	°C
Operation Temperature		T_{OPT}	0	70	°C
Latch-up Current		I_{LATCH}	>500		mA

Note: The maximum ratings are the limit value that must never be exceeded even for short time.

12.2 RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions represents recommended values that assure normal logic operation. As long as the device is used within the recommended operating conditions, the electrical characteristics (DC and AC characteristics) are guaranteed.

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	I/O	$V_{DDI/O}$	3.0	3.3	3.6	V
	Core	V_{DDCore}	1.95	2.0	2.05	V
Junction Temperature		T_j			125	°C
Low-level input voltage		V_{IL}	-0.5		1.0	V
High-level input voltage		V_{IH}	2.0		5.5	V

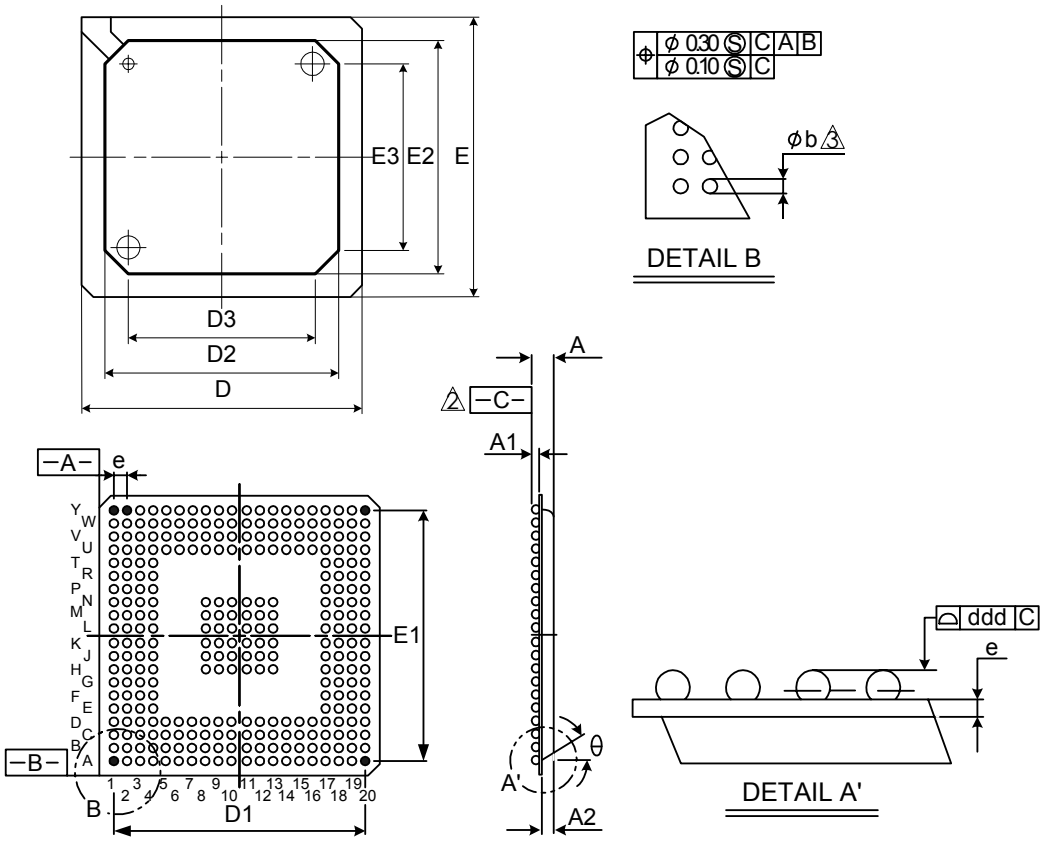
12.3 DC CHARACTERISTICS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Output low voltage	V_{OL}			0.4	V
Output high voltage	V_{OH}	2.4			V
Low level output current @VOL=0.4V	I_{OL}	8.8	14.1	17.0	mA
High level output current @VOH=2.4V	I_{OH}	12.8	25.7	40.0	mA
Input Treshold point	V_T	1.46	1.60	1.76	V
GMII Input (Schmitt trig.) Low to High treshold point *1	V_{T+}	1.66	1.75	1.79	V
GMII Input (Schmitt trig.) High to Low treshold point *1	V_{T-}	0.93	1.01	1.06	V
Input leakage current (High and Low)	I_I		+/-10	+/-1000	nA
Tri-state output leakage current (High and Low)	I_{OZ}		+/-10	+/-1000	nA
Pull-up resistor	R_{PU}	56	77	122	KΩ
Pull-down resistor	R_{PD}	51	69	127	KΩ

Note: *1 This refers to all inputs described as GMII in the Pin Listing section.

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13 Package Detail



Symbol	Dimensions In mm			Dimensions In inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	2.20	2.33	2.50	0.087	0.092	0.098
A1	------	0.60	------	------	0.024	------
A2	1.12	1.17	1.22	0.044	0.046	0.048
b	------	0.75	------	------	0.030	------
c	0.51	0.56	0.61	0.020	0.022	0.024
D	26.80	27.00	27.20	1.055	1.063	1.071
D1	------	24.13	------	------	0.950	------
D2	23.80	24.00	24.20	0.937	0.945	0.953
D3	17.95	18.00	18.05	0.707	0.709	0.711
E	26.80	27.00	27.20	1.055	1.063	1.071
E1	------	24.13	------	------	0.950	------
E2	23.80	24.00	24.20	0.937	0.945	0.953
E3	17.95	18.00	18.05	0.707	0.709	0.711
e	------	1.27	------	------	0.050	------
ddd	------	------	0.15	------	------	0.006
θ	30° TYP			30° TYP		

Note:
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25 mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.

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