Dual Channel 300mA Regulator + Reset IC

Features

- Low Quiescent Current : 110µA (No load)
- Low Dropout Voltage :
  V_{DROP1}=350mV@300mA
  V_{DROP2}=350mV@300mA
- Fixed Output Voltage :
  V_{OUT1}=3.3V/300mA
  V_{OUT2}=3.3V/300mA
- Stable with 2.2µF Output Capacitor
- Stable with Aluminum, Tantalum or Ceramic Capacitors
- Built in Thermal Protection
- Fast Transient Response
- Short Setting Time
- SOP-8, SOP-8-P with Thermal Pad Packages
- Adjustment-free Reset Detection Voltage :
  3.9V or 4.2V typ
- Easy to Set Delay Time from Voltage Detection to Reset Release

Applications

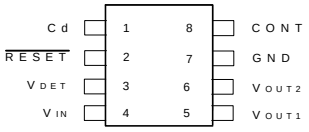
- CD-ROM drive.

General Description

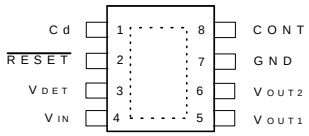
The APL5538 is a dual-channel regulator with reset function (specific voltage monitoring), and internal delay circuit, set to detect 3.9V or 4.2V. Maximum input voltage is 6V, output1 and output2 deliver up to 300mA. V_{OUT1} typical dropout voltage is 350mV at 300mA loading and V_{OUT2} typical dropout voltage is 350mV at 300mA loading. Design with an internal P-channel MOSFET pass transistor, the APL5538 maintains a low supply current. Other features include, thermal-shutdown protection, current limit protection to ensure specified output current. The APL5538 come in miniature SOP-8 and SOP-8-P packages.

Pinouts

SOP-8 Top View



SOP-8-P Top View



APL5538

= Thermal Pad
(connected to GND plane for better heat dissipation)

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

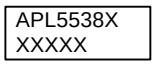
Ordering and Marking Information

APL5538 - □ □□-□□ □

- Lead Free Code
- Handling Code
- Temp. Range
- Package Code
- Detection Voltage

Package Code
K : SOP-8 KA : SOP-8-P
Temp. Range
C : 0 to 70 °C I : -40 to 85 °C
Handling Code
TR : Tape & Reel
Detection Voltage :
A : 3.9V B : 4.2V
Lead Free Code
L : Lead Free Device Blank : Orginal Device

APL5538 K / KA :



X - Detection Voltage
XXXXX - Date Code

Pin Description

PIN		I/O	Description
No.	Name		
1	Cd		Delay time capacitor pin, RESET pin output delay time can be set by the capacitor connected to the Cd pin. tPLH = 130000∗C, tPLH : transmission delay time (s), C:capacitor value (F)
2	$\overline{\text{RESET}}$	O	Input voltage detection output pin , low = V_{DET}<VS , high = V_{DET}>VS
3	V_{DET}	I	Input pin of voltage detection.
4	V_{IN}	I	Voltage supply input pin.
5	V_{OUT1}	O	Regulator output pin.
6	V_{OUT2}	O	Regulator output pin.
7	GND		GND pin
8	CONT	I	V_{OUT1} on/off-control pin, V_{OUT1} will be turn off when CONT pull to low.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{IN}, V_{OUT}	Input Voltage or Out Voltage	6.5	V
CONT	V_{OUT1} Shutdown Control Pin	6.5	V
V_{DET}	RESET Pin Supply Voltage	6.5	V
$R_{TH,JA}$	Thermal Resistance – Junction to Ambient SOP-8 SOP-8-P	 130 80	°C/W
$R_{TH,JC}$	Thermal Resistance – Junction to Case SOP-8 SOP-8-P	 30 5	°C/W
P_D	Power Dissipation	Internally Limited	W
T_J	Operating Junction Temperature Control Section Power Transistor	 0 to 125 0 to 150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (Soldering, 10 second)	260	°C

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Electrical Characteristics

Unless otherwise noted these specifications apply over full temperature , V_{IN}=5V, C_{IN}=1µF,C_{OUT1}=2.2µF, C_{OUT2}=2.2µF, CONT=V_{IN}, T_J=0 to 125°C . Typical values refer to T_J=25°C .

Symbol	Parameter	Test Conditions	APL5538			Unit
			Min.	Typ.	Max.	
V_{IN}	Input Voltage				6	V
I_Q	Quiescent Current	I_{OUT1} =0mA, I_{OUT2} =0mA		110	220	µA
	Shutdown Supply Current	CONT = low, I_{OUT2}=0mA		70	140	µA
I_{CONT}	Shutdown Input Bias current	V_{CONT} =V_{IN}			0.1	µA
V_{CONT}	High Threshold Voltage		1.6		V_{IN}+0.3	V
	Low Threshold Voltage		-0.3		0.4	
I_{CCQ}	V_{DET} Input Current	V_{DET} =5V		20	40	µA
Regulator1						
V_{OUT1}	Output Voltage	V_{IN}=5V	3.234	3.3	3.366	V
I_{LIMIT}	Circuit Current Limit	V_{IN}=5V		800		mA
I_{OUT}	Load Current		300			mA
REG_{LINE}	Line Regulation	V_{OUT}+0.5V< V_{IN}<6.0V, I_{OUT}=10mA		4	6	mV
REG_{LOAD}	Load Regulation	V_{IN} =5V, 0mA< I_{OUT} < I_{MAX}		20	60	mV
V_{DROP}	Dropout Voltage(Note) (VOUT(Nominal)=3.3V Version)	I_{OUT} =300mA		350	450	mV
PSRR	Ripple Rejection	F≤1kHz, 1Vpp at I_{OUT}=50mA	45	50		dB
OTS	Over Temperature Shutdown			150		°C
	Over Temperature Shutdown Hysteresis	Hysteresis		10		°C
TC	Output Voltage Temperature Coefficient	T_a= -20 ~ 80°C		100		ppm/°C
C_{OUT}	Output Capacitor			2.2		µF
	ESR		0.01		1	Ohm
Regulator2						
V_{OUT2}	Output Voltage	V_{IN}=5V	3.234	3.3	3.366	V
I_{LIMIT}	Circuit Current Limit	V_{IN}=5V		800		mA
I_{OUT}	Load Current		300			mA

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Electrical Characteristics (Cont.)

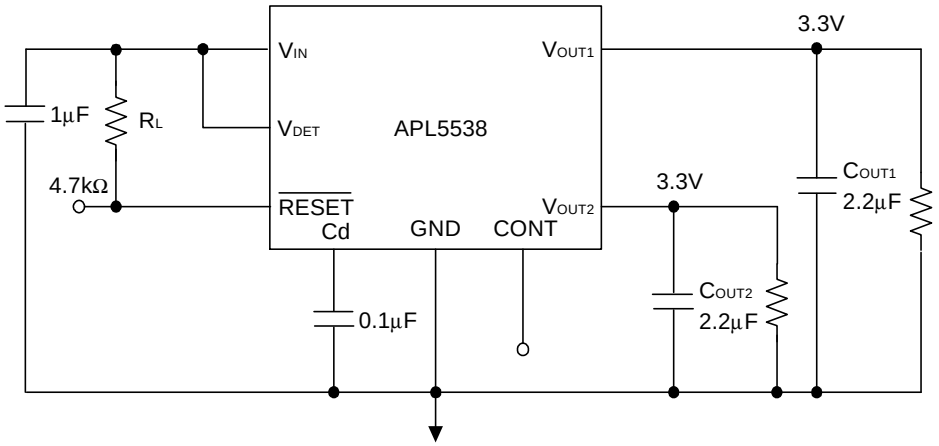
Unless otherwise noted these specifications apply over full temperature , V_{IN}=5V, C_{IN}=1µF,C_{OUT1}=2.2µF, C_{OUT2}=2.2µF, CONT=V_{IN}, T_J=0 to 125°C . Typical values refer to T_J=25°C .

Symbol	Parameter	Test Conditions	APL5538			Unit
			Min.	Typ.	Max.	
REG_{LINE}	Line Regulation	V_{OUT}+0.5V< V_{IN}<6.0V, I_{OUT}=10mA		4	6	mV
REG_{LOAD}	Load Regulation	V_{IN} =5V, 0mA< I_{OUT} < I_{MAX}		20	60	mV
V_{DROP}	Dropout Voltage(Note) (VOUT(Nominal)=3.3V Version)	I_{OUT} =300mA		350	450	mV
PSRR	Ripple Rejection	F≤1kHz, 1Vpp at I_{OUT}=50mA	45	50		dB
OTS	Over Temperature Shutdown			150		°C
	Over Temperature Shutdown Hysteresis	Hysteresis		10		°C
TC	Output Voltage Temperature Coefficient	T_a= -20 ~ 80°C		100		ppm/°C
C_{OUT}	Output Capacitor			2.2		µF
	ESR		0.01		1	Ohm
$\overline{RESET}$ / RESET						
VS	Detection Voltage	V_{DET}=H→L (APL5538A)	3.822	3.9	3.978	V
		V_{DET}=H→L (APL5538B)	4.116	4.2	4.284	
ΔVS/ΔT	Vs Temperature Coefficient	T_a = -20~+80°C		100		ppm/°C
ΔVS	Hysteresis Voltage	V_{DET} = H→L→H	100	150	200	mV
V_{OL}	Low-level Output Voltage	V_{DET} = 3.9V, R_L = 4.7kΩ		12	60	mV
I_{OH}	Output Leakage Current	V_{DET} = 5V		0.5	1	µA
I_{OL1}	Output Current1	V_{DET} =3.9V, V_{RESET} = 0.4V	25	30		mA
I_{OL2}	Output Current2	V_{DET} = 3.9V, V_{RESET} = 0.4V T_a = -20~+80°C	20	25		mA
t_{PLH}	"H" Transmission Delay Time	Cd = 0µF		42	90	µs
t_{PLH1}	Reset Delay Time	V_{DET} = 3.7V→5V, Cd = 0.1µF	8	13	18	ms
t_{PHL}	"L" Transmission Delay Time	Cd = 0µF		4	90	µs
V_{OPL}	Threshold Operating Voltage	V_{RESET} = 0.4V		0.95	1.25	V

Note : Dropout voltage definition : V_{IN}- V_{OUT} when V_{OUT} is 2% below the value of V_{OUT} for V_{IN}=5V

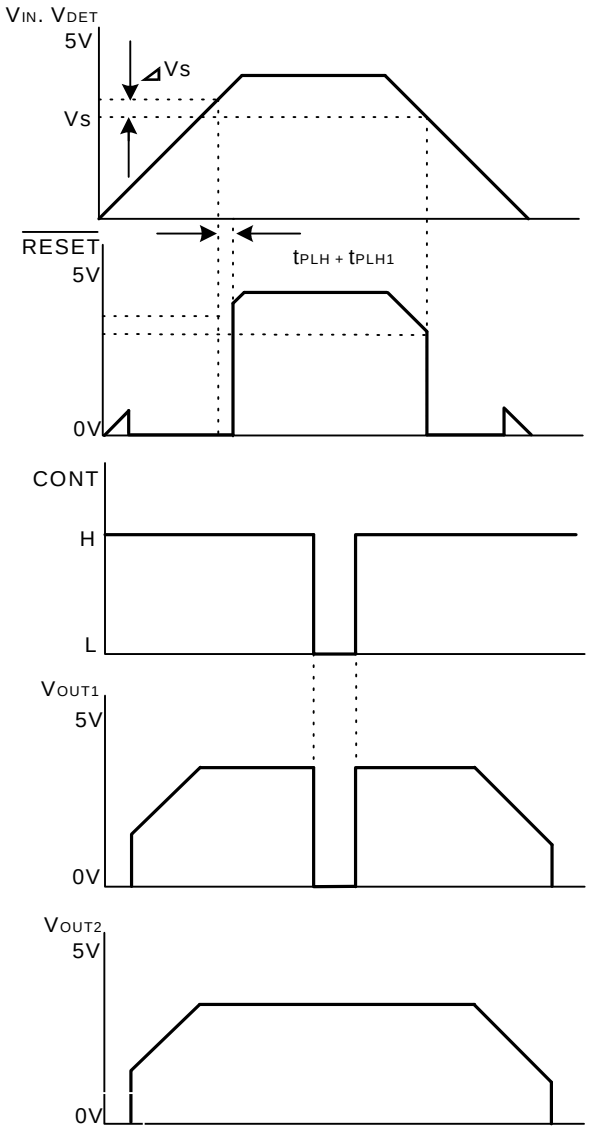
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Application Circuit



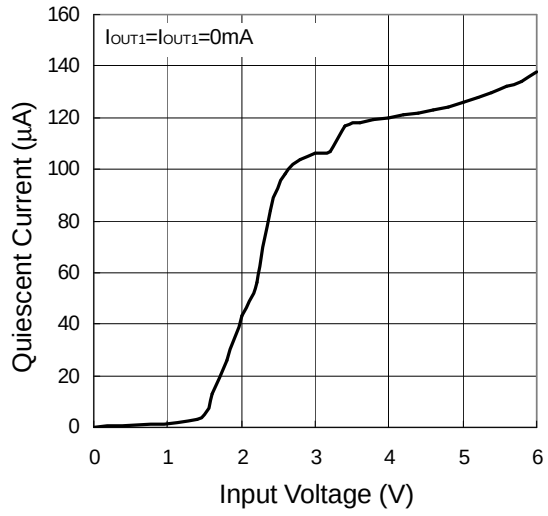
Timing Chart

APL5538

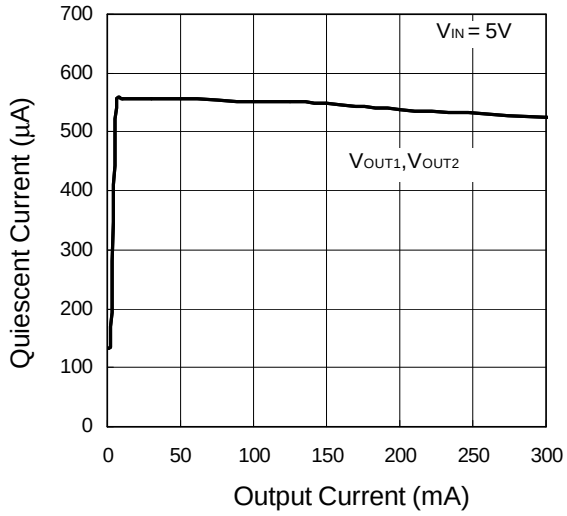


Typical Characteristics

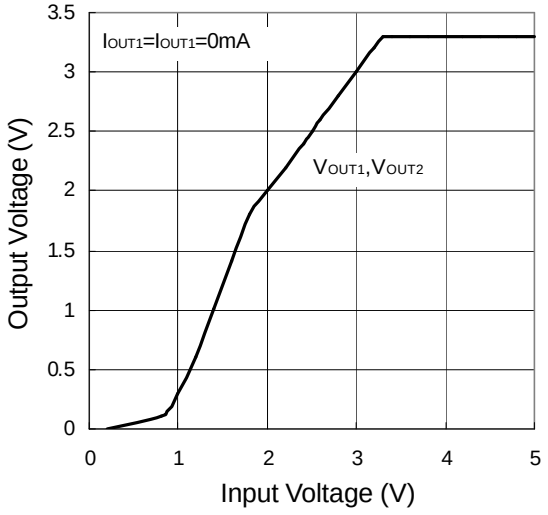
Quiescent Current vs. Input Voltage



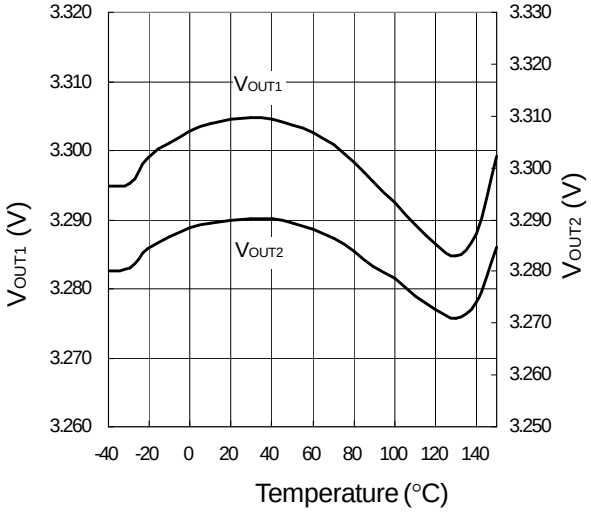
Quiescent Current vs. Output Current



Output Voltage vs. Input Voltage

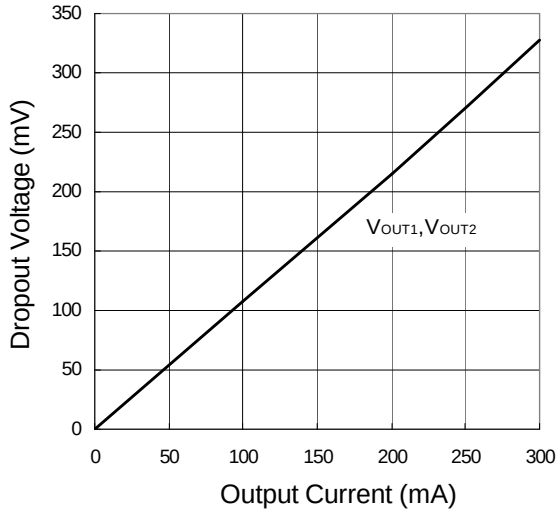


Output Voltage vs. Temperature

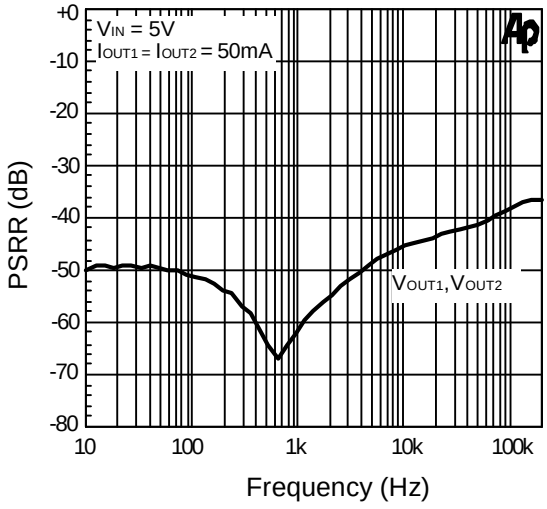


Typical Characteristics

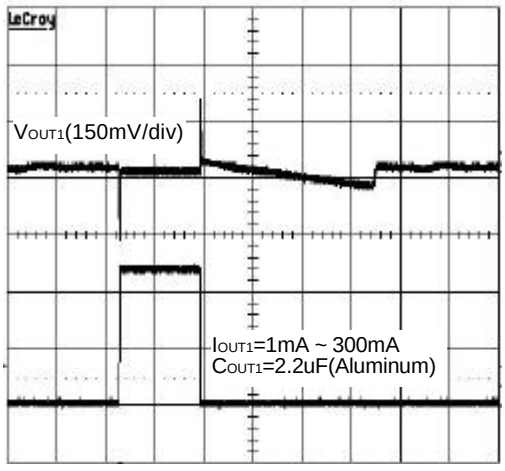
Dropout Voltage vs. Output Current



PSRR vs. Frequency

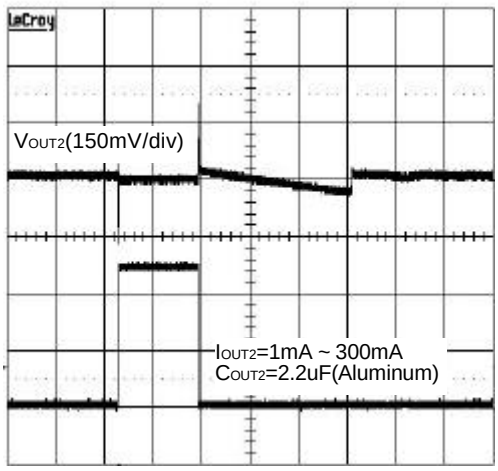


Load-Transient Response



Time (0.1ms/div)

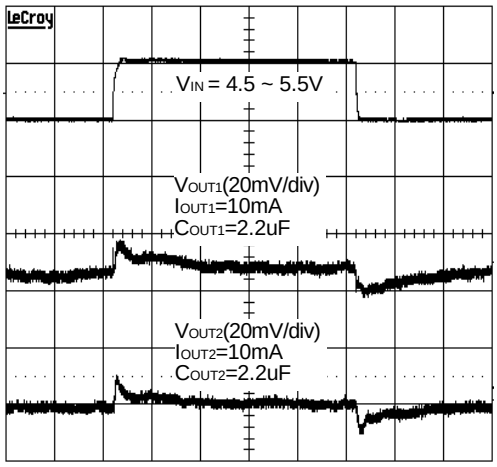
Load-Transient Response



Time(0.1ms/div)

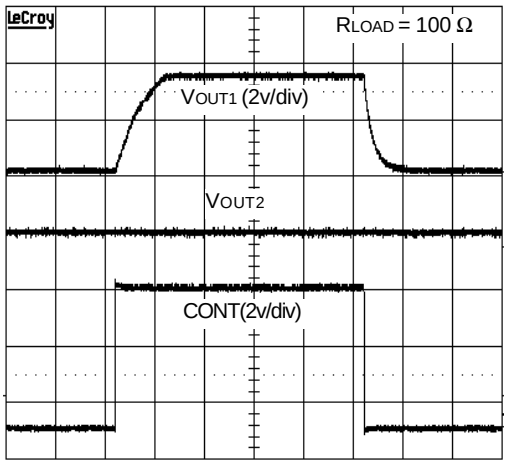
Typical Characteristics

Line-Transient Response



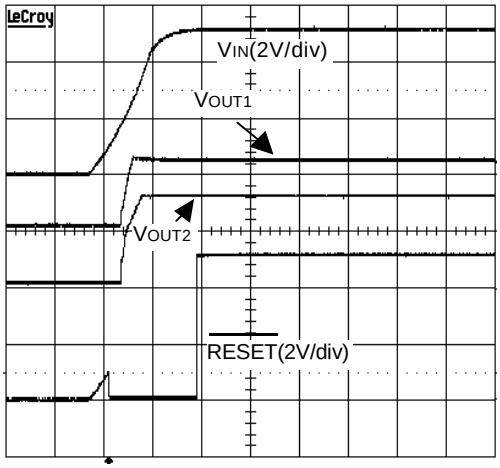
Time(20μs/div)

Shutdown Response



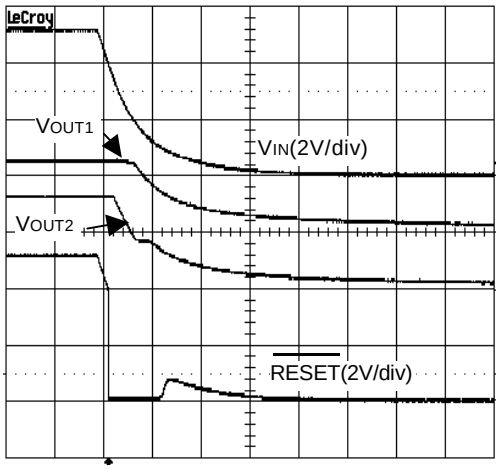
Time (1ms/div)

Powering On



Time(10ms/div)

Powering Off

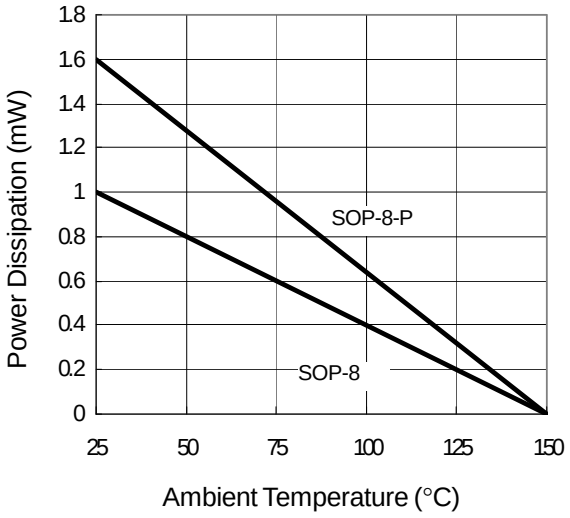


Time(0.2ms/div)

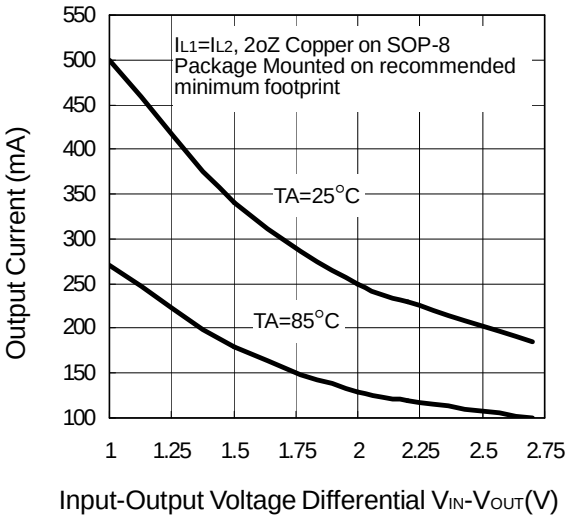
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Typical Characteristics

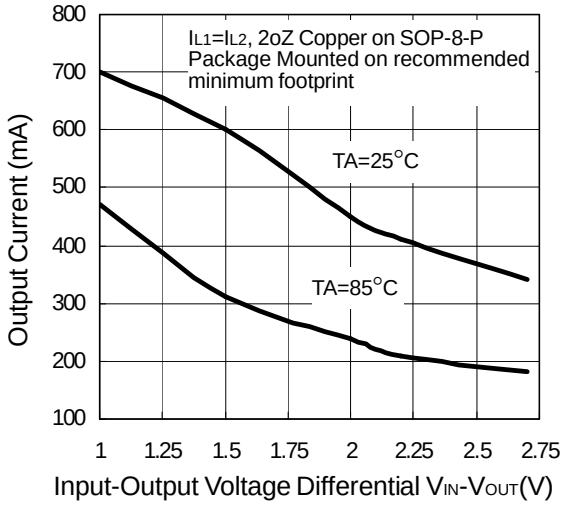
Power Dissipation vs. Ambient Temperature



Safe Operating Area (Power Dissipation Limit)



Safe Operating Area (Power Dissipation Limit)



Application Information

Capacitor Selection and Regulator Stability

The APL5538 uses at least a 1uF capacitor on the input. This capacitor can use Aluminum, Tantalum or Ceramic capacitors. Input capacitor with large value and low ESR provides better PSRR and line-transient response. The output capacitor also can use Aluminum, Tantalum or Ceramic capacitors, and it's minimum values is recommended 2.2uF, ESR muse be above 0.01Ω. Large output capacitor values can reduce noise and improve load-transient response, stability, and PSRR. Note that some ceramic dielectrics exhibit large capacitance and ESR variation with Temperature. If use this capacitor, it may be necessary to use 2.2uF or more to ensure stability at temperature below -10°C.

Load-Transient Considerations

The APL5538 load-transient response graphs in Typical Characteristics show the transient response. A step change in the load current from 1mA to 300mA at 1u second will cause less than 200mV transient spike. Large output capacitor's value and low ESR can reduce transient spike.

Shutdown/Enable

The APL5538 has an active high enable function. Force CONT high (>1.6V) enables the V_{OUT1} , CONT low (<0.4V) disables the V_{OUT1} and V_{OUT2} can not be affected by CONT. Enter the shutdown mode, it also causes the output voltage to discharge through a 500 Ω resistance to ground. In shutdown mode, the quiescent current can reduce to 100uA. The CONT pin cannot be floating, a floating CONT pin may cause an indeterminate state on the output. If it is no use, connect to V_{IN} for normal operation.

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ pin is asserted whenever V_{DET} falls below the reset threshold voltage or if CONT is forced low at some special IC(refer timing chart and pin description). The reset function ensures the microprocessor is properly reset and powers up into a known condition after a power failure. $\overline{\text{RESET}}$ will remain valid with V_{IN} as low as 0.95V. The $\overline{\text{RESET}}$ output is a simple open-drain N channel MOSET structure. A pull-up resistor must be used to pull this output up to some voltage. For most application, this voltage will be the same power supply that supplies V_{IN} to the APL5538. The APL5538 is relatively immune to negative-going glitches below the reset threshold. Typically reset delay time is 13ms while using o.1uF at Cd pin. If more transient immunity is needed, a Cd capacitor can be placed as larger as possible.

Input-Output (Dropout)Voltage

The minimun input-output voltage differential (dropout) determines the lowest usable supply voltage. The dropout voltage is a function of drain-to-source on resistance multiplied by the load current.

Current Limit

APL5538 includes two separate current-limit circuitry for each linear regulator. The current limit protection, which sense the current flows the P-channel MOSFET, and controls the output voltage. The point where limiting occurs is I_{OUT}=950mA. The output can be shorted to ground for an indefinite amount of time without damaging to the part.

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Application Information

Thermal Protection

Thermal protection limits total power dissipation in the APL5538. When the junction temperature exceeds T_J=+150°C, the thermal sensor generate a logic signal to turn off the pass transistor and let IC to cool. When the IC's junction temperature cools by 10°C, the thermal sensor will turn the pass transistor on again, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of fault conditions. For continual operation, do not exceed the absolute maximum junction temperature rating of T_J=+150°C.

Operating Region and Power Dissipation

The thermal resistance of the case and circuit board, ambient and junction air temperature, and the rate of air flow all control the APL5538 maximum power dissipation. The power dissipation across the device is $P = I_{OUT}(V_{IN}-V_{OUT})$. The maximum power dissipation is:

$P_{MAX} = (T_J-T_A) / (\theta_{JB} +\theta_{BA})$

where T_J-T_A is the temperature difference between the junction and ambient air.

θ_{JB} is the thermal resistance of the package, θ_{BA} is the thermal resistance through the printed circuit board, copper traces, and other materials to the surrounding air. The GND pin provides an electrical connection to ground and channeling heat away. Connect the GND pin to ground using a large pad or ground plane as a heat sink, it can improve maximize thermal dissipation.

See figure 1. The SOP-8-P utilizes a bottom thermal pad to minimize the thermal resistance of the package, making the package suitable for high current applications. The thermal pad is soldered to the top ground pad and is connected to the internal or bottom ground plane by several vias. The printed circuit board (PCB) forms a heat sink and dissipates most of the heat into ambient air. The vias are recommended to have proper size to retain solder, helping heat conduction.

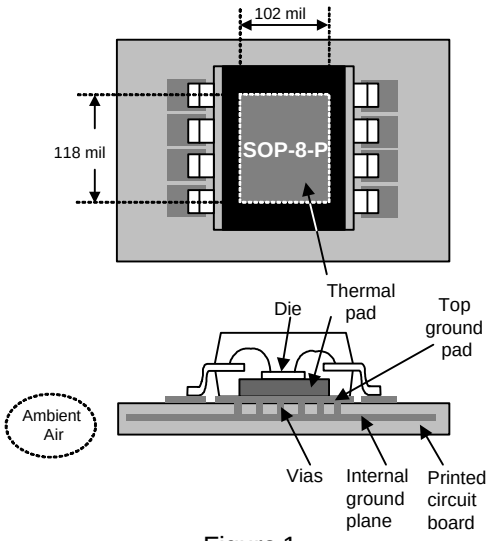
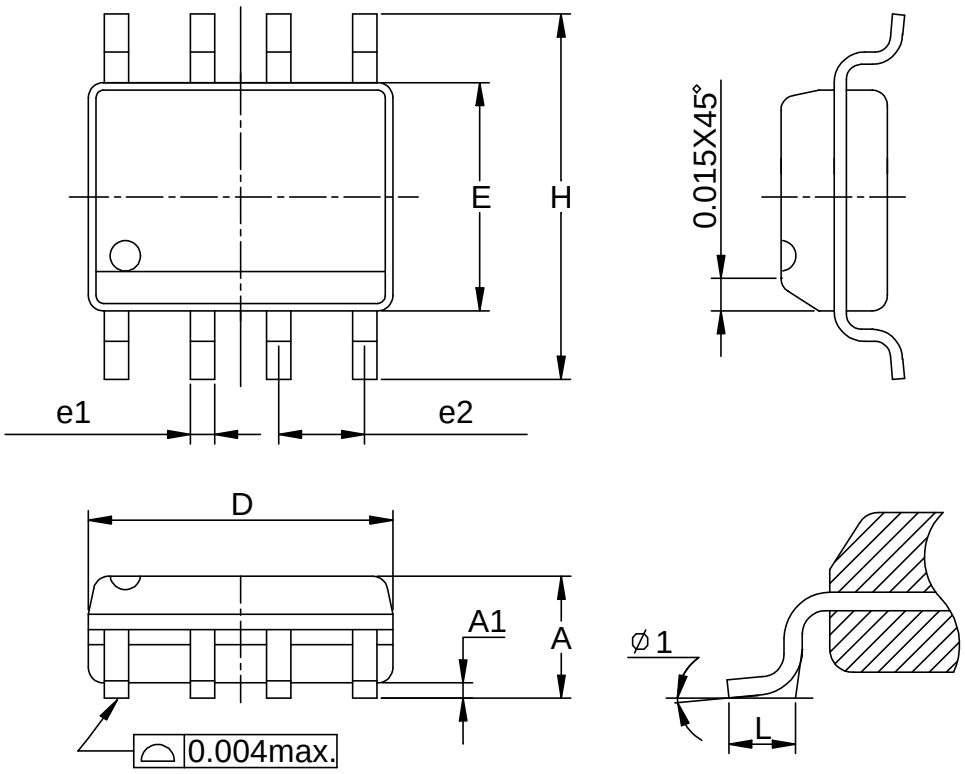


Figure 1

Packaging Information

SOP-8 pin (Reference JEDEC Registration MS-012)

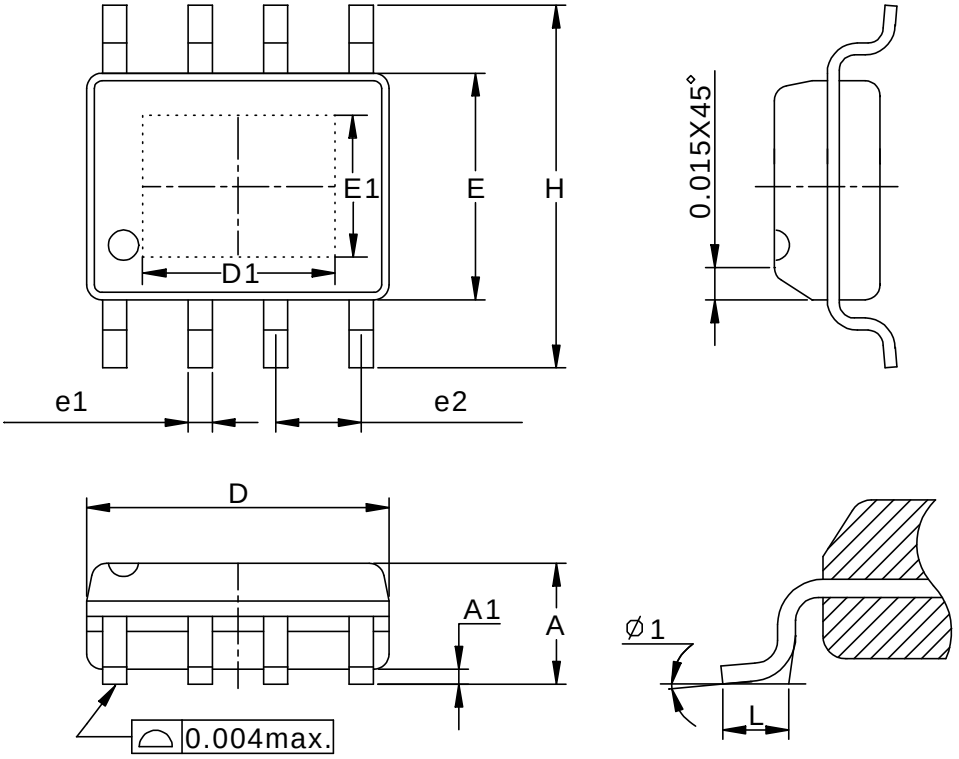


Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
ϕ 1	8°		8°	

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Packaging Information

SOP-8-P pin (Reference JEDEC Registration MS-012)



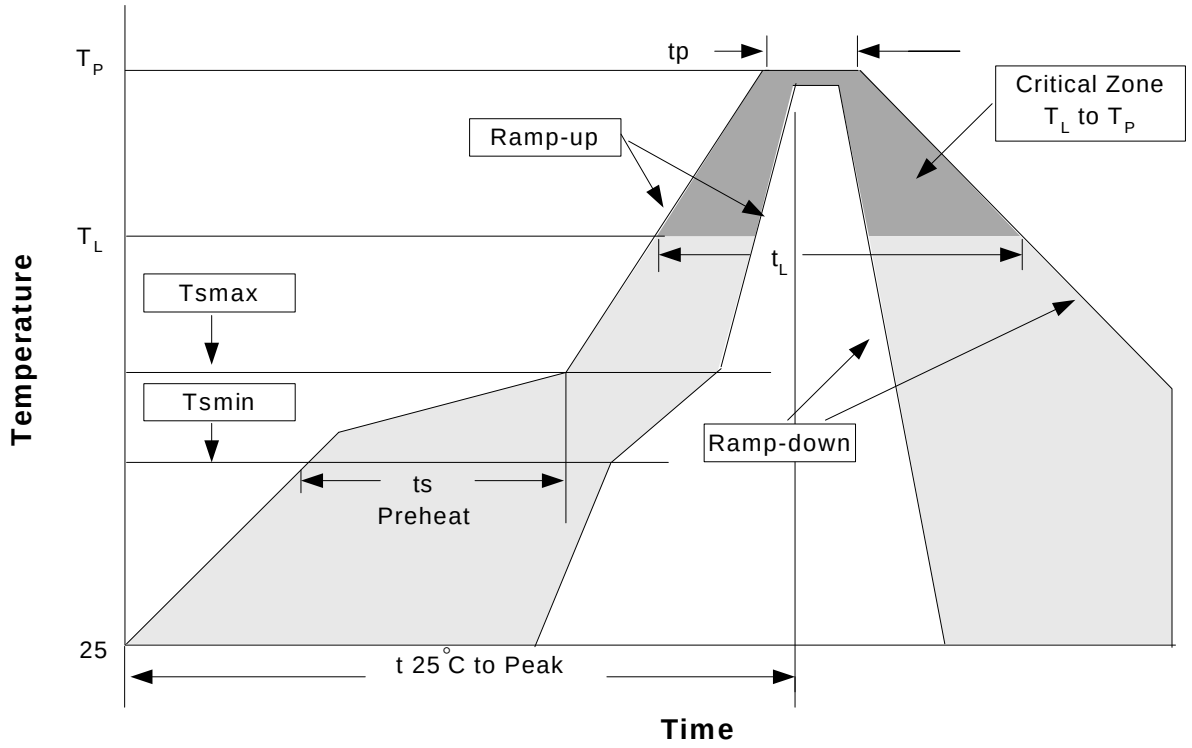
Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0	0.15	0	0.006
D	4.80	5.00	0.189	0.197
D1	3.00REF		0.118REF	
E	3.80	4.00	0.150	0.157
E1	2.60REF		0.102REF	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
ϕ 1	8°		8°	

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Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



ClassificatinReflowProfiles

Profile Feature	Sn-Pb Eutectic Assembly		Pb-Free Assembly	
	Large Body	Small Body	Large Body	Small Body
Average ramp-up rate (T_L to T_P)	3°C/second max.		3°C/second max.	
Preheat - Temperature Min (Tsmin) - Temperature Mix (Tsmax) - Time (min to max)(ts)	100°C 150°C 60-120 seconds		150°C 200°C 60-180 seconds	
Tsmax to T_L - Ramp-up Rate			3°C/second max	
Tsmax to T_L - Temperature(T_L) - Time (t_L)	183°C 60-150 seconds		217°C 60-150 seconds	
Peak Temperature(Tp)	225 +0/-5°C	240 +0/-5°C	245 +0/-5°C	250 +0/-5°C
Time within 5°C of actual Peak Temperature(tp)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.		6°C/second max.	
Time 25°C to Peak Temperature	6 minutes max.		8 minutes max.	

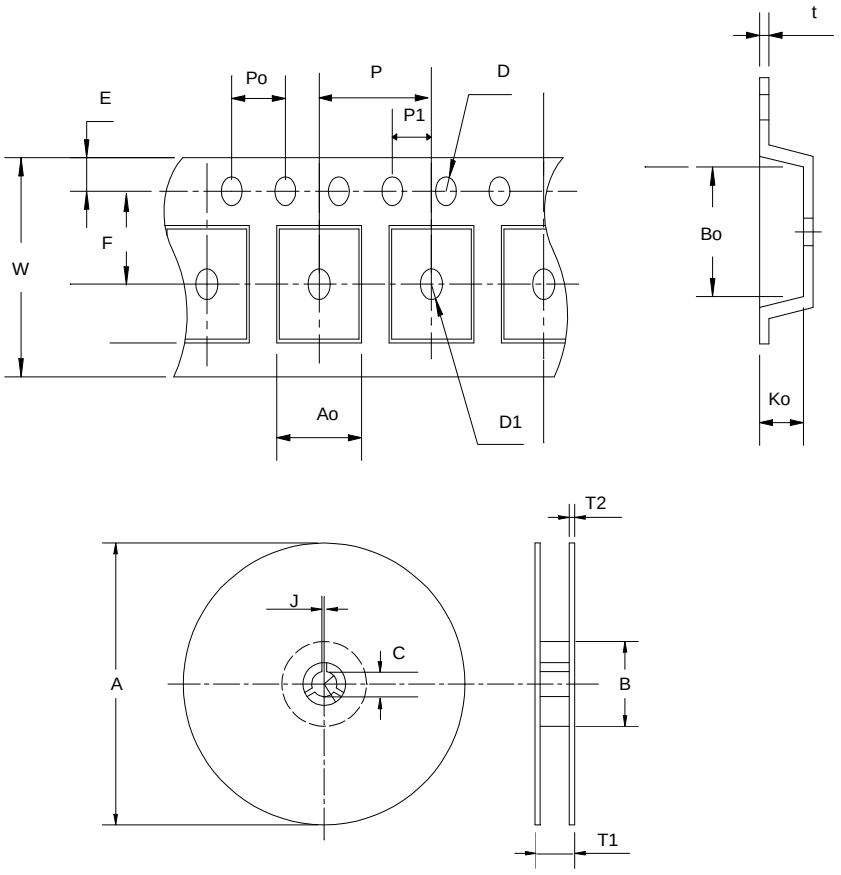
Note: All temperatures refer to topside of the package. Measured on the body surface.

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Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I_{tr} > 100mA

Carrier Tape



Application	A	B	C	J	T1	T2	W	P	E
SOP- 8/-P	330 ± 1	62 +1.5	12.75+ 0.15	2 ± 0.5	12.4 ± 0.2	2 ± 0.2	12± 0. 3	8± 0.1	1.75±0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5± 1	1.55 +0.1	1.55+ 0.25	4.0 ± 0.1	2.0 ± 0.1	6.4 ± 0.1	5.2± 0. 1	2.1± 0.1	0.3±0.013

(mm)

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Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 8/-P	12	9.3	2500

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