

- ◇ STRUCTURE Silicon Monolithic Integrated Circuit
- ◇ PRODUCT SPI BUS 32Kbit (4,096 × 8bit) EEPROM
- ◇ PART NUMBER BR25L320-W Series

| PART NUMBER | PACKAGE |
|--------------|---------|
| BR25L320F-W | SOP8 |
| BR25L320FJ-W | SOP-J8 |

- ◇ FEATURES Serial Peripheral Interface
 Single power supply (1.8V~5.5V)
 1,000,000 erase/write cycles endurance

◇ ABSOLUTE MAXIMUM RATING (Ta=25°C)

| Parameter | Symbol | Rating | Unit |
|-----------------------|--------|-----------------------|------|
| Supply Voltage | Vcc | -0.3~6.5 | V |
| Power Dissipation | Pd | 450 (BR25L320F-W) *1 | mW |
| | | 450 (BR25L320FJ-W) *2 | |
| Storage Temperature | Tstg | -65~125 | °C |
| Operating Temperature | Topr | -40~85 | °C |
| Terminal Voltage | — | -0.3~Vcc+0.3 | V |

* Degradation is done at 4.5mW/°C (*1,2) for operation above 25°C

◇ RECOMMENDED OPERATING CONDITION

| Parameter | Symbol | Rating | Unit |
|----------------|--------|---------|------|
| Supply Voltage | Vcc | 1.8~5.5 | V |
| Input Voltage | VIN | 0~Vcc | V |

Status of this document

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

◇MEMORY CELL CHARACTERISTICS(Ta=25°C, Vcc=1.8~5.5V)

| Parameter | | Specification | | | Unit |
|-------------------|----|---------------|------|------|-------|
| | | Min. | Typ. | Max. | |
| Write/Erase Cycle | *1 | 1,000,000 | - | - | Cycle |
| Data Retention | *1 | 40 | - | - | Year |

○Initial Data:Memory array FFh, Status Register WPEN:0, BP1:0, BP0:0
*1 Not 100% TESTED

◇ DC OPERATING CHARACTERISTICS

(Unless otherwise specified Ta=-40~85°C, Vcc=1.8~5.5V)

| Parameter | Symbol | Specification | | | Unit | test condition |
|-------------------------|--------|---------------|------|---------|------|--|
| | | Min. | Typ. | Max. | | |
| "H" Input Voltage1 | VIH1 | 0.7xVcc | - | Vcc+0.3 | V | 1.8V ≤ Vcc ≤ 5.5V |
| "L" Input Voltage1 | VIL1 | -0.3 | - | 0.3xVcc | V | 1.8V ≤ Vcc ≤ 5.5V |
| "L" Output Voltage1 | VOL1 | 0 | - | 0.4 | V | IOL=2.1mA (Vcc=2.5V~5.5V) |
| "L" Output Voltage2 | VOL2 | 0 | - | 0.2 | V | IOL=150 μA (Vcc=1.8V~5.5V) |
| "H" Output Voltage1 | VOH1 | Vcc-0.5 | - | Vcc | V | IOH=-0.4mA (Vcc=2.5V~5.5V) |
| "H" Output Voltage2 | VOH2 | Vcc-0.2 | - | Vcc | V | IOH=-100 μA (Vcc=1.8V~5.5V) |
| Input Leakage Current | ILI | -1 | - | 1 | μA | VIN=0V~Vcc |
| Output Leakage Current | ILO | -1 | - | 1 | μA | VOU=0V~Vcc, CSB=Vcc |
| Operating Current Write | ICC1 | - | - | 1 | mA | Vcc=1.8V, fSCK=2MHz, tE/W=5ms Byte Write, Page Write, Write Status Register |
| | ICC2 | - | - | 2 | mA | Vcc=2.5V, fSCK=5MHz, tE/W=5ms Byte Write, Page Write, Write Status Register |
| | ICC3 | - | - | 3 | mA | Vcc=5.5V, fSCK=5MHz, tE/W=5ms Byte Write, Page Write, Write Status Register |
| Operating Current Read | ICC4 | - | - | 1.5 | mA | Vcc=2.5V, fSCK=5MHz Read, Read Status Register |
| | ICC5 | - | - | 2 | mA | Vcc=5.5V, fSCK=5MHz Read, Read Status Register |
| Standby Current | ISB | - | - | 2 | μA | Vcc=5.5V CS=HOLD=WP=Vcc SCK=SI=Vcc or GND, SO=OPEN |

○This product is not designed for protection against radioactive rays.

◇ AC OPERATING CHARACTERISTICS

(Unless otherwise specified Ta=-40~85°C, CL=100pF)

| Parameter | Symbol | 1.8V ≤ Vcc ≤ 2.5V | | | 2.5V ≤ Vcc ≤ 5.5V | | | Unit |
|--|--------|-------------------|------|------|-------------------|------|------|------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| SCK clock Frequency | fSCK | - | - | 2 | - | - | 5 | MHz |
| SCK High Time | tSCKWH | 200 | - | - | 85 | - | - | ns |
| SCK Low Time | tSCKWL | 200 | - | - | 85 | - | - | ns |
| CS High Time | tCS | 200 | - | - | 85 | - | - | ns |
| CS Setup Time | tCSS | 200 | - | - | 90 | - | - | ns |
| CS Hold Time | tCSH | 200 | - | - | 85 | - | - | ns |
| SCK Setup Time | tSCKS | 200 | - | - | 90 | - | - | ns |
| SCK Hold Time | tSCKH | 200 | - | - | 90 | - | - | ns |
| SI Setup Time | tDIS | 40 | - | - | 20 | - | - | ns |
| SI Hold Time | tDIH | 50 | - | - | 40 | - | - | ns |
| Output Data Delay Time1 | tPD1 | - | - | 150 | - | - | 70 | ns |
| Output Data Delay Time2 (CL=30pF) | tPD2 | - | - | 145 | - | - | 55 | ns |
| Output Hold Time | tOH | 0 | - | - | 0 | - | - | ns |
| Output Disable Time | tOZ | - | - | 250 | - | - | 100 | ns |
| Clock High Setup Time before HOLD Active | tHFS | 120 | - | - | 60 | - | - | ns |
| Clock Low Hold Time after HOLD Active | tHFH | 90 | - | - | 40 | - | - | ns |
| Clock High Setup Time before HOLD not Active | tHRS | 120 | - | - | 60 | - | - | ns |
| Clock Low Hold Time after HOLD not Active | tHRH | 140 | - | - | 70 | - | - | ns |
| HOLD to Output High-Z | tHOZ | - | - | 250 | - | - | 100 | ns |
| HOLD to Output Valid | tHPD | - | - | 150 | - | - | 70 | ns |
| SCK Rise Time | *1 tRC | - | - | 1 | - | - | 1 | μs |
| SCK Fall Time | *1 tFC | - | - | 1 | - | - | 1 | μs |
| Output Rise Time | *1 tRO | - | - | 100 | - | - | 50 | ns |
| Output Fall Time | *1 tFO | - | - | 100 | - | - | 50 | ns |
| Write Cycle Time | tE/W | - | - | 5 | - | - | 5 | ms |

*1 Not 100% TESTED

◇ BLOCK DIAGRAM

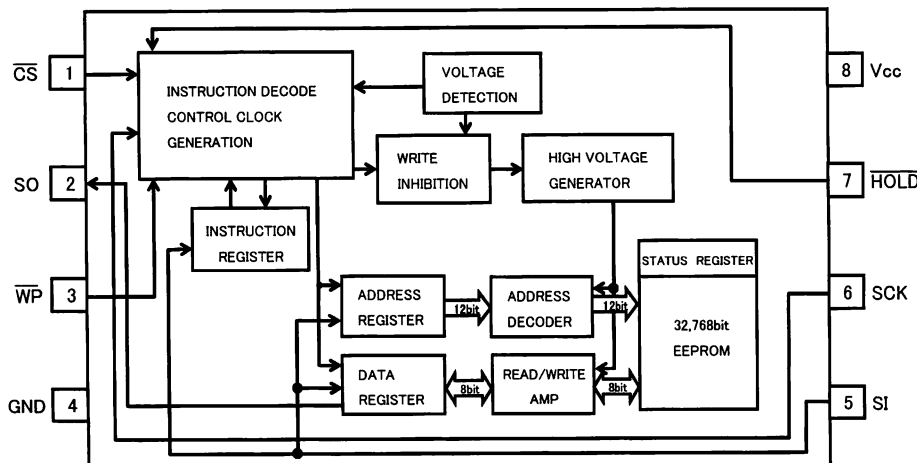


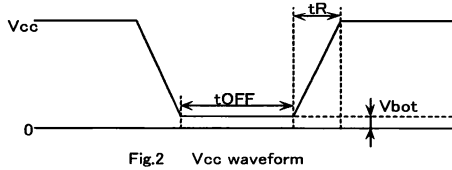
Fig.1 BLOCK DIAGRAM

◇ PIN No. / PIN NAME

| PIN No. | PIN NAME |
|---------|----------|
| 1 | CS |
| 2 | SO |
| 3 | WP |
| 4 | GND |
| 5 | SI |
| 6 | SCK |
| 7 | HOLD |
| 8 | Vcc |

◇NOTES FOR POWER SUPPLY

In order to prevent an inadvertent write, the device has the feature of P.O.R.
 After the power is on, the device is in the write disable mode. P.O.R. works only during power up. The noise may force the device write enable mode with \overline{CS} ="H" during power ON/OFF. In the case of power up, keep the following conditions to ensure to make the function of P.O.R.



◇RECOMMENDED CONDITIONS OF tR, tOFF, Vbot

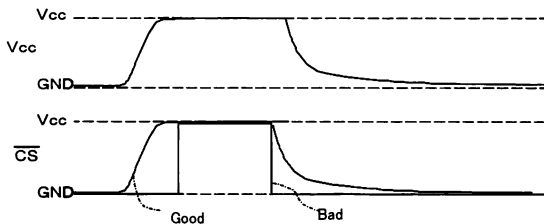
| tR | tOFF | Vbot |
|-------------|------------|------------|
| Below 10ms | Above 10ms | Below 0.3V |
| Below 100ms | Above 10ms | Below 0.2V |

Please keep \overline{CS} "H" during power ON/OFF.

The device is an active state during \overline{CS} is low. The extraordinary function or data collaption may occur because of noise etc., if power-up is done with \overline{CS} "L". In order to prevent above errors from happening, keep \overline{CS} "H" (=Vcc) during power ON. (The device does not receive any command during \overline{CS} is high.)

It may continue at low Vcc by capacitance of Vcc line during power off.

Please keep \overline{CS} "H" during power off because of the device may make malfunction and inadvertent write.



(Good example)
 \overline{CS} follows Vcc. (\overline{CS} is pull up to Vcc)

(Bad example)
 \overline{CS} is low during power ON/OFF.

Please take more than 10ms between power ON and power OFF, or the internal circuit is not always reset.

Fig.3 \overline{CS} TIMING DURING POWER ON/OFF

◇CAUTIONS ON USE

(1) Absolute maximum ratings

If the absolute maximum ratings such as impressed voltage and operating temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(2) GND electric potential

Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltages is lower than that of GND terminal.

(3) Heat design

In consideration of permissible dissipation in actual use condition, carry out heat design with sufficient margin.

(4) Terminal to terminal shortcircuit and wrong packaging

When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(5) Strong electromagnetic field

Use in a strong electromagnetic field may cause malfunction, therefore, evaluated design sufficiently.

◇PHYSICAL DIMENSION

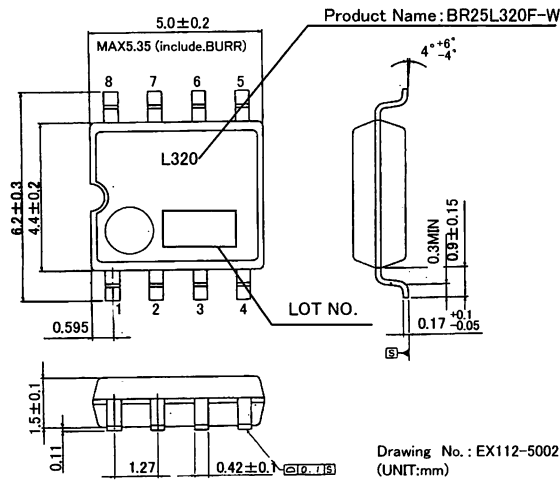


Fig4-(a) PHYSICAL DIMENSION
SOP-8 (BR25L320F-W)

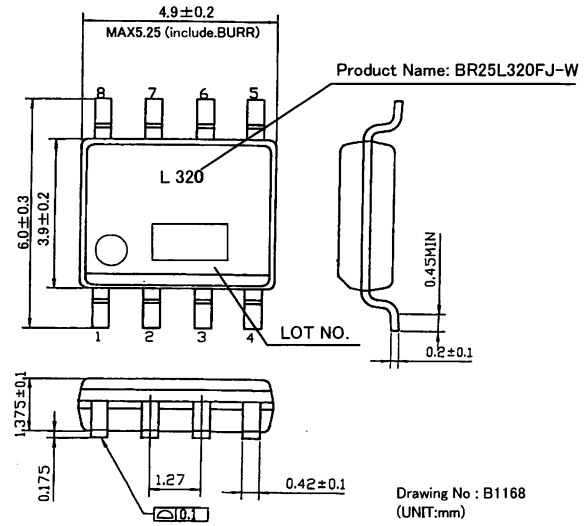


Fig4-(b) PHYSICAL DIMENSION
SOP-J8 (BR25L320FJ-W)

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