

ADC Architectures IV: Sigma-Delta ADC Advanced Concepts and Applications

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INTRODUCTION

[Tutorial MT-022](#) discussed the basics of Σ - Δ ADCs. In this tutorial, we will look at some of the more advanced concepts including idle tones, multi-bit Σ - Δ , MASH, bandpass Σ - Δ , as well as some example applications.

IDLE TONE CONSIDERATIONS

In our discussion of Σ - Δ ADCs up to this point, we have made the assumption that the quantization noise produced by the Σ - Δ modulator (see Figure 1) is random and uncorrelated with the input signal. Unfortunately, this is not entirely the case, especially for the first-order modulator. Consider the case where we are averaging 16 samples of the modulator output in a 4-bit Σ - Δ ADC.

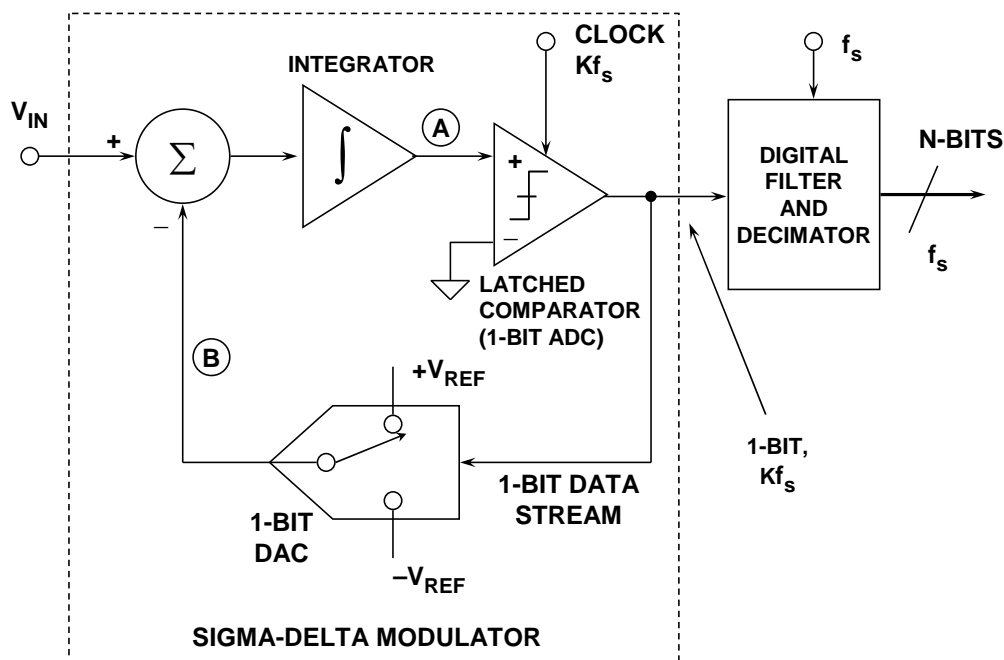


Figure 1: First-Order Sigma-Delta ADC

Figure 2 shows the bit pattern for two input signal conditions: an input signal having the value $8/16$, and an input signal having the value $9/16$. In the case of the $9/16$ signal, the modulator output bit pattern has an extra "1" every 16th output. This will produce energy at $Kf_s/16$, which translates into an unwanted tone. If the oversampling ratio (K) is less than 8, this tone will fall

into the passband. In audio, the idle tones can be heard just above the noise floor as the input changes from negative to positive fullscale.

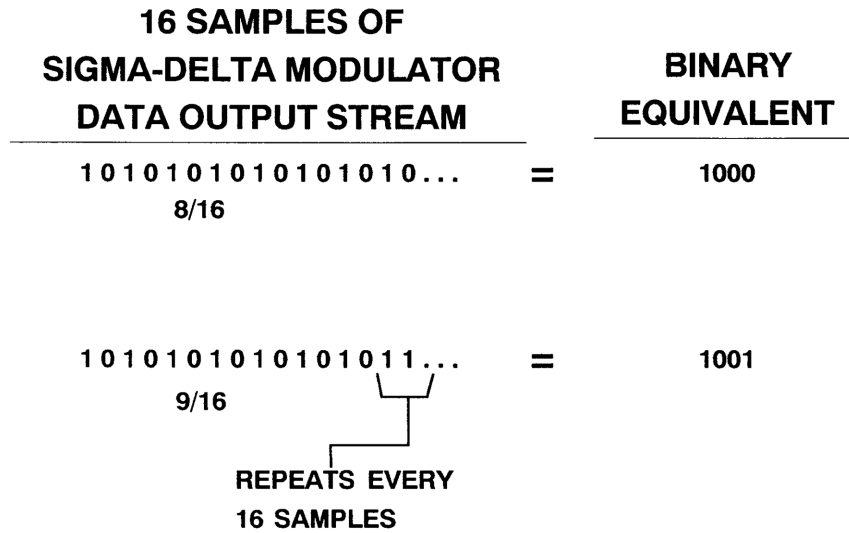


Figure 2: Repetitive Bit Pattern in Sigma-Delta Modulator Output

Figure 3 shows the correlated idling pattern behavior for a first order Σ - Δ modulator, and Figure 4 shows the relatively uncorrelated pattern for a second-order modulator. For this reason, virtually all Σ - Δ ADCs contain at least a second-order modulator loop, and some use up to fifth-order loops.

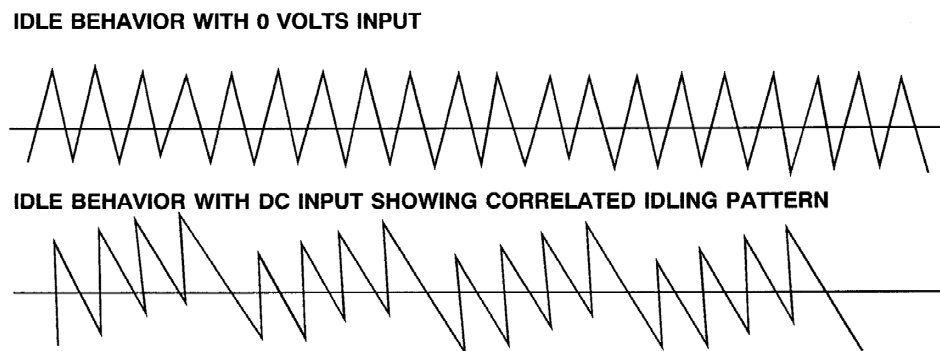


Figure 3: Idling Patterns for First-Order Sigma-Delta Modulator (Integrator Output)

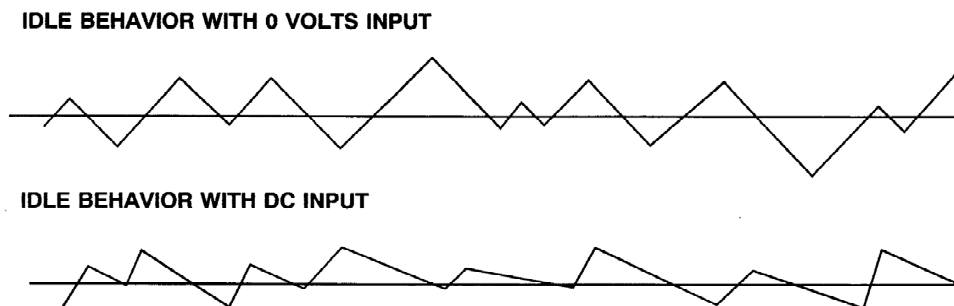


Figure 4: Idling Patterns for Second-Order Sigma-Delta Modulator (Integrator Output)

HIGHER ORDER LOOP CONSIDERATIONS

In order to achieve wide dynamic range, Σ - Δ modulator loops greater than second-order are necessary, but present real design challenges. First of all, the simple linear models previously discussed are no longer fully accurate. Loops of order greater than two are generally not guaranteed to be stable under all input conditions. The instability arises because the comparator is a nonlinear element whose effective "gain" varies inversely with the input level. This mechanism for instability causes the following behavior: if the loop is operating normally, and a large signal is applied to the input that overloads the loop, the average gain of the comparator is reduced. The reduction in comparator gain in the linear model causes loop instability. This causes instability even when the signal that caused it is removed.

In actual practice, such a circuit would normally oscillate on power-up due to initial conditions caused by turn-on transients. The [AD1879](#) dual audio ADC released in 1994 by Analog Devices used a 5th order loop. Extensive nonlinear stabilization techniques were required in this and similar higher-order loop designs (References 1-5).

MULTI-BIT SIGMA-DELTA CONVERTERS

So far we have considered only Σ - Δ converters which contain a single-bit ADC (comparator) and a single-bit DAC (switch). The block diagram of Figure 5 shows a multi-bit Σ - Δ ADC which uses an n-bit flash ADC and an n-bit DAC. Obviously, this architecture will give a higher dynamic range for a given oversampling ratio and order of loop filter. Stabilization is easier, since second-order loops can generally be used. Idling patterns tend to be more random thereby minimizing tonal effects.

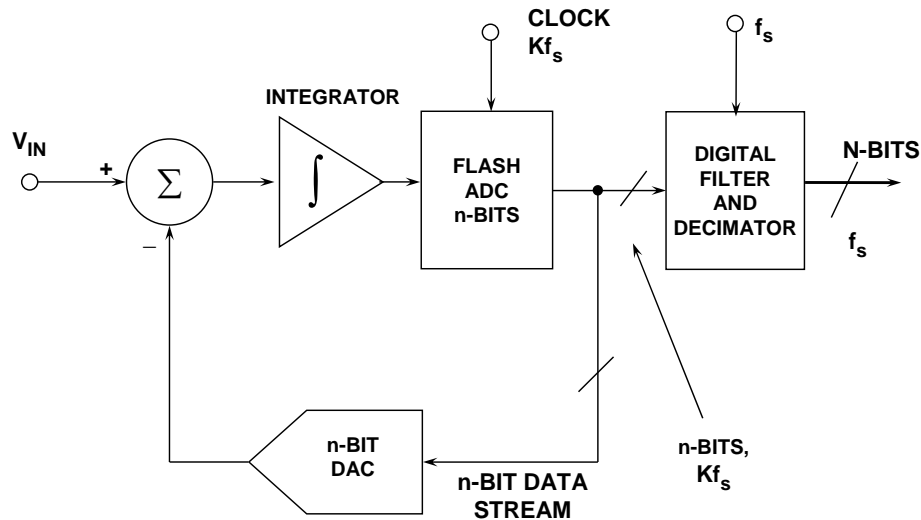


Figure 5: Multi-Bit Sigma-Delta ADC

The real disadvantage of this technique is that the linearity depends on the DAC linearity, and thin film laser trimming is required to approach 16-bit performance levels. This makes the multi-bit architecture extremely impractical to implement on mixed-signal ICs using traditional binary DAC techniques.

However, fully decoded thermometer DACs (see [Tutorial MT-014](#)) coupled with proprietary data scrambling techniques as used in a number of Analog Devices' audio ADCs and DACs, including the 24-bit stereo [AD1871](#) (see References 6 and 7) can achieve high SNR and low distortion using the multi-bit architecture. The multi-bit data scrambling technique both minimizes idle tones and ensures better differential linearity. A simplified block diagram of the AD1871 ADC is shown in Figure 6.

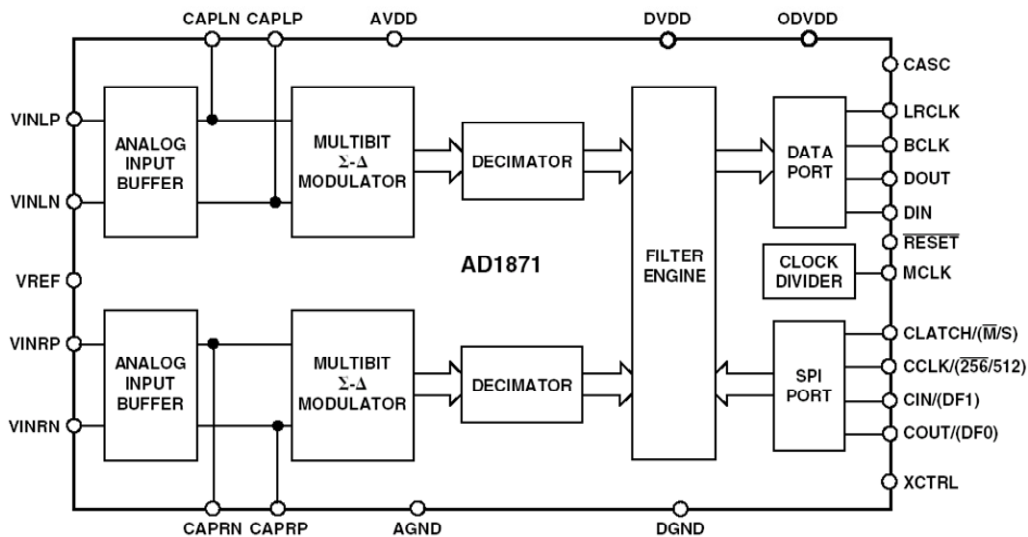


Figure 6: [AD1871](#) 24-Bit 96-kSPS Stereo Audio Multi-Bit Sigma-Delta ADC

The AD1871's analog Σ - Δ modulator section comprises a second order multi-bit implementation using Analog Device's proprietary technology for best performance. As shown in Figure 7, the two analog integrator blocks are followed by a flash ADC section that generates the multi-bit samples.

The output of the flash ADC, which is thermometer encoded, is decoded to binary for output to the filter sections and is scrambled for feedback to the two integrator stages. The modulator is optimized for operation at a sampling rate of 6.144 MHz (which is $128 \times f_s$ at 48-kHz sampling and $64 \times f_s$ at 96-kHz sampling). The A-weighted dynamic range of the AD1871 is typically 105 dB.

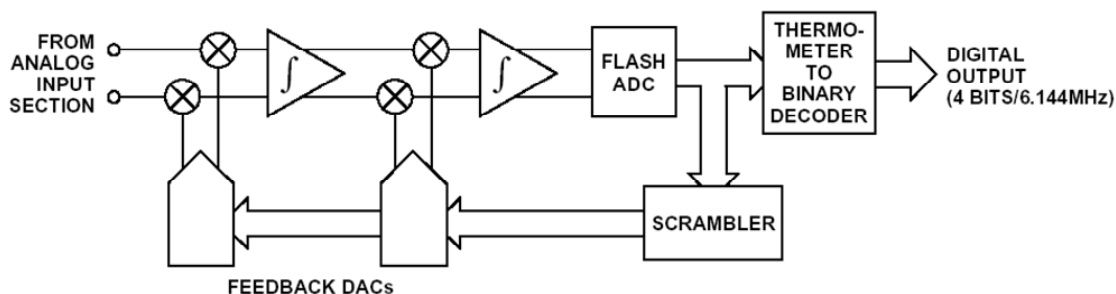


Figure 7: Details of the AD1871 Second-Order Modulator and Data Scrambler

DIGITAL FILTER IMPLICATIONS ON MULTIPLEXED APPLICATIONS

The digital filter is an integral part of all Σ - Δ ADCs—there is no way to remove it. The settling time of this filter affects certain applications especially when using Σ - Δ ADCs in multiplexed applications. The output of a multiplexer can present a step function input to an ADC if there are different input voltages on adjacent channels. In fact, the multiplexer output can represent a full-scale step voltage to the Σ - Δ ADC when channels are switched. Adequate filter settling time must be allowed, therefore, in such applications. This does not mean that Σ - Δ ADCs shouldn't be used in multiplexed applications, just that the settling time of the digital filter must be considered. Some newer Σ - Δ ADCs such are actually optimized for use in multiplexed applications.

For example, the group delay through the AD1871 digital filter is 910 μ s (sampling at 48 kSPS) and 460 μ s (sampling at 96 kSPS)—this represents the time it takes for a step function input to propagate through one-half the number of taps in the digital filter. The total settling time is therefore approximately twice the group delay time. The input oversampling frequency is 6.144 MSPS for both conditions. The frequency response of the digital filter in the AD1871 ADC is shown in Figure 8. This filter uses a finite impulse response (FIR) design, and therefore has linear phase over the audio passband. Duplicating this performance using an analog filter would require considerable design effort as well as rather costly components.

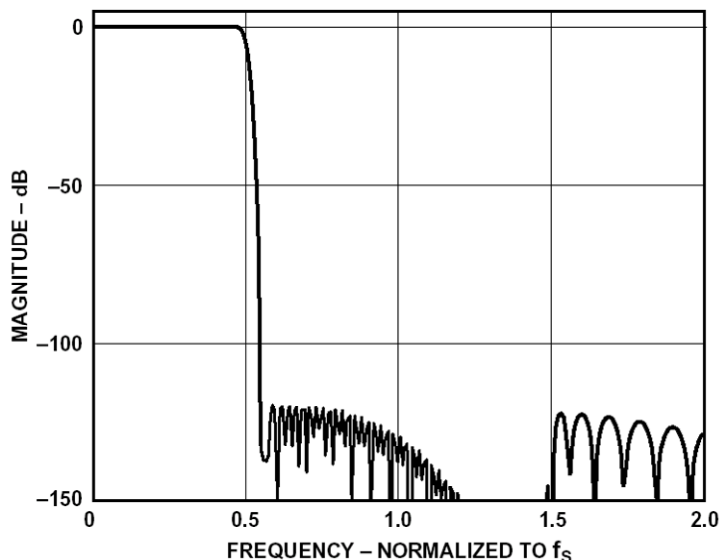


Figure 8: [AD1871](#) 24-Bit, 96-kSPS Stereo Sigma-Delta ADC Digital Filter Characteristics

In other applications, such as low frequency, high resolution 24-bit measurement Σ - Δ ADCs (such as the AD77xx-series), other types of digital filters may be used. For instance, the SINC³ response is popular because it has zeros at multiples of the throughput rate. A 10-Hz throughput rate produces zeros at 50 Hz and 60 Hz which aids in ac power line rejection.

Regardless of the type of digital filter, Σ - Δ ADCs require that sufficient settling time is allowed after the application of a step function input.

MULTISTAGE NOISE SHAPING (MASH) SIGMA-DELTA CONVERTERS

As has been discussed, nonlinear stabilization techniques can be difficult for 3rd order loops or higher. In many cases, the multi-bit architecture is preferable. An alternative approach to either of these, called multistage noise shaping (MASH), utilizes cascaded stable first-order loops (see References 8 and 9). Figure 9 shows a block diagram of a three-stage MASH ADC. The output of the first integrator is subtracted from the first DAC output to yield the first stage quantization noise, Q1. Q1 is then quantized by the second stage. The output of the second integrator is subtracted from the second DAC output to yield the second stage quantization noise which is in turn quantized by the third stage.

The output of the first stage is summed with a single digital differentiation of the second stage output and a double differentiation of the third stage output to yield the final output. The result is that the quantization noise Q1 is suppressed by the second stage, and the quantization noise Q2 is suppressed by the third stage yielding the same suppression as a third-order loop. Since this result is obtained using three first-order loops, stable operation is assured.

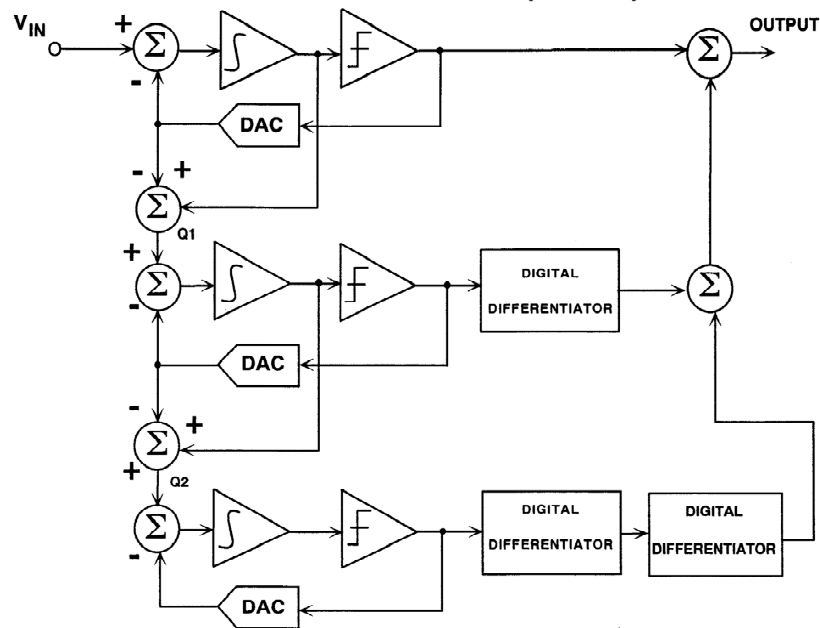


Figure 9: Multi-Stage Noise Shaping Sigma-Delta ADC (MASH)

HIGH RESOLUTION MEASUREMENT SIGMA-DELTA ADCS

While older integrating architectures such as dual-slope are still used in digital voltmeters, CMOS Σ - Δ ADCs are the dominant converter for today's industrial measurement applications. These converters offer excellent 50-Hz/60-Hz power line common-mode rejection and resolutions up to 24 bits with various digital features, such as on-chip calibration. Many have programmable gain amplifiers (PGAs) which allow the direct digitization of small signals from bridge and thermocouple transducers without the need for additional external signal conditioning circuits.

In order to better understand the capability of Σ - Δ measurement ADCs and the power of the technique, a modern example, the 24-bit [AD7799](#), will be examined in detail. The AD7799 is a member of the AD77xx family and is shown in Figure 10. This ADC was specifically designed to interface directly to low-level sensor outputs such as bridges in weigh scale applications. The device accepts low-level signals directly from a bridge and outputs a serial digital word. There are three multiplexed and buffered differential inputs which drive an internal instrumentation amplifier. The in-amp can be programmed for eight different gains: 1, 2, 4, 8, 16, 32, 64, and 128.

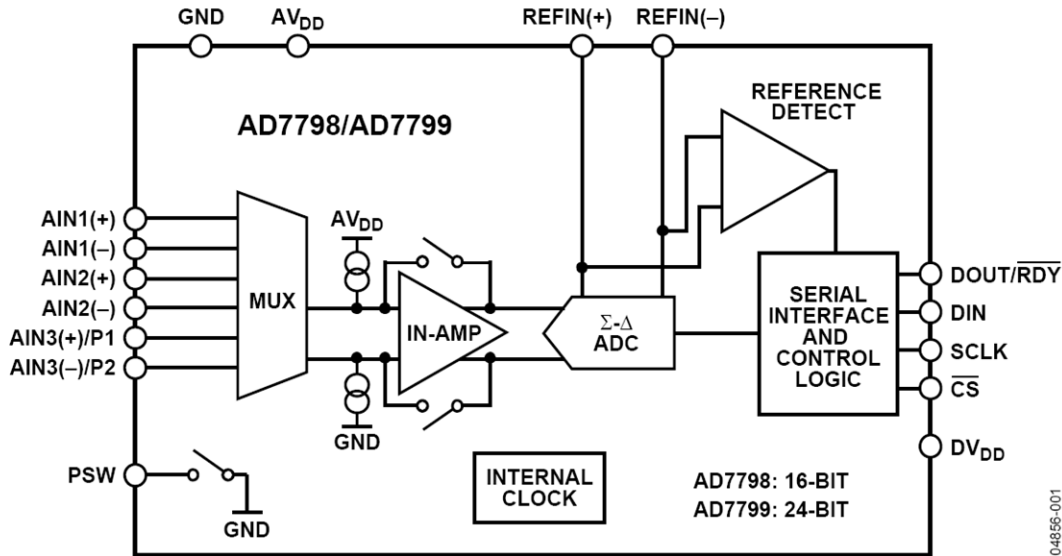


Figure 10: [AD7799](#) Sigma-Delta Single-Supply Bridge ADC

Figure 11 shows a direct connection between a bridge-based load cell and a high resolution Σ - Δ ADC, the AD7799. The fullscale bridge output of 10 mV is digitized to approximately 16 noise-free bits by the ADC at a throughput rate of 4.17 Hz. Ratiometric operation eliminates the need for a precision voltage reference. The AD7799 can be operated at throughput rates from 4.17 Hz to 500 Hz. The part operates with a power supply from 2.7 V to 5.25 V and consumes 380 μ A typical.

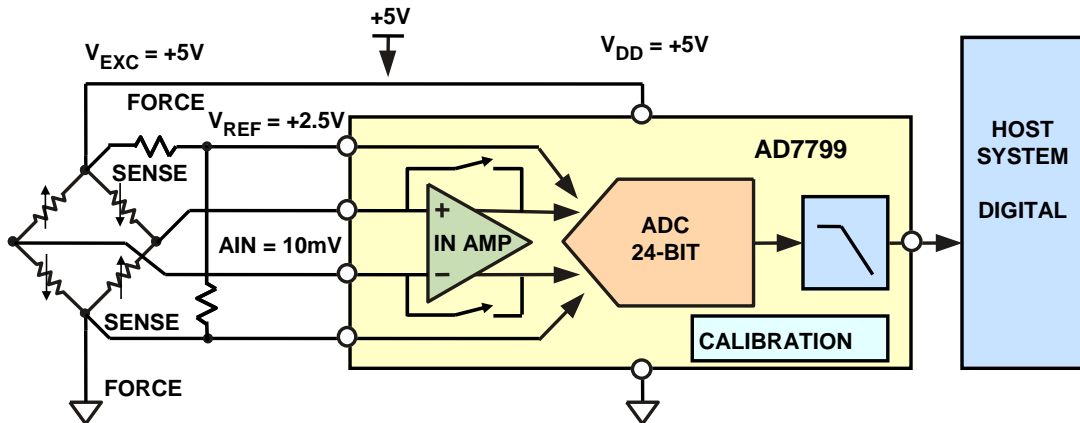


Figure 11: Load Cell Conditioning Using a High Resolution Sigma-Delta ADC

BANDPASS SIGMA-DELTA CONVERTERS

The Σ - Δ ADCs that we have described so far contain integrators, which are low pass filters, whose passband extends from dc. Thus, their quantization noise is pushed up in frequency. At present, most commercially available Σ - Δ ADCs are of this type (although some which are intended for use in audio or telecommunications applications contain bandpass rather than lowpass digital filters to eliminate any system dc offsets). But there is no particular reason why the filters of the Σ - Δ modulator should be LPFs, except that traditionally ADCs have been thought of as being baseband devices, and that integrators are somewhat easier to construct than bandpass filters. If we replace the integrators in a Σ - Δ ADC with bandpass filters (BPFs) as shown in Figure 12, the quantization noise is moved up and down in frequency to leave a virtually noise-free region in the pass-band (see References 10, 11, and 12). If the digital filter is then programmed to have its pass-band in this region, we have a Σ - Δ ADC with a bandpass, rather than a lowpass characteristic. Such devices would appear to be useful in direct IF-to-digital conversion, digital radios, ultrasound, and other undersampling applications. However, the modulator and the digital BPF must be designed for the specific set of frequencies required by the system application, thereby somewhat limiting the flexibility of this approach.

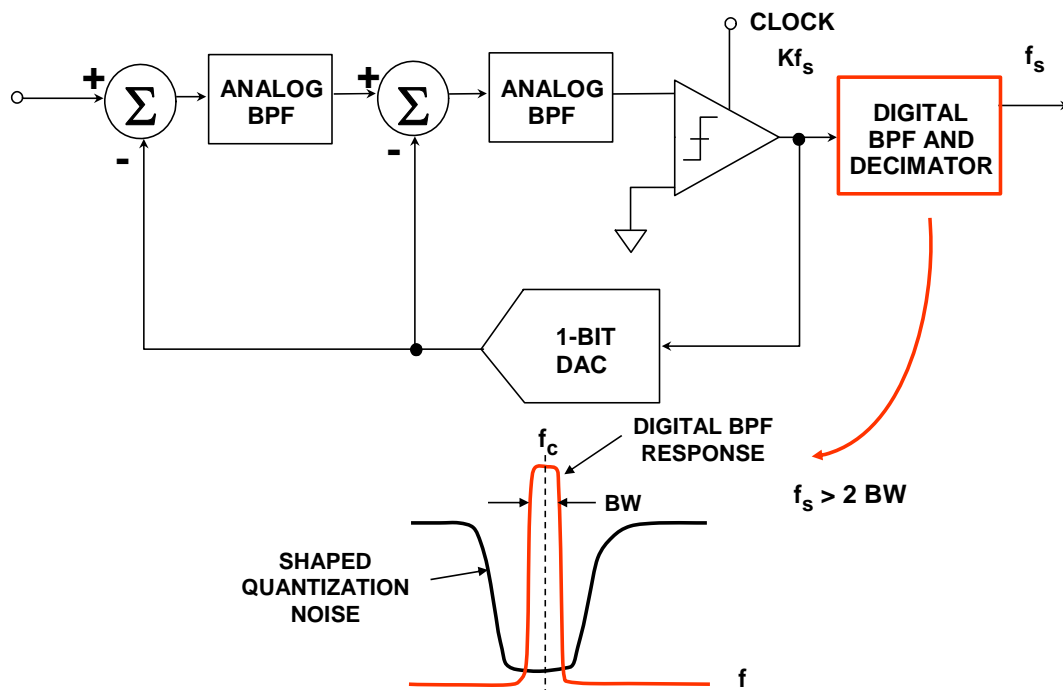


Figure 12: Replacing Integrators with Resonators Gives a Bandpass Sigma-Delta ADC

In an undersampling application of a bandpass Σ - Δ ADC, the minimum sampling frequency must be at least twice the signal bandwidth, BW . The signal is centered around a carrier frequency, f_c . A typical digital radio application using a 455-kHz center frequency and a signal bandwidth of 10 kHz is described in Reference 11. An oversampling frequency $Kf_s = 2$ MSPS and an output rate $f_s = 20$ kSPS yielded a dynamic range of 70 dB within the signal bandwidth.

An early example of a bandpass Σ - Δ ADC is the [AD9870](#) IF Digitizing Subsystem having a nominal oversampling frequency of 18 MSPS, a center frequency of 2.25 MHz, and a bandwidth of 10 kHz to 150 kHz (see details in Reference 12).

The [AD9874](#) and [AD9864](#) are general purpose IF subsystems that digitize low level 10-300 MHz IF signals with bandwidths up to 270 kHz (see details in Reference 13). The signal chain contains a low noise amplifier, mixer, bandpass Σ - Δ ADC and a decimation filter with programmable decimation factor. An AGC circuit provides 12 dB of continuous gain adjustment.

SUMMARY

Sigma-delta ADCs and DACs have proliferated into many modern applications including measurement, voiceband, audio, etc. The technique takes full advantage of low cost CMOS processes and therefore makes integration with highly digital functions such as DSPs practical. Modern techniques such as the multi-bit data scrambled architecture minimize problems with idle tones which plagued early Σ - Δ products. Resolutions up to 24-bits are currently available, and the requirements on analog antialiasing/anti-imaging filters are greatly relaxed due to oversampling. The internal digital filter in audio Σ - Δ ADCs can be designed for linear phase, which is a major requirement in those applications. For high resolution Σ - Δ ADCs designed for measurement applications, the digital filter is generally designed so that zeros occur at the mains frequencies of 50 Hz and 60 Hz.

Many Σ - Δ converters offer a high level of user programmability with respect to output data rate, digital filter characteristics, and self-calibration modes. Multi-channel Σ - Δ ADCs are now available for data acquisition systems, and most users are well-educated with respect to the settling time requirements of the internal digital filter in these applications.

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