SONY

CXD3003R

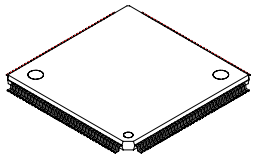
CD Digital Signal Processor with Built-in Digital Servo and DAC

For the availability of this product, please contact the sales office.

Description

The CXD3003R is a digital signal processor LSI for CD players. This LSI incorporates a digital servo, digital filter and 1-bit DAC.

144 pin LQFP (Plastic)



Features

- All digital signal processing during playback is performed with a single chip
- Highly integrated mounting possible due to a built-in RAM

Digital Signal Processor (DSP) Block

- Playback mode supporting CAV (Constant Angular Velocity)
- Frame jitter free
- 0.5× to 24× continuous playback possible with a low external clock
- Allows relative rotational velocity readout
- Wide capture range playback mode
- Spindle rotational velocity following method
- Supports 1× to 24× playback by switching the built-in VCO
- The bit clock, which strobes the EFM signal, is generated by the digital PLL
- EFM data demodulation
- Enhanced EFM frame sync signal protection
- Refined super strategy-based powerful error correction
  C1: double correction, C2: quadruple correction
  Supported during 24× playback
- Noise reduction during track jumps
- Auto zero-cross mute
- Subcode demodulation and Sub Q data error detection
- Digital spindle servo (built-in oversampling filter)
- 16-bit traverse counter
- Asymmetry compensation circuit
- CPU interface on serial bus
- Error correction monitor signal, etc. output from a new CPU interface
- Servo auto sequencer
- Fine search performs track jumps with high accuracy
- Digital audio interface outputs
- Digital level meter, peak meter
- Bilingual compatible
- VCO control mode

Digital Servo (DSSP) Block

- Microcomputer software-based flexible servo control
- Offset cancel function for servo error signal
- Auto gain control function for servo loop
- E:F balance, focus bias adjustment function
- Surf jump function supporting micro two-axis

Digital Filter and DAC Blocks

- Digital de-emphasis
- Digital attenuation
- 4Fs oversampling filter
- Adoption of a secondary $\Delta\Sigma$ noise shaper
- Supports double-speed playback

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings

• Supply voltage	V_{DD}	–0.3 to +4.6	V
• Input voltage	V_I	–0.3 to +4.6	V
		(V_{SS} – 0.3V to V_{DD} + 0.3V)	
• Output voltage	V_O	–0.3 to +4.6	V
• Storage temperature	Tstg	–40 to +125	°C
• Supply voltage difference			
	V_{SS} – AV_{SS}	–0.3 to +0.3	V
	V_{DD} – AV_{DD}	–0.3 to +0.3	V

Recommended Operating Conditions

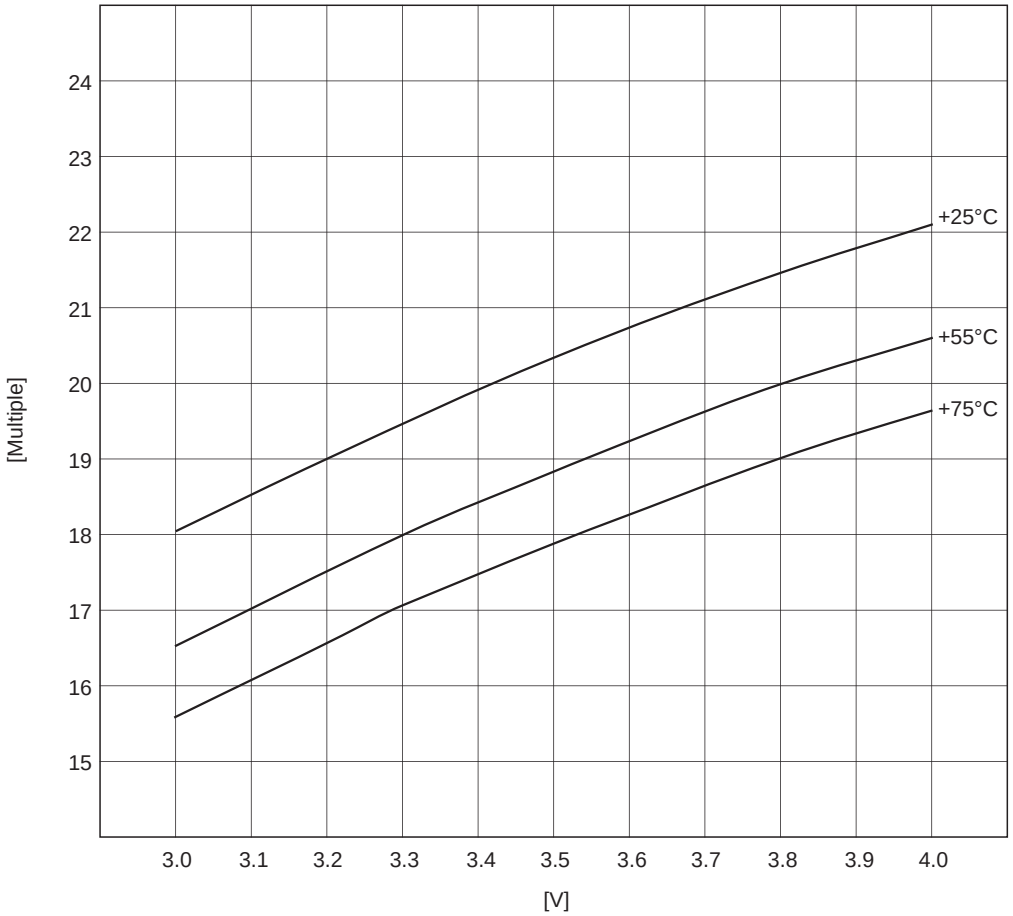
• Supply voltage	V_{DD}*	3.0 to 4.0	V
• Operating temperature			
	Topr	–20 to +75	°C

* The V_{DD} (min.) for the CXD3003R varies according to the playback speed and built-in VCO selection. The V_{DD} (min.) for the CXD3003R under various conditions are as shown on the following page.

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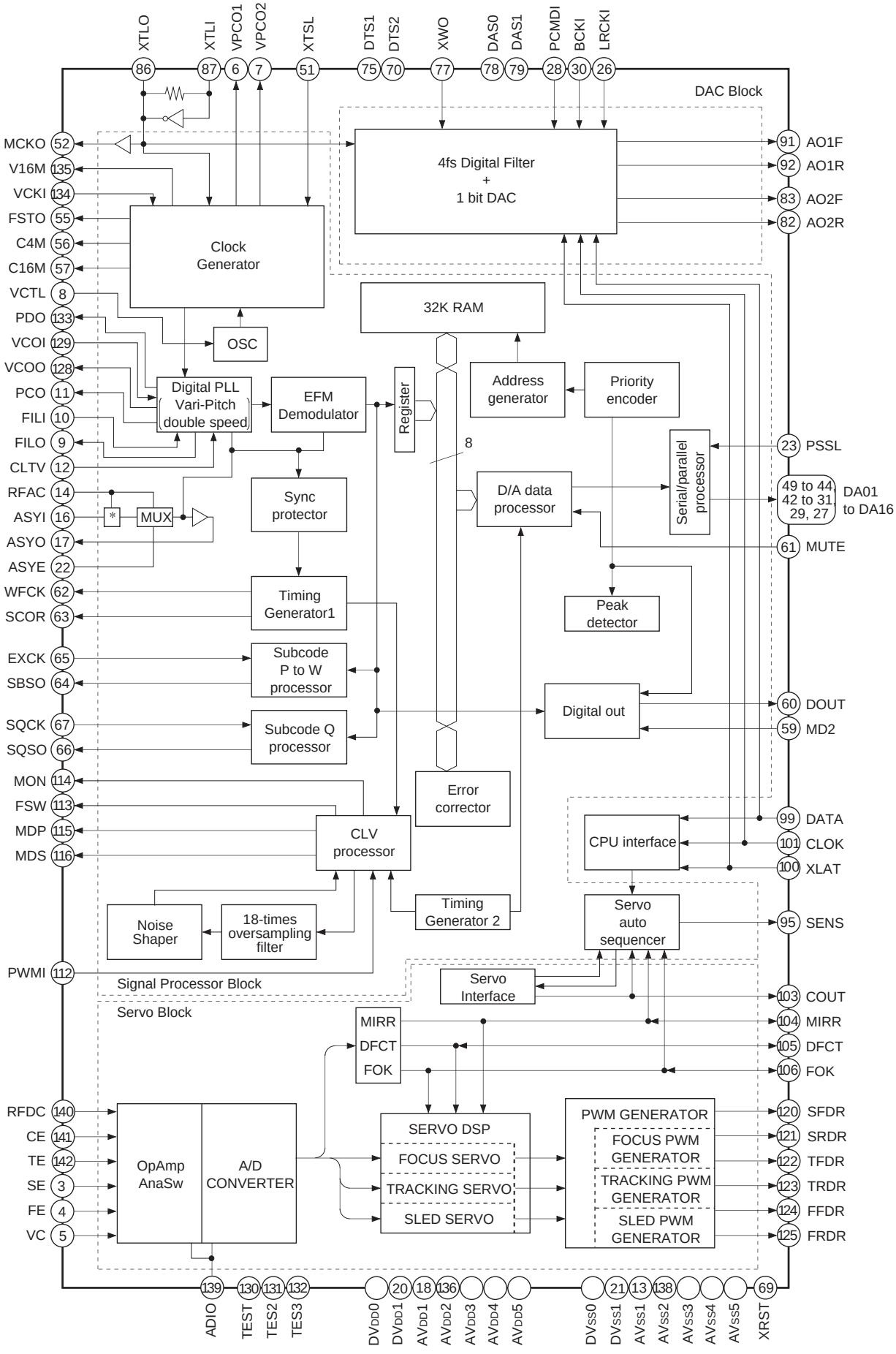
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Maximum Operating Speed

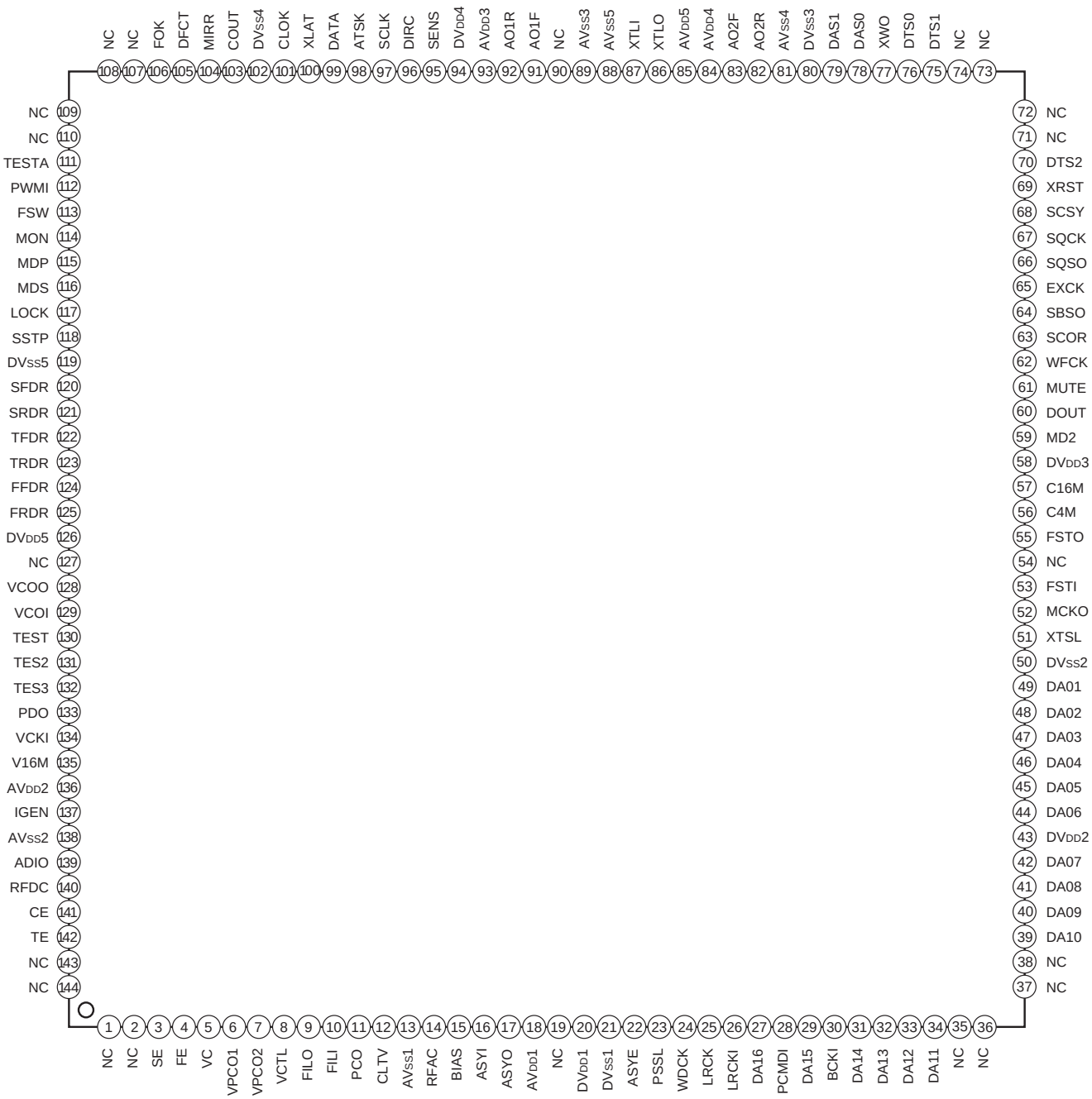


The maximum operating speed graph shows the playback speed V_{DD} (min.) at various temperatures.
The playback conditions are middle-speed VCO1 and high-speed VCO2 selected in CAV-W mode with DSPB = 1.

Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O		Description
3	SE	I		Sled error signal input.
4	FE	I		Focus error signal input.
5	VC	I		Center voltage input.
6	VPCO1	O	1, Z, 0	Wide-band EFM PLL VCO2 charge pump output.
7	VPCO2	O	1, Z, 0	Wide-band EFM PLL VCO2 charge pump output 2. Turned on and off by $E command FCSW.
8	VCTL	I		Wide-band EFM PLL VCO2 control voltage input.
9	FILO	O	Analog	Master PLL filter output (slave = digital PLL).
10	FILI	I		Master PLL filter input.
11	PCO	O	1, Z, 0	Master PLL charge pump output.
12	CLTV	I		Multiplier VCO control voltage input.
13	$AV_{SS}1$			Analog GND.
14	RFAC	I		EFM signal input.
15	BIAS	I		Asymmetry circuit constant current input.
16	ASYI	I		Asymmetry comparator voltage input.
17	ASYO	O	1, 0	EFM full-swing output (low = V_{SS}, high = V_{DD}).
18	$AV_{DD}1$			Analog power supply.
20	$DV_{DD}1$			Digital power supply.
21	$DV_{SS}1$			Digital GND.
22	ASYE	I		Asymmetry circuit on/off (low = off, high = on).
23	PSSL	I		Audio data output mode switching input (low: serial, high: parallel).
24	WDCK	O	1, 0	D/A interface for 48-bit slot. Word clock f = 2Fs.
25	LRCK	O	1, 0	D/A interface for 48-bit slot. LR clock f = Fs.
26	LRCKI	I		LR clock input to DAC (48-bit slot).
27	DA16	O	1, 0	DA16 (MSB) output when PSSL = 1, 48-bit slot serial data output (two's complement, MSB first) when PSSL = 0.
28	PCMDI	I		Audio data input to DAC (48-bit slot).
29	DA15	O	1, 0	DA15 output when PSSL = 1, 48-bit slot bit clock output when PSSL = 0.
30	BCKI	I		Bit clock input to DAC (48-bit slot).
31	DA14	O	1, 0	DA14 output when PSSL = 1, 64-bit slot serial data output (two's complement, LSB first) when PSSL = 0.
32	DA13	O	1, 0	DA13 output when PSSL = 1, 64-bit slot bit clock output when PSSL = 0.
33	DA12	O	1, 0	DA12 output when PSSL = 1, 64-bit slot LR clock output when PSSL = 0.
34	DA11	O	1, 0	DA11 output when PSSL = 1, GTOP output when PSSL = 0.
39	DA10	O	1, 0	DA10 output when PSSL = 1, XUGF output when PSSL = 0.
40	DA09	O	1, 0	DA09 output when PSSL = 1, XPLCK output when PSSL = 0.

Pin No.	Symbol	I/O		Description
41	DA08	O	1, 0	DA08 output when PSSL = 1, GFS output when PSSL = 0.
42	DA07	O	1, 0	DA07 output when PSSL = 1, RFCK output when PSSL = 0.
43	$DV_{DD}2$			Digital power supply.
44	DA06	O	1, 0	DA06 output when PSSL = 1, C2PO output when PSSL = 0.
45	DA05	O	1, 0	DA05 output when PSSL = 1, XRAOF output when PSSL = 0.
46	DA04	O	1, 0	DA04 output when PSSL = 1, MNT3 output when PSSL = 0.
47	DA03	O	1, 0	DA03 output when PSSL = 1, MNT2 output when PSSL = 0.
48	DA02	O	1, 0	DA02 output when PSSL = 1, MNT1 output when PSSL = 0.
49	DA01	O	1, 0	DA01 output when PSSL = 1, MNT0 output when PSSL = 0.
50	$DV_{SS}2$			Digital GND.
51	XTSL	I		Crystal selection input.
52	MCKO	O	1, 0	Clock output. Inverted output of XTLI.
53	FSTI	I		2/3 frequency division input for XTLI pin.
55	FSTO	O	1, 0	2/3 frequency division output for XTLI pin. Does not change with variable pitch.
56	C4M	O	1, 0	1/4 frequency division output for XTLI pin. Changes with variable pitch.
57	C16M	O	1, 0	16.9344MHz output. Changes simultaneously with variable pitch.
58	$DV_{DD}3$			Digital power supply.
59	MD2	I		Digital Out on/off control (low = off, high = on).
60	DOUT	O	1, 0	Digital Out output.
61	MUTE	I		Mute (low: off, high: on).
62	WFCK	O	1, 0	WFCK (Write Frame Clock) output.
63	SCOR	O	1, 0	Outputs a high signal when either subcode sync S0 or S1 is detected.
64	SBSO	O	1, 0	Sub P to W serial output.
65	EXCK	I		SBSO readout clock input.
66	SQSO	O	1, 0	Sub Q 80-bit and PCM peak and level data 16-bit output.
67	SQCK	I		SQSO readout clock input.
68	SCSY	I		GRSCOR re-synchronization input. Normally low, re-syncronization is executed when high.
69	XRST	I		System reset. Reset when low.
70	DTS2	I		DAC test pin. Normally fixed to high.
75	DTS1	I		DAC test pin. Normally fixed to high.
76	DTS0	I		DAC test pin. Normally fixed to low.
77	XWO	I		DAC sync window open input. Normally high, window open when low.
78	DAS0	I		DAC test pin. Normally fixed to high.
79	DAS1	I		DAC test pin. Normally fixed to low.
80	$DV_{SS}3$			Digital GND.
81	$AV_{SS}4$			Analog GND.
82	AO2R	O	1, Z, 0	Channel 2 DAC PWM output (reversed phase).

Pin No.	Symbol	I/O		Description
83	AO2F	O	1, Z, 0	Channel 2 DAC PWM output (forward phase).
84	$AV_{DD}4$			Analog power supply.
85	$AV_{DD}5$			Master clock power supply.
86	XTLO	O	1, 0	Master clock crystal oscillation circuit output.
87	XTLI	I		Master clock crystal oscillation circuit input.
88	$AV_{SS}5$			Master clock GND.
89	$AV_{SS}3$			Analog GND.
91	AO1F	O	1, Z, 0	Channel 1 DAC PWM output (forward phase).
92	AO1R	O	1, Z, 0	Channel 1 DAC PWM output (reversed phase).
93	$AV_{DD}3$			Analog power supply.
94	$AV_{DD}4$			Digital power supply.
95	SENS	O	1, Z, 0	SENS output to CPU.
96	DIRC	I		Used during 1-track jumps.
97	SCLK	I		SENS serial data readout clock input.
98	ATSK	I		Anti-shock pin.
99	DATA	I		Serial data input from CPU.
100	XLAT	I		Latch input from CPU. Serial data is latched at the falling edge.
101	CLOK	I		Serial data transfer clock input from CPU.
102	$DV_{SS}4$			Digital GND.
103	COUT	I/O	1, 0	Track count signal I/O.
104	MIRR	I/O	1, 0	Mirror signal I/O.
105	DFCT	I/O	1, 0	Defect signal I/O.
106	FOK	I/O	1, 0	Focus OK signal I/O.
111	TESTA			Test pin. Leave this open.
112	PWMI	I		Spindle motor external pin input.
113	FSW	O	1, Z, 0	Spindle motor output filter switching output. GRSCOR output when $8 command SCOR SEL = high.
114	MON	O	1, 0	Spindle motor on/off control output.
115	MDP	O	1, Z, 0	Spindle motor servo control output.
116	MDS	O	1, Z, 0	Spindle motor servo control output.
117	LOCK	I/O	1, 0	GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low. Input when LKIN = high.
118	SSTP	I		Disc innermost track detection signal input.
119	$DV_{SS}5$			Digital GND.
120	SFDR	O	1, 0	Sled drive output.
121	SRDR	O	1, 0	Sled drive output.
122	TFDR	O	1, 0	Tracking drive output.

Pin No.	Symbol	I/O		Description
123	TRDR	O	1, 0	Tracking drive output.
124	FFDR	O	1, 0	Focus drive output.
125	FRDR	O	1, 0	Focus drive output.
126	$DV_{DD}5$			Digital power supply.
128	VCOO	O	1, 0	Analog EFM PLL oscillation circuit output.
129	VCOI	I		Analog EFM PLL oscillation circuit input. flock = 8.6436MHz
130	TEST	I		Test pin. Normally fixed to low.
131	TES2	I		Test pin. Normally fixed to low.
132	TES3	I		Test pin. Normally fixed to low.
133	PDO	O	1, Z, 0	Analog EFM PLL charge pump output.
134	VCKI	I		Variable pitch clock input from the external VCO. fcenter = 16.9344MHz Set VCKI to low when the external clock is not input to this pin.
135	V16M	O	1, Z, 0	Wide-band EFM PLL VCO2 oscillation output.
136	$AV_{DD}2$			Analog power supply.
137	IGEN	I		Connects the operational amplifier current source reference resistance connection.
138	$AV_{SS}2$			Analog GND.
139	ADIO	O		Operational amplifier output.
140	RFDC	I		RF signal input.
141	CE	I		Center servo analog input.
142	TE	I		Tracking error signal input.

* In the CXD3003R, the following pins are NC.
Pins 1, 2, 19, 35, 36, 37, 38, 54, 71, 72, 73, 74, 90, 107, 108, 109, 110, 127, 143 and 144

Notes)
- The 64-bit slot is an LSB first, two's complement output. The 48-bit slot is an MSB first, two's complement output.
- GTOP is used to monitor the frame sync protection status. (High: sync protection window released.)
- XUGF is the frame sync obtained from the EFM signal, and is negative pulse. It is the signal before sync protection.
- XPLCK is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge and the EFM signal transition point coincide.
- The GFS signal goes high when the frame sync and the insertion protection timing match.
- RFCK is derived from the crystal accuracy, and has a cycle of 136µs.
- C2PO represents the data error status.
- XRAOF is generated when the 32K RAM exceeds the ±28F jitter margin.

Electrical Characteristics

1. DC Characteristics

(V_{DD} = AV_{DD} = 3.3V ± 10%, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C)

Item			Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level input voltage	V_{IH} (1)		0.7V_{DD}			V	*1, *12
	Low level input voltage	V_{IL} (1)				0.2V_{DD}	V	
Input voltage (2)	High level input voltage	V_{IH} (2)	Schmitt input	0.7V_{DD}			V	*2
	Low level input voltage	V_{IL} (2)				0.2V_{DD}	V	
Input voltage (3)	High level input voltage	V_{IH} (3)	$V_I \leq 5.5V$	0.7V_{DD}			V	*3
	Low level input voltage	V_{IL} (3)				0.2V_{DD}	V	
Input voltage (4)	High level input voltage	V_{IH} (4)	$V_I \leq 5.5V$ Schmitt input	0.7V_{DD}			V	*4
	Low level input voltage	V_{IL} (4)				0.2V_{DD}	V	
Input voltage (5)	Input voltage	V_{IN} (5)	Analog input	V_{SS}		V_{DD}	V	*5
Input voltage (6)	Input voltage	V_{IN} (6)	Analog input	V_{SS}		V_{DD}	V	*6
Output voltage (1)	High level output voltage	V_{OH} (1)	I_{OH} = –8mA	V_{DD} – 0.4		V_{DD}	V	*9
	Low level output voltage	V_{OL} (1)	I_{OL} = 8mA	0		0.4	V	
Output voltage (2)	High level output voltage	V_{OH} (2)	I_{OH} = –4mA	V_{DD} – 0.4		V_{DD}	V	*7, *10 *12
	Low level output voltage	V_{OL} (2)	I_{OL} = 4mA	0		0.4	V	
Output voltage (3)	High level output voltage	V_{OH} (3)	I_{OH} = –2mA	V_{DD} – 0.2		V_{DD}	V	*7, *10 *12
	Low level output voltage	V_{OL} (3)	I_{OL} = 4mA	0		0.4	V	
Output voltage (4)	Low level output voltage	V_{OL} (4)	I_{OL} = 4mA	0		0.4	V	*8
Output voltage (5)	High level output voltage	V_{OH} (5)	I_{OH} = –0.28mA	V_{DD} – 0.5		V_{DD}	V	*11
	Low level output voltage	V_{OL} (5)	I_{OH} = 0.36mA	0		0.4	V	
Input leak current (1)		I_{LI} (1)	V_I = 0 to 5.5V	–10		10	µA	*3, *4, *5
Input leak current (2)		I_{LI} (2)	V_I = 0.25V_{DD} to 0.75V_{DD}	–20		20	µA	*6
Tri-state pin output leak current		I_{LO}	V_O = 0 to 3.6V	–5		5	µA	*10

Applicable pins

*1 BCKI, DTS0, DTS1, DTS2, LRCKI, PCMDI, TES2, TES3, TEST

*2 ASYE, FSTI, VCKI

*3 ATSK, DATA, DIRC, MD2, PWMI, SSTP, XLAT, XTSL, XWO

*4 CLOK, EXCK, MUTE, SCLK, SCSY, SQCK, XRST

*5 ASYI, BIAS, CLTV, FILI, IGEN, RFAC, VCTL

*6 CE, FE, SE, TE, VC, RFDC

*7 ASYO, C16M, C4M, DA01 to DA16, DAS0, DAS1, DOUT, FFDR, FRDR, FSTO, LRCK, MON, PSSL, SBSO, SCOR, SFDR, SQSO, SRDR, TFDR, TRDR, WDCK, WFCK

*8 FSW

*9 MCKO

*10 AO1F, AO1R, AO2F, AO2R, MDP, MDS, PCO, PDO, SENS, V16M, VPCO1, VPCO2

*11 FILO

*12 COUT, DFCT, FOK, LOCK, MIRR

2. AC Characteristics

(1) XTLI pin, VCOI pin

(a) When using self-excited oscillation

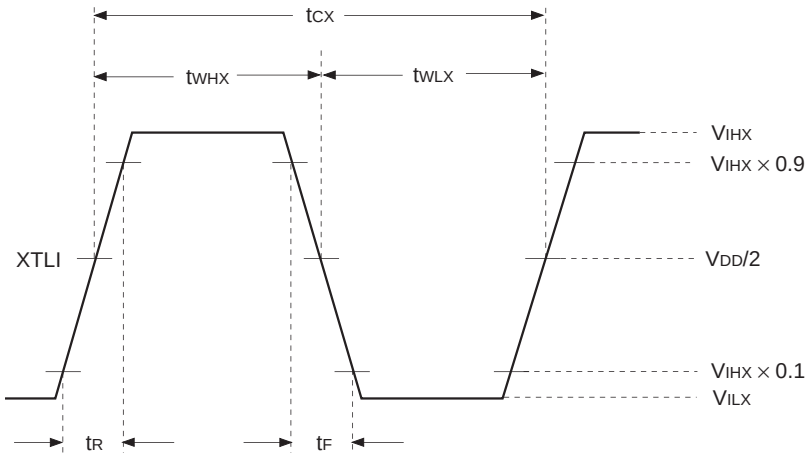
(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 3.3V ±10%)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{MAX}	7		34	MHz

(b) When inputting pulses to XTLI and VCOI pins

(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 3.3V ±10%)

Item	Symbol	Min.	Typ.	Max.	Unit
High level pulse width	t_{WHX}	13		500	ns
Low level pulse width	t_{WLX}	13		500	ns
Pulse cycle	t_{CX}	26		1000	ns
Input high level	V_{IHX}	V_{DD} – 1.0			V
Input low level	V_{ILX}			0.8	V
Rise time, fall time	t_R, t_F			10	ns



(c) When inputting sine waves to XTLI and VCOI pins via a capacitor

(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 3.3V ±10%)

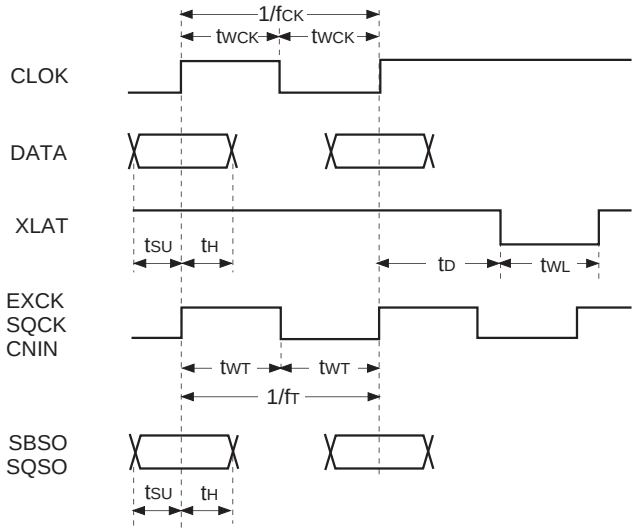
Item	Symbol	Min.	Typ.	Max.	unit
Input amplitude	V_I	2.0		V_{DD} + 0.3	Vp-p

(2) CLOK, DATA, XLAT, SQCK and EXCK pins

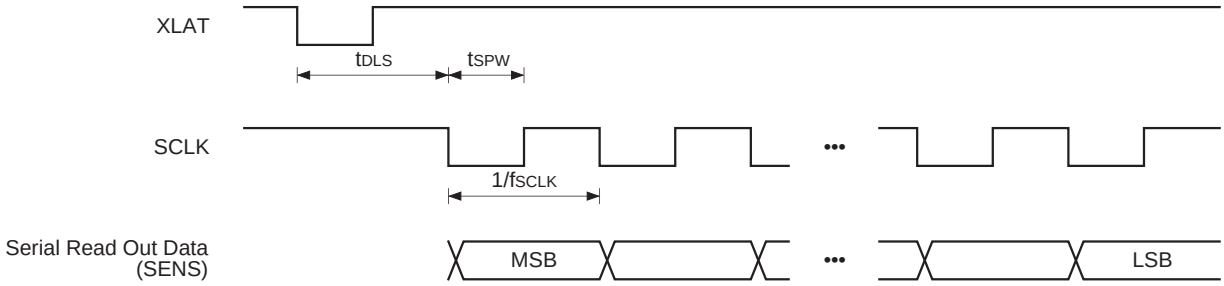
(V_{DD} = AV_{DD} = 3.3V ±10%, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CK}			16	MHz
Clock pulse width	t_{WCK}	30			ns
Setup time	t_{SU}	30			ns
Hold time	t_H	30			ns
Delay time	t_D	30			ns
Latch pulse width	t_{WL}	750			ns
EXCK SQCK frequency	f_T			0.65	MHz
EXCK SQCK pulse width	t_{WT}	750			ns
CNIN frequency*	f_T			65	kHz
CNIN pulse width*	t_{WT}	7.5			µs

* Only when $44 and $45 are executed.



(3) SCLK pin



Item	Symbol	Min.	Typ.	Max.	Unit
SCLK frequency	f_{SCLK}			16	MHz
SCLK pulse width	t_{SPW}	31.3			ns
Delay time	t_{DLS}	15			µs

(4) COUT, MIRR and DFCT pins

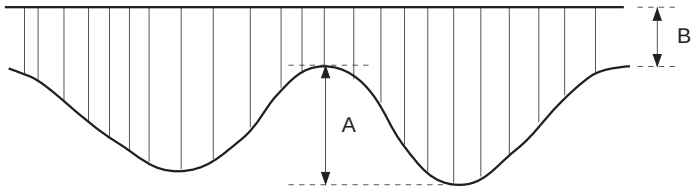
Operating frequency

(V_{DD} = AV_{DD} = 3.3V ±10%, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
COUT maximum operating frequency	f_{COUT}	40			kHz	*1
MIRR maximum operating frequency	f_{MIRR}	40			kHz	*2
DFCT maximum operating frequency	f_{DFCTH}	5			kHz	*3

*1 When using a high-speed traverse TZC.

*2



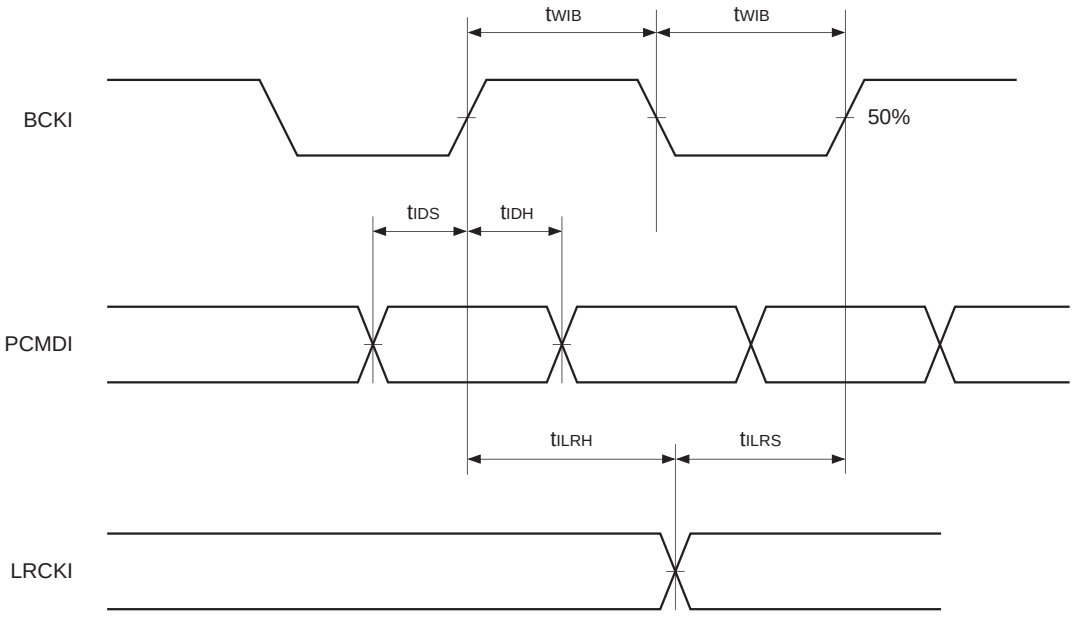
When the RF signal continuously satisfies the following conditions during the above traverse.

- A = 0.11V_{DD} to 0.23V_{DD}
- $\frac{B}{A+B} \leq 25\%$

*3 During complete RF signal omission.
When settings related to DFCT signal generation are Typ.

(5) BCKI, LRCKI and PCMDI pins (V_{DD} = 3.3V ±10%, Topr = –20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Input BCKI frequency	t_{BCK}			4.5	MHz
Input BCKI pulse width	t_{WIB}	100			ns
Input data setup time	t_{IDS}	10			
Input data hold time	t_{IDH}	15			
Input LRCK setup time	t_{ILRH}	10			
Input LRCK hold time	t_{ILRS}	15			



DAC Analog Characteristics

Measurement conditions

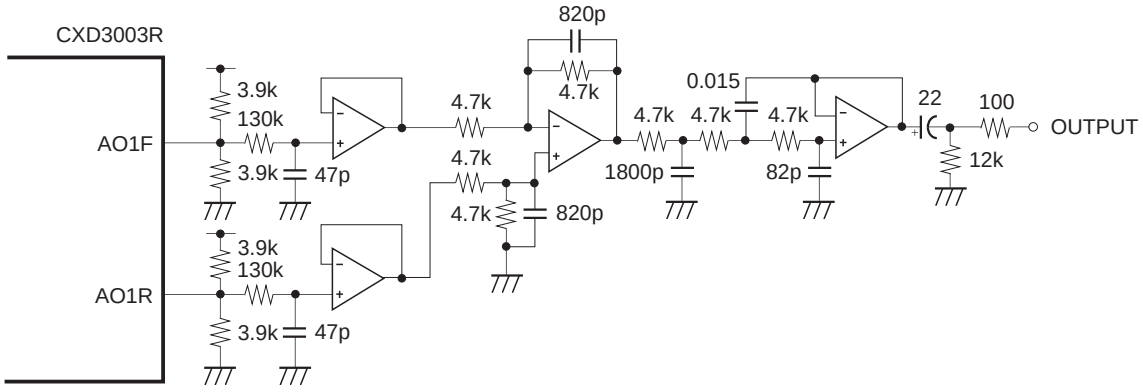
(Ta = 25°C, V_{DD} = 3.3V, Fs = 44.1kHz, signal frequency = 1kHz, measurement band = 4Hz to 20kHz, master clock = 768Fs)

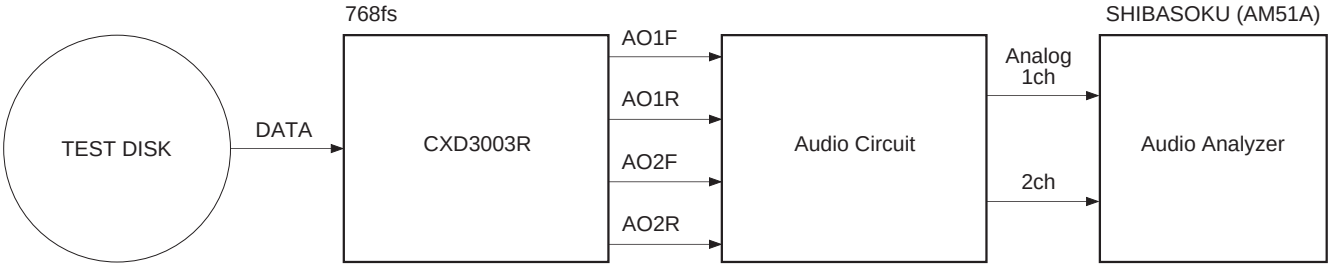
Item	Typ.	Unit	Remarks
S/N ratio	93	dB	(EIAJ) *1
THD + N	0.015	%	(EIAJ)
Dynamic range	91	dB	(EIAJ) *1, *2
Channel separation	91	dB	(EIAJ)
Output level	1.7	V (rms)	
Difference in gain between channels	0.1	dB	

*1 Using "A" weighting filter

*2 –60 dB, 1kHz input

The analog characteristics measurement circuit is shown below.





Block diagram of analog characteristics measurement

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[1] CPU Interface
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Explanation of abbreviations

AVRG:	Average
AGCNTL:	Auto gain control
FCS:	Focus
TRK:	Tracking
SLD:	Sled
DFCT:	Defect

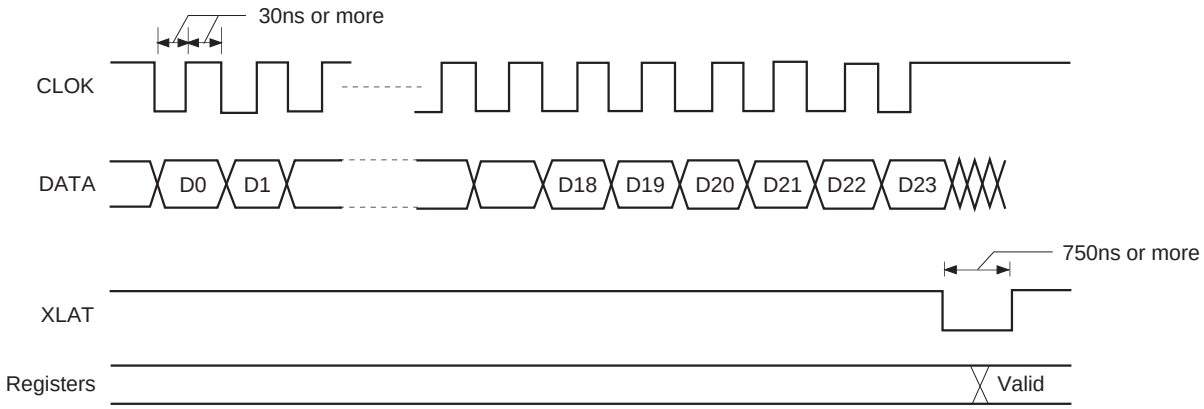
[1] CPU Interface

§1-1. CPU Interface Timing

• CPU interface

This interface uses DATA, CLOK and XLAT to set the modes.

The interface timing chart is shown below.



• The internal registers are initialized by a reset when XRST = 0.

§1-2. CPU Interface Command Table

Total bit length for each register

Register	Total bit length
0 to 2	8 bits
3	8 to 24 bits
4 to 6	16 bits
7	20 bits
8	24 bits
9	20 bits
A	28 bits
B	20 bits
C	16 bits
D	20 bits
E	20 bits

Command Table ($0X to 1X)

Register	Command	Address	Data 1				Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	FOCUS CONTROL	0 0 0 0	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO ON (FOCUS GAIN NORMAL)
			1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO ON (FOCUS GAIN DOWN)
			0	—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO OFF, 0V OUT
			0	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO OFF, FOCUS SEARCH VOLTAGE OUT
			0	—	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SEARCH VOLTAGE DOWN
			0	—	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SEACH VOLTAGE UP
1	TRACKING CONTROL	0 0 0 1	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANTI SHOCK ON
			0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANTI SHOCK OFF
			—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BRAKE ON
			—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BRAKE OFF
			—	—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN NORMAL
			—	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP
			—	—	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP FILTER SELECT 1
			—	—	—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP FILTER SELECT 2

—: Don’t care

Command Table ($2X to 3X)

Register	Command	Address	Data 1				Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
2	TRACKING MODE	0 0 1 0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING SERVO OFF
			0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING SERVO ON
			1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FORWARD TRACK JUMP
			1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REVERSE TRACK JUMP
			—	—	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED SERVO OFF
			—	—	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED SERVO ON
			—	—	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FORWARD SLED MOVE
			—	—	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REVERSE SLED MOVE

Register	Command	Address			Data 1		Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±1 × basic value) (Default)
			0	0	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±2 × basic value)
			0	0	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±3 × basic value)
			0	0	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±4 × basic value)

—: Don't care

Command Table ($340X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0011	0100	0000	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K00) SLED INPUT GAIN
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K01) SLED LOW BOOST FILTER A-H
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K02) SLED LOW BOOST FILTER A-L
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K03) SLED LOW BOOST FILTER B-H
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K04) SLED LOW BOOST FILTER B-L
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K05) SLED OUTPUT GAIN
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K06) FOCUS INPUT GAIN
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K07) SLED AUTO GAIN
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K08) FOCUS HIGH CUT FILTER A
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K09) FOCUS HIGH CUT FILTER B
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0A) FOCUS LOW BOOST FILTER A-H
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0B) FOCUS LOW BOOST FILTER A-L
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0C) FOCUS LOW BOOST FILTER B-H
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0D) FOCUS LOW BOOST FILTER B-L
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0E) FOCUS PHASE COMPENSATE FILTER A
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0F) FOCUS DEFECT HOLD GAIN

Command Table ($341X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0011	0100	0001	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K10) FOCUS PHASE COMPENSATE FILTER B
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K11) FOCUS OUTPUT GAIN
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K12) ANTI SHOCK INPUT GAIN
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K13) FOCUS AUTO GAIN
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K14) HPTZC / AUTO GAIN HIGH PASS FILTER A
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K15) HPTZC / AUTO GAIN HIGH PASS FILTER B
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K16) ANTI SHOCK HIGH PASS FILTER A
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K17) HPTZC / AUTO GAIN LOW PASS FILTER B
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K18) FIX
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K19) TRACKING INPUT GAIN
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1A) TRACKING HIGH CUT FILTER A
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1B) TRACKING HIGH CUT FILTER B
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1C) TRACKING LOW BOOST FILTER A-H
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1D) TRACKING LOW BOOST FILTER A-L
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1E) TRACKING LOW BOOST FILTER B-H
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1F) TRACKING LOW BOOST FILTER B-L

Command Table ($342X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0011	0100	0010	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K20) TRACKING PHASE COMPENSATE FILTER A
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K21) TRACKING PHASE COMPENSATE FILTER B
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K22) TRACKING OUTPUT GAIN
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K23) TRACKING AUTO GAIN
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K24) FOCUS GAIN DOWN HIGH CUT FILTER A
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K25) FOCUS GAIN DOWN HIGH CUT FILTER B
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K26) FOCUS GAIN DOWN LOW BOOST FILTER A-H
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K27) FOCUS GAIN DOWN LOW BOOST FILTER A-L
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K28) FOCUS GAIN DOWN LOW BOOST FILTER B-H
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K29) FOCUS GAIN DOWN LOW BOOST FILTER B-L
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2A) FOCUS GAIN DOWN PHASE COMPENSATE FILTER A
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2B) FOCUS GAIN DOWN DEFECT HOLD GAIN
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2C) FOCUS GAIN DOWN PHASE COMPENSATE FILTER B
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2D) FOCUS GAIN DOWN OUTPUT GAIN
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2E) NOT USED
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2F) NOT USED

Command Table ($343X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0011	0100	0011	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K30) FIX
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K31) ANTI SHOCK LOW PASS FILTER B
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K32) NOT USED
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K33) ANTI SHOCK HIGH PASS FILTER B-H
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K34) ANTI SHOCK HIGH PASS FILTER B-L
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K35) ANTI SHOCK FILTER COMPARATE GAIN
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K36) TRACKING GAIN UP2 HIGH CUT FILTER A
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K37) TRACKING GAIN UP2 HIGH CUT FILTER B
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K38) TRACKING GAIN UP2 LOW BOOST FILTER A-H
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K39) TRACKING GAIN UP2 LOW BOOST FILTER A-L
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3A) TRACKING GAIN UP2 LOW BOOST FILTER B-H
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3B) TRACKING GAIN UP2 LOW BOOST FILTER B-L
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3C) TRACKING GAIN UP PHASE COMPENSATE FILTER A
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3D) TRACKING GAIN UP PHASE COMPENSATE FILTER B
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3E) TRACKING GAIN UP OUTPUT GAIN
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3F) NOT USED

Command Table ($344X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0011	0100	0100	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K40) TRACKING HOLD FILTER INPUT GAIN
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K41) TRACKING HOLD FILTER A-H
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K42) TRACKING HOLD FILTER A-L
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K43) TRACKING HOLD FILTER B-H
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K44) TRACKING HOLD FILTER B-L
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K45) TRACKING HOLD FILTER OUTPUT GAIN
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K46) NOT USED
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K47) NOT USED
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K48) FOCUS HOLD FILTER INPUT GAIN
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K49) FOCUS HOLD FILTER A-H
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4A) FOCUS HOLD FILTER A-L
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4B) FOCUS HOLD FILTER B-H
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4C) FOCUS HOLD FILTER B-L
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4D) FOCUS HOLD FILTER OUTPUT GAIN
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4E) NOT USED
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4F) NOT USED

Command Table ($34FX to 3FX)

Register	Command	Address 1					Address 2						Data 1		Data 2				Data 3				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0	1	0	0	1	1	1	1	1	0	FBL9	FBL8	FBL7	FBL6	FBL5	FBL4	FBL3	FBL2	FBL1	—	FOCUS BIAS LIMIT
			0	1	0	0	1	1	1	1	0	1	FB9	FB8	FB7	FB6	FB5	FB4	FB3	FB2	FB1	—	FOCUS BIAS DATA
			0	1	0	0	1	1	1	1	0	0	TV9	TV8	TV7	TV6	TV5	TV4	TV3	TV2	TV1	TV0	TRVSC DATA
		Address					Data 1				Data 2				Data 3				Data 4				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
		0 0 1 1	0	1	0	1	FT1	FT0	FS5	FS4	FS3	FS2	FS1	FS0	FTZ	FG6	FG5	FG4	FG3	FG2	FG1	FG0	FOCUS SEARCH SPEED/ VOLTAGE/AUTO GAIN
			0	1	1	0	TDZC	DTZC	TJ5	TJ4	TJ3	TJ2	TJ1	TJ0	SFJP	TG6	TG5	TG4	TG3	TG2	TG1	TG0	DTZC/TRACK JUMP VOLTAGE/AUTO GAIN
			0	1	1	1	FZSH	FZSL	SM5	SM4	SM3	SM2	SM1	SM0	AGS	AGJ	AGGF	AGGT	AGV1	AGV2	AGHS	AGHT	FZSL/SLED MOVE/ Voltage/AUTO GAIN
			1	0	0	0	VCLM	VCLC	FLM	FLC0	RFLM	RFLC	AGF	AGT	DFSW	LKSW	TBLM	TCLM	FLC1	TLC2	TLC1	TLC0	LEVEL/AUTO GAIN/ DFSW/ (Initialize)
			1	0	0	1	DAC	SD6	SD5	SD4	SD3	SD2	SD1	SD0	0	0	0	0	0	0	0	0	SERIAL DATA READ MODE/SELECT
			1	0	1	0	0	FBON	FBSS	FBUP	FBV1	FBV0	0	TJD0	FPS1	FPS0	TPS1	TPS0	0	SJHD	INBK	MTI0	FOCUS BIAS
			1	0	1	1	SFO2	SFO1	SDF2	SDF1	MAX2	MAX1	SFOX	BTF	D2V2	D2V1	D1V2	D1V1	RINT	0	0	0	Operation for MIRR/ DFCT/FOK
			1	1	0	0	COSS	COTS	CETZ	CETF	COT2	COT1	MOT2	0	BTS1	BTS0	MRC1	MRC0	0	0	0	0	TZC/COUT BOTTOM/MIRR
			1	1	0	1	SFID	SFSK	THID	THSK	0	TLD2	TLD1	TLD0	0	0	0	0	0	0	0	0	SLED FILTER
			1	1	1	0	F1NM	F1DM	F3NM	F3DM	T1NM	T1UM	T3NM	T3UM	DFIS	TLCD	0	LKIN	COIN	MDFI	MIRI	XT1D	Filter
			1	1	1	1	0	AGG4	XT4D	XT2D	0	DRR2	DRR1	DRR0	0	ASFG	FTQ	LPAS	SRO1	SRO0	AGHF	0	Others

—: Don't care

Command Table ($4X to EX)

Register	Command	Address				Data 1				Data 2				Data 3				Data 4			
		D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8
4	Auto sequence	0	1	0	0	AS3	AS2	AS1	AS0	MT3	MT2	MT1	MT0	LSSL	0	0	0	—	—	—	—
5	Blind (A, E), Brake (B), Overflow (C, G)	0	1	0	1	TR3	TR2	TR1	TR0	0	0	0	0	0	0	0	0	—	—	—	—
6	Sled KICK, BRAKE (D), KICK (F)	0	1	1	0	SD3	SD2	SD1	SD0	KF3	KF2	KF1	KF0	0	0	0	0	—	—	—	—
7	Auto sequence (N) track jump count setting	0	1	1	1	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1
8	MODE specification	1	0	0	0	CD-ROM	DOUT Mute	DOUT Mute-F	WSEL	VCO SEL	ASHS	SOCT	VCO SEL2	KSL3	KSL2	KSL1	KSL0	VC01 CS1	VCO1 CS0	XVCO2 THRU	VCO2 CS
9	Function specification	1	0	0	1	DCLV ON/OFF	DSPB ON/OFF	ASEQ ON/OFF	DPLL ON/OFF	BiliGL MAIN	BiliGL SUB	FLFC	XWOC	DAC EMP	DAC ATT	0	0	PLM3	PLM2	PLM1	PLM0
A	Audio CTRL	1	0	1	0	0	0	Mute	ATT	PCT1	PCT2	DADS	SOC2	AT1D7	AT1D6	AT1D5	AT1D4	AT1D3	AT1D2	AT1D1	AT1D0
B	Traverse monitor counter setting	1	0	1	1	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1
C	Spindle servo coefficient setting	1	1	0	0	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	Gain DCLV1	Gain DCLV0	PCC1	PCC0	0	0	0	0	—	—	—	—
D	CLV CTRL	1	1	0	1	DCLV PWM MD	TB	TP	CLVS Gain	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	VP CTL1	VP CTL0	0	0
E	SPD mode	1	1	1	0	CM3	CM2	CM1	CM0	EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON	Gain CAV1	Gain CAV0	FCSW	INV VPCO

—: Don't care

Register	Command	Address	Data 1	Data 2	Data 3	Data 4	Data 5				Data 6			
							D7	D6	D5	D4	D3	D2	D1	D0
8	MODE specification	1 0 0 0					ERC4	SCOR SEL	SCSY	0	—	—	—	—
A	Audio CTRL	1 0 1 0					AT2D7	AT2D6	AT2D5	AT2D4	AT2D3	AT2D2	AT2D1	AT2D0

§1-3. CPU Command Presets

Command Preset Table ($0X to 34X)

Register	Command	Address	Data 1				Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	FOCUS CONTROL	0 0 0 0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO OFF, 0V OUT
1	TRACKING CONTROL	0 0 0 1	0	0	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP FILTER SELECT 1
2	TRACKING MODE	0 0 1 0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING SERVO OFF SLED SERVO OFF
Register	Command	Address			Data 1		Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D0	D0	
3	SELECT	0 0 1 1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±1 × basic value) (Default)
		Address 1					Address 2				Address 3				Data 1				Data 2				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D0	D0	
		0 0 1 1	0	1	0	0	0	See "Coefficient ROM Preset Values Table".															KRAM DATA ($3400XX to $344fXX)

—: Don't care

Command Preset Table ($34FX to 3FX)

Register	Command	Address 1					Address 2						Data 1		Data 2				Data 3				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0	1	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	FOCUS BIAS LIMIT
			0	1	0	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	FOCUS BIAS DATA
			0	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	TRVSC DATA
		Address					Data 1				Data 2				Data 3				Data 4				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
		0 0 1 1	0	1	0	1	0	1	0	1	1	0	0	0	0	0	1	0	1	1	0	1	FOCUS SEARCH SPEED/ VOLTAGE AUTO GAIN
			0	1	1	0	0	0	0	0	1	1	1	0	0	0	1	0	1	1	1	0	DTZC/TRACK JUMP VOLTAGE AUTO GAIN
			0	1	1	1	0	1	0	1	0	0	0	0	1	0	1	1	1	0	1	0	FZSL/SLED MOVE/ Voltage/AUTO GAIN
			1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LEVEL/AUTO GAIN/ DFSW/ (Initialize)
			1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SERIAL DATA READ MODE/SELECT
			1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FOCUS BIAS
			1	0	1	1	1	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	Operation for MIRR/ DFCT/FOK
			1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	TZC/COUT BOTTOM/MIRR
			1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SLED FILTER
			1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Filter
			1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Others

—: Don't care

Command Preset Table ($4X to EX)

Register	Command	Address				Data 1				Data 2				Data 3				Data 4			
		D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8
4	Auto sequence	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—
5	Blind (A, E), Brake (B), Overflow (C, G)	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	—	—	—	—
6	Sled KICK, BRAKE (D), KICK (F)	0	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	—	—	—	—
7	Auto sequence (N) track jump count setting	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
8	MODE specification	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	Function specification	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1
A	Audio CTRL	1	0	1	0	0	0	1	1	0	0	0	0	1	1	1	1	1	1	1	1
B	Traverse monitor counter setting	1	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
C	Spindle servo coefficient setting	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—
D	CLV CTRL	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
E	SPD mode	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

—: Don't care

Register	Command	Address	Data 1	Data 2	Data 3	Data 4	Data 5				Data 6			
							D7	D6	D5	D4	D3	D2	D1	D0
8	MODE specification	1 0 0 0					0	0	0	0	—	—	—	—
A	Audio CTRL	1 0 1 0					1	1	1	1	1	1	1	1

<Coefficient ROM Preset Values Table (1)>

ADDRESS	DATA	CONTENTS
K00	E0	SLED INPUT GAIN
K01	81	SLED LOW BOOST FILTER A-H
K02	23	SLED LOW BOOST FILTER A-L
K03	7F	SLED LOW BOOST FILTER B-H
K04	6A	SLED LOW BOOST FILTER B-L
K05	10	SLED OUTPUT GAIN
K06	14	FOCUS INPUT GAIN
K07	30	SLED AUTO GAIN
K08	7F	FOCUS HIGH CUT FILTER A
K09	46	FOCUS HIGH CUT FILTER B
K0A	81	FOCUS LOW BOOST FILTER A-H
K0B	1C	FOCUS LOW BOOST FILTER A-L
K0C	7F	FOCUS LOW BOOST FILTER B-H
K0D	58	FOCUS LOW BOOST FILTER B-L
K0E	82	FOCUS PHASE COMPENSATE FILTER A
K0F	7F	FOCUS DEFECT HOLD GAIN
K10	4E	FOCUS PHASE COMPENSATE FILTER B
K11	32	FOCUS OUTPUT GAIN
K12	20	ANTI SHOCK INPUT GAIN
K13	30	FOCUS AUTO GAIN
K14	80	HPTZC / Auto Gain HIGH PASS FILTER A
K15	77	HPTZC / Auto Gain HIGH PASS FILTER B
K16	80	ANTI SHOCK HIGH PASS FILTER A
K17	77	HPTZC / Auto Gain LOW PASS FILTER B
K18	00	Fix*
K19	F1	TRACKING INPUT GAIN
K1A	7F	TRACKING HIGH CUT FILTER A
K1B	3B	TRACKING HIGH CUT FILTER B
K1C	81	TRACKING LOW BOOST FILTER A-H
K1D	44	TRACKING LOW BOOST FILTER A-L
K1E	7F	TRACKING LOW BOOST FILTER B-H
K1F	5E	TRACKING LOW BOOST FILTER B-L
K20	82	TRACKING PHASE COMPENSATE FILTER A
K21	44	TRACKING PHASE COMPENSATE FILTER B
K22	18	TRACKING OUTPUT GAIN
K23	30	TRACKING AUTO GAIN
K24	7F	FOCUS GAIN DOWN HIGH CUT FILTER A
K25	46	FOCUS GAIN DOWN HIGH CUT FILTER B
K26	81	FOCUS GAIN DOWN LOW BOOST FILTER A-H
K27	3A	FOCUS GAIN DOWN LOW BOOST FILTER A-L
K28	7F	FOCUS GAIN DOWN LOW BOOST FILTER B-H
K29	66	FOCUS GAIN DOWN LOW BOOST FILTER B-L
K2A	82	FOCUS GAIN DOWN PHASE COMPENSATE FILTER A
K2B	44	FOCUS GAIN DOWN DEFECT HOLD GAIN
K2C	4E	FOCUS GAIN DOWN PHASE COMPENSATE FILTER B
K2D	1B	FOCUS GAIN DOWN OUTPUT GAIN
K2E	00	NOT USED
K2F	00	NOT USED

<Coefficient ROM Preset Values Table (2)>

ADDRESS	DATA	CONTENTS
K30	80	SLED INPUT GAIN (Only when TRK Gain Up2 is accessed with SFSK = 1.)
K31	66	ANTI SHOCK LOW PASS FILTER B
K32	00	NOT USED
K33	7F	ANTI SHOCK HIGH PASS FILTER B-H
K34	6E	ANTI SHOCK HIGH PASS FILTER B-L
K35	20	ANTI SHOCK FILTER COMPARATE GAIN
K36	7F	TRACKING GAIN UP2 HIGH CUT FILTER A
K37	3B	TRACKING GAIN UP2 HIGH CUT FILTER B
K38	80	TRACKING GAIN UP2 LOW BOOST FILTER A-H
K39	44	TRACKING GAIN UP2 LOW BOOST FILTER A-L
K3A	7F	TRACKING GAIN UP2 LOW BOOST FILTER B-H
K3B	77	TRACKING GAIN UP2 LOW BOOST FILTER B-L
K3C	86	TRACKING GAIN UP PHASE COMPENSATE FILTER A
K3D	0D	TRACKING GAIN UP PHASE COMPENSATE FILTER B
K3E	57	TRACKING GAIN UP OUTPUT GAIN
K3F	00	NOT USED
K40	04	TRACKING HOLD FILTER INPUT GAIN
K41	7F	TRACKING HOLD FILTER A-H
K42	7F	TRACKING HOLD FILTER A-L
K43	79	TRACKING HOLD FILTER B-H
K44	17	TRACKING HOLD FILTER B-L
K45	6D	TRACKING HOLD FILTER OUTPUT GAIN
K46	00	TRACKING HOLD FILTER INPUT GAIN (Only when TRK Gain Up2 is a accessed with THSK = 1.)
K47	00	NOT USED
K48	02	FOCUS HOLD FILTER INPUT GAIN
K49	7F	FOCUS HOLD FILTER A-H
K4A	7F	FOCUS HOLD FILTER A-L
K4B	79	FOCUS HOLD FILTER B-H
K4C	17	FOCUS HOLD FILTER B-L
K4D	54	FOCUS HOLD FILTER OUTPUT GAIN
K4E	00	NOT USED
K4F	00	NOT USED

§1-4. Description of SENS Signals

SENS output

Microcomputer serial register (latching not required)	ASEQ = 0	ASEQ = 1	Output data length
$0X	Z	FZC	—
$1X	Z	AS	—
$2X	Z	TZC	—
$38	Z	AGOK*	—
$38	Z	XAVEBSY*	—
$30 to 37	Z	SSTP	—
$3A	Z	FBIAS Count STOP	—
$3B to 3F	Z	SSTP	—
$3904	Z	TE Avrg Reg.	9 bit
$3908	Z	FE Avrg Reg.	9 bit
$390C	Z	VC Avrg Reg.	9 bit
$391C	Z	TRVSC Reg.	9 bit
$391D	Z	FB Reg.	9 bit
$391F	Z	RFDC Avrg Reg.	8 bit
$4X	Z	XBUSY	—
$5X	Z	FOK	—
$6X	Z	Servo SENS	—
$AX	GFS	GFS	—
$BX	COMP	COMP	—
$CX	COUT	COUT	—
$EX	$\overline{OV64}$	$\overline{OV64}$	—
$7X, 8X, 9X, DX, FX	Z	0	—

* $38 outputs AGOK during AGT and AGF command settings, and XAVEBSY during AVRG measurement. SSTP is output in all other cases.

Description of SENS Signals

SENS output	
Z	The SENS pin is high impedance.
XBUSY	Low while the auto sequencer is in operation, high when operation terminates.
FOK	Outputs the same signal as the FOK pin. High for "focus OK".
GFS	High when the regenerated frame sync is obtained with the correct timing.
COMP	Counts the number of tracks set with Reg.B. High when Reg.B is latched, low when the initial Reg.B number is input by CNIN.
COUT	Counts the number of tracks set with Reg.B. High when Reg.B is latched, toggles each time the Reg.B number is input by CNIN. While $44 and $45 are being executed, toggles with each CNIN 8-count instead of the Reg.B number.
$\overline{\text{OV64}}$	Low when the EFM signal is lengthened by 64 channel clock pulses or more after passing through the sync detection filter.

The meaning of the data for each address is explained below.

$4X commands

Register name	Data 1				Data 2				Data 3			
4	Command				MAX timer value				Timer range			
	AS3	AS2	AS1	AS0	MT3	MT2	MT1	MT0	LSSL	0	0	0

Command	AS3	AS2	AS1	AS0
Cancel	0	0	0	0
Fine Search	0	1	0	RXF
Focus-on	0	1	1	1
1-Track Jump	1	0	0	RXF
10-Track Jump	1	0	1	RXF
2N-Track Jump	1	1	0	RXF
M Track Move	1	1	1	RXF

RXF = 0 Forward

RXF = 1 Reverse

- When the Focus-on command ($47) is canceled, $02 is sent and the auto sequence is interrupted.
- When the Track jump commands ($44 to $45, $48 to $4D) are canceled, $25 is sent and the auto sequence is interrupted.

MAX timer value				Timer range			
MT3	MT2	MT1	MT0	LSSL	0	0	0
23.2ms	11.6ms	5.8ms	2.9ms	0	0	0	0
1.49s	0.74s	0.37s	0.18s	1	0	0	0

- To disable the MAX timer, set the MAX timer value to 0.

$5X commands

Timer	TR3	TR2	TR1	TR0
Blind (A, E), Overflow (C, G)	0.18ms	0.09ms	0.045ms	0.022ms
Brake (B)	0.36ms	0.18ms	0.09ms	0.045ms

$6X commands

Register name	Data 1				Data 2			
6	KICK (D)				KICK (F)			
	SD3	SD2	SD1	SD0	KF3	KF2	KF1	KF0

Timer	SD3	SD2	SD1	SD0
When executing KICK (D) $44 or $45	23.2ms	11.6ms	5.8ms	2.9ms
When executing KICK (D) $4C or $4D	11.6ms	5.8ms	2.9ms	1.45ms

Timer	KF3	KF2	KF1	KF0
KICK (F)	0.72ms	0.36ms	0.18ms	0.09ms

$7X commands

Auto sequence track jump count setting

Command	Data 1				Data 2				Data 3				Data 4			
	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8
Auto sequence track jump count setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

This command is used to set N when a 2N-track jump is executed, to set M when an M-track move is executed and to set the jump count when fine search is executed for auto sequence.

- The maximum track count is 65,535, but note that with a 2N-track jump the maximum track jump count depends on the mechanical limitations of the optical system.
- When the track jump count is from 0 to 15, the COUT signal counted for 2N-track jumps and M-track moves; when the count is 16 or over, the MIRR signal is counted. For fine search, the COUT signal is counted.

$8X commands

Command	Data 1				Data 2			
	D23	D22	D21	D20	D19	D18	D17	D16
MODE specification	CD-ROM	DOUT Mute	DOUT Mute-F	WSEL	VCO SEL1	ASHS	SOCT	VCO SEL2

Command bit	C2PO timing	Processing
CDROM = 1	1-3	CDROM mode; average value interpolation and pre-value hold are not performed.
CDROM = 0	1-3	Audio mode; average value interpolation and pre-value hold are performed.

Command bit	Processing
DOUT Mute = 1	When Digital Out is on (MD2 pin = 1), DOUT output is muted.
DOUT Mute = 0	When Digital Out is on, DOUT output is not muted.

Command bit	Processing
D. out Mute F = 1	When Digital Out is on (MD2 pin = 1), DA output is muted.
D. out Mute F = 0	DA output mute is not affected when Digital Out is either on or off.

MD2	Other mute conditions*	DOUT Mute	D.out Mute F	DOUT output	DA output for 48-bit slot	DA output for 64-bit slot
0	0	0	0	OFF	0dB	0dB
0	0	0	1			
0	0	1	0			– ∞dB
0	0	1	1			
0	1	0	0		– ∞dB	
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0	0dB	0dB	0dB
1	0	0	1		– ∞dB	– ∞dB
1	0	1	0	– ∞dB	0dB	
1	0	1	1		– ∞dB	
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

* See mute conditions (1), (2), and (4) to (6) under $AX commands for other mute conditions.

Command bit	Sync protection window width	Application
WSEL = 1	±26 channel clock	Anti-rolling is enhanced.
WSEL = 0	±6 channel clock	Sync window protection is enhanced.

* In normal-speed playback, channel clock = 4.3218MHz.

Command bit	Function
ASHS = 0	The command transfer rate to SSP is set to normal speed.
ASHS = 1	The command transfer rate to SSP is set to half speed.

* See "§4-8. Playback Speed" for settings.

Command bit	Function
SOCT = 0	Sub Q is output from the SQSO pin.
SOCT = 1	Each output signal is output from the SQSO pin. Input the readout clock to SQCK. (See Timing Chart 2-4.)

Command	Data 2				Data 3			
	D19	D18	D17	D16	D15	D14	D13	D12
MODE specification	VCO SEL1	ASHS	SOCT	VCO SEL2	KSL3	KSL2	KSL1	KSL0

See the previous page.

Command bit	Processing
VCOSEL1 = 0	Multiplier PLL VCO1 is set to normal speed.
VCOSEL1 = 1	Multiplier PLL VCO1 is set to approximately twice the normal speed.

* This setting is valid only when the low-speed VCO is selected by VCO1 CS1 and CS0.

Command bit		Processing
KSL3	KSL2	
0	0	Output of multiplier PLL VCO1 selected by VCO1 CS1 and CS0 is 1/1 frequency-divided.
0	1	Output of multiplier PLL VCO1 selected by VCO1 CS1 and CS0 is 1/2 frequency-divided.
1	0	Output of multiplier PLL VCO1 selected by VCO1 CS1 and CS0 is 1/4 frequency-divided.
1	1	Output of multiplier PLL VCO1 selected by VCO1 CS1 and CS0 is 1/8 frequency-divided.

Command bit	Processing
VCOSEL2 = 0	Wide-band PLL VCO2 is set to normal speed.
VCOSEL2 = 1	Wide-band PLL VCO2 is set to approximately twice the normal speed.

* This setting is valid only when the low-speed VCO is selected by VCO2 CS.

Command bit		Processing
KSL1	KSL0	
0	0	Output of wide-band PLL VCO2 selected by VCO2 CS is 1/1 frequency-divided.
0	1	Output of wide-band PLL VCO2 selected by VCO2 CS is 1/2 frequency-divided.
1	0	Output of wide-band PLL VCO2 selected by VCO2 CS is 1/4 frequency-divided.
1	1	Output of wide-band PLL VCO2 selected by VCO2 CS is 1/8 frequency-divided.

Command	Data 4			
	D11	D10	D9	D8
MODE specification	VCO1 CS1	VCO1 CS0	XVCO2 THRU	VCO2 CS

Command bit		Processing
VCO1CS1	VCO1CS0	
0	0	No.1 (Low-speed VCO for CXD3003)
0	1	No.2 (Middle-speed VCO for CXD3003)
1	0	No.3 (High-speed VCO for CXD3003)
1	1	No.4

* The CXD3003R has four multiplier PLL VCO1s, and this command selects one of these VCO1s. Four VCOs are No.3, No.4, No.2 and No.1 in order of the maximum frequency.

Command bit	Processing
XVCO2 THRU = 0	V16M output is connected internally to VCKI.
XVCO2 THRU = 1	V16M output is not connected internally. Input the clock from VCKI.

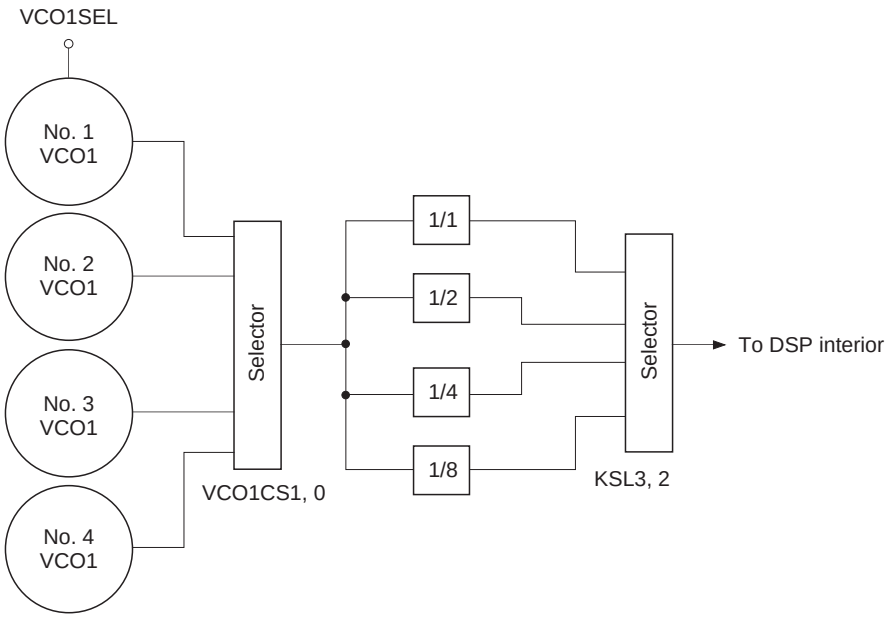
* This command sets internal or external connection for the VCO2 used in CAV-W mode.

Command bit	Processing
VCO2 CS = 0	Low-speed wide-band PLL VCO2 is selected.
VCO2 CS = 1	High-speed wide-band PLL VCO2 is selected.

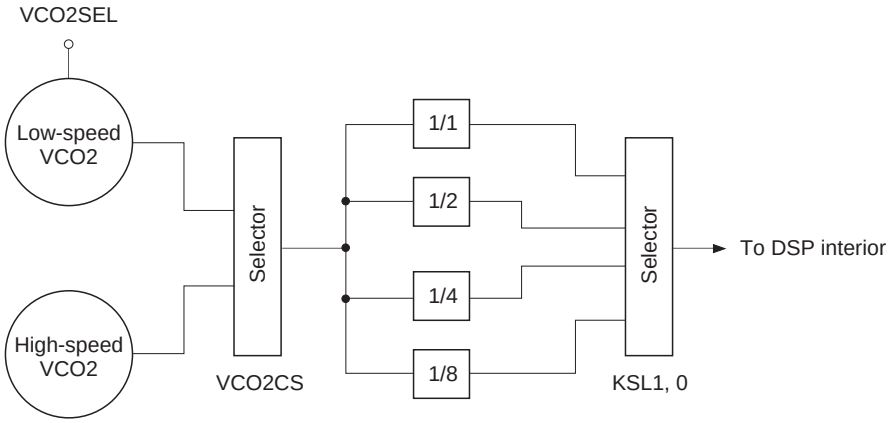
* The CXD3003R has two wide-band PLL VCO2, and this command selects one of these VCO1.

* Block diagram for VCO1 and VCO2 including VCOSEL1, VCOSEL2, KSL0 to 3, VCO1CS0, VCO1CS1 and VCO2 CS.

* **Block Diagram of VCO Internal Path**



VCO1 internal path



VCO2 internal path

Command	Data 5			
	D7	D6	D5	D4
MODE specification	ERC4	SCOR SEL	SCSY	0

Command bit	Processing
ERC4 = 0	C2 error double correction is performed when DSPB = 1.
ERC4 = 1	C2 error quadruple correction is performed when DSPB = 1.

Command bit	Processing
SCOR SEL = 0	FSW signal is output.
SCOR SEL = 1	GRSCOR (protected SCOR) is output.

* Used when outputting GRSCOR from the FSW pin.

Command bit	Processing
SCSY = 0	No processing.
SCSY = 1	GRSCOR (protected SCOR) synchronization is applied again.

* Used to resynchronize GRSCOR.

the rising edge signal of this command bit is used internally. Therefore, when resynchronizing GRSCOR, first return the setting to 0 and then set to 1.

GRSCOR achieves the crystal accuracy by removing the jitter components included in the SCOR signal. This signal is synchronized with PCMDATA.

The resynchronization conditions are when GTOP = high or when the SCSY pin = high.

(Same as when SCSY = 1 is sent by the $8X command.)

$9X commands

Command	Data 1				Data 2			
	D23	D22	D21	D20	D19	D18	D17	D16
Function specification	DCLV ON-OFF	DSPB ON-OFF	A.SEQ ON-OFF	D.PLL ON-OFF	BiliGL MAIN	BiliGL SUB	FLFC	XWOC

Command bit	CLV mode	Contents	
DCLV on/off = 0	In CLVS mode	FSW = low, MON = high, MDS = Z; MDP = servo control signal, carrier frequency of 230Hz at T_B = 0 and 460Hz at T_B = 1.	
	In CLVP mode	FSW = Z, MON = high; MDS = speed control signal, carrier frequency of 7.35kHz; MDP = phase control signal, carrier frequency of 1.8kHz.	
DCLV on/off = 1 (FSW, MON not required)	In CLVS and CLVP modes	When DCLV PWM and MD = 1 (Prohibited in CLV-W and CAV-W modes)	MDS = PWM polarity signal, carrier frequency of 132kHz MDP = PWM absolute value output (binary), carrier frequency of 132kHz
		When DCLV PWM and MD = 0	MDS = Z MDP = ternary PWM output, carrier frequency of 132kHz

When DCLV on/off = 1 for the Digital CLV servo, the sampling frequency of the internal digital filter switches simultaneously with the CLVP/CLVS switching.

Therefore, the cut-off frequency for the CLVS is fc = 70Hz when T_B = 0, and fc = 140Hz when T_B = 1.

Command bit	Processing
DSPB = 0	Normal-speed playback, C2 error quadruple correction.
DSPB = 1	Double-speed playback, C2 error double correction. (quadruple correction when ERC4 = 1)

FLFC is normally 0.

FLFC is 1 in CAV-W mode, for any playback speed.

Command bit	Meaning
DPLL = 0 *	RFPLL is analog. PDO, VCOI and VCOO are used.
DPLL = 1	RFPLL is digital. PDO is high impedance.

* External parts for the FILI, FILO and PCO pins are required even when analog PLL is selected.

Command bit	BiliGL MAIN = 0	BiliGL MAIN = 1
BiliGL SUB = 0	STEREO	MAIN
BiliGL SUB = 1	SUB	Mute

Definition of bilingual capable MAIN, SUB and STEREO

The left channel input is output to the left and right channels for MAIN.

The right channel input is output to the left and right channels for SUB.

The left and right channel inputs are output to the left and right channels for STEREO.

Command bit	External pin	Processing
XWOC	XWO	
0	L	DAC sync window is open.
0	H	
1	L	
1	H	DAC sync window is not open.

* This is used to perform resynchronization to DAC.

This command has the function equal to the external pin XWO's.
Set to high or 1 for the external pin or unused side of the command register.

• I/O sync circuit

Related pins: LRCK and XWO, Related command: XWOC
During normal operation, the I/O sync circuit automatically synchronizes with the input LRCK, and its operation proceeds in phase with the serial input data. However, there is a chance that synchronization will not be performed if there is a great deal of jitter in LRCK, or if the power has just been turned on, etc. In this case, forced synchronization is possible by setting the XWO pin or command XWOC low (0) for 2/Fs or more. Forced synchronization must also be performed when switching the clock system such as when switching from CLV mode to CAV mode and vice versa, or when switching the operating frequency, etc. The forced synchronization operation is performed at the second rising edge of LRCK after the XWO pin is set low or the XWOC command 19 set to 0.

Command	Data 3			
	D15	D14	D13	D12
Function specification	DAC EMPH	DAC ATT	0	0

These command bits control the DAC.

Command bit	Processing
DAC EMPH = 1	Applies digital de-emphasis. The emphasis constants are $\tau 1$ = 50µs and $\tau 2$ = 15µs when Fs = 44.1kHz.
DAC EMPH = 0	Turns digital de-emphasis off.

Command bit	Processing
DAC ATT = 1	Identical digital attenuation control is used for both channels 1 and 2. When common attenuation data is specified, the attenuation values for channel 1 are used.
DAC ATT = 0	Independent digital attenuation control is used for both channels 1 and 2.

Note) For normal stereo, channel 1 is the left channel and channel 2 is the right channel.

Command	Data 4			
	D11	D10	D9	D8
Function specification	PLM3	PLM2	PLM1	PLM0

• DAC PLAY MODE

By controlling these command bits, the DAC outputs channel 1 and channel 2 can be output in 16 different combinations of left channel, right channel, left + right channel, and mute.

The relationship between the commands and the outputs is shown in the table on the following page.

PLM3	PLM2	PLM1	PLM0	Channel 1 output	Channel 2 output	Remarks
0	0	0	0	Mute	Mute	Mute
0	0	0	1	L	Mute	
0	0	1	0	R	Mute	
0	0	1	1	L + R	Mute	
0	1	0	0	Mute	L	
0	1	0	1	L	L	
0	1	1	0	R	L	Reverse
0	1	1	1	L + R	L	
1	0	0	0	Mute	R	
1	0	0	1	L	R	Stereo
1	0	1	0	R	R	
1	0	1	1	L + R	R	
1	1	0	0	Mute	L + R	
1	1	0	1	L	L + R	
1	1	1	0	R	L + R	
1	1	1	1	L + R	L + R	Mono

Note) For normal stereo, channel 1 is the left channel and channel 2 is the right channel.
The output data of L + R is (L + R)/2 to prevent overflow.

$AX commands

Command	Data 1				Data 2			
	D23	D22	D21	D20	D19	D18	D17	D16
Audio CTRL	0	0	Mute	ATT	PCT1	PCT2	DADS	SOC2

Command bit	Meaning
Mute = 0	Mute off if other mute conditions are not set.
Mute = 1	Mute on. Peak register reset.

Command bit	Meaning
ATT = 0	Attenuation off
ATT = 1	–12dB

Mute conditions

(1) When register A mute = 1.
(2) When Mute pin = 1.
(3) When register 8 D.out Mute F = 1 and the Digital Out is on (MD2 pin = 1).
(4) When GFS stays low for over 35ms (during normal speed).
(5) When register 9 BiliGL MAIN = Sub = 1.
(6) When register A PCT1 = 1 and PCT2 = 0.

(1) to (4) perform zero-cross muting with a 1ms time limit.

Command bit		Meaning	PCM Gain	ECC error correction ability
PCT1	PCT2			
0	0	Normal mode	× 0dB	C1: double; C2: quadruple
0	1	Level meter mode	× 0dB	C1: double; C2: quadruple
1	0	Peak meter mode	Mute	C1: double; C2: double
1	1	Normal mode	× 0dB	C1: double; C2: double

Description of level meter mode (see Timing Chart 1-4.)

- When the LSI is set to this mode, it performs digital level meter functions.
- When the 96-bit clock is input to SQCK, 96 bits of data are output to SQSO.
  The initial 80 bits are Sub Q data (see §2. Subcode Interface). The last 16 bits are LSB first, which are 15-bit PCM data (absolute values) and an L/R flag.
  The L/R flag is high when the 15-bit PCM data is from the left channel and low when the data is from the right channel.
- The PCM data is reset and the L/R flag is reversed after one readout.
  Then maximum value measuring continues until the next readout.

Description of peak meter mode (see Timing Chart 1-5.)

- When the LSI is set to this mode, the maximum PCM data value is detected regardless of if it comes from the left or right channel.
  The 96-bit clock must be input to SQCK to read out this data.
- When the 96-bit clock is input, 96 bits of data are output to SQSO and the value is set in the LSI internal register again.
  In other words, the PCM maximum value detection register is not reset by the readout.
- To reset the PCM maximum value register to zero, set PCT1 = PCT2 = 0 or set the $AX mute.
- The Sub Q absolute time is automatically controlled in this mode.
  In other words, after the maximum value is generated, the absolute time for CRC to become OK is retained in the memory. Normal operation is conducted for the relative time.
- The final bit (L/R flag) of the 96-bit data is normally 0.
- The pre-value hold and average value interpolation data are fixed to level (– ∞) in this mode.

Command bit	Processing
DADS = 0	Set to 0 when crystal = 33.8688MHz.
DADS = 1	Set to 1 when crystal = 16.9344MHz.

Command bit	Processing
SOC2 = 0	The SENS signal is output from the SENS pin as usual.
SOC2 = 1	The SQSO pin signal is output from the SENS pin.

SENS output switching

- This command enables the SQSO pin signal to be output from the SENS pin.
  When SOC2 = 0, SENS output is performed as usual.
  When SOC2 = 1, the SQSO pin signal is output from the SENS pin.
  At this time, the readout clock is input to the SCLK pin.

Note) SOC2 should be switched when SQCK = SCLK = high.

• DAC digital attenuator

Command	Data 3				Data 4				Data 5				Data 6			
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Audio Ctrl	AT1D 7	AT1D 6	AT1D 5	AT1D 4	AT1D 3	AT1D 2	AT1D 1	AT1D 0	AT2D 7	AT2D 6	AT2D 5	AT2D 4	AT2D 3	AT2D 2	AT2D 1	AT2D 0

Note) AT1D7 to AT1D0 are the channel 1 ATT control bits.
AT2D7 to AT2D0 are the channel 2 ATT control bits.

Command bits AT1D7 to AT1D0 (AT2D7 to AT2D0)	Audio output
FF (H)	0dB
FE (H) ↓ 01 (H)	–0.034dB ↓ –48.131dB
00 (H)	– ∞

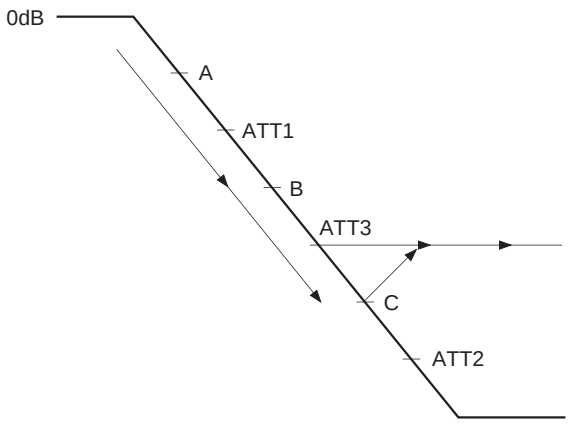
The attenuation data consists of 8 bits each for channels 1 and 2; the DAC ATT bit can be used to control channels 1 and 2 with common attenuation data. (When common attenuation data is specified, the attenuation values for channel 1 are used.)

An attenuation value, from 00 (H) to FF (H), is determined according to the following equation:
ATT = 20 log [input data/255] dB

Example: When the attenuation data is FA (H):
ATT = 20 log [250/255] dB = –0.172dB

• Soft mute
With the soft mute function, when the attenuation data goes from FF (H) and 00 (H) and vice versa, muting is turned on and off over the muting time of 1024Fs [s] = 23.2 [ms] (Fs = 44.1kHz).

• Attenuation
Assume the attenuation data ATT1, ATT2 and ATT3, where ATT1 > ATT3 > ATT2. First, assume ATT1 is transferred and then ATT2 is transferred. If ATT2 is transferred before ATT1 is reached (state "A" in the diagram), then the value continues approaching ATT2. Next, if ATT3 is transferred before ATT2 is reached (state "B" or "C" in the diagram), the attenuation begins approaching ATT3 from the current point. Note that it takes 1024/Fs [s] (Fs = 44.1kHz for CD players) to transit between attenuation data (from 0dB to – ∞).



Handling of the Attenuation Value

$BX commands

This command sets the traverse monitor count.

Command	Data 1				Data 2				Data 3				Data 4			
	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8
Traverse monitor count setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

- When the set number of tracks are counted during fine search, the sled control for the traverse cycle control goes off.
- The traverse monitor count is set to monitor the traverse status from the SENS output as COMP and COUT.

$CX commands

Command	Data 1				Data 2				Description
	D23	D22	D21	D20	D19	D18	D17	D16	
Servo coefficient setting	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	Gain DCLV1	Gain DCLV0	PCC1	PCC0	Valid only when DCLV = 1.
CLV CTRL ($DX)				Gain CLVS					Valid when DCLV = 1 or 0.

The spindle servo gain is externally set when DCLV = 1.

• CLVS mode gain setting: GCLVS

Gain MDS1	Gain MDS0	Gain CLVS	GCLVS
0	0	0	–12dB
0	0	1	–6dB
0	1	0	–6dB
0	1	1	0dB
1	0	0	0dB
1	0	1	+6dB

Note) When DCLV = 0, the CLVS gain is as follows.
When Gain CLVS = 0, GCLVS = –12dB.
When Gain CLVS = 1, GCLVS = 0dB.

• CLVP mode gain setting: GMDP: GMDS

Gain MDP1	Gain MDP0	GMDP
0	0	–6dB
0	1	0dB
1	0	+6dB

Gain MDS1	Gain MDS0	GMDS
0	0	–6dB
0	1	0dB
1	0	+6dB

• DCLV overall gain setting: GDCLV

Gain DCLV1	Gain DCLV0	GDCLV
0	0	0dB
0	1	+6dB
1	0	+12dB

Command bit		Processing
PCC1	PCC0	
0	0	The VPCO1 and 2 signals are output.
0	1	The VPCO1 and 2 pin outputs are high impedance.
1	0	The VPCO1 and 2 pin outputs are low.
1	1	The VPCO1 and 2 pin outputs are high.

• This command controls the VPCO1 and VPCO2 pin signals.

Identical control can be performed for both VPCO1 and VPCO2 output with this setting. However, VPCO2 can also be set to high impedance with the $E command FCSW separately from this setting.

• Processing for the $CX commands PCC1 and PCC2 and the $EX command FCSW is shown below.

Command bit			Processing
FCSW	PCC1	PCC0	
0	0	0	The VPCO1 signal is output and the VPCO2 pin is high impedance.
0	0	1	The VPCO1 and 2 pin outputs are high impedance.
0	1	0	The VPCO1 pin output is low and the VPCO2 pin is high impedance.
0	1	1	The VPCO1 pin output is high and the VPCO2 pin is high impedance.
1	0	0	The VPCO1 and 2 signals are output.
1	0	1	The VPCO1 and 2 pin outputs are high impedance.
1	1	0	The VPCO1 and 2 pin outputs are low.
1	1	1	The VPCO1 and 2 pin outputs are high.

$DX commands

Command	Data 1			
	D23	D22	D21	D20
CLV CTRL	DCLV PWM MD	TB	TP	Gain CLVS

See "$CX commands".

Command bit	Description
DCLV PWM MD = 1	Digital CLV PWM mode specified. Both MDS and MDP are used. CLV-W and CAV-W modes cannot be used.
DCLV PWM MD = 0	Digital CLV PWM mode specified. Ternary MDP values are output. CLV-W and CAV-W modes can be used.

Command bit	Description
TB = 0	Bottom hold at a cycle of RFCK/32 in CLVS and CLVH modes.
TB = 1	Bottom hold at a cycle of RFCK/16 in CLVS and CLVH modes.
TP = 0	Peak hold at a cycle of RFCK/4 in CLVS mode.
TP = 1	Peak hold at a cycle of RFCK/2 in CLVS mode.

Command	Data 2				Data 3				Data 4			
	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8
CLV CTRL	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	VP CTL1	VP CTL0	0	0

Command bit	Processing
VP0 to 7	The spindle rotational velocity is set.

Command bit		Processing
VPCTL1	VPCTL0	
0	0	The setting of VP0 to 7 is multiplied by 1.
0	1	The setting of VP0 to 7 is multiplied by 2.
1	0	The setting of VP0 to 7 is multiplied by 3.
1	1	The setting of VP0 to 7 is multiplied by 4.

* The above setting should be 0, 0 except for the CAV-W operating mode.

The rotational velocity R of the spindle can be expressed with the following equation.

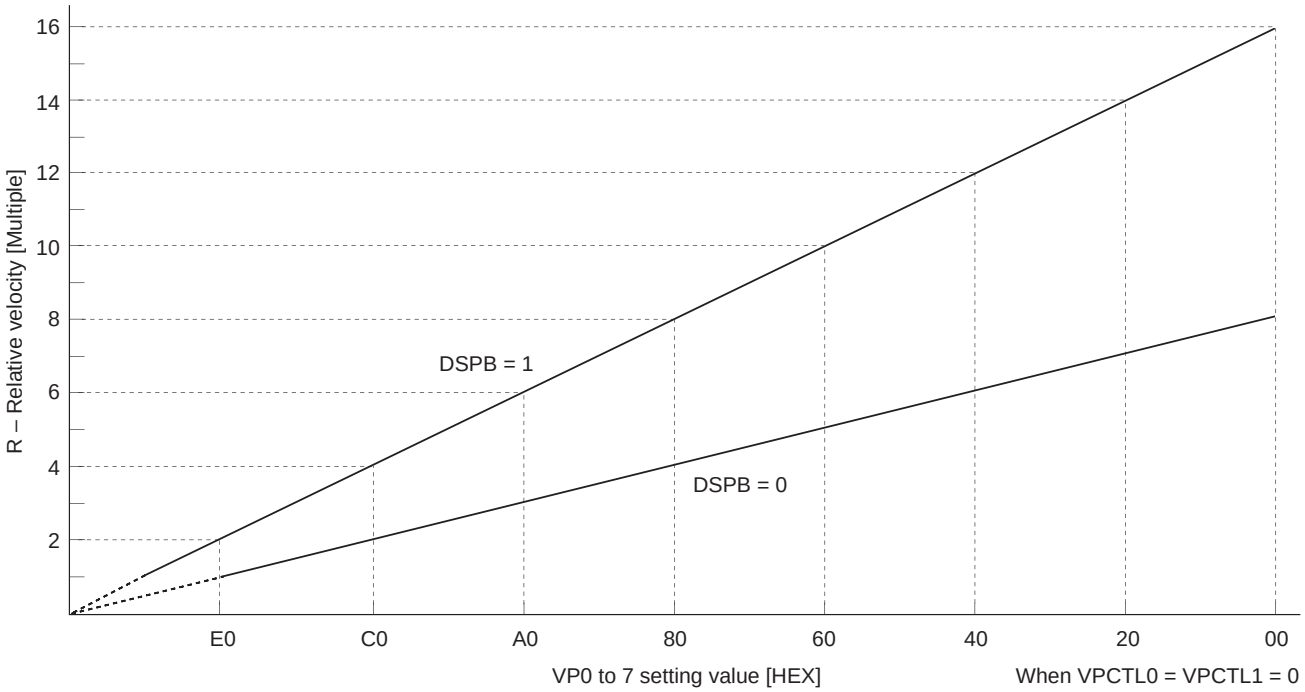
$$R = \frac{256 - n}{32} \times I$$

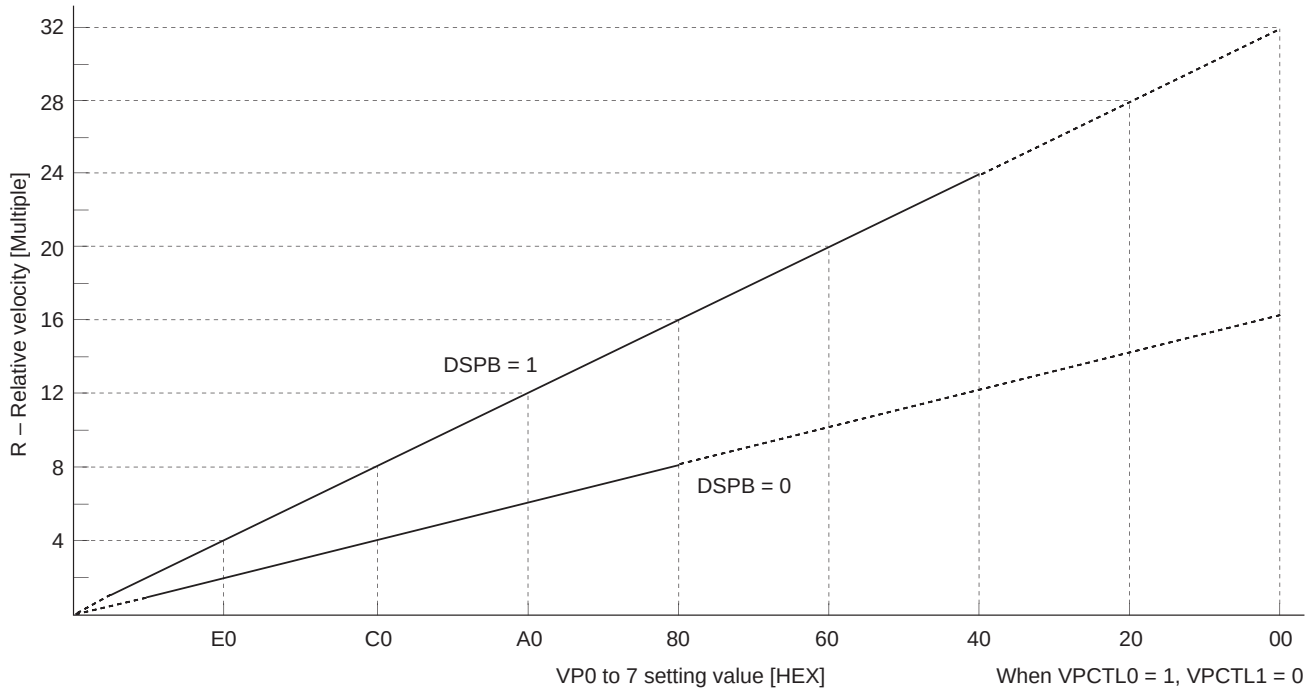
R: Relative velocity at normal speed = 1
n: VP0 to 7 setting value
I: Multiple by VPCTL0, 1

Command bit	Description
VP0 to 7 = F0 (H)	Playback at 1/2 (1, 2) × speed
:	to
VP0 to 7 = E0 (H)	Playback at 1 (2, 4) × speed
:	to
VP0 to 7 = C0 (H)	Playback at 2 (4, 8) × speed
:	to
VP0 to 7 = A0 (H)	Playback at 3 (6, 12) × speed
:	to
VP0 to 7 = 80 (H)	Playback at (8, 16) × speed
:	to
VP0 to 7 = 60 (H)	Playback at (10, 20) × speed
:	to
VP0 to 7 = 40 (H)	Playback at (12, 24) × speed
VP0 to 7 = 20 (H)	Playback at (14, –) × speed
VP0 to 7 = 00 (H)	Playback at (16, –) × speed

Notes)

1. Values when crystal is 16.9344MHz and XTSL is low or when crystal is 33.8688MHz and XTLS is high.
2. Regarding the values in parentheses, the former ones are for when DSPB = 1 and VPCTL0, 1 = 0, and the latter ones are for when DSPB = 1, VPCTL0 = 1 and VPCTL1 = 0.


16
14
12
10
8
6
4
2
R – Relative velocity [Multiple]
DSPB = 1
DSPB = 0
E0
C0
A0
80
60
40
20
00
VP0 to 7 setting value [HEX]
When VPCTL0 = VPCTL1 = 0


32
28
24
20
16
12
8
4
R – Relative velocity [Multiple]
DSPB = 1
DSPB = 0
E0
C0
A0
80
60
40
20
00
VP0 to 7 setting value [HEX]
When VPCTL0 = 1, VPCTL1 = 0

$EX commands

Command	Data 1				Data 2				Data 3			
	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
SPD mode	CM3	CM2	CM1	CM0	EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON

Command bit				Mode	Description
CM3	CM2	CM1	CM0		
0	0	0	0	STOP	Spindle stop mode.*
1	0	0	0	KICK	Spindle forward rotation mode.*
1	0	1	0	BRAKE	Spindle reverse rotation mode. Valid only when LPWR = 0 in any mode.*
1	1	1	0	CLVS	Rough servo mode. When the RF-PLL circuit isn't locked, this mode is used to pull the disc rotations within the RF-PLL capture range.
1	1	1	1	CLVP	PLL servo mode.
0	1	1	0	CLVA	Automatic CLVS/CLVP switching mode. Used for normal playback.

* See Timing Charts 1-6 to 1-12.

Command bit									Mode	Description
EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON	INV VPCO		
0	0	0	0	0	0	0	0	0	CLV-N	Crystal reference CLV servo.
0	0	0	0	1	1	0	0	0	CLV-W	Used for playback in CLV-W mode.*1
0	1	1	0	0	1	0	1	0	CAV-W	Spindle control with VP0 to 7.
1	0	1	0	0	1	0	1	0	CAV-W	Spindle control with the external PWM.
0	0	0	0	0	1	0	1	1	VCO-C	VCO control.*2

*1 Figs. 3-1 and 3-2 show the control flow with the microcomputer software in CLV-W mode.

*2 Fig. 3-3 shows the control flow with the microcomputer software in VCO-C mode.

Mode	DCLV	DCLV PWM MD	LPWR	Command	Timing chart
CLV-N	0	0	0	KICK	1-6 (a)
				BRAKE	1-6 (b)
				STOP	1-6 (c)
	1	0	0	KICK	1-7 (a)
				BRAKE	1-7 (b)
				STOP	1-7 (c)
		1	0	KICK	1-8 (a)
				BRAKE	1-8 (b)
				STOP	1-8 (c)
CLV-W	1	0	0	KICK	1-9 (a)
				BRAKE	1-9 (b)
				STOP	1-9 (c)
			1	KICK	1-10 (a)
				BRAKE	1-10 (b)
				STOP	1-10 (c)
CAV-W	1	0	0	KICK	1-11 (a)
				BRAKE	1-11 (b)
				STOP	1-11 (c)
			1	KICK	1-12 (a)
				BRAKE	1-12 (b)
				STOP	1-12 (c)

Mode	DCLV	DCLV PWM MD	LPWR	Timing chart
CLV-N	1	0	0	1-13
		1	0	1-14
CLV-W	1	0	0	1-15
			1	1-16
CAV-W	1	0	0	1-17 (EPWM = 0)
			1	1-18 (EPWM = 0)
			0	1-19 (EPWM = 1)
			1	1-20 (EPWM = 1)

Note) CLV-W and CAV-W modes support control only by the ternary output of the MDP pin. Therefore, set DCLV to 1 and DCLV PWM MD to 0 in CLV-W and CAV-W modes.

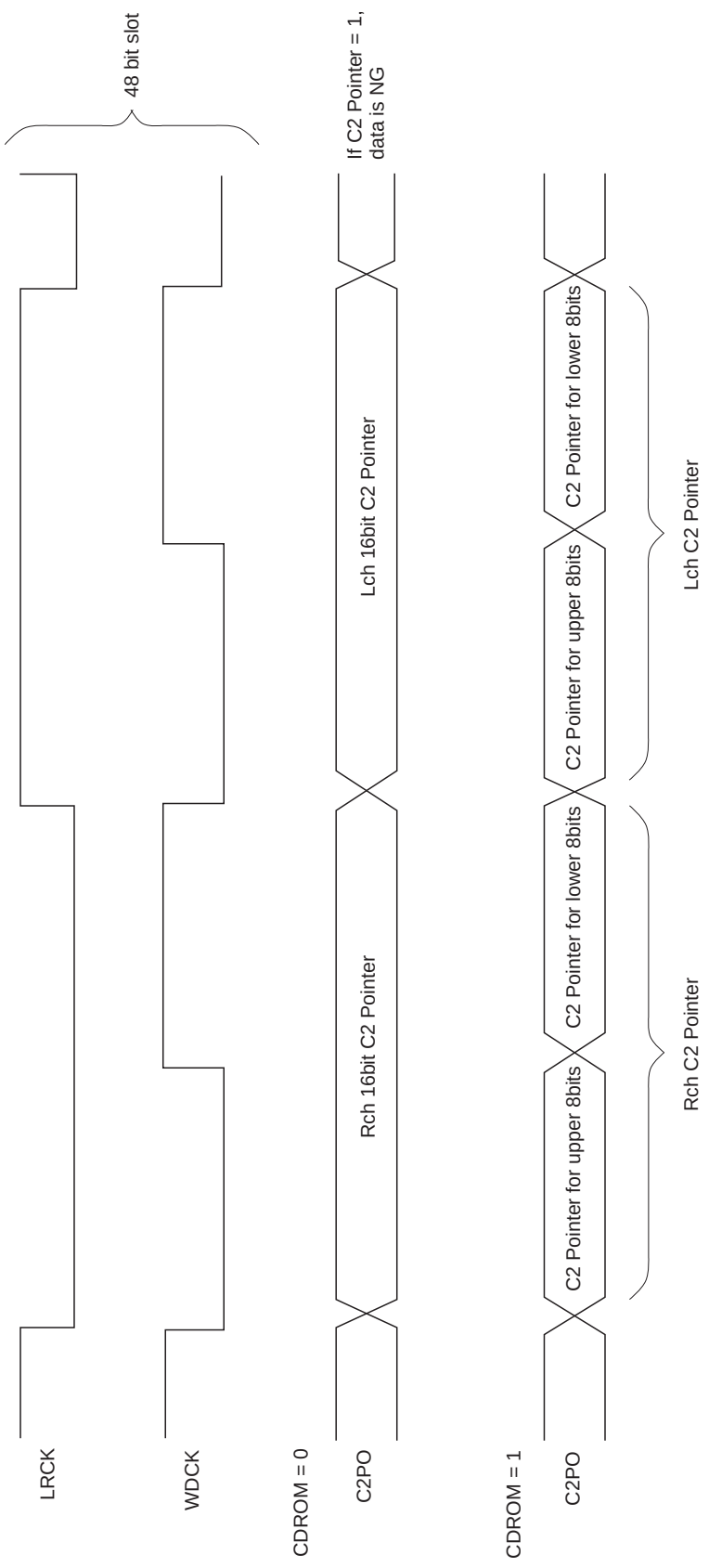
Command	Data 4			
	D11	D10	D9	D8
SPD mode	Gain CAV1	Gain CAV0	FCSW	INV NPCO

Gain CAV1	Gain CAV0	Gain
0	0	0dB
0	1	–6dB
1	0	–12dB
1	1	–18dB

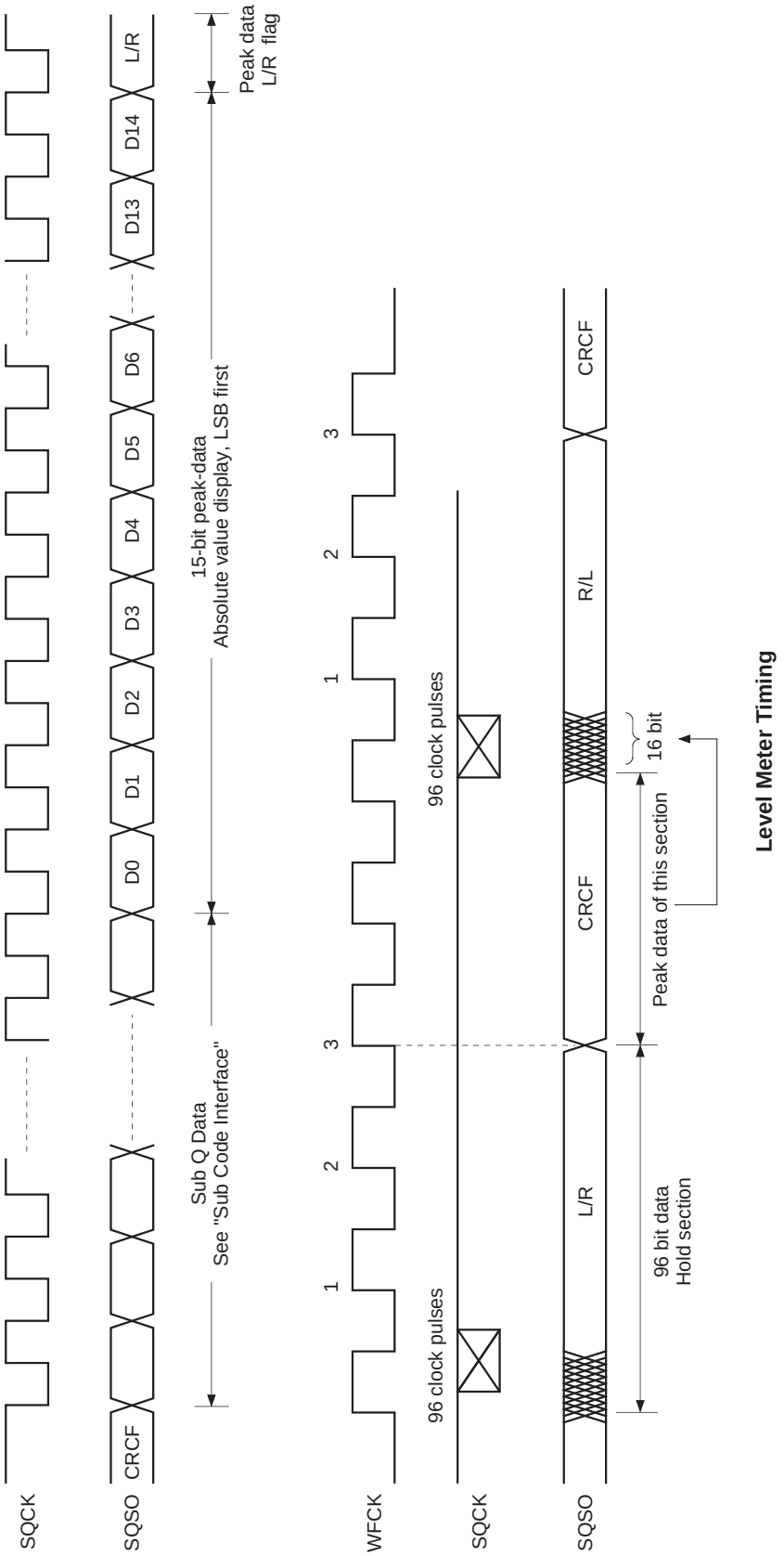
• This sets the gain when controlling the spindle with the phase comparator in CAV-W mode.

Command bit	Processing
FCSW = 0	The VPCO2 pin is not used and it is high impedance.
FCSW = 1	The VPCO2 pin is used and the pin signal is the same as VPCO1.

Timing Chart 1-3

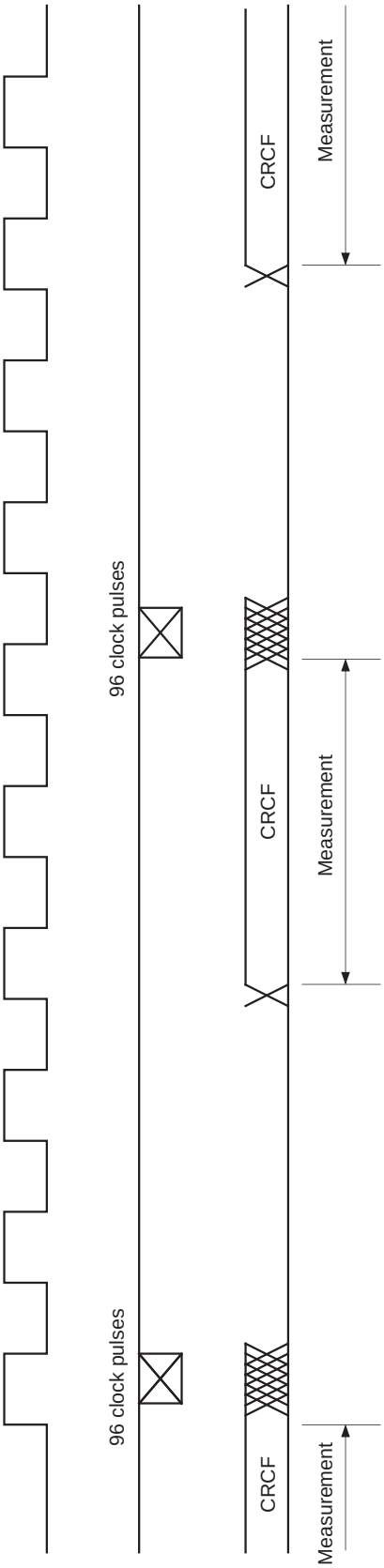


Timing Chart 1-4



Level Meter Timing

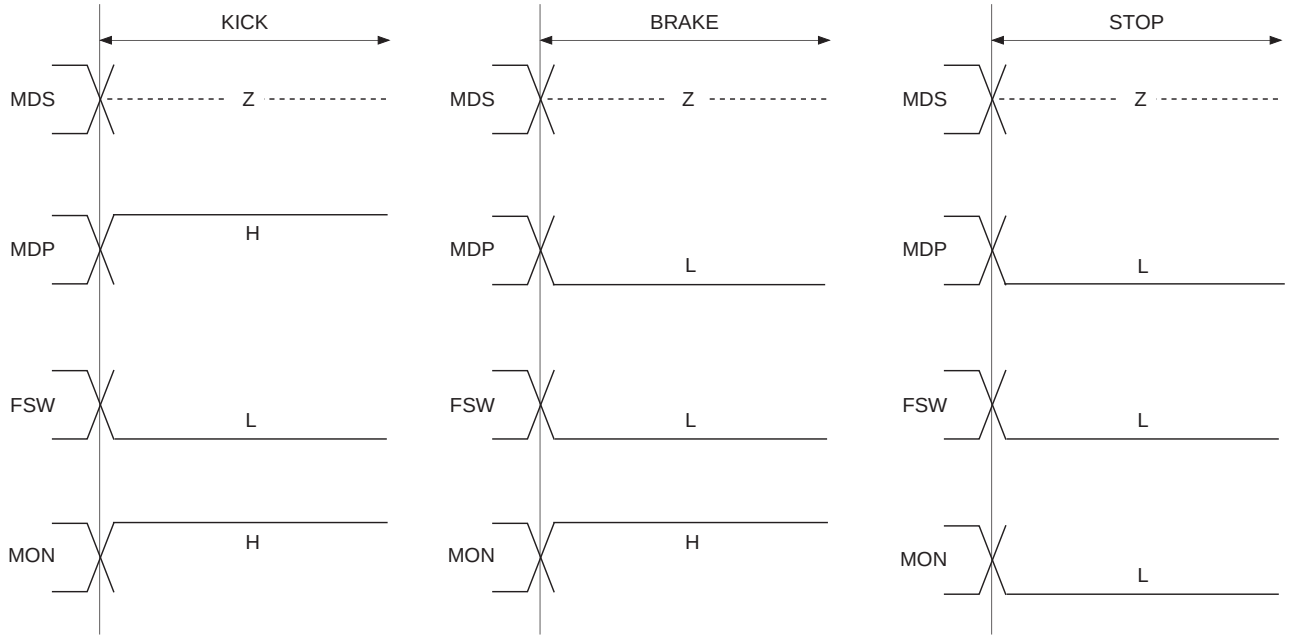
Timing Chart 1-5



Peak Meter Timing

Timing Chart 1-6

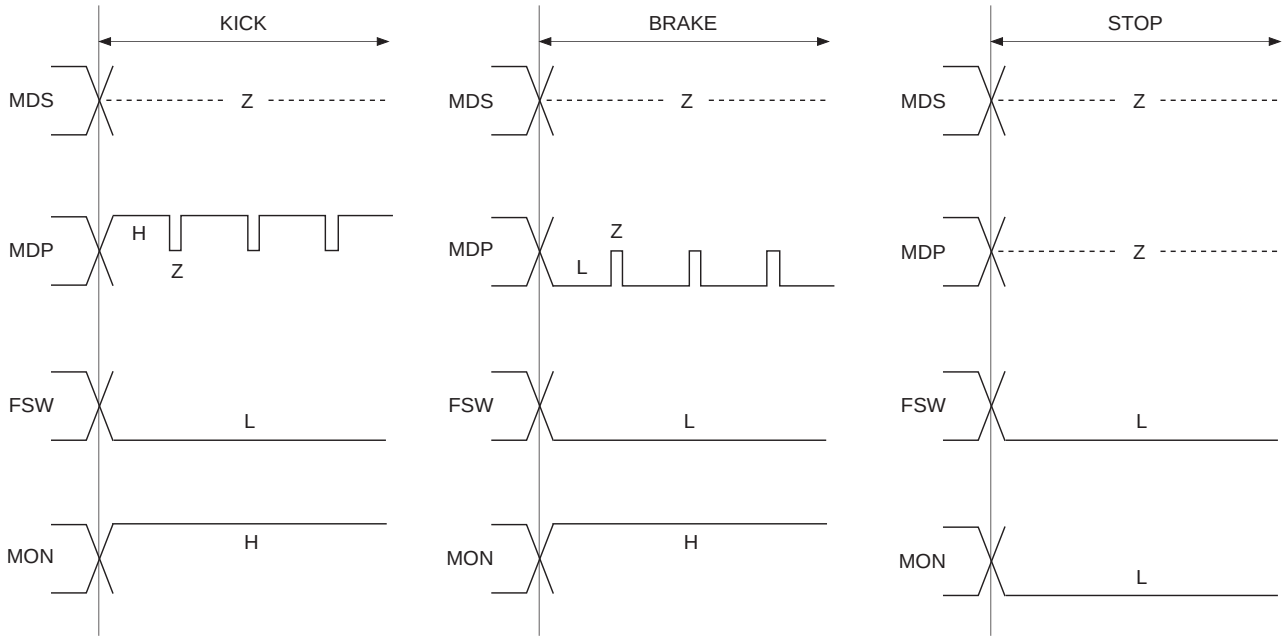
CLV-N mode DCLV = DCLV PWM MD = LPWR = 0



(a) KICK (b) BRAKE (c) STOP

Timing Chart 1-7

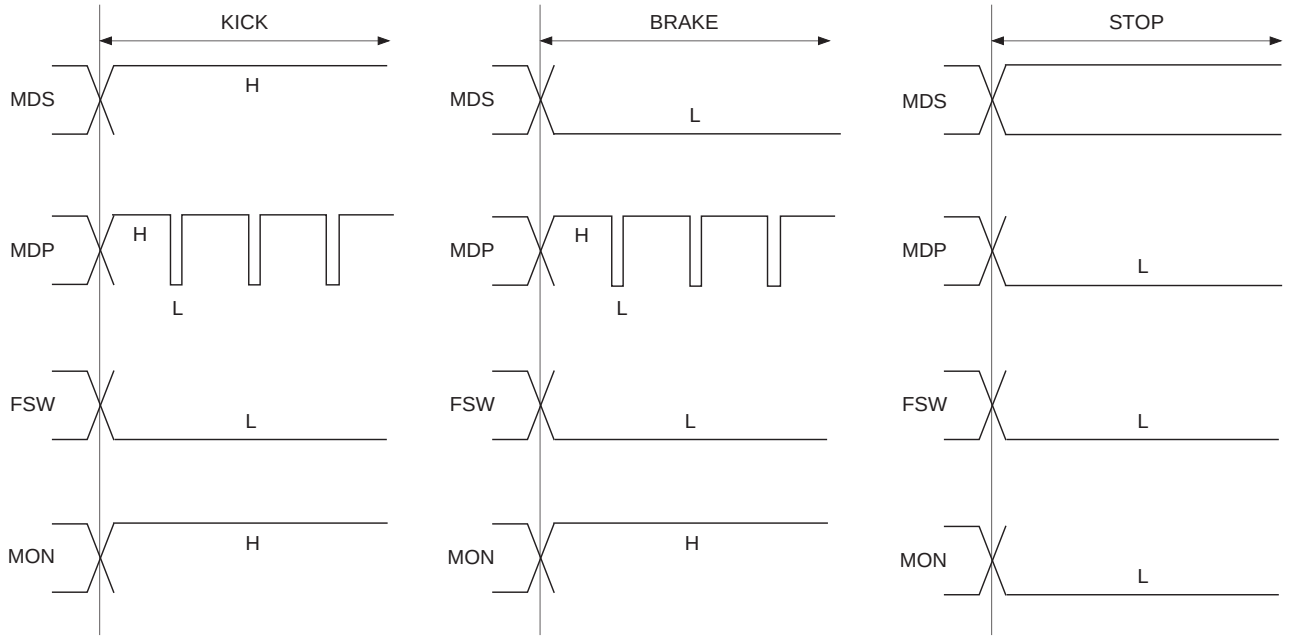
CLV-N mode DCLV = 1, DCLV PWM MD = LPWR = 0



(a) KICK (b) BRAKE (c) STOP

Timing Chart 1-8

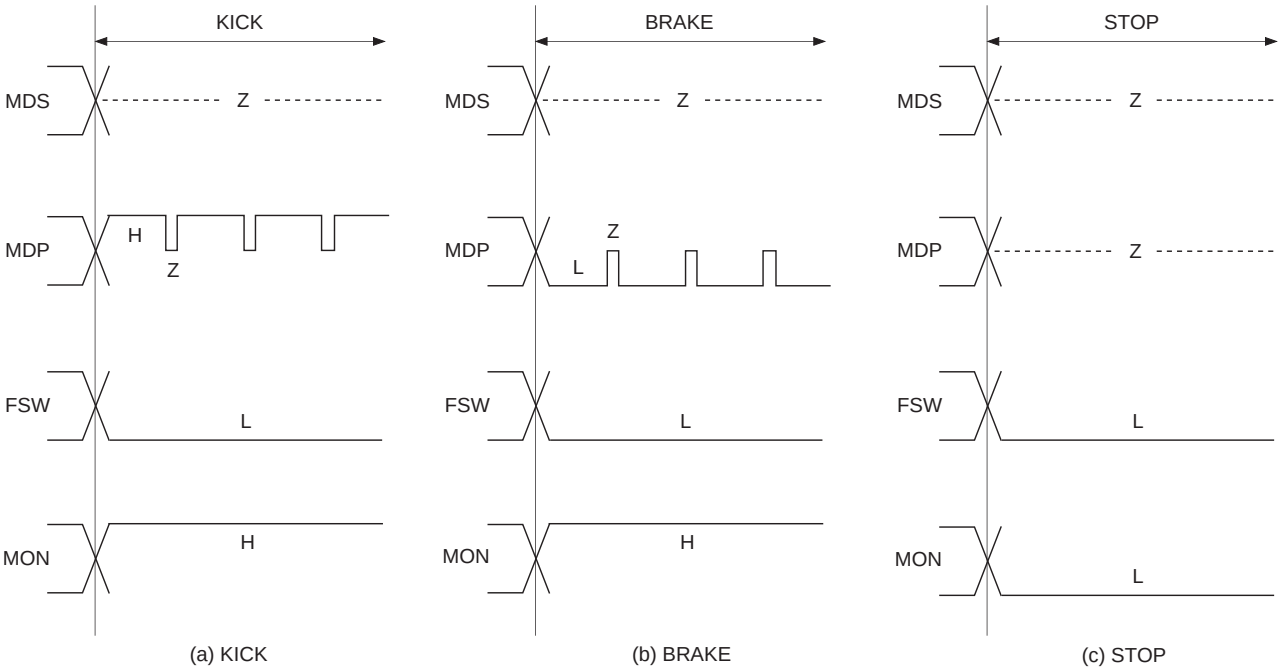
CLV-N mode DCLV = DCLV PWM MD = 1, LPWR = 0



(a) KICK (b) BRAKE (c) STOP

Timing Chart 1-9

CLV-W mode (when following the spindle rotational velocity) DCLV = 1, DCLV PWM MD = LPWR = 0



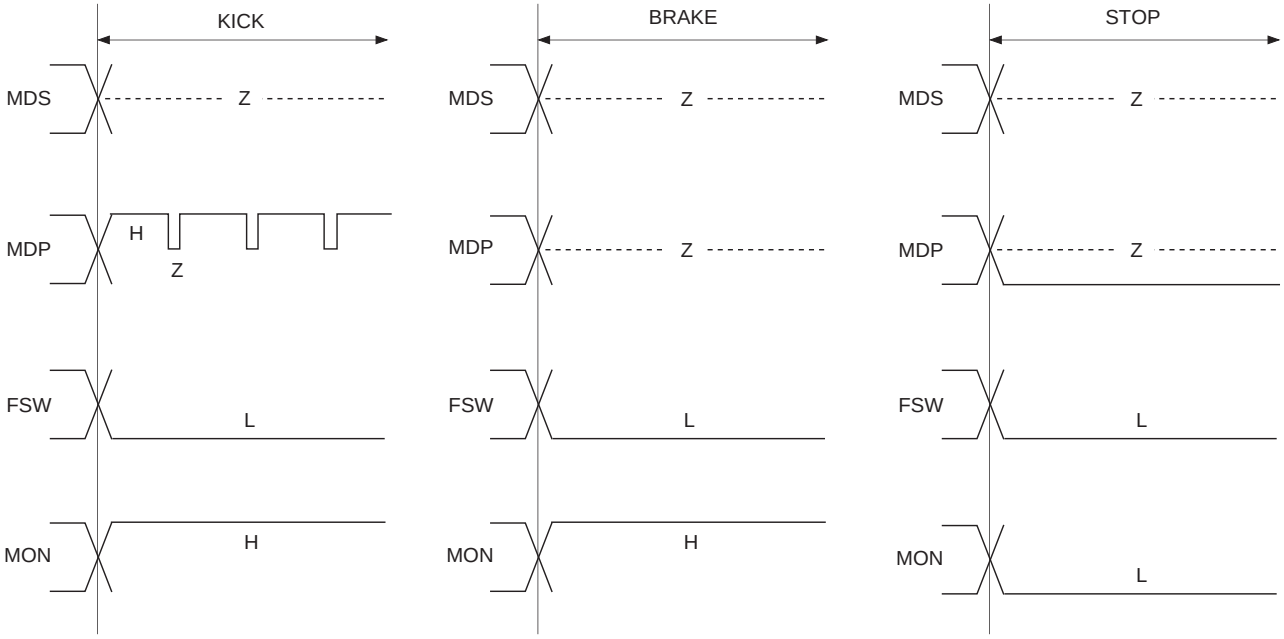
(a) KICK (b) BRAKE (c) STOP

Other than when following the velocity, the timing is the same as Timing Chart 1-6 (a).

Other than when following the velocity, the timing is the same as Timing Chart 1-6 (b).

Timing Chart 1-10

CLV-W mode (when following the spindle rotational velocity) DCLV = 1, DCLV PWM MD = 0, LPWR = 1

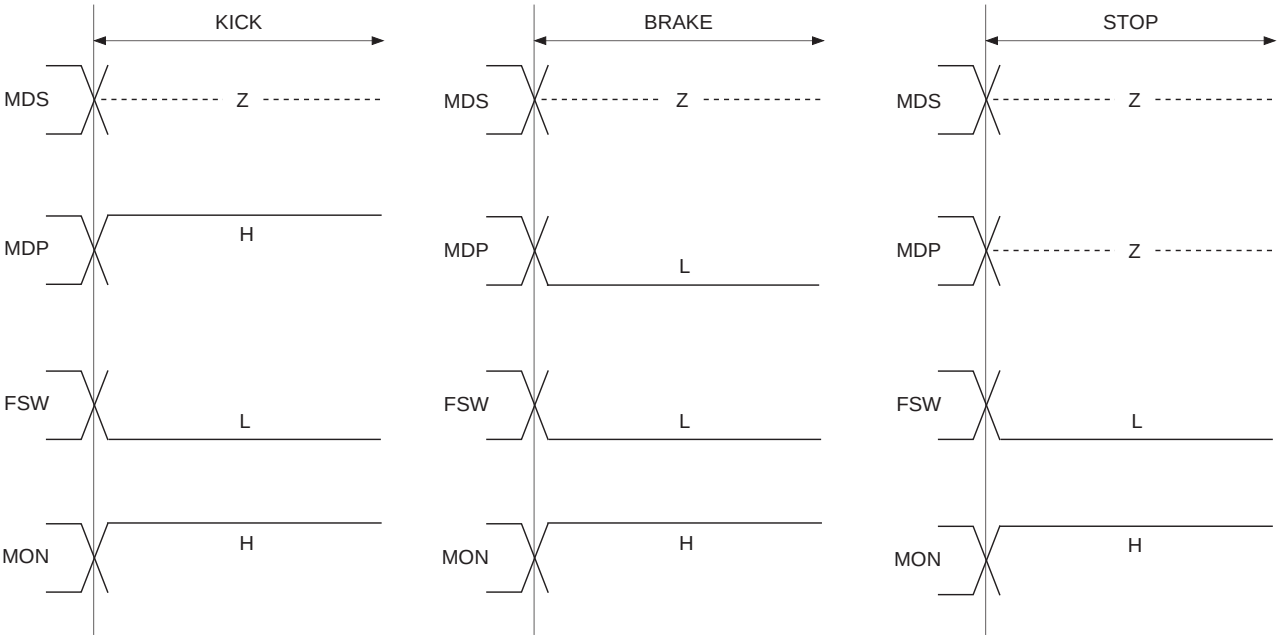


(a) KICK (b) BRAKE (c) STOP

Other than when following the velocity,
the timing is the same as Timing Chart 1-6 (a).

Timing Chart 1-11

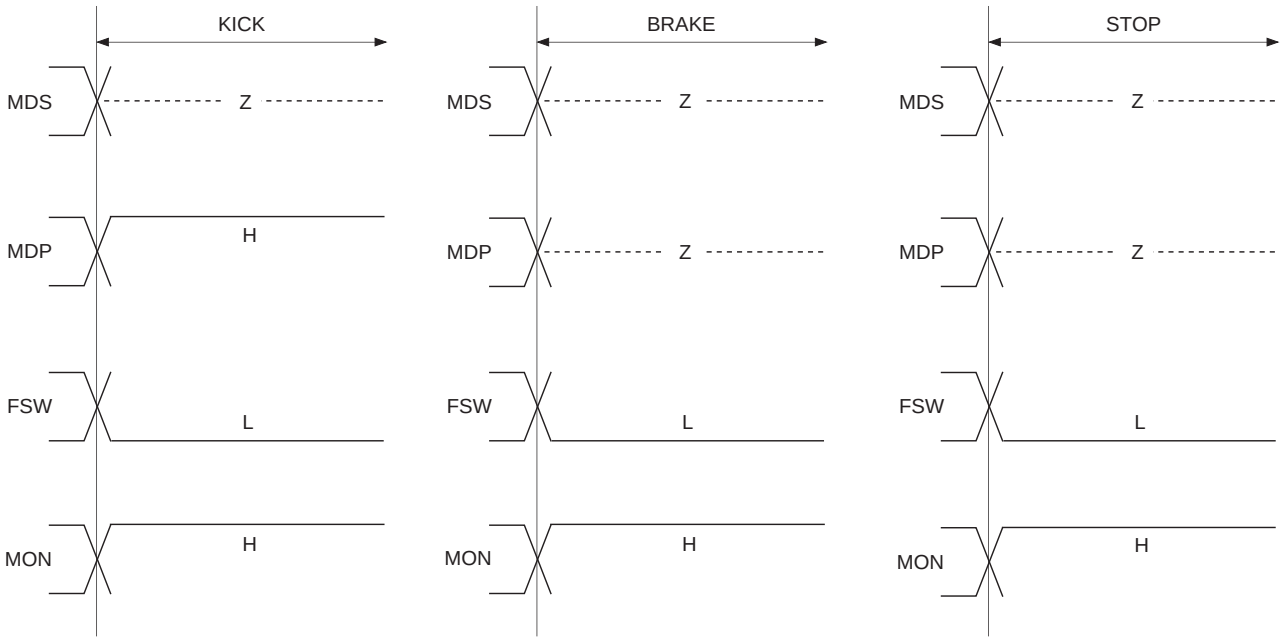
CAV-W mode DCLV = 1, DCLV PWM MD = LPWR = 0



(a) KICK (b) BRAKE (c) STOP

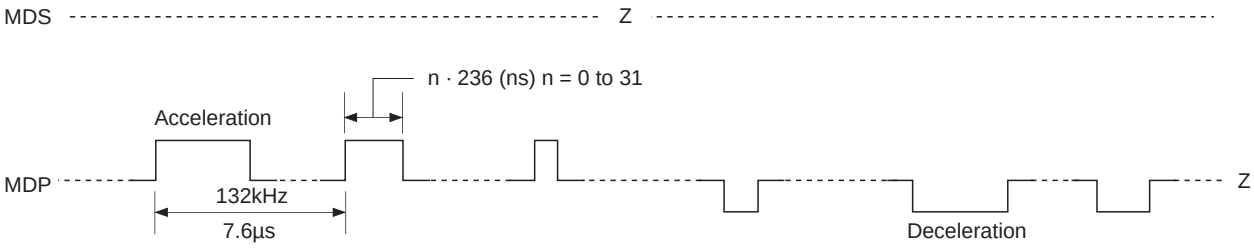
Timing Chart 1-12

CAV-W mode DCLV = 1, DCLV PWM MD = 0, LPWR = 1



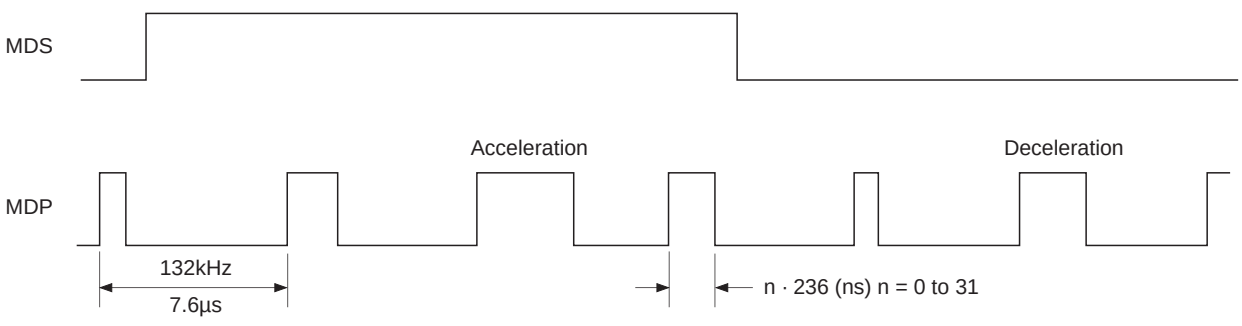
Timing Chart 1-13

CLV-N mode DCLV PWM MD = LPWR = 0



Timing Chart 1-14

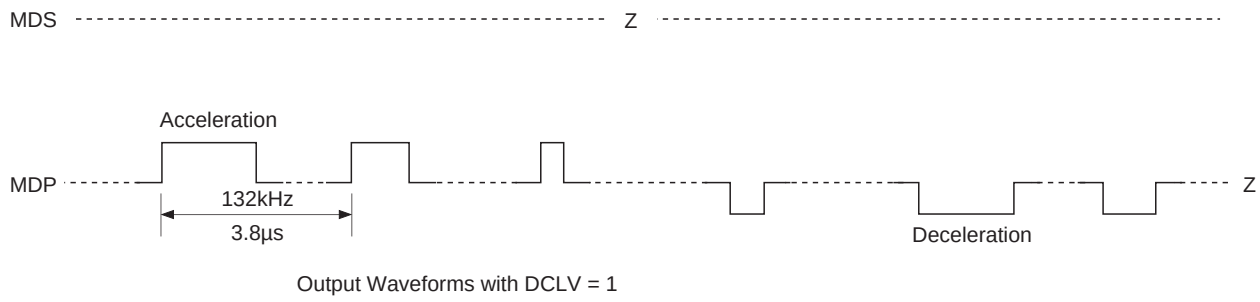
CLV-N mode DCLV PWM MD = 1, LPWR = 0



Output Waveforms with DCLV = 1

Timing Chart 1-15

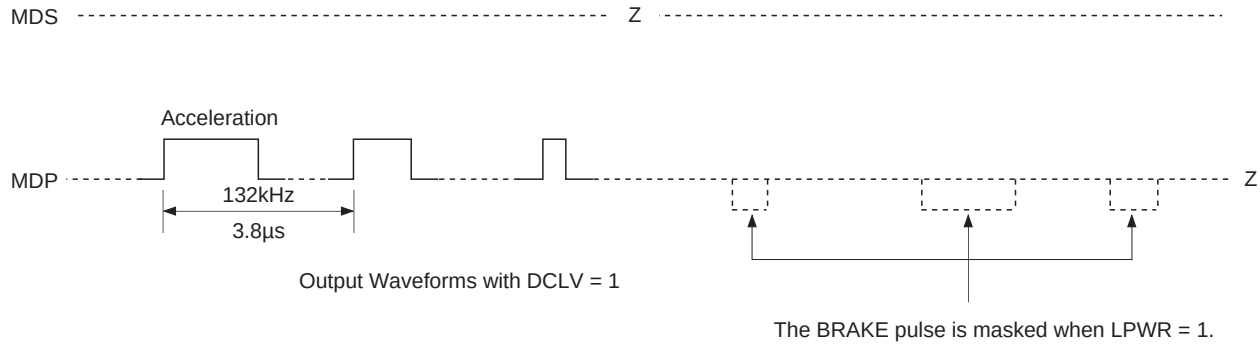
CLV-W mode DCLV PWM MD = LPWR = 0



Output Waveforms with DCLV = 1

Timing Chart 1-16

CLV-W mode DCLV PWM MD = 0, LPWR = 1

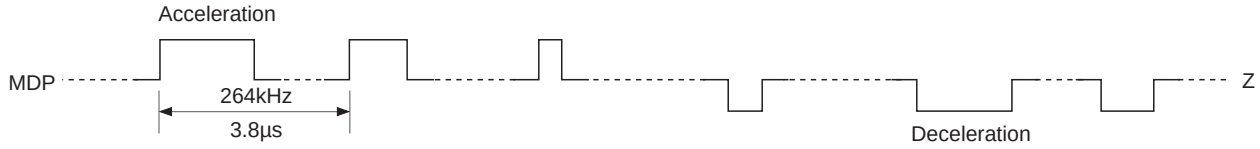


Output Waveforms with DCLV = 1

The BRAKE pulse is masked when LPWR = 1.

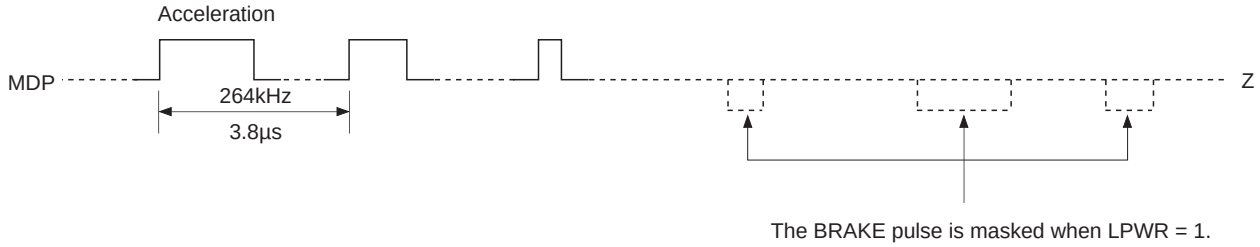
Timing Chart 1-17

CAV-W mode EPWM = DCLV PWM MD = LPWR = 0



Timing Chart 1-18

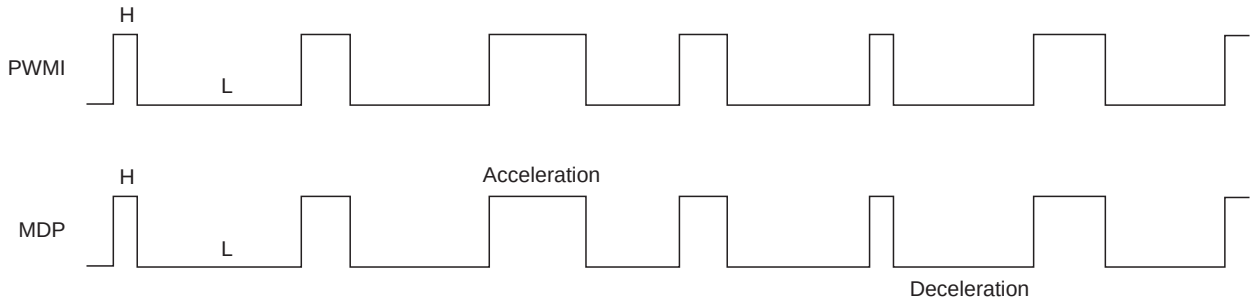
CAV-W mode EPWM = DCLV PWM MD = 0, LPWR = 1



The BRAKE pulse is masked when LPWR = 1.

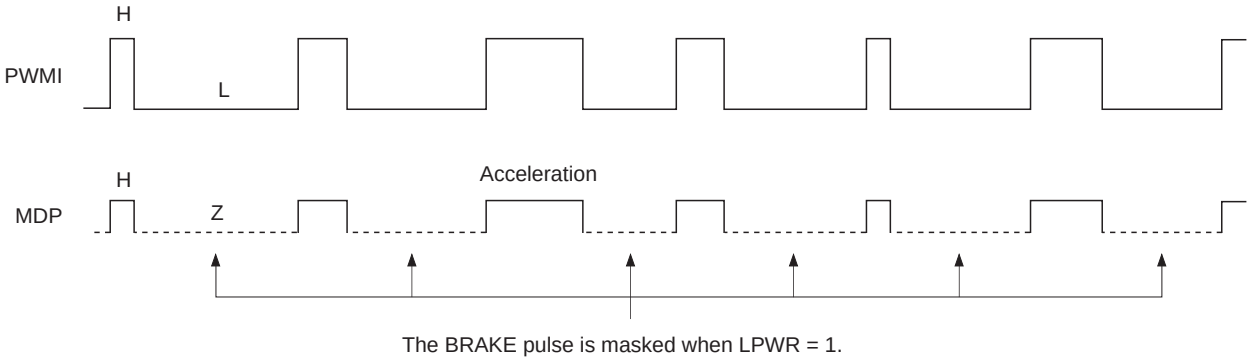
Timing Chart 1-19

CAV-W mode EPWM = 1, DCLV PWM MD = LPWR = 0



Timing Chart 1-20

CAV-W mode EPWM = 1, DCLV PWM MD = 0, LPWR = 1



Note) CLV-W and CAV-W modes support control only by the ternary output of the MDP pin. Therefore, set DCLV PWM MD to 0 in CLV-W and CAV-W modes.

[2] Subcode Interface

There are two methods for reading out a subcode externally.
The 8-bit subcodes P to W can be read out from SBSO by inputting EXCK.
Sub Q can be read out after checking CRC of the 80 bits in the subcode frame.
Sub Q can be read out from the SQSO pin by inputting 80 clock pulses to the SQCK pin when SCOR comes correctly and CRCF is high.

§2-1. P to W Subcode Readout

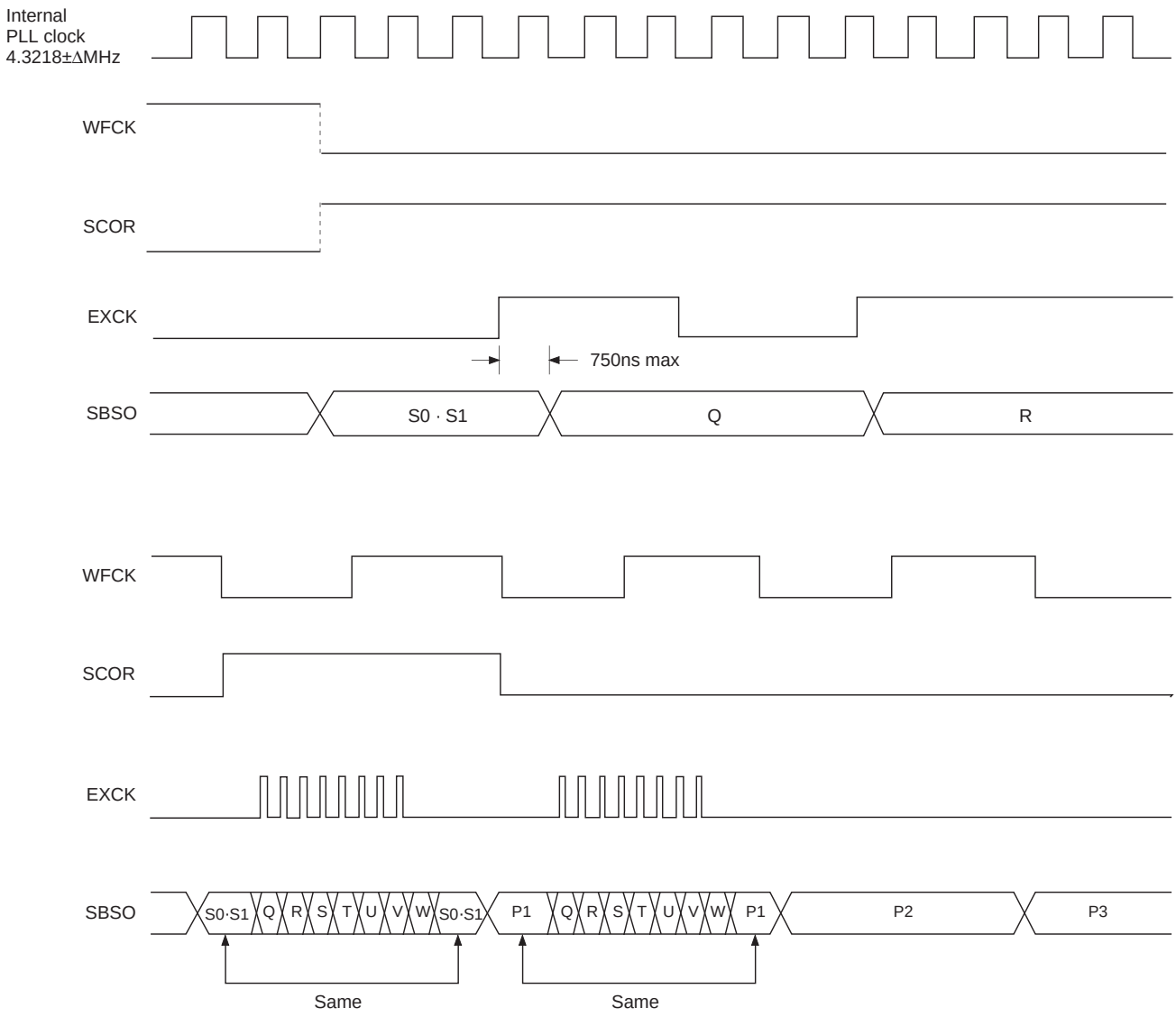
Data can be read out by inputting EXCK immediately after WFCK falls. (See Timing Chart 2-1.)

§2-2. 80-bit Sub Q Readout

Fig. 2-2 shows the peripheral block of the 80-bit Sub Q register.

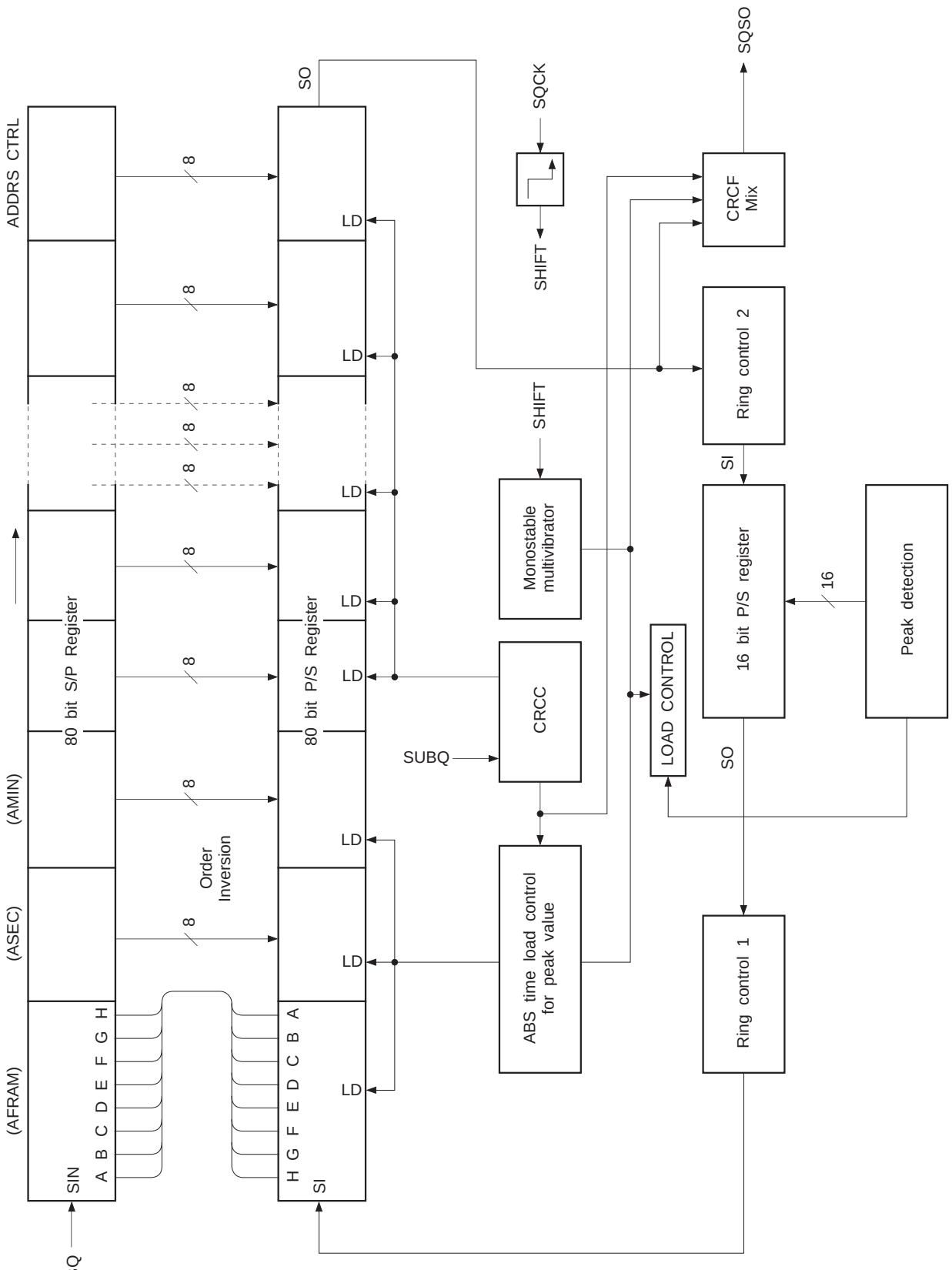
- First, Sub Q, regenerated at one bit per frame, is input to the 80-bit serial/parallel register and the CRC check circuit.
- 96-bit Sub Q is input, and if the CRC is OK, it is output to SQSO with CRCF = 1. In addition, 80 bits are loaded into the parallel/serial register.
  When SQSO goes high after SCOR is output, the CPU determines that new data (which passed the CRC check) has been loaded.
- When the 80-bit data is loaded, the order of the MSB and LSB is inverted within each byte. As a result, although the sequence of the bytes is the same, the bits within the bytes are now ordered LSB first.
- Once the 80-bit data load is confirmed, SQCK is input so that the data can be read.
  The SQCK input is detected, and the retriggerable monostable multivibrator is reset while the input is low.
- The retriggerable monostable multivibrator has a time constant from 270 to 400µs. When the duration when SQCK is high is less than this time constant, the monostable multivibrator is kept reset; during this interval, the serial/parallel register is not loaded into the parallel/serial register.
- While the monostable multivibrator is being reset, data cannot be loaded in the peak detection parallel/serial register or the 80-bit parallel/serial register.
  In other words, while reading out with a clock cycle shorter than this time constant, the register will not be rewritten by CRCOK and others.
- The previously mentioned peak detection register can be connected to the shift-in of the 80-bit parallel/serial register.
  For ring control 1, input and output are shorted during peak meter and level meter modes.
  For ring control 2, input and output are shorted during peak meter mode.
  This is because the register is reset with each readout in level meter mode, and to prevent readout destruction in peak meter mode.
  As a result, the 96-bit clock must be input in peak meter mode.
- The absolute time after peak is stored in the memory in peak meter mode. (See Timing Chart 2-3.)
- The high and low intervals for SQCK should be between 750ns and 120µs.

Timing Chart 2-1

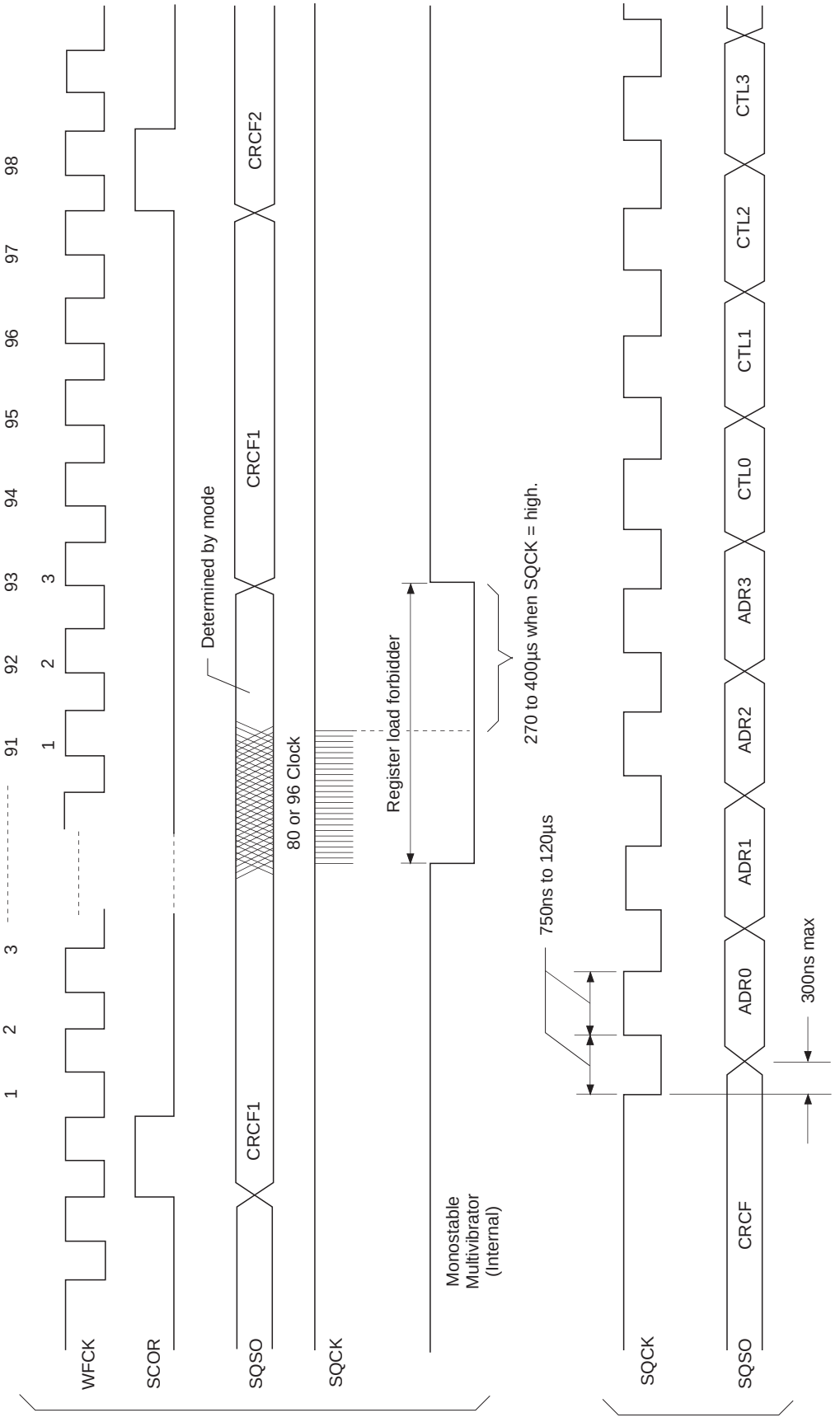


Subcode P.Q.R.S.T.U.V.W Read Timing

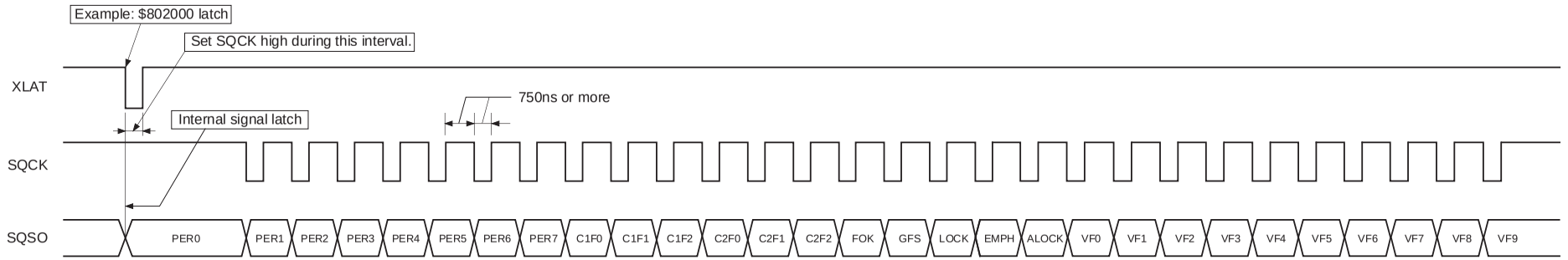
Block Diagram 2-2



Timing Chart 2-3



Timing Chart 2-4

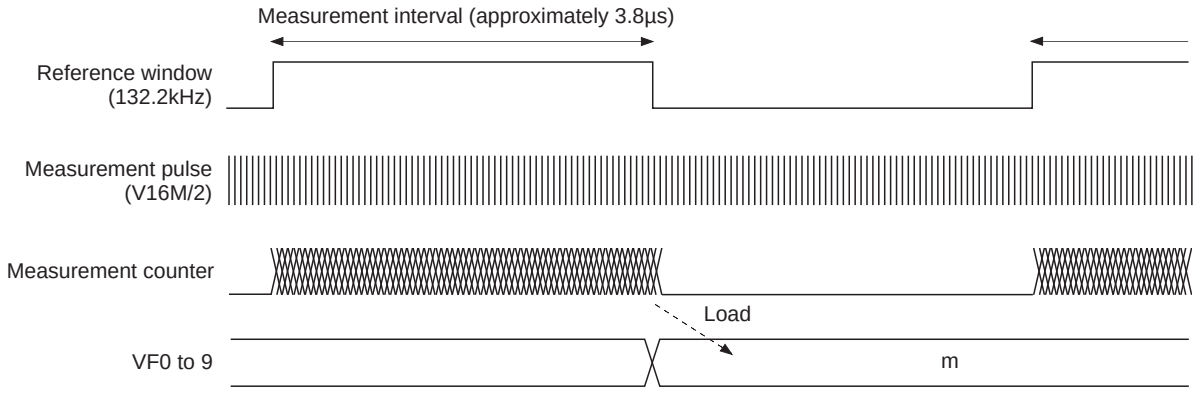


Signal	Description
PER0 to 7	RF jitter amount (used to adjust the focus bias). 8-bit binary data in PER0 = LSB, PER7 = MSB.
FOK	Focus OK
GFS	High when the frame sync and the insertion protection timing match.
LOCK	GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low.
EMPH	High when the playback disc has emphasis.
ALOCK	GFS is sampled at 460Hz; when GFS is high eight consecutive samples, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low.
VF0 to 9	Used in CAV-W mode. The result obtained by measuring the rotational velocity of the disc. (See Timing Chart 2-5.) VF0 = LSB, VF7 = MSB.

C1F2	C1F1	C1F0	Description
0	0	0	No C1 errors; C1 pointer reset
0	0	1	One C1 error corrected; C1 pointer reset
0	1	0	—
0	1	1	—
1	0	0	No C1 errors; C1 pointer set
1	0	1	One C1 error corrected; C1 pointer set
1	1	0	Two C1 errors corrected; C1 pointer set
1	1	1	C1 correction impossible; C1 pointer set

C2F2	C2F1	C2F0	Description
0	0	0	No C2 errors; C2 pointer reset
0	0	1	One C2 error corrected; C2 pointer reset
0	1	0	Two C2 errors corrected; C2 pointer reset
0	1	1	Three C2 errors corrected; C2 pointer reset
1	0	0	Four C2 errors corrected; C2 pointer reset
1	0	1	—
1	1	0	C2 correction impossible; C1 pointer copy
1	1	1	C2 correction impossible; C2 pointer set

Timing Chart 2-5



The relative velocity of the disc can be obtained with the following equation.

$$R = \frac{m + 1}{32}$$ (R: Relative velocity, m: Measurement results)

VF0 to 9 is the result obtained by counting VLKI/2 pulses while the reference signal (132.2kHz) generated from XTAL (XTLI, XTLO) (384Fs) is high. This value is 31 when the disc is rotating at normal speed and 63 when it is rotating at double speed (when DSPB is low).

[3] Description of Modes

This LSI has three basic operating modes using a combination of spindle control and the PLL. The operations for each mode are described below.

§3-1. CLV-N Mode

This mode is compatible with the CXD2510Q, and operation is the same as for conventional control (however, variable pitch cannot be used). The PLL capture range is ±150kHz.

§3-2. CLV-W Mode

This is the wide capture range mode. This mode allows PLL to follow the rotational velocity of the disc. This rotational following control has two types: using the built-in VCO2 or providing an external VCO. The spindle is the same CLV servo as for the conventional series. Operation using the built-in VCO2 is described below. (When using an external VCO, input the signal from the VPCO pin to the low-pass filter, use the output from the low-pass filter as the control voltage for the external VCO, and input the oscillation from the VCO to the VCKI pin.)

When starting to rotate the disc and/or speeding up to the lock range from the condition where the disc is stopped, CAV-W mode should be used. Specifically, first send $E665X to set CAV-W mode and kick the disc, then send $E60CX to set CLV-W mode if ALOCK is high, which can be read out serially from the SQSO pin. CLV-W mode can be used while ALOCK is high. The microcomputer monitors the serial data output, and must return the operation to the speed adjusting state (CAV-W mode) when ALOCK becomes low. The control flow according to the microcomputer software in CLV-W mode is shown in Fig. 3-2.

In CLV-W mode (normal), low power consumption is achieved by setting LPWR to high. Control was formerly performed by applying acceleration and deceleration pulses to the spindle motor. However, when LPWR is set high, deceleration pulses are not output, thereby achieving low power consumption mode.

CLV-W mode supports control only by the ternary output of the MDP pin. Therefore, when using CLV-W mode, set DCLV PWM MD to low.

Note) The capture range for this mode is theoretically up to the signal processing limit.

§3-3. CAV-W Mode

This is CAV mode. In this mode, the external clock is fixed and it is possible to control the spindle to the desired rotational velocity. The rotational velocity is determined by the VP0 to 7 setting values or the external PWM. When controlling the spindle with VP0 to 7, setting CAV-W mode with the $E665X command and controlling VP0 to 7 with the $DX commands allows the rotational velocity to be varied from low speed to 20× speed. (See "$DX commands".) Also, when controlling the spindle with the external PWM, the PWMI pin is binary input which becomes KICK during high intervals and BRAKE during low intervals.

The microcomputer can know the rotational velocity using V16M. The reference frequency for the velocity measurement is a signal of 132.3kHz obtained by dividing XTAL (XTLI, XTLO) (384Fs) by 128. The velocity is obtained by counting V16M/2 pulses while the reference is high, and the result is output from the new CPU interface as 10 bits (VP0 to 9). These measurement results are 31 when the disc is rotating at normal speed or 127 when it is rotating at quadruple speed. These values match those of the 256 - n for control with VP0 to 7. (See Table 2-5 and Fig. 2-6.)

In CAV-W mode, the spindle is set to the desired rotational velocity and the operation speed for the entire system follows this rotational velocity. Therefore, the cycles for the Fs system clock, PCM data and all other output signals from this LSI change according to the rotational velocity of the disc.

Note) The capture range for this mode is theoretically up to the signal processing limit.

Note) Set FLFC to 1 for this mode

§3-4. VCO-C Mode

This is the VCO control mode. In this mode, the V16M oscillation frequency can be controlled by setting VP0 to 7, VPCTL0 and 1 of $D.

$$V16M = \frac{1\ (256 - n)}{32}$$

n: Setting value of VP0 to 7
1: Setting value of VPCTL0 and 1

V16M determines the VCO1 oscillation frequency. The VCO1 frequency can be expressed with the following equations.

- DSPB = 0

$$VCO1 = V16M \times \frac{49}{24}$$

- DSPB = 1

$$VCO1 = V16M \times \frac{49}{16}$$

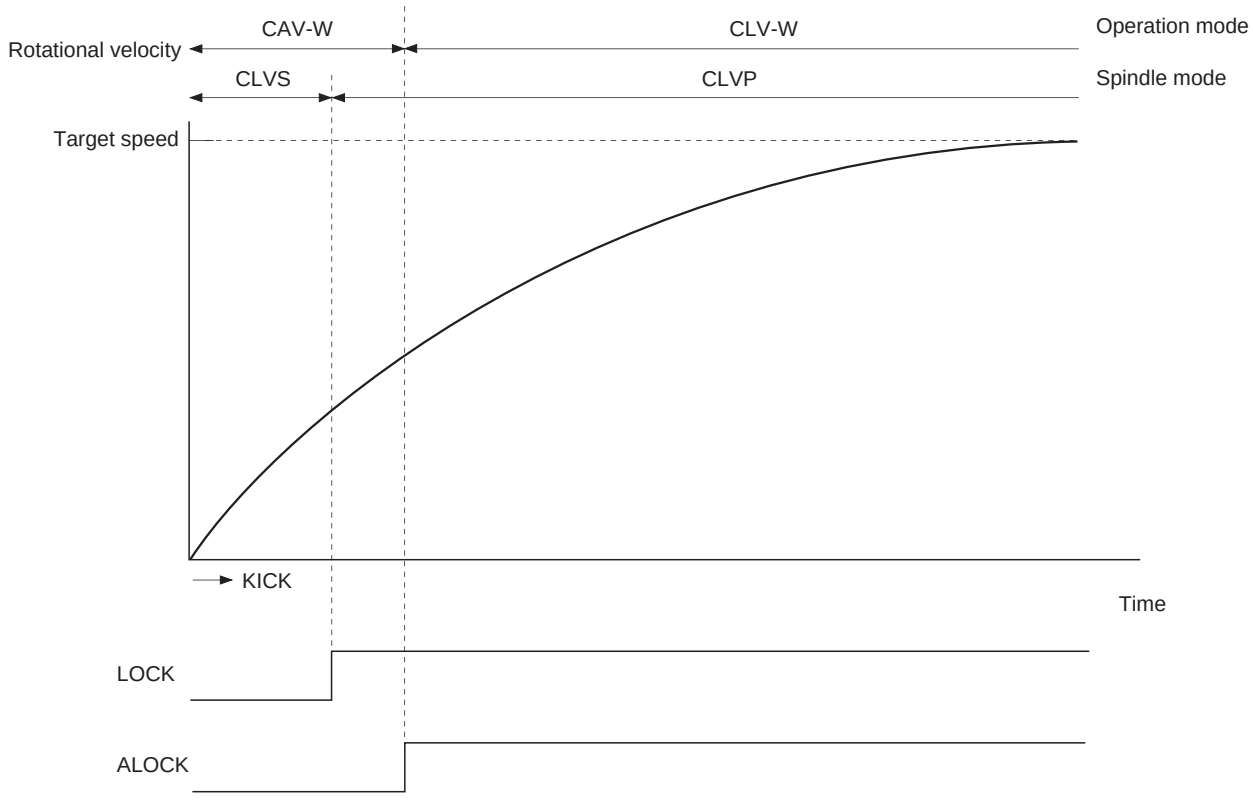


Fig. 3-1. Disc Stop to Regular Playback in CLV-W Mode

CLV-W Mode

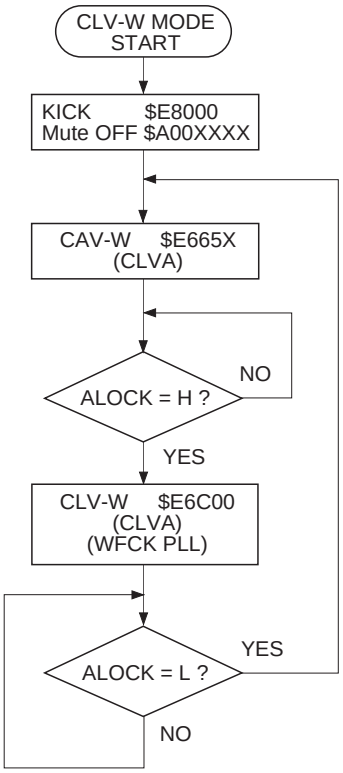


Fig. 3-2. CLV-W Mode Flow Chart

VCO-C Mode

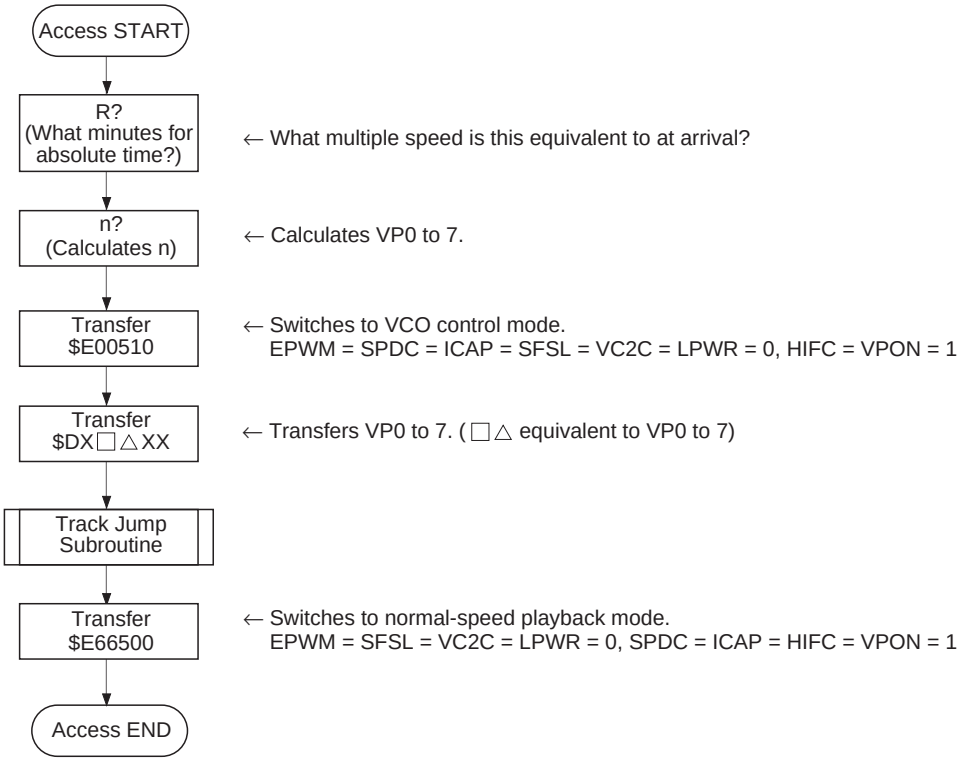


Fig. 3-3. Access Flow Chart Using VCO Control

[4] Description of Other Functions

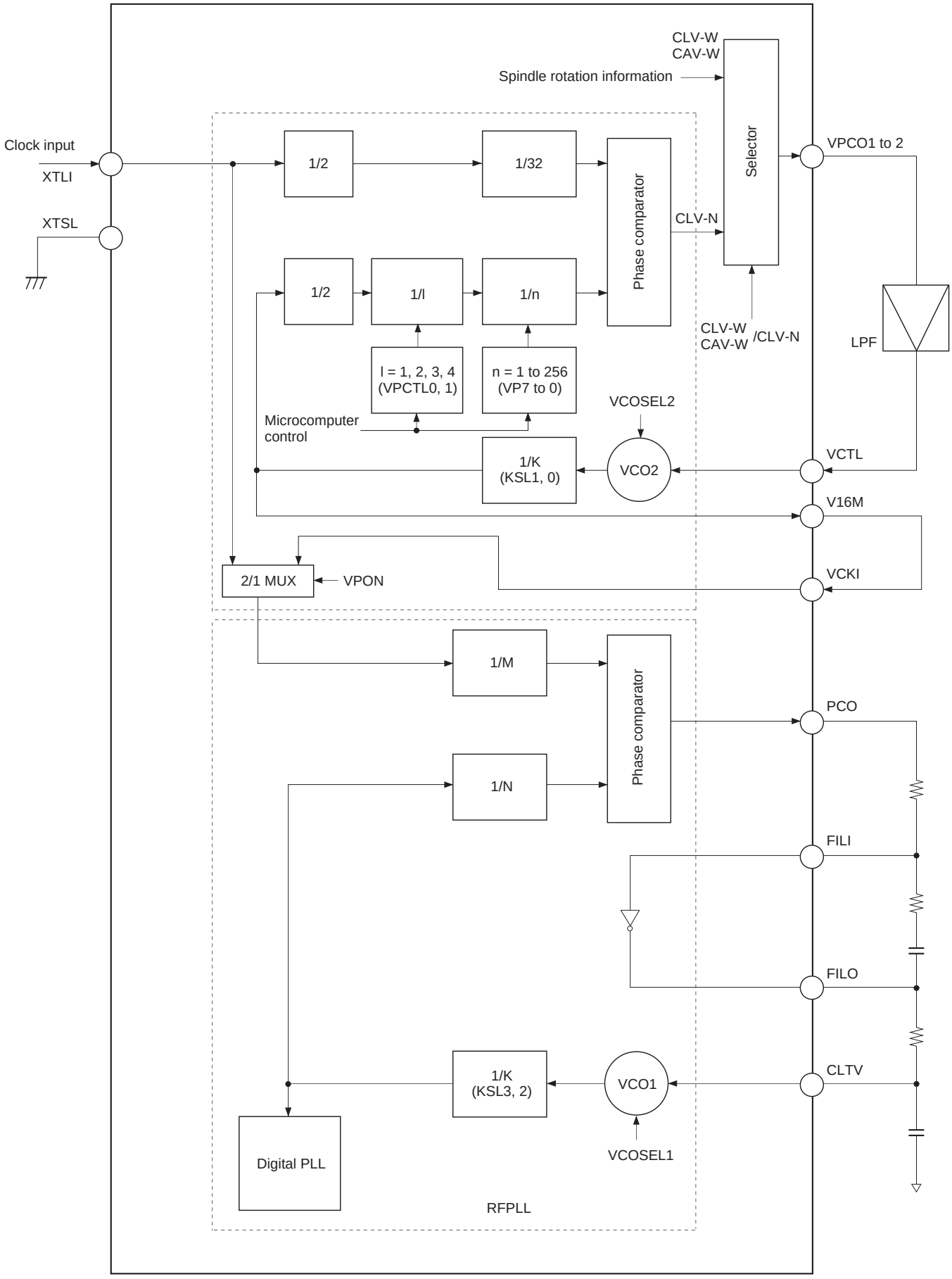
§4-1. Channel Clock Regeneration by the Digital PLL Circuit

- The channel clock is necessary for demodulating the EFM signal regenerated by the optical system.
  Assuming T as the channel clock cycle, the EFM signal is modulated in an integer multiple of T from 3T to 11T. In order to read the information in the EFM signal, this integer value must be read correctly. As a result, T, that is the channel clock, is necessary.
  In an actual player, a PLL is necessary for regenerating the channel clock because the fluctuation in the spindle rotation alters the width of the EFM signal pulses.

The block diagram of this PLL is shown in Fig. 4-1.
The CXD3003R has a built-in three-stage PLL.

- The first-stage PLL is a wide-band PLL. When using the internal VCO2, an external LPF is necessary; when not using the internal VCO2, external LPF and VCO are necessary.
  The output of this first-stage PLL is used as a reference for all clocks within the LSI.
- The second-stage PLL regenerates the high-frequency clock needed by the third-stage digital PLL.
- The third-stage PLL is a digital PLL that regenerates the actual channel clock.
- The digital PLL in CLV-N mode has a secondary loop, and is controlled by the primary loop (phase) and the secondary loop (frequency). When FLFC = 1, the secondary loop can be turned off. High frequency components such as 3T and 4T may contain deviations. In such as case, turning the secondary loop off yields better playability. However, in this case the capture range becomes ±50kHz.
- A new digital PLL has been provided for CLV-W mode to follow the rotational velocity of the disc in addition to the conventional secondary loop.

Block Diagram 4-1



§4-2. Frame Sync Protection

- In normal-speed playback, a frame sync is recorded approximately every 136µs (7.35kHz). This signal is used as a reference to recognize the data within a frame. Conversely, if the frame sync cannot be recognized, the data is processed as error data because the data cannot be recognized. As a result, recognizing the frame sync properly is extremely important for improving playability.

- In the CXD3003R, window protection and forward protection/backward protection have been adopted for frame sync protection. These functions achieve very powerful frame sync protection. There are two window widths; one for cases where a rotational disturbance affects the player and the other for cases where there is no rotational disturbance (WSEL = 0/1). In addition, the forward protection counter is fixed to 13, and the backward protection counter to 3. Concretely, when the frame sync is being played back normally and then cannot be detected due to scratches, a maximum of 13 frames are inserted. If the frame sync cannot be detected for 13 frames or more, the window opens to resynchronize the frame sync.
  In addition, immediately after the window opens and the resynchronization is executed, if a proper frame sync cannot be detected within 3 frames, the window opens immediately.

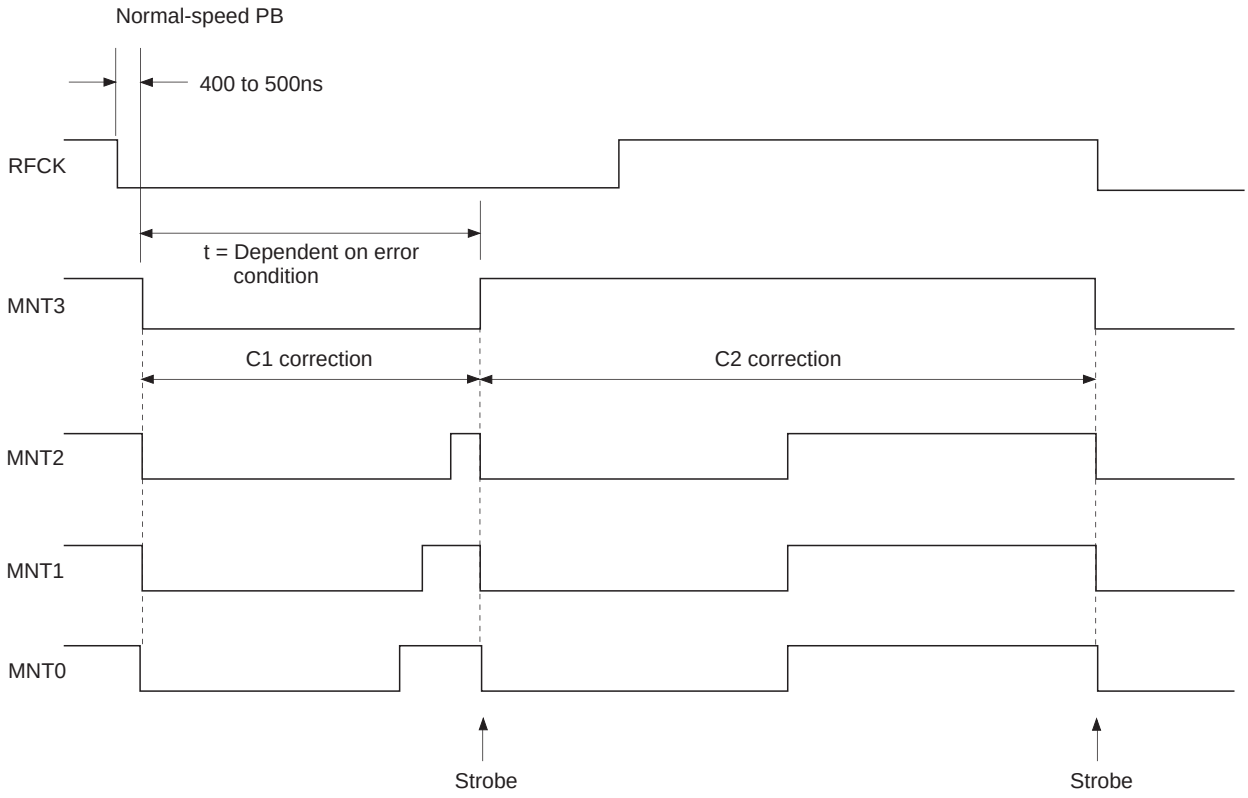
§4-3. Error Correction

- In the CD format, one 8-bit data contains two error correction codes, C1 and C2. For C1 correction, the code is created with 28-byte information and 4-byte C1 parity.
  For C2 correction, the code is created with 24-byte information and 4-byte parity.
  Both C1 and C2 are Reed Solomon codes with a minimum distance of 5.
- The CXD3003R uses refined super strategy to achieve double correction for C1 and quadruple correction for C2.
- In addition, to prevent C2 miscorrection, a C1 pointer is attached to data after C1 correction according to the C1 error status, the playback status of the EFM signal, and the operating status of the player.
- The correction status can be monitored externally. See Table 4-2.
- When the C2 pointer is high, the data in question was uncorrectable. Either the pre-value was held or an average value interpolation was made for the data.

MNT3	MNT2	MNT1	MNT0	Description	
0	0	0	0	No C1 errors;	C1 pointer reset
0	0	0	1	One C1 error corrected;	C1 pointer reset
0	0	1	0	—	
0	0	1	1	—	
0	1	0	0	No C1 errors;	C1 pointer set
0	1	0	1	One C1 error corrected;	C1 pointer set
0	1	1	0	Two C1 errors corrected;	C1 pointer set
0	1	1	1	C1 correction impossible;	C1 pointer set
1	0	0	0	No C2 errors;	C2 pointer reset
1	0	0	1	One C2 error corrected;	C2 pointer reset
1	0	1	0	Two C2 errors corrected;	C2 pointer reset
1	0	1	1	Three C2 errors corrected;	C2 pointer reset
1	1	0	0	Four C2 errors corrected;	C2 pointer reset
1	1	0	1	—	
1	1	1	0	C2 correction impossible;	C1 pointer copy
1	1	1	1	C2 correction impossible;	C2 pointer set

Table 4-2.

Timing Chart 4-3



§4-4. DA Interface

• The CXD3003R has two DA interface modes.

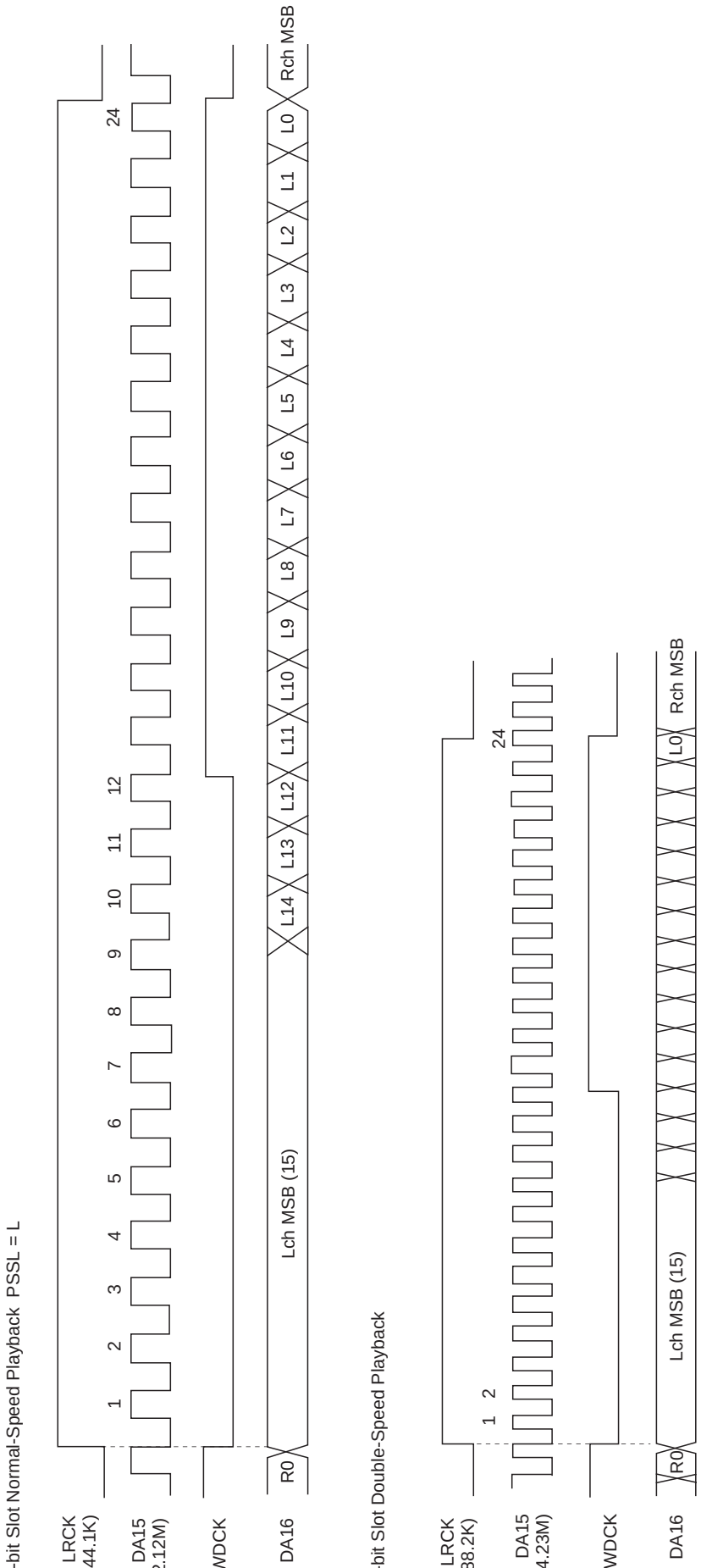
a) 48-bit slot interface

This interface includes 48 cycles of the bit clock within one LRCK cycle, and is MSB first. When LRCK is high, the data is for the left channel.

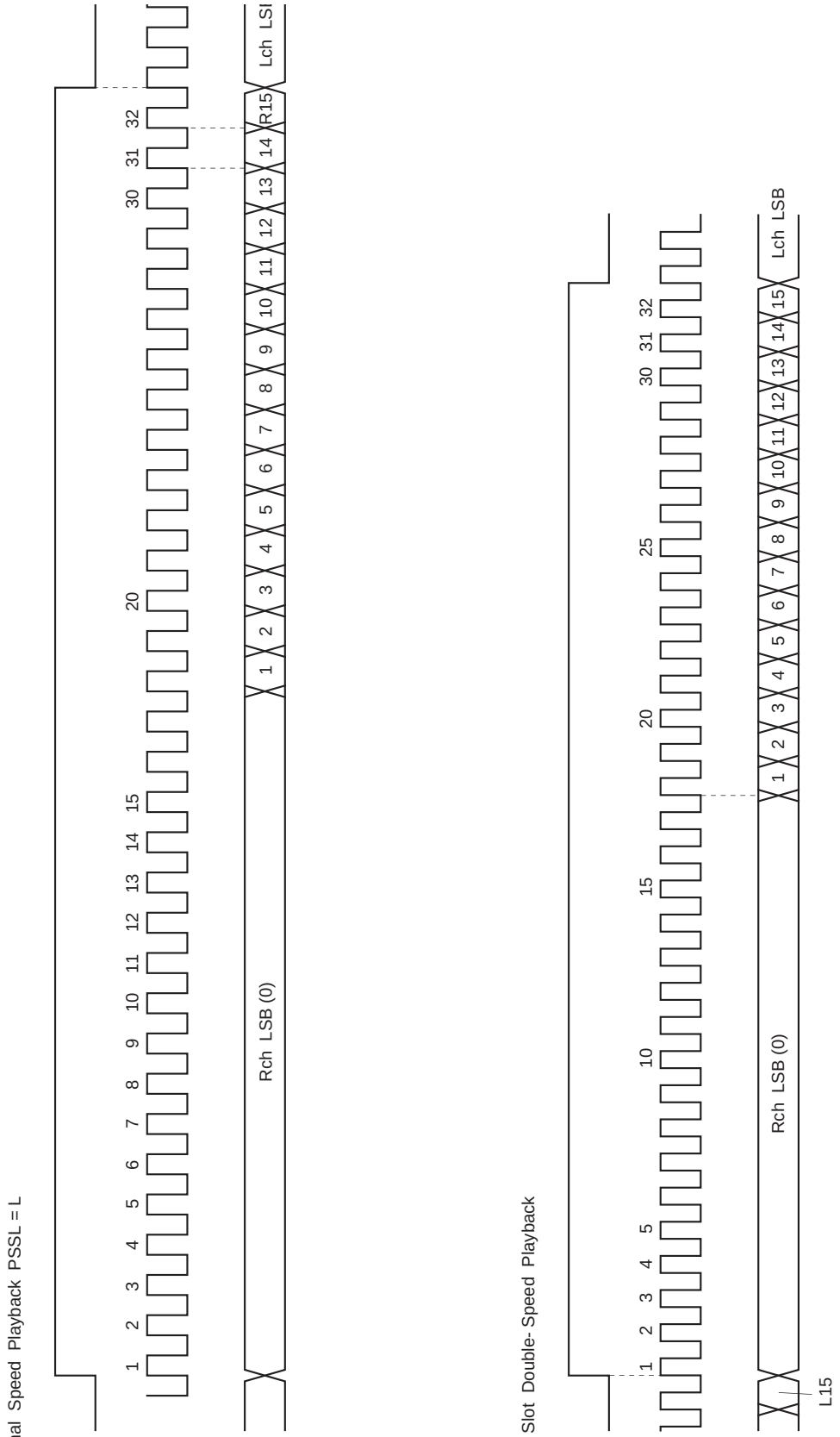
b) 64-bit slot interface

This interface includes 64 cycles of the bit clock within one LRCK cycle, and is LSB first. When LRCK is low, the data is for the left channel.

Timing Chart 4-4



Timing Chart 4-5



§4-5. Digital Out

There are three Digital Out: the type 1 format for broadcasting stations, the type 2 form 1 format for home use, and the type 2 form 2 format for the manufacture of software.

The CXD3003R supports type 2 form 1.

The channel status clock accuracy is automatically set to level II when using the crystal clock and to level III in CAV-W mode. In addition, Sub Q data which are matched twice in succession after a CRC check are input to the first four bits (bits 0 to 3).

DOUT is output when the crystal is 34MHz and DSPB is set to 1 with XTSL high in CLV-N or CLV-W mode. Therefore, set MD2 to 0 and turn DOUT off.

Digital Out C bit

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	From sub Q				0	0	0	0	1	0	0	0	0	0	0	0
	ID0	ID1	COPY	Emph												
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0	0
32																
48																
								0								
176																

Bits 0 to 3 Sub Q control bits that matched twice with CRCOK

Bit 29 VPON: 1 Crystal: 0

Table 4-6.

§4-6. Servo Auto Sequence

This function performs a series of controls, including auto focus and track jumps. When the auto sequence command is received from the CPU, auto focus, 1-track jump, 2N-track jump, fine search and M-track move are executed automatically.

The servo is used in an exclusive manner during the auto sequence execution (when XBUSY = low), so that commands from the CPU are not transferred to the servo, but can be sent to the CXD3003R.

In addition, when using the auto sequence, turn the A.SEQ of register 9 on.

When CLOK goes from low to high while XBUSY is low, XBUSY does not become high for a maximum of 100µs after that point. This is to prevent the transfer of erroneous data to the servo when XBUSY changes from low to high by the monostable multivibrator, which is reset by CLOK being low (when XBUSY is low).

In addition, a MAX timer is built into this LSI as a countermeasure against abnormal operation due to external disturbances, etc. When the auto sequence command is sent from the CPU, this command assumes a $4XY format, in which X specifies the command and Y sets the MAX timer value and timer range. If the executed auto sequence command does not terminate within the set timer value, the auto sequence is interrupted (like $40). See [1] "$4X commands" concerning the timer value and range. Also, the MAX timer is invalidated by inputting $4X0.

Although this command is explained in the format of $4X in the following command descriptions, the timer value and timer range are actually sent together from the CPU.

(a) Auto focus ($47)

Focus search-up is performed, FOK and FZC are checked, and the focus servo is turned on.

If $47 is received from the CPU, the focus servo is turned on according to Fig. 4-8. The auto focus starts with focus search-up, and note that the pickup should be lowered beforehand (focus search-down). In addition, blind E of register 5 is used to eliminate FZC chattering. Concretely, the focus servo is turned on at the falling edge of FZC after FZC has been continuously high for a longer time than E.

(b) Track jump

1, 10 and 2N-track jumps are performed respectively. Always use this when the focus, tracking, and sled servos are on. Note that tracking gain-up and braking-on ($17) should be sent beforehand because they are not involved in this sequence.

- 1-track jump

  When $48 ($49 for REV) is received from the CPU, a FWD (REV) 1-track jump is performed in accordance with Fig. 4-9. Set blind A and brake B with register 5.

- 10-track jump

  When $4A ($4B for REV) is received from the CPU, a FWD (REV) 10-track jump is performed in accordance with Fig. 4-10. The principal difference from the 1-track jump is to kick the sled. In addition, after kicking the actuator, when 5 tracks have been counted through COUT, the brake is applied to the actuator. Then, when the actuator speed is found to have slowed up enough (determined by the COUT cycle becoming longer than the overflow C set with register 5), the tracking and sled servos are turned on.

- 2N-track jump

  When $4C ($4D for REV) is received from the CPU, a FWD (REV) 2N-track jump is performed in accordance with Fig. 4-11. The track jump count N is set with register 7. Although N can be set to 216 tracks, note that the setting is actually limited by the actuator. COUT is used for counting the number of jumps when N is less than 16, and MIRR is used with N is 16 or more.

  Although the 2N-track jump basically follows the same sequence as the 10-track jump, the one difference is that after the tracking servo is turned on, the sled continues to move only for "D", set with register 6.

- Fine search

  When $44 ($45 for REV) is received from the CPU, a FWD (REV) fine search (N-track jump) is performed in accordance with Fig. 4-12. The differences from a 2N-track jump are that a higher precision is achieved by controlling the traverse speed, and a longer distance jump achieved by controlling the sled. The track jump count is set with register 7. N can be set to 216 tracks. After kicking the actuator and sled, the traverse speed is controlled based on the overflow G. Set kick D and F with register 6 and overflow G with register 5. Also, sled speed control during traverse can be turned off by causing COMP to fall. Set the number of tracks during which COMP falls with register B. After N tracks have been counted through COUT, the brake is applied to the actuator and sled. (This is performed by turning on the tracking servo for the actuator, and by kicking the sled in the opposite direction during the time for kick D set with register 6.) Then, the tracking and sled servos are turned on.

  Set overflow G to the speed required to slow up just before the track jump terminates. (The speed should be such that it will come on-track when the tracking servo turns on at the termination of the track jump.) For example, set the target track count N – α for the traverse monitor counter which is set with register B, and COMP will be monitored. When the falling edge of this COMP is detected, overflow G can be reset.

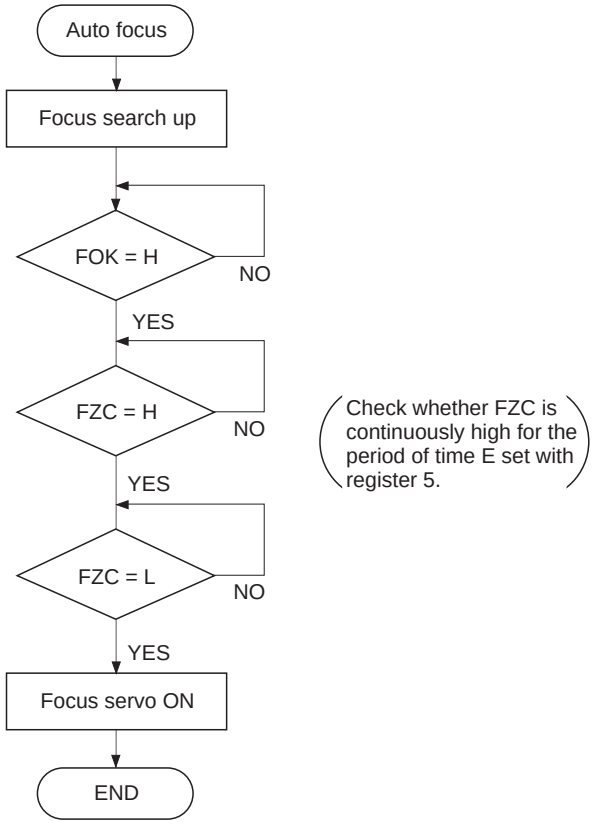


Fig. 4-8-(a). Auto Focus Flow Chart

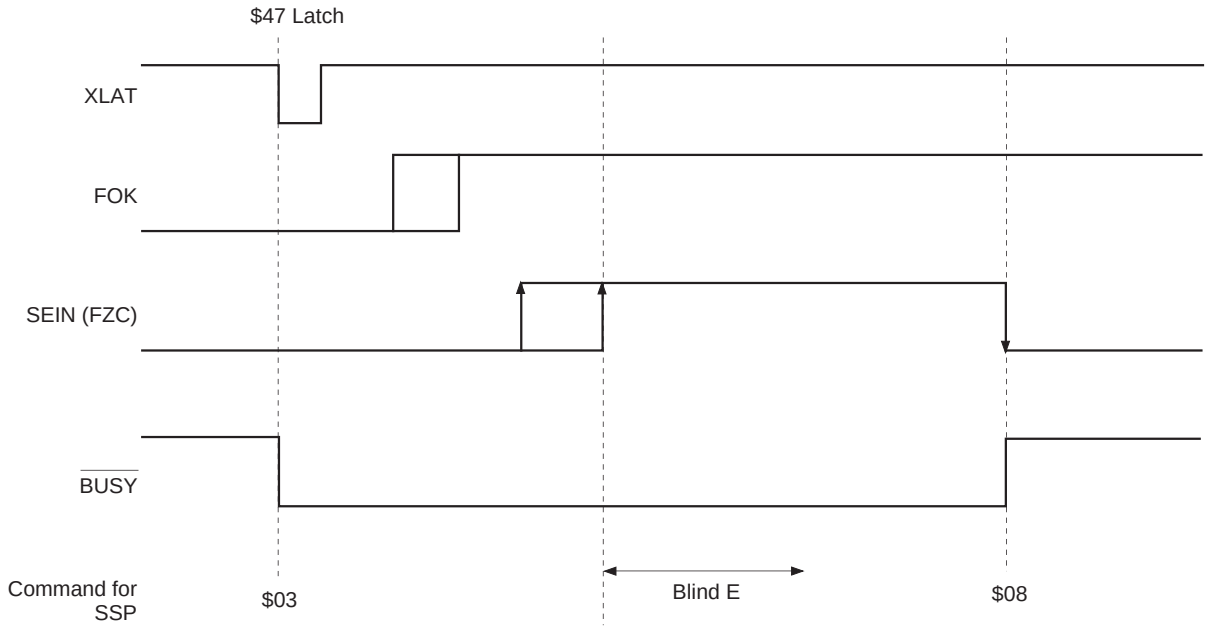


Fig. 4-8-(b). Auto Focus Timing Chart

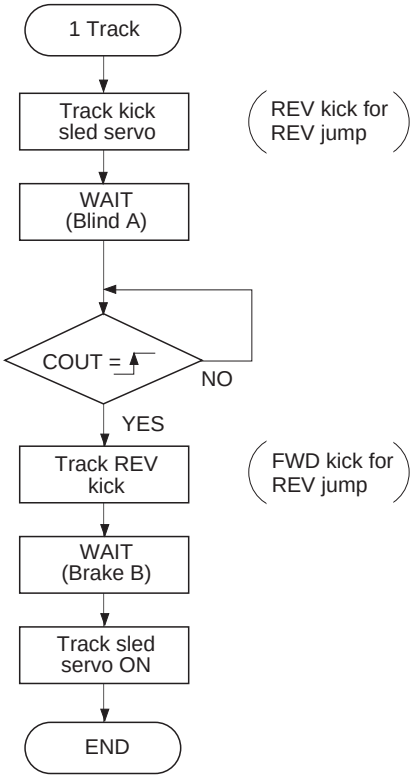


Fig. 4-9-(a). 1-Track Jump Flow Chart

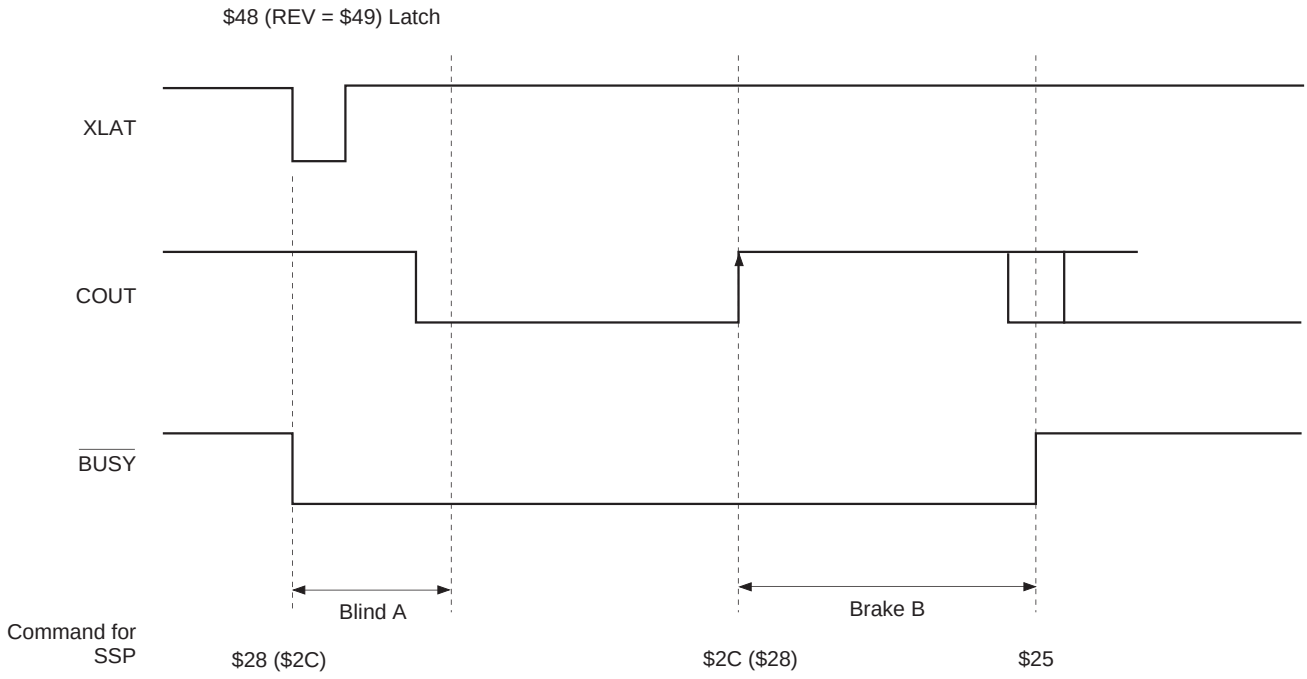


Fig. 4-9-(b). 1-Track Jump Timing Chart

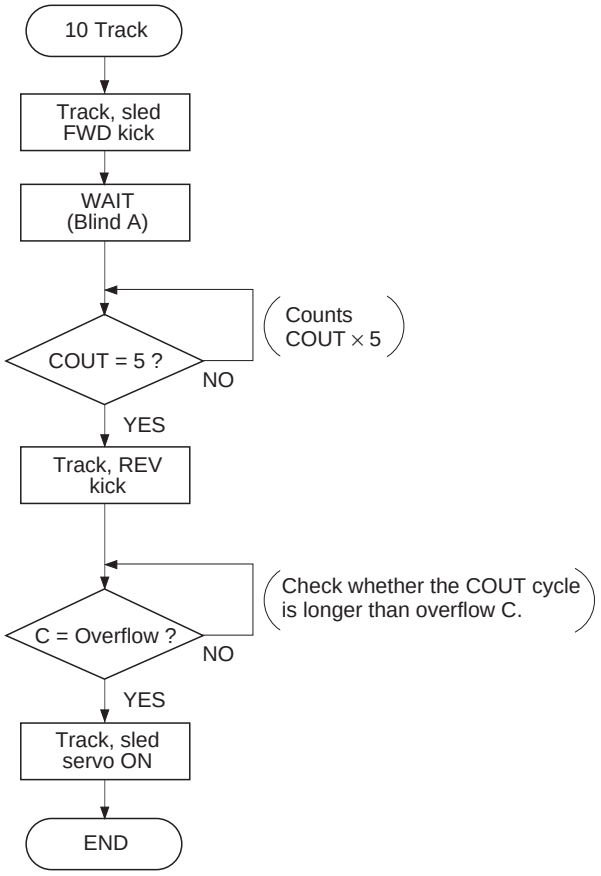


Fig. 4-10-(a). 10-Track Jump Flow Chart

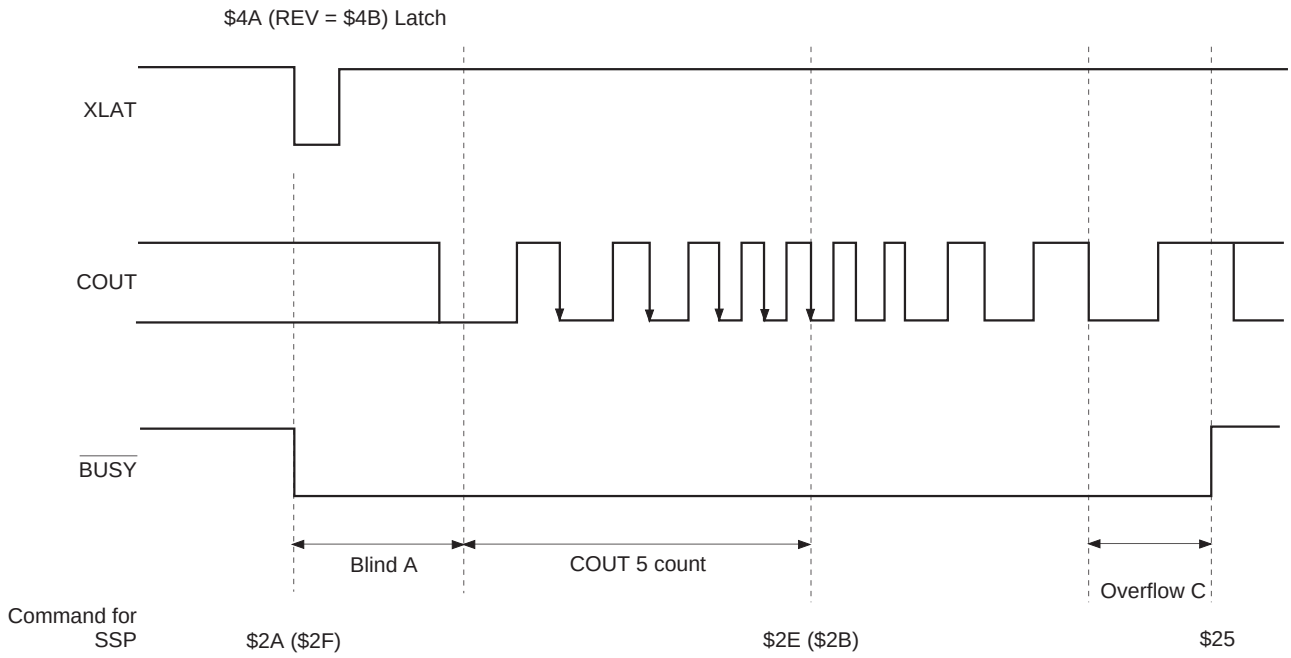


Fig. 4-10-(b). 10-Track Jump Timing Chart

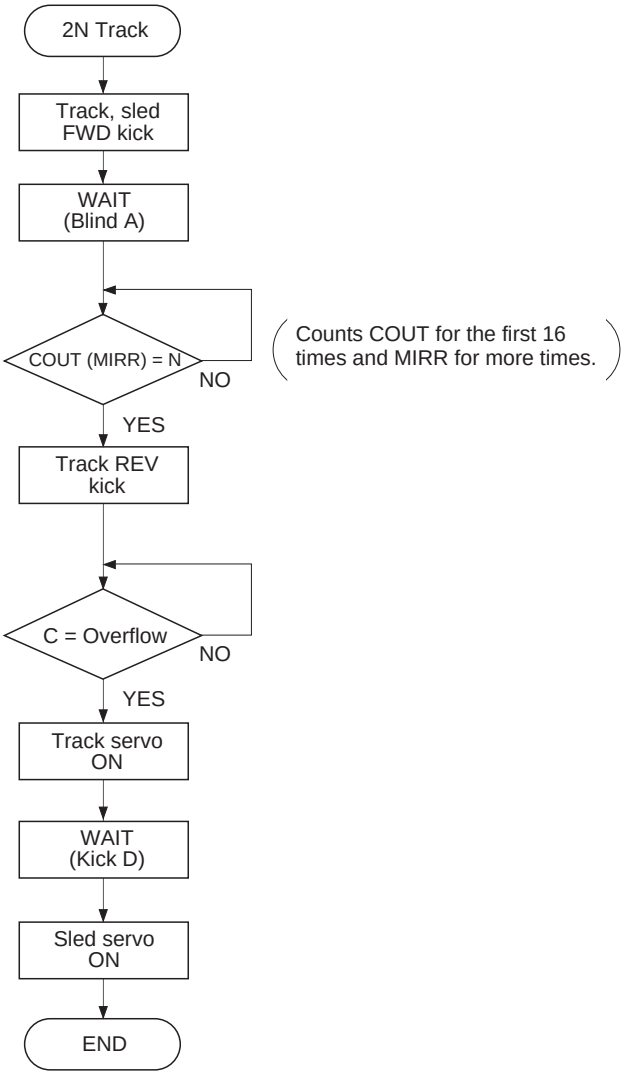


Fig. 4-11-(a). 2N-Track Jump Flow Chart

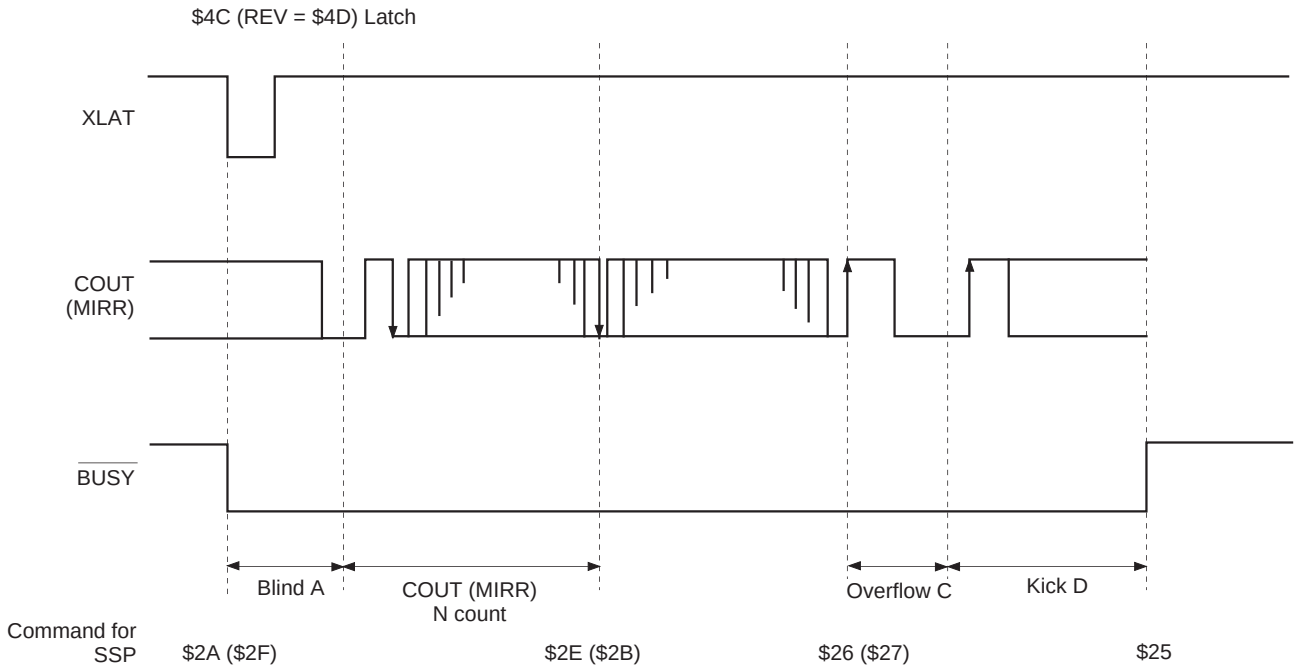


Fig. 4-11-(b). 2N-Track Jump Timing Chart

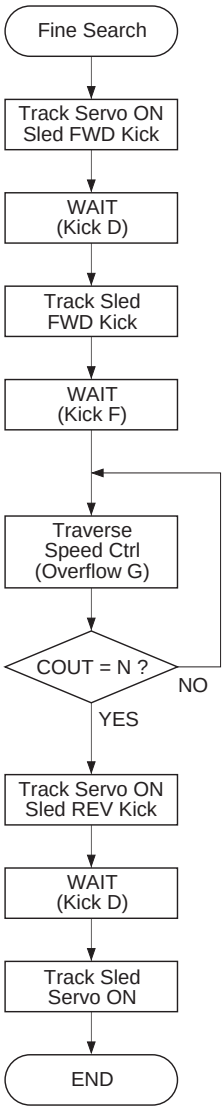


Fig. 4-12-(a). Fine Search Flow Chart

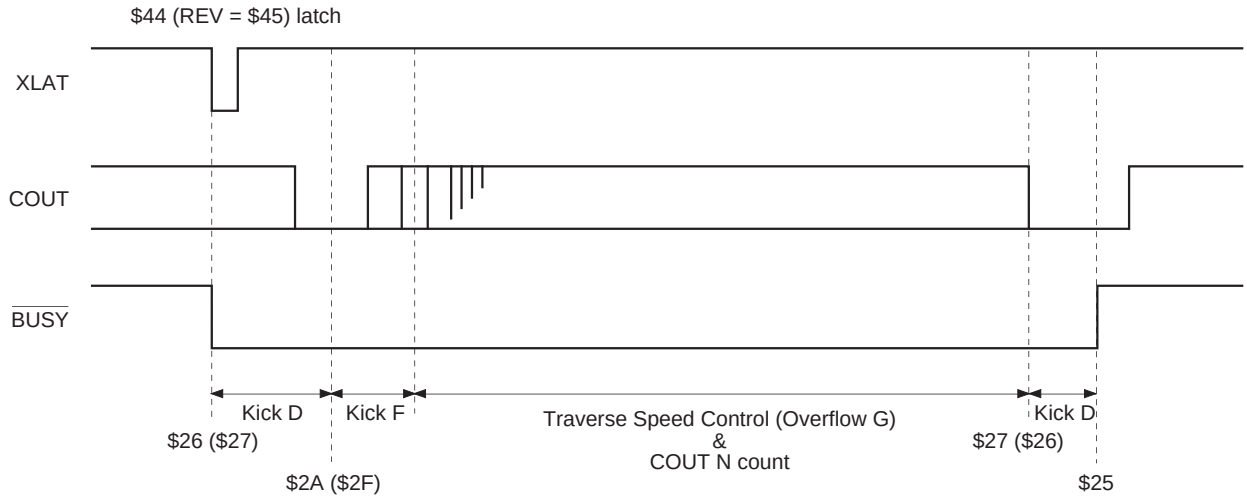


Fig. 4-12-(b). Fine Search Timing Chart

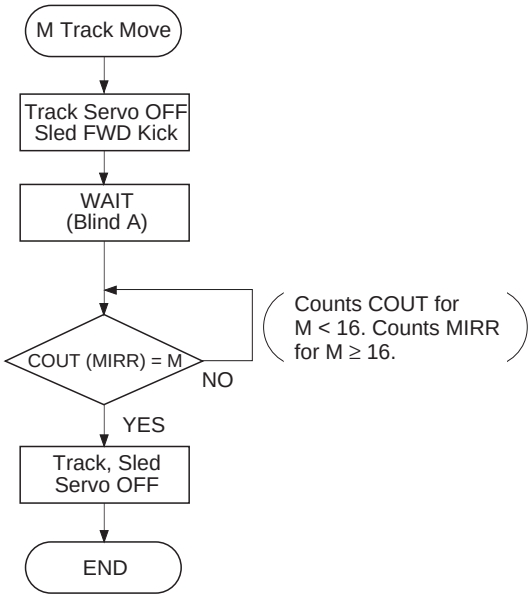


Fig. 4-13-(a). M-Track Move Flow Chart

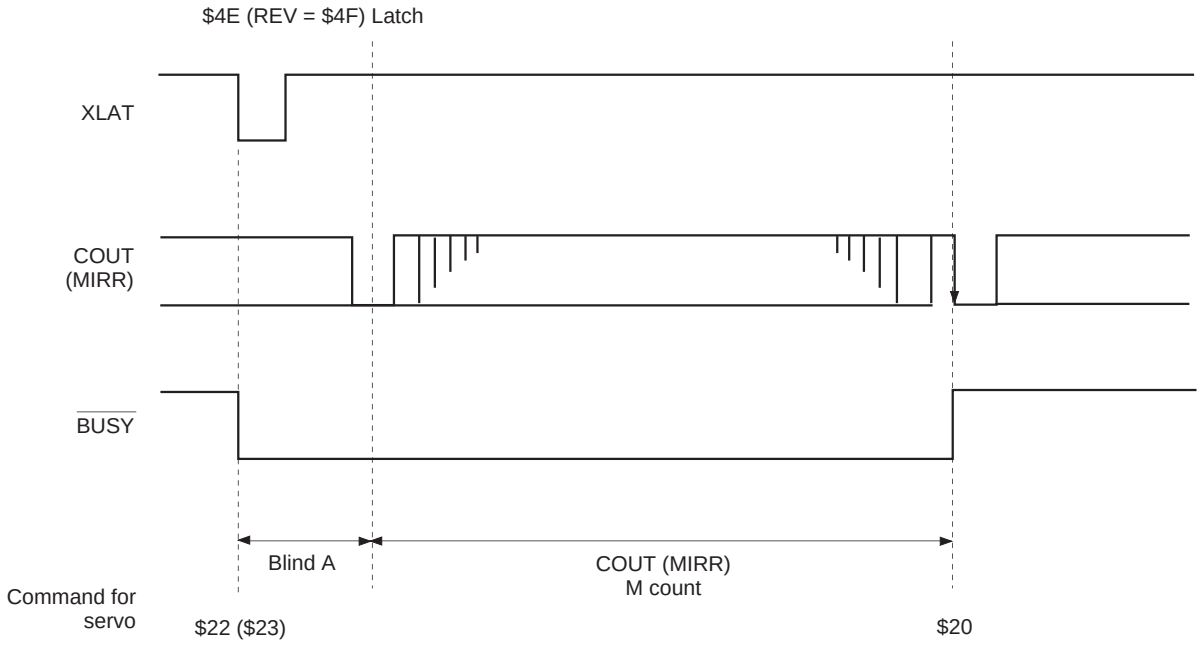
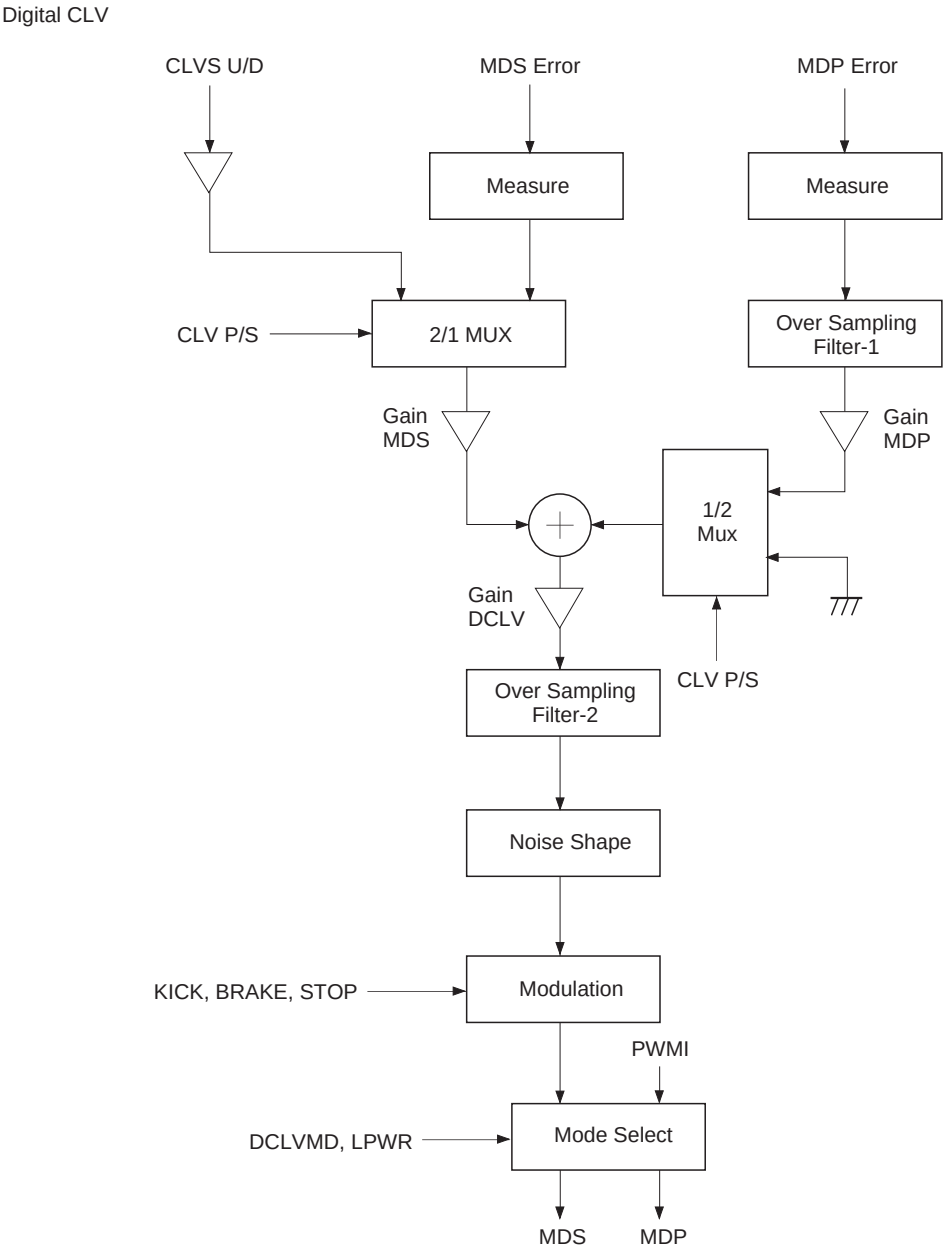


Fig. 4-13-(b). M-Track Move Timing Chart

§4-7. Digital CLV

Fig. 4-14 shows the block diagram. Digital CLV outputs MDS error and MDP error signals with PWM, with the sampling frequency increased up to 130kHz during normal-speed playback in CLVS, CLVP and other modes. In addition, the digital spindle servo gain is variable.



CLVS U/D : Up/down signal from CLVS servo
MDS error: Frequency error for CLVP servo
MDP error: Phase error for CLVP servo
PWMI: Spindle drive signal from the microcomputer for CAV servo

Fig. 4-14. Block Diagram

§4-8. Playback Speed

In the CXD3003R, the following playback modes can be selected through different combinations of XTLI, XTSL pin, double-speed command (DSPB), VCO1 selection command (VCOSEL1), VCO1 frequency division commands (KSL3, KSL2) and command transfer rate selector (ASHS) in CLV-N or CLV-W mode.

Mode	XTLI	XTSL	DSPB	VCOSEL1*1	ASHS	Playback speed	Error correction
1	768Fs	1	0	0/1	0	1×	C1: double; C2: quadruple
2	768Fs	1	1	0/1	0	2×	C1: double; C2: double
3	768Fs	0	0	1	1	2×	C1: double; C2: quadruple
4	768Fs	0	1	1	1	4×	C1: double; C2: double
5	384Fs	0	0	0/1	0	1×	C1: double; C2: quadruple
6	384Fs	0	1	0/1	0	2×	C1: double; C2: double
7	384Fs	1	1	0/1	0	1×	C1: double; C2: double

*1 Actually, the optimal value should be used together with KSL3 and KSL2.

The playback speed can be varied by setting VP0 to 7 in CAV-W mode. See "§3. Description of Modes" for details.

§4-9. DAC Block Playback Speed

• The DAC block playback speed is controlled by sending the DADS command to the DSP block.

Mode	X'tal	DADS
1	768fs	0
2	384fs	1

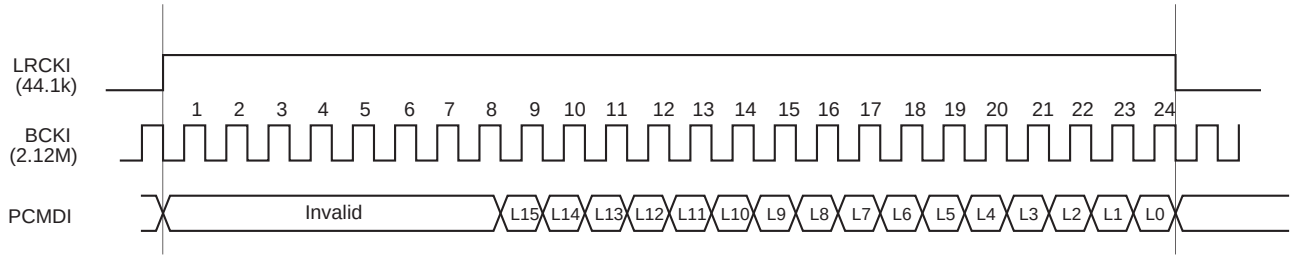
§4-10. DAC Block Input Timing

The DAC input timing chart is shown below.

Audio data is not transferred from the CD signal processor block to the DAC block inside the CXD3003R. This is to allow data to be sent to the DAC block via the audio DSP, etc.

When the data is input to the DAC block without using the audio DSP, the data must be connected outside the LSI. In this case, LRCK, BCK and PCMD can be connected directly with LRCKI, BCKI and PCMDI, respectively. (See the Application Circuit.)

Normal-Speed Playback



§4-11. Asymmetry Compensation

Fig. 4-15 shows the block diagram and circuit example.

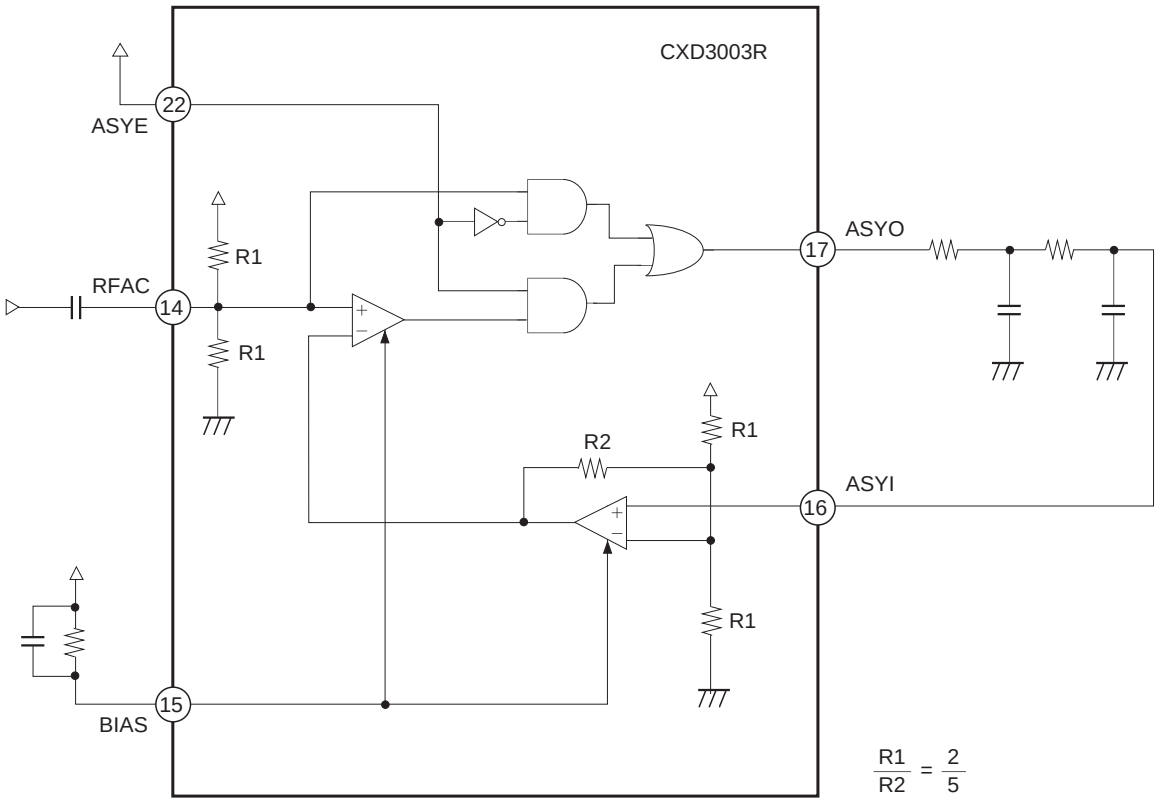
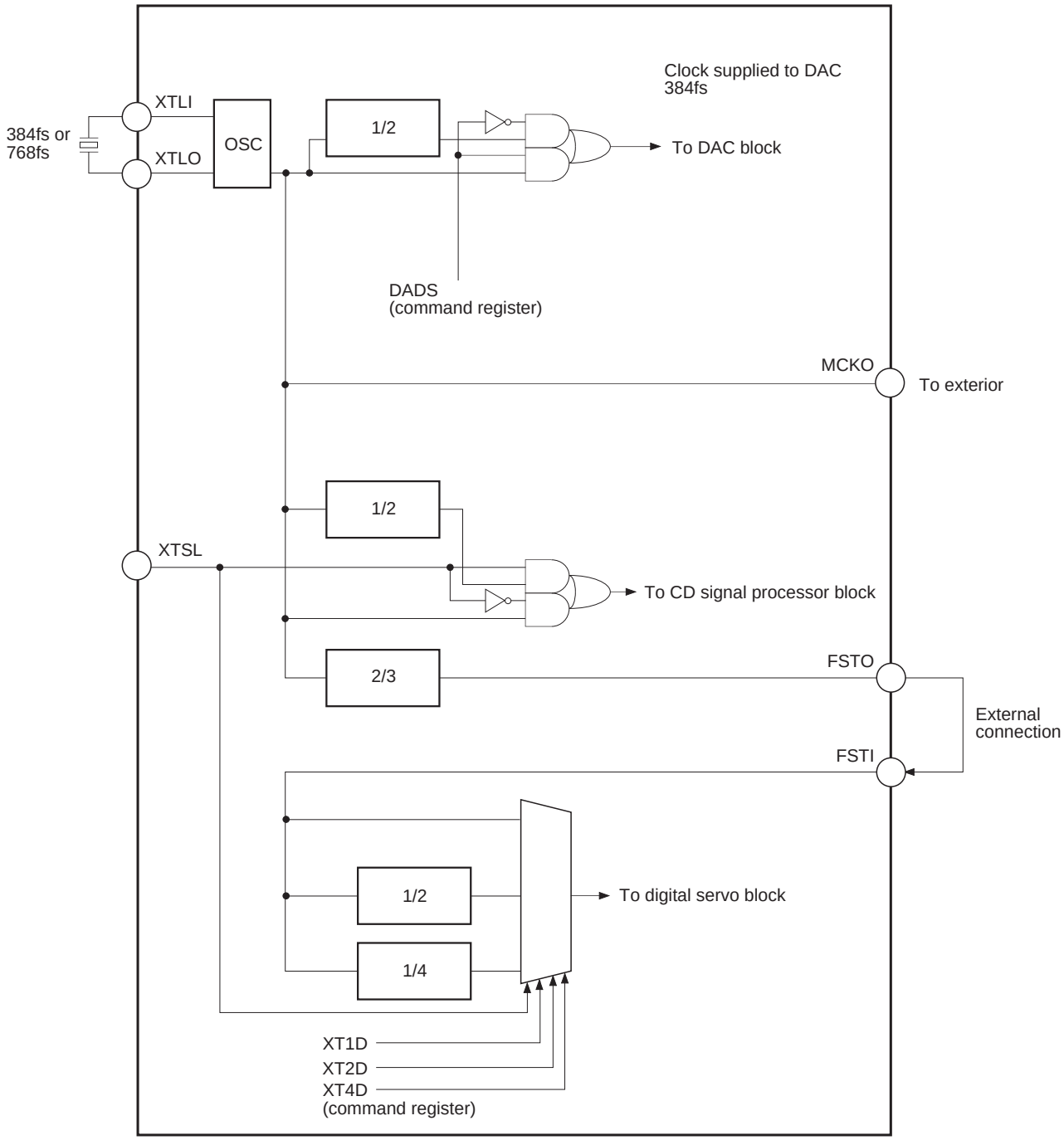


Fig. 4-15. Asymmetry Compensation Application Circuit.

§4-12. CXD3003R Clock System

The DAC, digital signal processor and digital servo blocks can be switched to each playback mode according to how the crystal and clock circuit are connected. Each circuit is as shown in the diagram below; during normal use, FSTO and FSTI are directly connected to each other.



[5] Description of Servo Signal Processing System Functions and Commands

§5-1. General Description of the Servo Signal Processing System (V_{DD}: Supply voltage)

Focus servo

Sampling rate:	88.2kHz (when MCK = 128Fs)
Input range:	1/4V_{DD} to 3/4V_{DD}
Output format:	7-bit PWM
Other:	Offset cancel
	Focus bias adjustment
	Focus search
	Gain-down function
	Defect countermeasure
	Auto gain control

Tracking servo

Sampling rate:	88.2kHz (when MCK = 128Fs)
Input range:	1/4V_{DD} to 3/4V_{DD}
Output format:	7-bit PWM
Other:	Offset cancel
	E:F balance adjustment
	Track jump
	Gain-up function
	Defect countermeasure
	Drive cancel
	Auto gain control
	Vibration countermeasure

Sled servo

Sampling rate:	345Hz (when MCK = 128Fs)
Input range:	1/4V_{DD} to 3/4V_{DD}
Output format:	7-bit PWM
Other:	Sled move

FOK, MIRR, DFCT signal generation

RF signal sampling rate:	1.4MHz (when MCK = 128Fs)
Input range:	1/4V_{DD} to 3/4V_{DD}
Other:	RF zero level automatic measurement

§5-2. Digital Servo Block Master Clock (MCK)

The FSTI pin is the reference clock input pin. The internal master clock (MCK) is generated by dividing the frequency of the signal input to FSTI. The frequency division ratio is 1, 1/2 or 1/4.

Table 5-1 below assumes that the crystal clock generated from the digital signal processor block which is 2/3 frequency-divided of XTLI is input to the FSTI pin by externally connecting the FSTI pin and the FSTO pin.

The XT4D and XT2D command can be set with D13 and D12 of $3F, and the XT1D command can be set with D1 of $3E. (Default = 0)

The digital servo block is designed with an MCK frequency of 5.6448MHz (128Fs) as typical.

Mode	XTLI	FSTO (FSTI)	XTSL	XT4D	XT2D	XT1D	Frequency division ratio	MCK
1	384Fs	256Fs	*	*	*	1	1	256Fs
2	384Fs	256Fs	*	*	1	0	1/2	128Fs
3	384Fs	256Fs	0	0	0	0	1/2	128Fs
4	768Fs	512Fs	*	*	*	1	1	512Fs
5	768Fs	512Fs	*	*	1	0	1/2	256Fs
6	768Fs	512Fs	*	1	0	0	1/4	128Fs
7	768Fs	512Fs	1	0	0	0	1/4	128Fs

Fs = 44.1kHz, *: Don't care

Table 5-1.

§5-3. AVRG (Average) Measurement and Compensation

The CXD3003R has a circuit that measures AVRG of RFDC, VC, FE and TE and a circuit that compensates these signals to control the servo effectively.

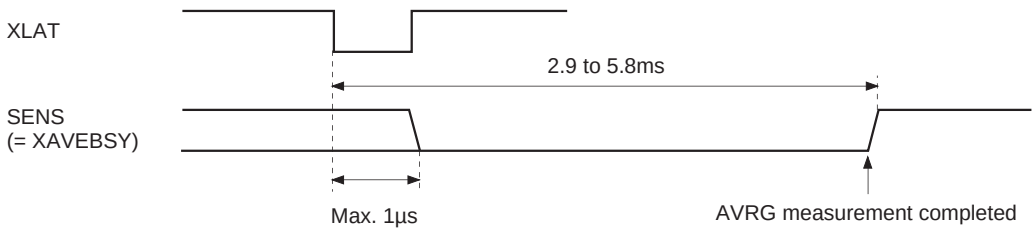
AVRG measurement and compensation is necessary to initialize the CXD3003R, and is able to cancel the offset.

The level applied to the VC, FE, RFDC and TE pins can be measured by setting D15 (VCLM), D13 (FLM), D11 (RFLM) and D4 (TCLM) of $38 respectively to 1.

AVRG measurement takes the level applied to each analog input pin as the average of 256 samples, and then loads each value into the AVRG register.

AVRG measurement requires approximately 2.9ms to 5.8ms (when MCK = 128Fs) after the command is received.

During AVRG measurement, if the upper 8 bits of the command register are 38 (Hex), the completion of AVRG measurement operation can be confirmed through the SENS pin. (See Timing Chart 5-2.)



Timing Chart 5-2.

<Measurement>

• VC AVRG

The offset can be canceled by measuring the VC level which is the center voltage for the system and using that value to apply compensation to each input error signal.

• FE AVRG

The FE signal DC level is measured. In addition, compensation is applied to the FZC comparator level output from the SENS pin during FCS SEARCH (focus search) using these measurement results.

• TE AVRG

The TE signal DC level is measured.

• RF AVRG

The MIRR, DFCT and FOK signals are generated from the RF signal. Since the FOK signal is generated by comparing the RF signal at a certain level, it is necessary to establish a zero level which becomes the comparator level reference. Therefore, the RF signal is measured before playback, and is compensated to take this level as the zero level.

An example of sending AVRG measurement and compensation commands is shown below.

(Example) $380800 (RF AVRG measurement on)
$382000 (FE AVRG measurement on)
$380010 (TE AVRG measurement on)
$388000 (VC AVRG measurement on)
(Complete each AVRG measurement before starting the next.)
$38140A (RFLC, FLC0, FLC1 and TLC1 commands on)
(The required compensation should be turned on together; see Fig. 5-3.)

An interval of 5.8ms (when MCK = 128Fs) or more must be maintained between each command, or the SENS pin must be monitored to confirm that the previous command has been completed before the next AVRG command is sent.

<Compensation>

See Fig. 5-3 for the contents of each compensation below.

• RFLC

The difference by which the RF signal exceeds the RF AVRG value is input to the RF In register.
(00 is input when the RF signal is lower than the RF AVRG value.)

• TCL0

The value obtained by subtracting the VC AVRG value from the TE signal is input to the TRK In register.

• TCL1

The value obtained by subtracting the TE AVRG value from the TE signal is input to the TRK In register.

• VCLC

The value obtained by subtracting the VC AVRG value from the FE signal is input to the FCS In register.

• FLC1

The value obtained by subtracting the FE AVRG value from the FE signal is input to the FCS In register.

• FLC0

The value obtained by subtracting the FE AVRG value from the FE signal is input to the FZC register.

§5-4. E:F Balance Adjustment Function

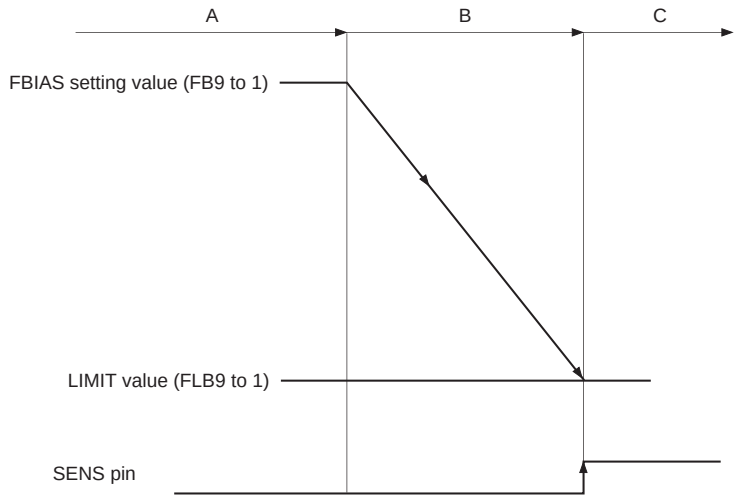
When the disc is rotated with the laser on, and with the FCS (focus) servo on via FCS Search (focus search), the traverse waveform appears in the TE signal due to disc eccentricity.
In this condition, the low-frequency component can be extracted from the TE signal using the built-in TRK hold filter by setting D5 (TBLM) of $38 to 1.
The extracted low-frequency component is loaded into the TRVSC register as a digital value, and the TRVSC register value is established when TBLM returns to 0.
Next, setting D2 (TLC2) of $38 to 1 compensates TE and SE values with the TRVSC register value (subtraction), resulting the E:F balance offset to be adjusted. (See Fig. 5-3.)

§5-5. FCS Bias (Focus Bias) Adjustment Function

The FBIAS register value can be added to the FCS servo filter input by setting D14 (FBON) of $3A to 1. (See Fig. 5-3.)
When the FBIAS register value is set when D11 = 0 and D10 = 1 with $34F, data can be written using the 9-bit value of D9 to D1 (D9: MSB).
In addition, the RF jitter can be monitored by setting the SOCT command of $8 to 1. (See "DSP Block Timing Chart".)

The FBIAS register can be used as a counter by setting D13 (FBSS) of $3A to 1. The FBIAS register functions as an up counter when D12 (FBUP) of $3A = 1, and as a down counter when D12 (FBUP) of $3A = 0.
The number of up and down steps can be changed by setting D11 and D10 (FBV1 and FBV0) of $3A.

When using the FBIAS register as a counter, the counter stops if the FBIAS value the value set beforehand in FLB9 to 1 of $34 matches. Also, if the upper 8 bits of the command register are $3A at this time, the counter stop can be monitored through SENS.



Here, assume the FBIAS setting value FB9 to 1 and the FBIAS LIMIT value FBL9 to 1 like status A. For example, if command registers FBUP = 0, FBV1 = 0, FBV0 = 0 and FBSS = 1 are set from this status, down count starts from status A and approaches the set LIMIT value. When the FBIAS value matches FBL9 to 1, the counter stops and the SENS pin goes to high. Note that the up/down counter counts at each sampling cycle of the focus servo filter. The number of steps by which the count value changes can be selected from 1, 2, 4 or 8 steps by FBV1 and FBV0. When converted to FE input, 1 step corresponds to $1/512 \times V_{DD}/2$.

A: Register mode
B: Counter mode
C: Counter mode (when stopped)

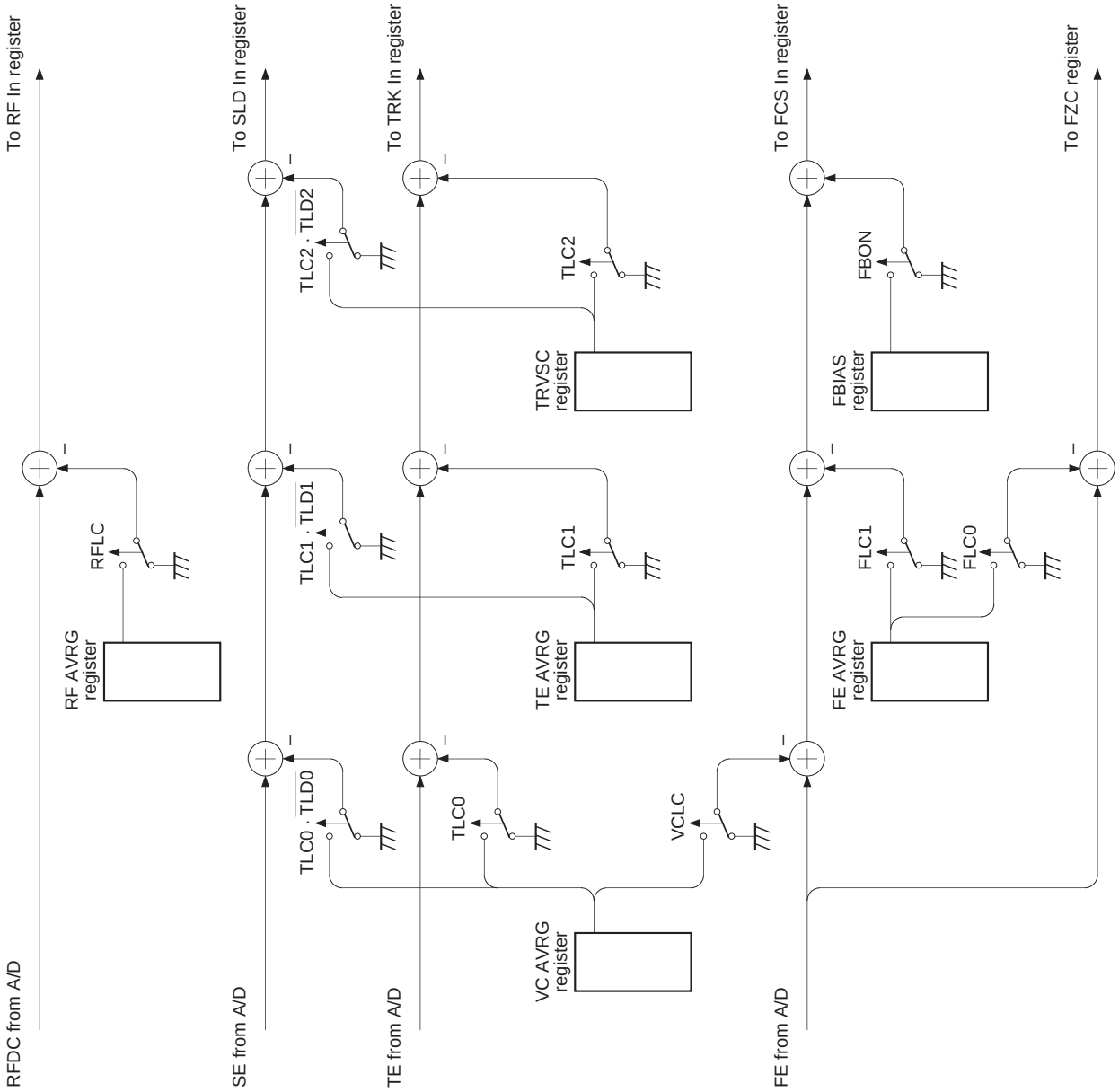

To RF In register
To SLD In register
To TRK In register
To FCS In register
To FZC register
RFDC from A/D
SE from A/D
TE from A/D
FE from A/D
RFLC
RF AVRG register
TLC0 . TLD0
TLC1 . TLD1
TLC2 . TLD2
TLC0
TLC1
TLC2
VCLC
VC AVRG register
TE AVRG register
TRVSC register
FLC1
FLC0
FE AVRG register
FBON
FBIAS register

Fig. 5-3.

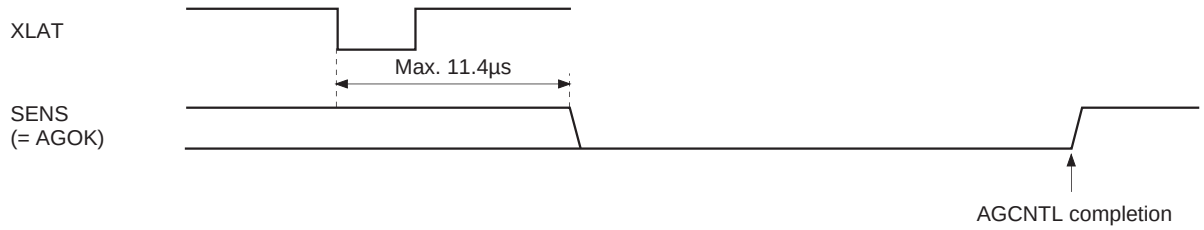
§5-6. AGCNTL (Automatic Gain Control) Function

The AGCNTL function automatically adjusts the filter internal gain in order to obtain the appropriate gain with the servo loop. AGCNTL not only copes with the sensitivity variation of the actuator and photo diode, etc., but also obtains the optimal gain for each disc.

The AGCNTL command is sent when each servo is turned on. During AGCNTL operation, if the upper 8 bits of the command register are 38 (Hex), the completion of AGCNTL operation can be confirmed through the SENS pin. (See Timing Chart 5-4 and "Description of SENS Signals".)

Setting D9 and D8 of $38 to 1 set FCS (focus) and TRK (tracking) respectively to AGCNTL operation.

Note) During AGCNTL operation, each servo filter gain must be normal, and the anti-shock circuit (described hereafter) must be disabled.



Timing Chart 5-4.

Coefficient K13 changes for AGF (focus AGCNTL) and coefficients K23 and K07 change for AGT (tracking AGCNTL) due to AGCNTL.

These coefficients change from 01 to 7F (Hex), and they must also be set within this range when written externally.

After AGCNTL operation has completed, these coefficient values can be confirmed by reading them out from the SENS pin with the serial readout function (described hereafter).

AGCNTL related settings

The following settings can be changed with $35, $36 and $37.

FG6 to FG0; AGF convergence gain setting, effective setting range: 00 to 57 (Hex)
TG6 to TG0; AGT convergence gain setting, effective setting range: 00 to 57 (Hex)
AGS; Self-stop on/off
AGJ; Convergence completion judgment time
AGGF; Internally generated sine wave amplitude (AGF)
AGGT; Internally generated sine wave amplitude (AGT)
AGV1; AGCNTL sensitivity 1 (during rough adjustment)
AGV2; AGCNTL sensitivity 2 (during fine adjustment)
AGHS; Rough adjustment on/off
AGHT; Fine adjustment time

Note) Converging servo loop gain values can be changed with the FG6 to 0 and TG6 to 0 setting values. In addition, these setting values must be within the effective setting range. The default settings aim for 0 dB at 1kHz. However, since convergence values vary according to the characteristics of each constituent element of the servo loop, FG and TG values should be set as necessary.

AGCNTL and default operation have two stages.
In the first stage, rough adjustment is performed with high sensitivity for a certain period of time (select 256/128ms with AGHT, when MCK = 128Fs), and the AGCNTL coefficient approaches the appropriate value. The sensitivity at this time can be selected from two types with AGV1.
In the second stage, the AGCNTL coefficient is finely adjusted to approach more appropriate value with relatively low sensitivity. The sensitivity for the second stage can be selected from two types with AGV2. In the second stage of default operation, when the AGCNTL coefficient reaches the appropriate value and stops changing, the CXD3003R confirms that the AGCNTL coefficient has not changed for a certain period of time (select 63/31ms with AGHJ, when MCK = 128Fs), and then completes AGCNTL operation. (Self-stop mode)
This self-stop mode can be canceled by setting AGS to 0.
In addition, the first stage is omitted for AGCNTL operation when AGHS is set to 0.
An example of AGCNTL coefficient transitions during AGCNTL in various settings are shown in Fig. 5-5.

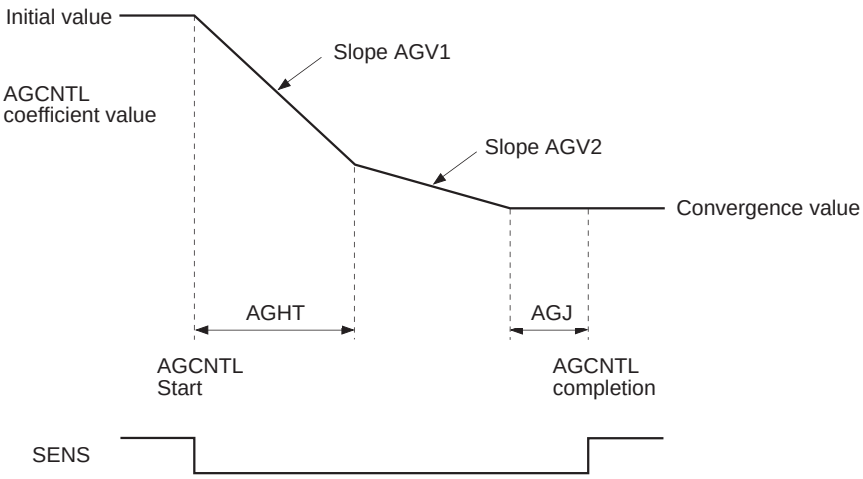


Fig. 5-5.

§5-7. FCS Servo and FCS Search (Focus Search)

The FCS servo is controlled by the 8-bit serial command $0X. (See Table 5-6.)

Register name	Command	D23 to D20	D19 to D16	
0	FOCUS CONTROL	0 0 0 0	1 0 ∗ ∗	FOCUS SERVO ON (FOCUS GAIN NORMAL)
			1 1 ∗ ∗	FOCUS SERVO ON (FOCUS GAIN DOWN)
			0 ∗ 0 ∗	FOCUS SERVO OFF, 0V OUT
			0 ∗ 1 ∗	FOCUS SERVO OFF, FOCUS SEARCH VOLTAGE OUT
			0 ∗ 1 0	FOCUS SEARCH VOLTAGE DOWN
			0 ∗ 1 1	FOCUS SEARCH VOLTAGE UP

∗: Don't care

Table 5-6.

FCS Search

FCS search is required in the course of turning on the FCS servo.

Fig. 5-7 shows the signals for sending commands $00 → $02 → $03 and performing only FCS search operation.
Fig. 5-8 shows the signals for sending $08 (FCS on) after that.

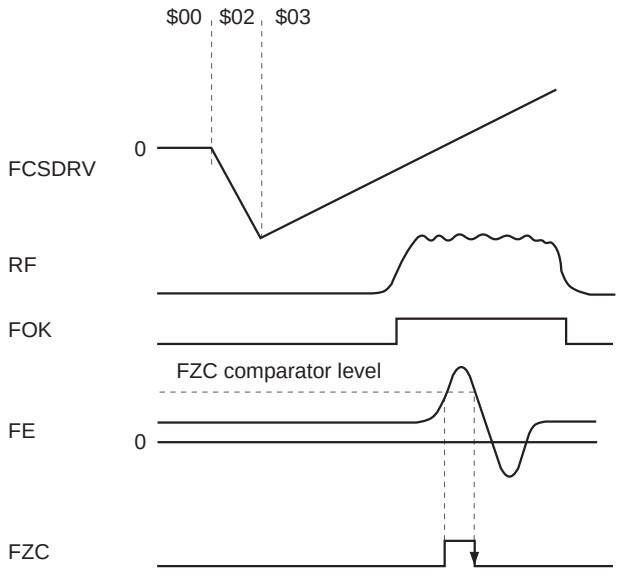


Fig. 5-7.

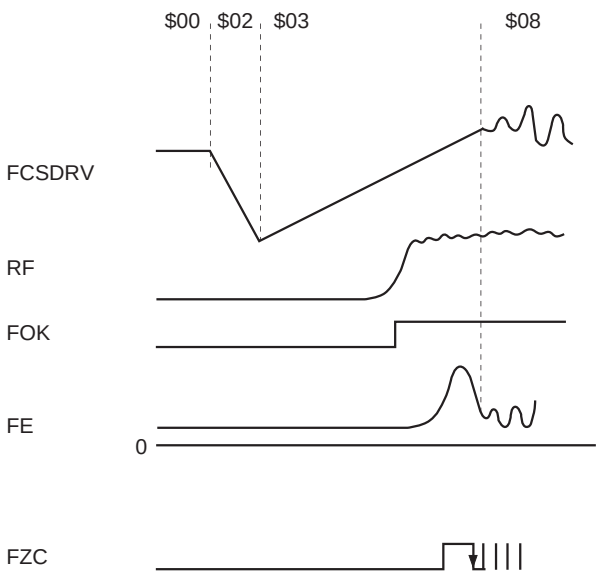


Fig. 5-8.

§5-8. TRK (Tracking) and SLD (Sled) Servo Control

The TRK and SLD servos are controlled by the 8-bit command $2X. (See Table 5-9.)
When the upper 4 bits of the command register are 2 (Hex), TZC is output to the SENS pin.

Register name	Command	D23 to D20	D19 to D16	
2	TRACKING MODE	0 0 1 0	0 0 ∗ ∗	TRACKING SERVO OFF
			0 1 ∗ ∗	TRACKING SERVO ON
			1 0 ∗ ∗	FORWARD TRACK JUMP
			1 1 ∗ ∗	REVERSE TRACK JUMP
			∗ ∗ 0 0	SLED SERVO OFF
			∗ ∗ 0 1	SLED SERVO ON
			∗ ∗ 1 0	FORWARD SLED MOVE
			∗ ∗ 1 1	REVERSE SLED MOVE

∗: Don't care

Table 5-9.

TRK Servo

The TRK JUMP (track jump) level can be set with 6 bits (D13 to D8) of $36.
In addition, when the TRK servo is on and D17 of $1 is set to 1, the TRK servo filter switches to gain-up mode. The filter also switches to gain-up mode when the LOCK signal goes low or when vibration is detected with the anti-shock circuit (described hereafter) enabled.
CXD3003R has 2 types of filters in TRK gain-up mode which can be selected by setting D16 of $1. (See Table 5-17.)

SLD Servo

The SLD MOV (sled move) output, composed of a basic value from 6 bits (D13 to D8) of $37, is determined by multiplying this value by 1×, 2×, 3× or 4× magnification set using D17 and D16 when D18 = D19 = 0 is set with $3. (See Table 5-10.)
SLD MOV must be performed continuously for 50µs or more. In addition, if the LOCK input signal goes low when the SLD servo is on, the SLD servo turns off.

Note) When the LOCK signal is low, the TRK servo switches to gain-up mode and the SLD servo is turned off by the default. These operations are disabled by setting D6 (LKSW) of $38 to 1.

Register name	Command	D23 to D20	D19 to D16	
3	SELECT	0 0 1 1	0 0 0 0	SLED KICK LEVEL (basic value × ±1)
			0 0 0 1	SLED KICK LEVEL (basic value × ±2)
			0 0 1 0	SLED KICK LEVEL (basic value × ±3)
			0 0 1 1	SLED KICK LEVEL (basic value × ±4)

Table 5-10.

§5-9. MIRR and DFCT Signal Generation

The RF signal obtained from the RFDC pin is sampled at approximately 1.4MHz (when MCK = 128Fs) and loaded. The MIRR and DFCT signals are generated from this RF signal.

MIRR Signal Generation

The loaded RF signal is applied to peak hold and bottom hold circuits.
An envelope is generated from the waveforms generated in these circuits, and the MIRR comparator level is generated from the average of this envelope waveform.
The MIRR signal is generated by comparing the waveform generated by subtracting the bottom hold value from the peak hold value with this MIRR comparator level. (See Fig. 5-11.)
The bottom hold speed and mirror sensitivity can be selected from 4 values using D7 and 6, and D5 and 4, respectively, of $3C.

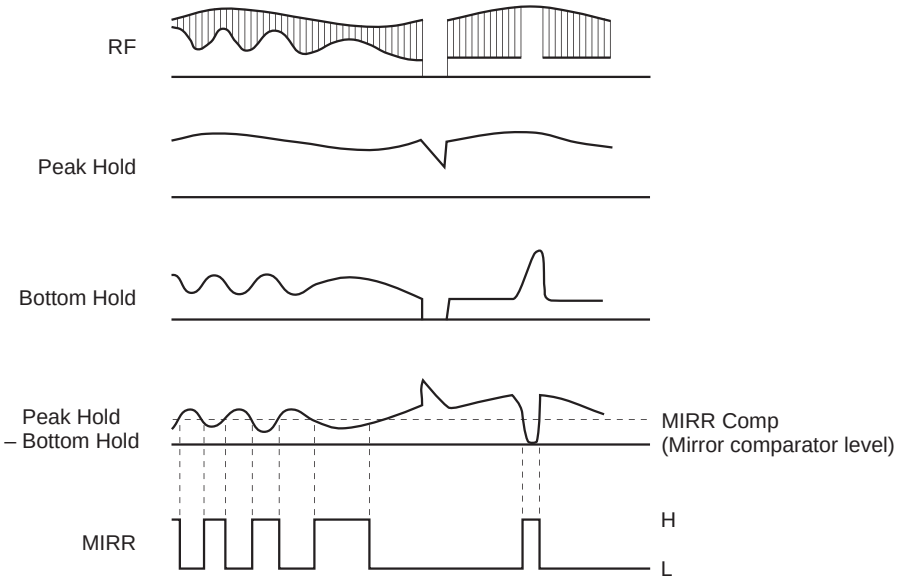


Fig. 5-11.

DFCT Signal Generation

The loaded RF signal is input to two peak hold circuits with different time constants, and the DFCT signal is generated by comparing the difference between these two peak hold waveforms with the DFCT comparator level. (See Fig. 5-12.)
The DFCT comparator level can be selected from four values using D13 and D12 of $3B.

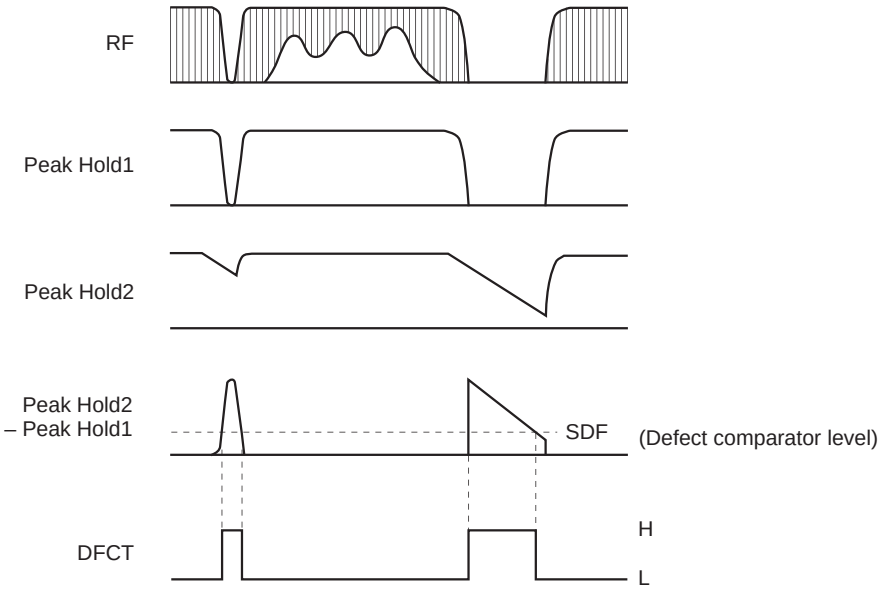


Fig. 5-12.

§5-10. DFCT Countermeasure Circuit

The DFCT countermeasure circuit maintains the directionality of the servo so that the servo does not become easily dislocated due to scratches or defects on discs.

Specifically, these operations are achieved by detecting scratch and defect with the DFCT signal generation circuit, and when DFCT goes high, applying the low frequency element of the error signal before DFCT went high to the FCS and TRK servo filter inputs. (See Fig. 5-13.)

In addition, these operations are activated by the default. They can be disabled by setting D7 (DFSW) of $38 to 1.

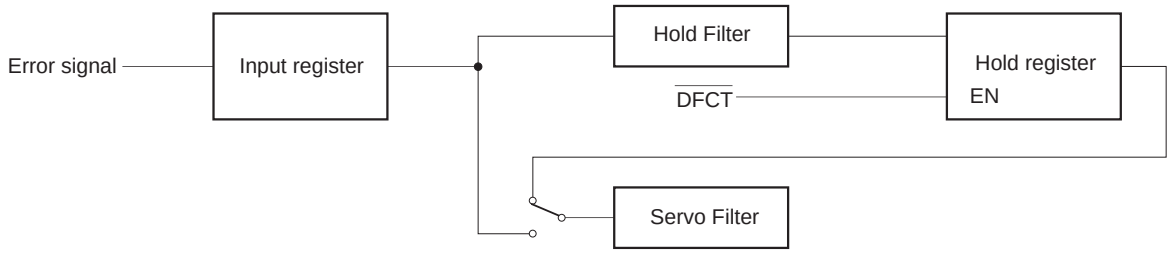


Fig. 5-13.

§5-11. Anti-Shock Circuit

When vibrations occurs in the CD player, this circuit forces the TRK filter to switch to gain-up mode so that the servo does not become easily dislocated. This circuit is for systems which require vibration countermeasures.

Concretely, vibrations are detected using an internal anti-shock filter and comparator circuit, and the gain is increased. (See Fig. 5-14.)

The comparator level is fixed to 1/16 of the maximum comparator input amplitude. However, the comparator level is practically variable by adjusting the value of the anti-shock filter output coefficient K35.

This function can be turned on and off by D19 of $1 when the brake circuit (described hereafter) is off. (See Table 5-17.)

This circuit can also support an external vibration detection circuit, and can set the TRK servo filter to gain-up mode by inputting high level to the ATSK pin.

When the upper 8 bits of the command register are $1, vibration detection can be monitored from the SENS pin.

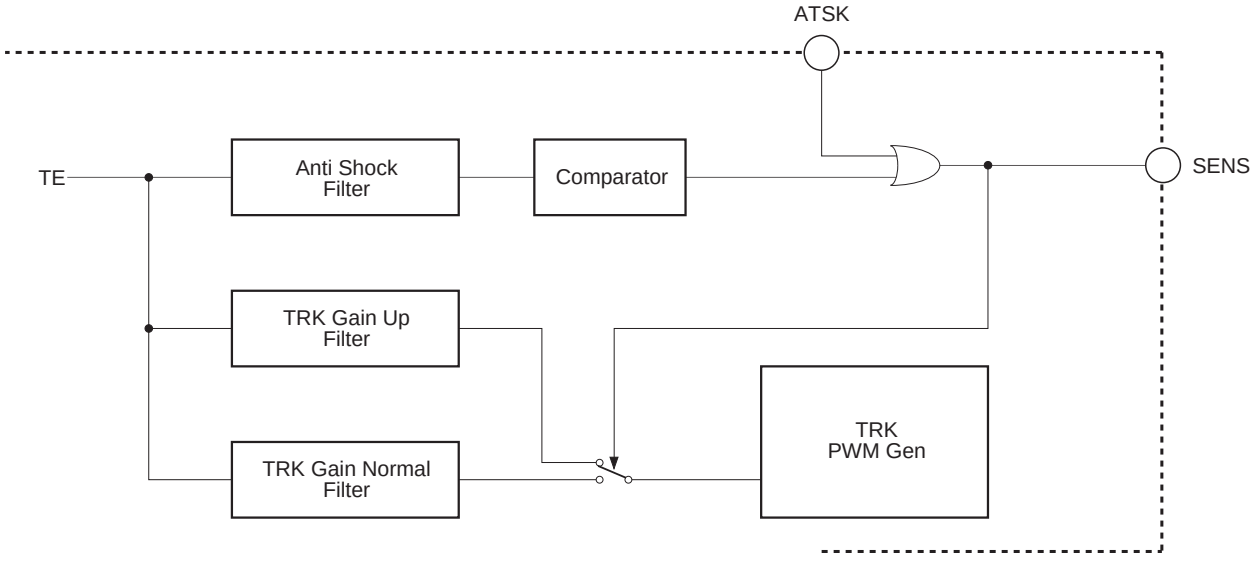


Fig. 5-14.

§5-12. Brake Circuit

Immediately after a long distance track jump it tends to be hard for the actuator to settle and for the servo to turn on.

The brake circuit prevents these phenomenon.

The brake circuit is to use tracking drive as a brake by cutting unnecessary portions of it utilizing the 180° offset in the RF envelope and tracking error phase relationship which occurs when the actuator traverses the track in the radial direction from the inner track to the outer track and vice versa. (See Figs. 5-15 and 5-16.)

Concretely, this operation is achieved by masking the tracking drive using the TRKCNCL signal generated by loading the MIRR signal at the edge of the TZC (Tracking Zero Cross) signal.

The brake circuit can be turned on and off by D18 of $1. (See Fig. 5-17.)

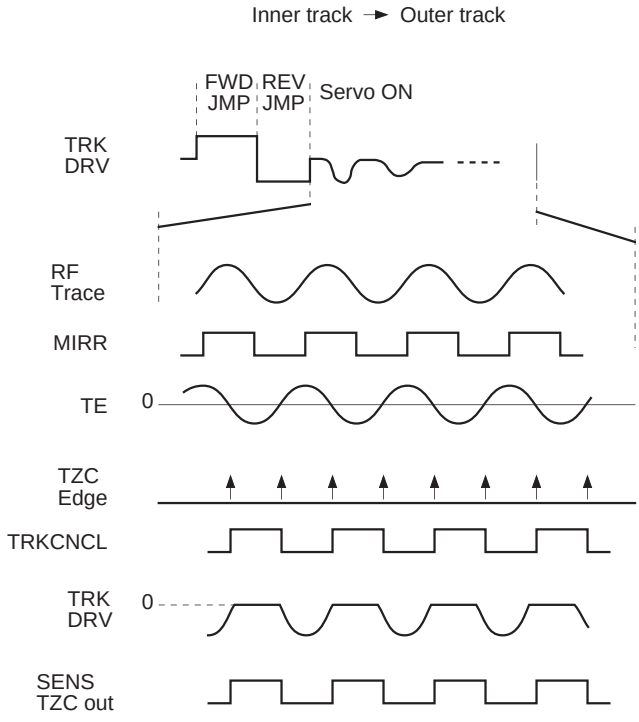


Fig. 5-15.

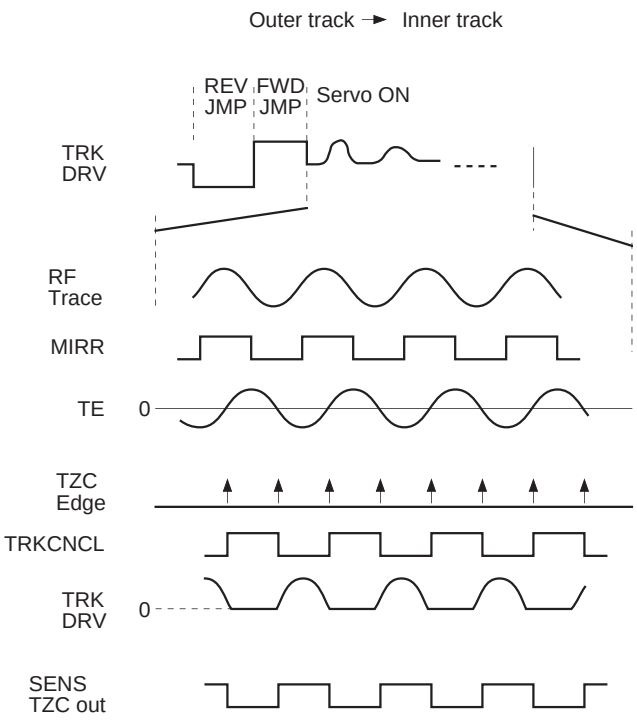


Fig. 5-16.

Register name	Command	D23 to D20	D19 to D16	
1	TRACKING CONTROL	0 0 0 1	1 0 ∗ ∗	ANTI SHOCK ON
			0 ∗ ∗ ∗	ANTI SHOCK OFF
			∗ 1 ∗ ∗	BRAKE ON
			∗ 0 ∗ ∗	BRAKE OFF
			∗ ∗ 0 ∗	TRACKING GAIN NORMAL
			∗ ∗ 1 ∗	TRACKING GAIN UP
			∗ ∗ ∗ 1	TRACKING GAIN UP FILTER SELECT 1
			∗ ∗ ∗ 0	TRACKING GAIN UP FILTER SELECT 2

∗: Don't care

Fig. 5-17.

§5-13. COUT Signal

The COUT signal is output to count the number of tracks during traverse, etc. It is basically generated by loading the MIRR signal at both edges of the TZC signal. And the used TZC signal can be selected among three different phases for each COUT signal application.

- HPTZC: For 1-track jumps
  Fast phase COUT signal generation with a fast phase TZC signal. (The TZC phase is advanced by a cut-off 1kHz digital HPF; when MCK = 128Fs.)
- STZC: For COUT signal generation when MIRR is externally input and for applications other than COUT generation.
  This is generated from sampling TE at 700kHz. (when MCK = 128Fs)
- DTZC: For High-speed traverse
  Reliable COUT signal generation with a delayed phase STZC signal.

Since it takes some time to generate the MIRR signal, it is necessary to delay the TZC signal in accordance with the MIRR signal delay during high-speed traverse.
The COUT signal output method is switched with D15 and 14 of $3.

When D15 = 1 : STZC
When D15 = 0 and D14 = 0 : HPTZC
When D15 = 0 and D14 = 1 : DTZC

When the DTZC is selected, the delay can be selected from two values with D14 of $36.

§5-14. Serial Readout Circuit

The following measurement and adjustment results can be read out from the SENS pin by inputting the readout clock to the SCLK pin by $39. (See Fig. 5-18, Table 5-19 and "Description of SENS Signals".)

Specified commands

$390C: VC AVRG measurement result
$3908: FE AVRG measurement result
$3904: TE AVRG measurement result
$391F: RF AVRG measurement result
$3953: FCS AGCNTL coefficient result
$3963: TRK AGCNTL coefficient result
$391C: TRVSC adjustment result
$391D: FBIAS register value

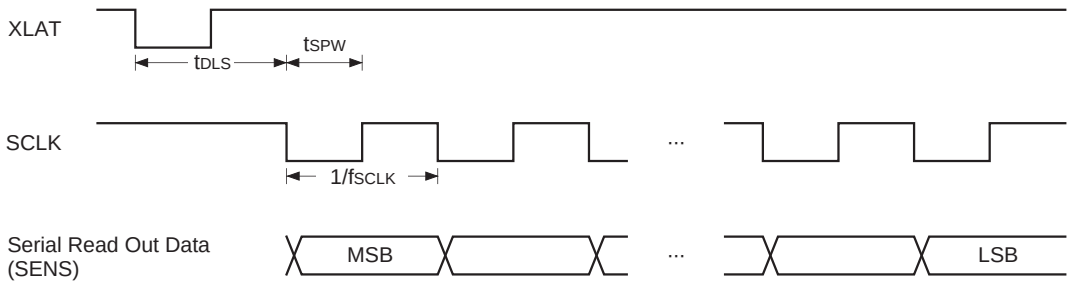


Fig. 5-18.

Item	Symbol	Min.	Typ.	Max.	Unit
SCLK frequency	f_{SCLK}			16	MHz
SCLK pulse width	t_{SPW}	31.3			ns
Delay time	t_{DLS}	15			µs

Table 5-19.

During readout, the upper 8 bits of the command register must be 39 (Hex).

§5-15. Writing to the Coefficient RAM

The coefficient RAM can be rewritten by $34. All coefficients have default values in the built-in ROM, and transfer from the ROM to the RAM is completed approximately 40µs (when MCK = 128Fs) after the XRST pin rises. (The coefficient RAM cannot be rewritten during this period.)

After that, the characteristics of each built-in filter can be finely adjusted by rewriting the data for each address of the coefficient RAM.

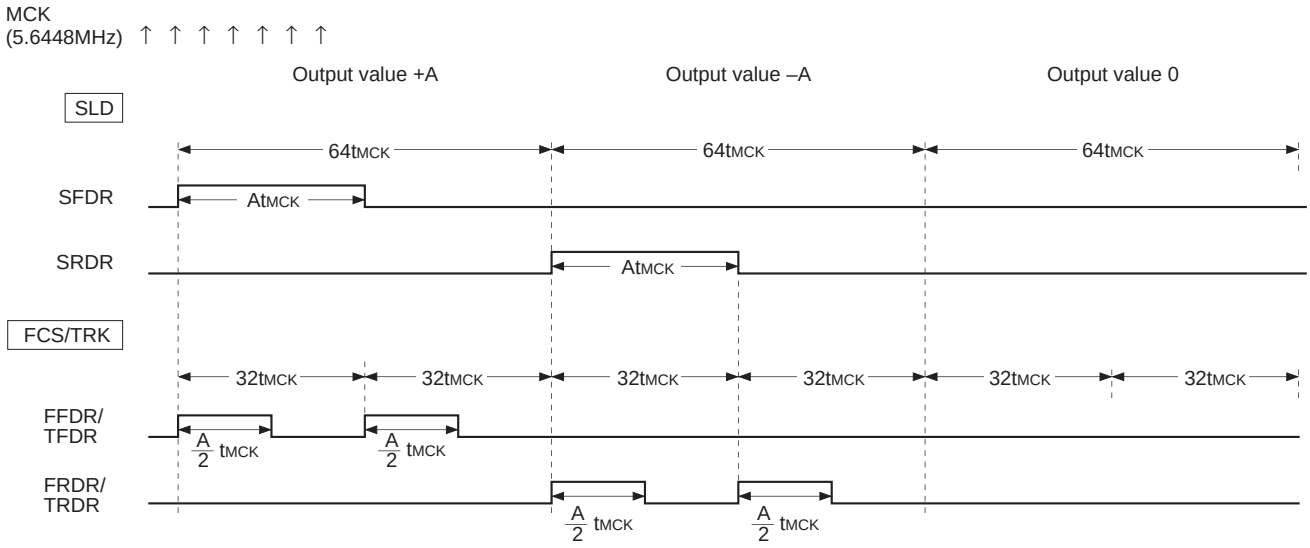
The coefficient rewrite command is comprised of 24 bits, with D14 to D8 of $34 as the address (D15 = 0) and D7 to D0 as data. Coefficient rewriting is completed 11.3µs (when MCK = 128Fs) after the command is received. When rewriting multiple coefficients, be sure to wait 11.3µs (when MCK = 128Fs) before sending the next rewrite command.

§5-16. PWM Output

FCS, TRK and SLD outputs are output as PWM waveforms.

In particular, FCS and TRK permit accurate drive by using a double oversampling noise shaper.

Timing Chart 5-20 and Fig. 5-21 show examples of output waveforms and drive circuits.



$$t_{MCK} = \frac{1}{5.6448MHz} \approx 180ns$$

Timing Chart 5-20.

Example of Drive Circuit

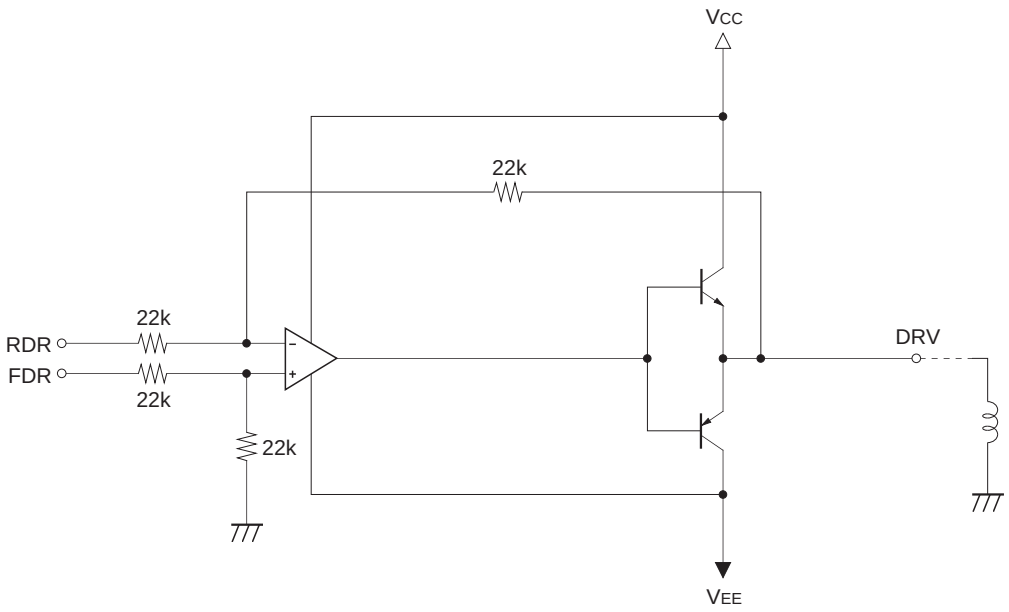
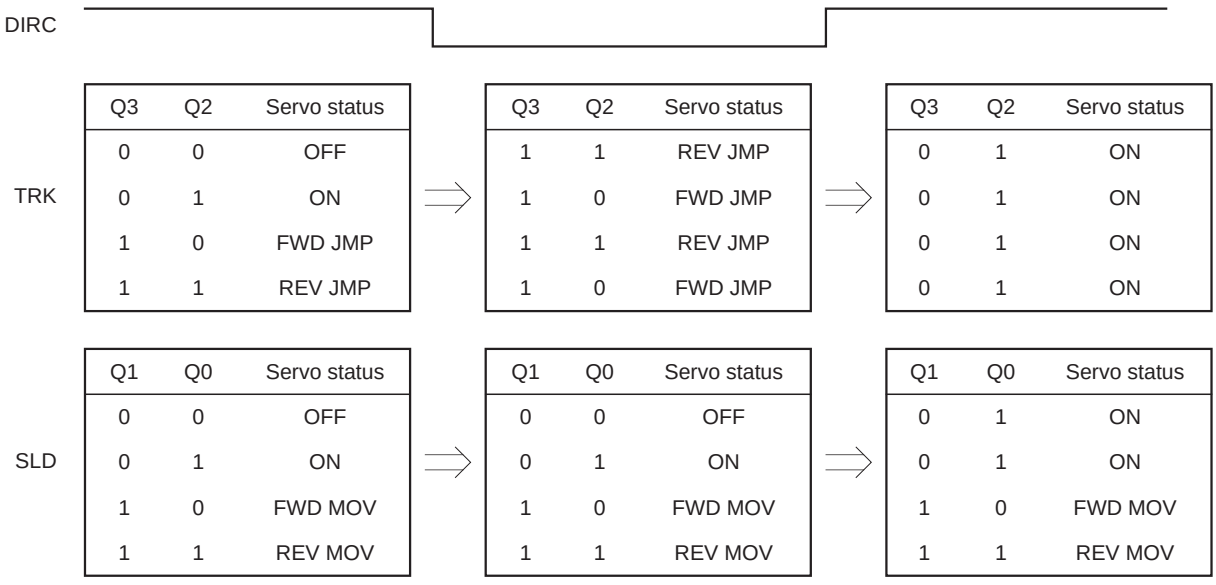


Fig. 5-21. Operational Amplifier Drive Circuit

§5-17. DIRC Input Pin

The $2 command register can be changed by operating the DIRC input pin.
Using the DIRC pin simplifies serial data transfer during TRKJMP.
Fig. 5-22 shows $2 command register changes produced by DIRC pin changes.
Also, Timing Chart 5-23 shows DIRC-based operations during TRKJMP.
High level must be input to the DIRC pin when the XRST pin rises from low to high.



TRK	Q3	Q2	Servo status
	0	0	OFF
	0	1	ON
	1	0	FWD JMP
	1	1	REV JMP

TRK	Q3	Q2	Servo status
	1	1	REV JMP
	1	0	FWD JMP
	1	1	REV JMP
	1	0	FWD JMP

TRK	Q3	Q2	Servo status
	0	1	ON
	0	1	ON
	0	1	ON
	0	1	ON

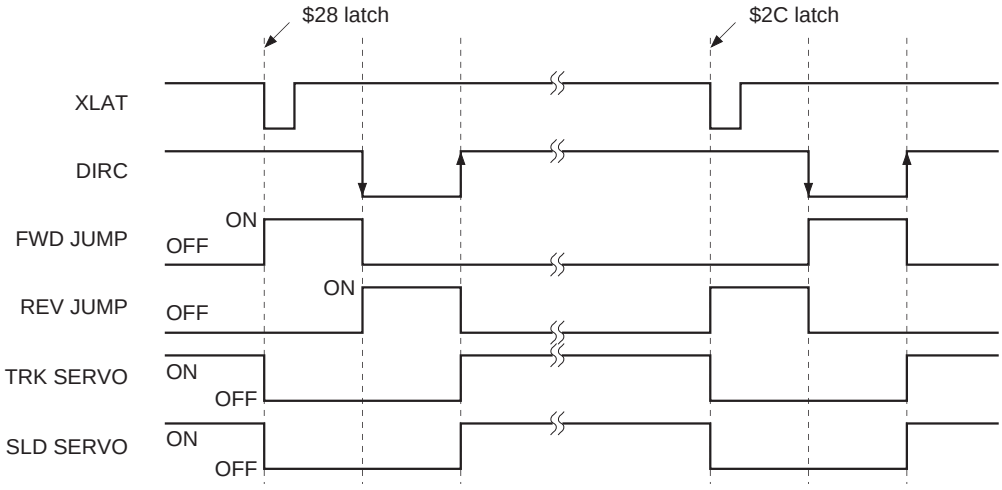
SLD	Q1	Q0	Servo status
	0	0	OFF
	0	1	ON
	1	0	FWD MOV
	1	1	REV MOV

SLD	Q1	Q0	Servo status
	0	0	OFF
	0	1	ON
	1	0	FWD MOV
	1	1	REV MOV

SLD	Q1	Q0	Servo status
	0	1	ON
	0	1	ON
	1	0	FWD MOV
	1	1	REV MOV

Q3, Q2, Q1 and Q0 correspond to D19, D18, D17 and D16 of $2.

Fig. 5-22.



Timing Chart 5-23.

§5-18. Servo Status Changes Produced by the LOCK Signal

When the LOCK signal becomes low, the TRK servo switches to the gain-up mode and the SLD servo turns off in order to prevent SLD free-running.
Setting D6 (LKSW) of $38 to 1 deactivates this function.
In other words, neither the TRK servo nor the SLD servo change even when the LOCK signal becomes low.
This enables microcomputer control.

§5-19. Description of Commands and Data Sets

The following description contains portions which convert internal voltages into the values when they are output externally and describe them as input conversion or output conversion.
Input conversion converts these voltages into the voltages entering input pins before A/D conversion.
Output conversion converts PWM output values into analog voltage values.

$34

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	KA6	KA5	KA4	KA3	KA2	KA1	KA0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0

When D15 = 0

KA6 to KA0: Coefficient address

KD7 to KD0: Coefficient data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	0	FBL9	FBL8	FBL7	FBL6	FBL5	FBL4	FBL3	FBL2	FBL1	—

When D15 = D14 = D13 = D12 = D11 = 1 ($34F)

D10 = 0

FBIAS LIMIT register write

FBL9 to FBL1: Data; data compared with FB9 to 1, FBL9 = MSB.

When using the FBIAS register in counter mode, counter operation stops when the value of FB9 to 1 matches with FBL9 to 1.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	0	1	FB9	FB8	FB7	FB6	FB5	FB4	FB3	FB2	FB1	—

When D15 = D14 = D13 = D12 = 1 ($34F)

D11 = 0, D10 = 1

FBIAS register write

FB9 to FB1: Data; FB9 is MSB two's complement data.

For FE input conversion, FB9 to FB1 = 011111111 corresponds to 255/256 × V_{DD}/4 and FB9 to FB1 = 100000000 to –256/256 × V_{DD}/4 respectively. (V_{DD}: supply voltage)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	0	0	TV9	TV8	TV7	TV6	TV5	TV4	TV3	TV2	TV1	TV0

When D15 = D14 = D13 = D12 = 1 ($34F)

D11 = 0, D10 = 0

TRVSC register write

TV9 to TV0: Data; TV9 is MSB two's complement data.

For TE input conversion, TV9 to TV0 = 0011111111 corresponds to 255/256 × V_{DD}/4 and TV9 to TV0 = 1100000000 to –256/256 × V_{DD}/4 respectively. (V_{DD}: supply voltage)

Note) • When the TRVSC register is read out, the data length is 9 bits. At this time, data corresponding to each bit TV8 to TV0 during external write are read out.

• When reading out internally measured values and then writing these values externally, set TV9 the same as TV8.

$35 (preset: $35 58 2D)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FT1	FT0	FS5	FS4	FS3	FS2	FS1	FS0	FTZ	FG6	FG5	FG4	FG3	FG2	FG1	FG0

FT1, FT0, FTZ: Focus search-up speed

Default value: 010 (0.673 × V_{DD} V/s)

Focus drive output conversion

	FT1	FT0	FTZ	Focus search speed [V/s]
*	0	0	0	1.35 × V_{DD}
	0	1	0	0.673 × V_{DD}
	1	0	0	0.449 × V_{DD}
	1	1	0	0.336 × V_{DD}
	0	0	1	1.79 × V_{DD}
	0	1	1	1.08 × V_{DD}
	1	0	1	0.897 × V_{DD}
	1	1	1	0.769 × V_{DD}

*: preset, V_{DD}: PWM driver supply voltage

FS5 to FS0: Focus search limit voltage

Default value: 011000 (±24/64 × V_{DD}, V_{DD}: PWM driver supply voltage)

Focus drive output conversion

FG6 to FG0: AGF convergence gain setting value

Default value: 0101101

$36 (preset: $36 0E 2E)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TDZC	DTZC	TJ5	TJ4	TJ3	TJ2	TJ1	TJ0	SFJP	TG6	TG5	TG4	TG3	TG2	TG1	TG0

TDZC: Selects the TZC signal for generating the TRKCNCL signal during brake circuit operation.

TDZC = 0: the edge of the HPTZC or STZC signal, whichever has the faster phase, is used.

TDZC = 1: the edge of the HPTZC or STZC signal or the tracking drive signal zero-cross, whichever has the faster phase, is used. (See §5-12.)

DTZC: DTZC delay (8.5/4.25µs, when MCK = 128Fs)

Default value: 0 (4.25µs)

TJ5 to TJ0: Track jump voltage

Default value: 001110 (≈ ±14/64 × V_{DD}, V_{DD}: PWM driver supply voltage)

Tracking drive output conversion

SFJP: Surf jump mode on/off

The tracking PWM output is made by adding the tracking filter output and TJReg (TJ5 to 0), by setting D7 to 1 (on)

TG6 to TG0: AGT convergence gain setting value

Default value: 0101110

$37 (preset: $37 50 BA)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FZSH	FZSL	SM5	SM4	SM3	SM2	SM1	SM0	AGS	AGJ	AGGF	AGGT	AGV1	AGV2	AGHS	AGHT

FZSH, FZSL: FZC (Focus Zero Cross) slice level

Default value: 01 (1/8 × V_{DD}/2, V_{DD}: supply voltage); FE input conversion

	FZSH	FZSL	Slice level
	0	0	1/4 × V_{DD}/2
*	0	1	1/8 × V_{DD}/2
	1	0	1/16 × V_{DD}/2
	1	1	1/32 × V_{DD}/2

*: preset

SM5 to SM0: Sled move voltage

Default value: 010000 (≈ ±16/64 × V_{DD}, V_{DD}: PWM driver supply voltage)

Sled drive output conversion

AGS: AGCNTL self-stop on/off

Default value: 1 (on)

AGJ: AGCNTL convergence completion judgment time during low sensitivity adjustment (31/63ms, when MCK = 128Fs)

Default value: 0 (63ms)

AGGF: Focus AGCNTL internally generated sine wave amplitude (small/large)

Default value: 1 (large)

AGGT: Tracking AGCNTL internally generated sine wave amplitude (small/large)

Default value: 1 (large)

		FE/TE input conversion
AGGF	0 (small)	1/32 × V_{DD}/2
	1 (large)*	1/16 × V_{DD}/2
AGGT	0 (small)	1/16 × V_{DD}/2
	1 (large)*	1/8 × V_{DD}/2

*: preset

AGV1: AGCNTL convergence sensitivity during high sensitivity adjustment; high/low

Default value: 1 (high)

AGV2: AGCNTL convergence sensitivity during low sensitivity adjustment; high/low

Default value: 0 (low)

AGHS: AGCNTL high sensitivity adjustment on/off

Default value: 1 (on)

AGHT: AGCNTL high sensitivity adjustment time (128/256ms, when MCK = 128Fs)

Default value: 0 (256ms)

$38 (preset: $38 00 00)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VCLM	VCLC	FLM	FLC0	RFLM	RFLC	AGF	AGT	DFS	LKSW	TBLM	TCLM	FLC1	TLC2	TLC1	TLC0

◎ VCLM: VC level measurement (on/off)
VCLC: VC level compensation for FCS In register (on/off)
◎ FLM: Focus zero level measurement (on/off)
FLC0: Focus zero level compensation for FZC register (on/off)
◎ RFLM: RF zero level measurement (on/off)
RFLC: RF zero level compensation (on/off)
AGF: Focus auto gain adjustment (on/off)
AGT: Tracking auto gain adjustment (on/off)
DFSW: Defect disable switch (on/off)
Setting this switch to 1 (on) disables the defect countermeasure circuit.
LKSW: Lock switch (on/off)
Setting this switch to 1 (on) disables the sled free-running prevention circuit.
TBLM: Traverse center measurement (on/off)
◎ TCLM: Tracking zero level measurement (on/off)
FLC1: Focus zero level compensation for FCS In register (on/off)
TLC2: Traverse center compensation (on/off)
TLC1: Tracking zero level compensation (on/off)
TLC0: VC level compensation for TRK/SLD In register (on/off)

Note) Commands marked with ◎ are accepted every 2.9ms. (when MCK = 128Fs)
All commands are on when set to 1.

$39

D15	D14	D13	D12	D11	D10	D9	D8
DAC	SD6	SD5	SD4	SD3	SD2	SD1	SD0

DAC: Serial data readout DAC mode (on/off)

SD6 to SD0: Serial readout data select

SD6	SD5	Readout data			Readout data length	
1	Coefficient RAM data for address = SD5 to SD0				8 bit	
0	1	Data RAM data for address = SD4 to SD0			16 bit	
0	0	SD4	SD3 to SD0			
		1	1 1 1 1	RF AVRG register	8 bit	$399F
			1 1 1 0	RFDC input signal	8 bit	$399E
			1 1 0 1	FBIAS register	9 bit	$399D
			1 1 0 0	TRVSC register	9 bit	$399C
			0 0 1 1	RFDC envelope (bottom)	8 bit	$3993
			0 0 1 0	RFDC envelope (peak)	8 bit	$3992
			0 0 0 1	RFDC envelope (peak) – (bottom)	8 bit	$3991
		0	1 1 * *	VC AVRG register	9 bit	$398C
			1 0 * *	FE AVRG register	9 bit	$3988
			0 1 * *	TE AVRG register	9 bit	$3984
			0 0 1 1	FE input signal	8 bit	$3983
			0 0 1 0	TE input signal	8 bit	$3982
			0 0 0 1	SE input signal	8 bit	$3981
			0 0 0 0	VC input signal	8 bit	$3980

Note) Coefficients K40 to K4F cannot be read out. *: Don't care

See the description for SRO1 and SRO0 of $3F concerning readout methods for the above data.

$3A (preset: $3A 00 00)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	FBON	FBSS	FBUP	FBV1	FBV0	0	TJD0	FPS1	FPS0	TPS1	TPS0	0	SJHD	INBK	MTI0

FBON: FBIAS (focus bias) register addition (on/off)
The FBIAS register value is added to the signal loaded into the FCS In register by FBON = 1 (on).

FBSS: FBIAS (focus bias) register/counter switching
FBSS = 0: register, FBSS = 1: counter.

FBUP: FBIAS (focus bias) counter up/down operation switching
This performs counter up/down control when FBSS = 1. FBUP = 0: down counter,
FBUP = 1: up counter.

FBV1, FBV0: FBIAS (focus bias) counter voltage switching
The number of FCS BIAS count-up/-down steps per cycle is decided by these bits.

	FBV1	FBV0	Number of steps per cycle
*	0	0	1
	0	1	2
	1	0	4
	1	1	8

*: preset

The counter changes once for each sampling cycle of the focus servo filter. When MCK is 128Fs, the sampling frequency is 88.2kHz. When converted to FE input, 1 step is approximately 1/29 × V_{DD}/2, V_{DD} = supply voltage.

TJD0: This sets the tracking servo filter data RAM to 0 when switched from track jump to servo on only when SFJP = 1 (during surf jump operation).

FPS1, FPS0: Gain setting when transferring data from the focus filter to the PWM block.

TPS1, TPS0: Gain setting when transferring data from the tracking filter to the PWM block.
This is effective for increasing the overall gain in order to widen the servo band.
Operation when FPS1, FPS0 (TPS1, TPS0) = 00 is the same as usual (7-bit shift). However, 6dB, 12dB and 18dB can be selected independently for focus and tracking by setting the relative gain to 0dB when FPS1, FPS0 (TPS1, TPS0) = 00.

	FPS1	FPS0	Relative gain
*	0	0	0dB
	0	1	+6dB
	1	0	+12dB
	1	1	+18dB

TPS1	TPS0	Relative gain	
0	0	0dB	*
0	1	+6dB	
1	0	+12dB	
1	1	+18dB	

*: preset

SJHD: This holds the tracking filter output at the value when surf jump starts during surf jump.

INBK: When INBK = 0 (off), the brake circuit masks the tracking drive signal with TRKCNCL which is generated by taking the MIRR signal at the TZC edge. When INBK = 1 (on), the tracking filter input is masked instead of the drive output.

MTI0: The tracking filter input is masked when the MIRR signal is high by setting MTI0 = 1 (on).

$3B (preset: $3B E0 50)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFO2	SFO1	SDF2	SDF1	MAX2	MAX1	SFOX	BTF	D2V2	D2V1	D1V2	D1V1	RINT	0	0	0

SFOX, SFO2, SFO1: FOK slice level

Default value: 011 (28/256 × V_{DD}/2, V_{DD} = supply voltage)

RFDC input conversion

	SFOX	SFO2	SFO1	Slice level
	0	0	0	16/256 × V_{DD}/2
	0	0	1	20/256 × V_{DD}/2
	0	1	0	24/256 × V_{DD}/2
*	0	1	1	28/256 × V_{DD}/2
	1	0	0	32/256 × V_{DD}/2
	1	0	1	40/256 × V_{DD}/2
	1	1	0	48/256 × V_{DD}/2
	1	1	1	56/256 × V_{DD}/2

*: preset

SDF2, SDF1: DFCT slice level
Default value: 10 (0.0313 × V_{DD}V)
RFDC input conversion

	SDF2	SDF1	Slice level
	0	0	0.0156 × V_{DD}
	0	1	0.0234 × V_{DD}
*	1	0	0.0313 × V_{DD}
	1	1	0.0391 × V_{DD}

∗: preset, V_{DD}: supply voltage

MAX2, MAX1: DFCT maximum time
Default value: 00 (no timer limit)

	MAX2	MAX1	DFCT maximum time
*	0	0	No timer limit
	0	1	2.00ms
	1	0	2.36
	1	1	2.72

∗: preset

BTF: Bottom hold double-speed count-up mode for MIRR signal generation
On/off (default: off)
On when set to 1.

D2V2, D2V1: Peak hold 2 for DFCT signal generation
Count-down speed setting
Default value: 01 (0.086 × V_{DD} V/ms, 44.1kHz)
[V/ms] unit items indicate RFDC input conversion; [kHz] unit items indicate the operating frequency of the internal counter.

	D2V2	D2V1	Count-down speed	
			[V/ms]	[kHz]
	0	0	0.0431 × V_{DD}	22.05
*	0	1	0.0861 × V_{DD}	44.1
	1	0	0.172 × V_{DD}	88.2
	1	1	0.344 × V_{DD}	176.4

∗: preset, V_{DD}: supply voltage

D1V2, D1V1: Peak hold 1 for DFCT signal generation
Count-down speed setting
Default value: 01 (0.688 × V_{DD} V/ms, 352.8kHz)
[V/ms] unit items indicate RFDC input conversion; [kHz] unit items indicate the operating frequency of the internal counter.

	D1V2	D1V1	Count-down speed	
			[V/ms]	[kHz]
	0	0	0.344 × V_{DD}	176.4
*	0	1	0.688 × V_{DD}	352.8
	1	0	1.38 × V_{DD}	705.6
	1	1	2.75 × V_{DD}	1411.2

∗: preset, V_{DD}: supply voltage

RINT: This initializes the initial-state registers of the circuits which generate MIRR, DFCT and FOK.

$3C (preset: $3C 00 80)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
COSS	COTS	CETZ	CETF	COT2	COT1	MOT2	0	BTS1	BTS0	MRC1	MRC0	0	0	0	0

COSS, COTS: These select the TZC signal used when generating the COUT signal.
Preset = HPTZC.

	COSS	COTS	TZC
	1	—	STZC
*	0	0	HPTZC
	0	1	DTZC

*: preset, —: don't care

STZC is the TZC generated by sampling the TE signal at 700kHz. (when MCK = 128Fs)
DTZC is the delayed phase STZC. (The delay amount can be selected by D14 of $36.)
HPTZC is the fast phase TZC passed through a HPF with a cut-off frequency of 1kHz.
See §5-13.

CETZ: The input from the TE pin normally enters the TRK filter and is used to generate the TZC signal. However, the input from the CE pin can also be used. This function is for the center error servo.
When CETZ = 0, the TZC signal is generated by using the TE input signal.
When CETZ = 1, the TZC signal is generated by using the CE input signal.

CETF: When CETF = 0, the signal input to the TE pin is input to the TRK servo filter.
When CETF = 1, the signal input to the CE pin is input to the TRK servo filter.

These commands output the TZC signal.
COT2, COT1: This outputs the TZC signal from the COUT pin.

	COT2	COT1	COUT pin output
	1	—	STZC
	0	1	HPTZC
*	0	0	COUT

*: preset, —: don't care

MOT2: The STZC signal is output from the MIRR pin by setting MOT2 to 1.

These commands set the MIRR signal generation circuit.

BTS1, BTS0: This sets the count-up speed for the bottom hold value of the MIRR generation circuit.
The time per step is approximately 708 ns (when MCK = 128Fs). The preset value is BTS1 = 1, BTS0 = 0 like the CXD2586R. However, this is valid only when BTF of $3B is 0.

MRC1, MRC0: This sets the minimum pulse width for masking the MIRR signal of the MIRR generation circuit.
As noted in §5-9, the MIRR signal is generated by comparing the waveform obtained by subtracting the bottom hold value from the peak hold value with the MIRR comparator level. Strictly speaking, however, for MIRR to become high, these levels must be compared continuously for a certain time. This sets that time.
The preset value is MRC1 = 0, MRC0 = 0 same time as the CXD2586R.

	BTS1	BTS0	Number of count-up steps per cycle
	0	0	1
	0	1	2
*	1	0	4
	1	1	8

MRC1	MRC0	Setting time [µs]
0	0	5.669 *
0	1	11.338
1	0	22.675
1	1	45.351

*: preset (when MCK = 128Fs)

$3D (preset: $3D 00 00)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFID	SFSK	THID	THSK	0	TLD2	TLD1	TLD0	0	0	0	0	0	0	0	0

SFID: SLED servo filter input can be obtained not from SLD in Reg, but from M0D, which is the TRK filter second-stage output.
When the low frequency component of the tracking error signal obtained from the RF amplifier is attenuated, the low frequency can be amplified and input to the SLD servo filter.

SFSK: Only during TRK servo gain up2 operation, coefficient K30 is used instead of K00. Normally the DC gain between the TE input pin and M0D changes for TRK filter gain normal and gain up2, and error occurs in the DC level at M0D. In this case, the DC level of the signal transmitted to M00 can be kept uniform by adjusting the K30 value even during the above switching.

THID: TRK hold filter input can be obtained not from SLD in Reg, but from M0D, which is the TRK filter second-stage output.
When signals other than the tracking error signal from the RF amplifier are input to the SE input pin, the signal transmitted from the TE pin can be obtained as TRK hold filter input.

THSK: Only during TRK servo gain up2 operation, coefficient K46 is used instead of K40. Normally the DC gain between the TE input pin and M0D changes for TRK filter gain moral and gain up 2, and error occurs in the DC level at M0D. In this case, the DC level of the signal transmitted to M18 can be kept uniform by adjusting the K46 value even during the above switching.

* Please refer to § 5-21. Filter Composition, for further information on SFID, SFSK, THID and THSK commands.

TLD0 to 2: SLD filter correction turns on and off independently of the TRK filter.
Please refer also to $38 (TLC0 to 2) and Figure 5-3.

	TLC2	TLD2	Traverse center correction	
			TRK filter	SLD filter
*	0	—	OFF	OFF
	1	0	ON	ON
		1	ON	OFF

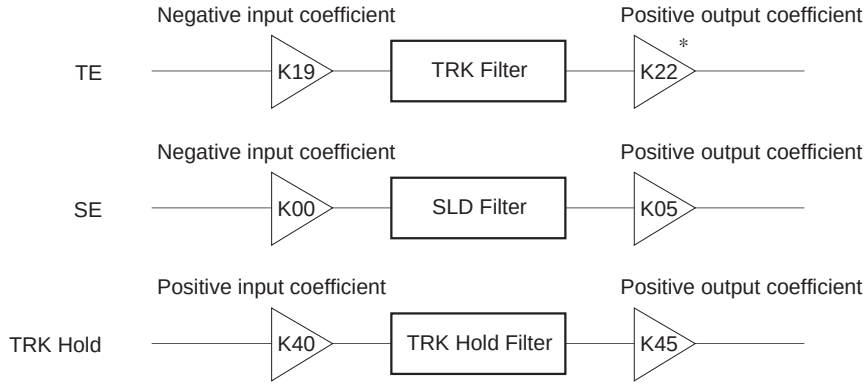
	TLC1	TLD1	Tracking zero level correction	
			TRK filter	SLD filter
*	0	—	OFF	OFF
	1	0	ON	ON
		1	ON	OFF

	TLC0	TLD0	VC level correction	
			TRK filter	SLD filter
*	0	—	OFF	OFF
	1	0	ON	ON
		1	ON	OFF

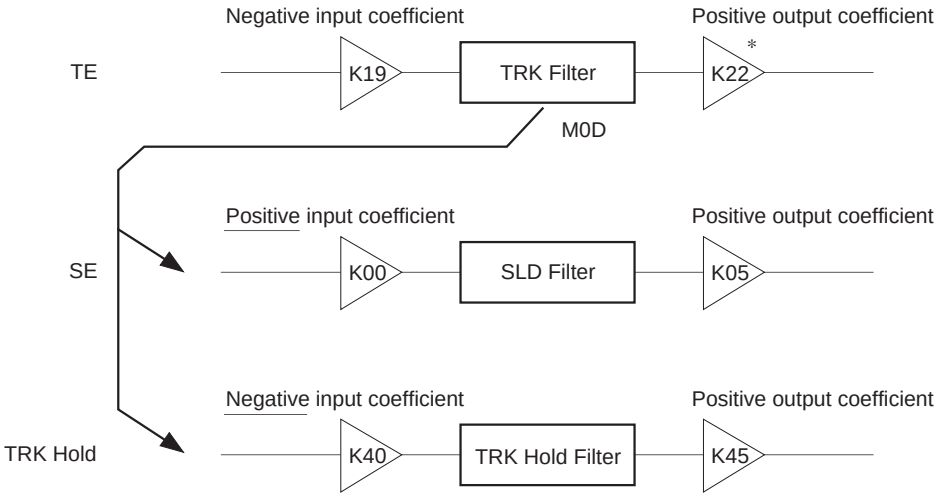
*: preset, — : Don't care

• Input coefficient inversion when SFID = 1 and THID = 1

The preset coefficients for the TRK filter are negative for input and positive for output. With this, the error input and servo that outputs reversed phase drive can be hypothesized.



When SFID = 1, the TRK filter negative input coefficient is applied to the SLD filter, so invert the SLD input coefficient (K00) code. (For example, inverting the code for coefficient K00: E0h results in 60h.)
For the same reason, when THID = 1, invert the TRK hold input coefficient (K40) code.



* for TRK servo gain normal
Please refer also to § 5-21. Filter Composition.

$3E (preset: $3E 00 00)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
F1NM	F1DM	F3NM	F3DM	T1NM	T1UM	T3NM	T3UM	DFIS	TLCD	0	LKIN	COIN	MDFI	MIRI	XT1D

F1NM, F1DM: Quasi double accuracy setting for FCS servo filter first-stage
On when set to 1; default = 0.
F1NM: Gain normal
F1DM: Gain down

T1NM, T1UM: Quasi double accuracy setting for TRK servo filter first-stage
On when set to 1; default = 0.
T1NM: Gain normal
T1UM: Gain up

F3NM, F3DM: Quasi double accuracy setting for FCS servo filter third-stage
On when set to 1; default = 0.
Generally, the advance amount of the phase becomes large by partially setting the FCS servo third-stage filter which is used as the phase compensation filter to double accuracy.
F3NM: Gain normal
F3DM: Gain down

T3NM, T3UM: Quasi double accuracy setting for TRK servo filter third-stage
On when set to 1; default = 0.
Generally, the advance amount of the phase becomes large by partially setting the TRK servo third-stage filter which is used as the phase compensation filter to double accuracy.
T3NM: Gain normal
T3UM: Gain up

Note) Filter first- and third-stage quasi double accuracy settings can be set individually.
See "FILTER Composition" at the end of this specification concerning quasi double accuracy.

DFIS: FCS hold filter input extraction node selection
0: M05 (Data RAM address 05); default
1: M04 (Data RAM address 04)

TLCD: This command masks the TLC2 command set by D2 of $38 only when FOK is low.
On when set to 1; default = 0

LKIN: When 0, the internally generated LOCK signal is output to the LOCK pin. (default)
When 1, the LOCK signal can be input from an external source to the LOCK pin.

COIN: When 0, the internally generated COUT signal is output to the COUT pin. (default)
When 1, the COUT signal can be input from an external source to the COUT pin.
The MIRR, DFCT and FOK signals can also be input from an external source.

MDFI: When 0, the MIRR, DFCT and FOK signals are generated internally. (default)
When 1, the MIRR, DFCT and FOK signals can be input from an external source through the MIRR, DFCT and FOK pins.

MIRI: When 0, the MIRR signal is generated internally. (default)
When 1, the MIRR signal can be input from an external source through the MIRR pin.

	MDFI	MIRI	
*	0	0	MIRR, DFCT and FOK are all generated internally.
	0	1	MIRR only is input from an external source.
	1	—	MIRR, DFCT and FOK are all input from an external source.

*: preset, —: don't care

XT1D: The clock input from FSTI can be used without being frequency-divided as the master clock for the servo block by setting D0 to 1. This command takes precedence over the XTSL pin, XT2D and XT4D. See the description of $3F for XT2D and XT4D.

$3F (preset: $3F 00 00)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	AGG4	XT4D	XT2D	0	DRR2	DRR1	DRR0	0	ASFG	FTQ	LPAS	SRO1	SRO0	AGHF	0

AGG4: This varies the amplitude of the internally generated sine wave using the AGGF and AGGT commands during AGC.
When AGG4 = 0, the default is used. When AGG4 = 1, the setting is as shown in the table below.

	AGGF (MSB)	AGGT (LSB)	TE/FE input conversion
*	0	0	$1/64 \times V_{DD}/2$
	0	1	$1/32 \times V_{DD}/2$
	1	0	$1/16 \times V_{DD}/2$
	1	1	$1/8 \times V_{DD}/2$

These settings are the same for both focus auto gain control and tracking auto gain control.

*: preset

XT4D, XT2D: MCK (digital servo master clock) frequency division setting
This command forcibly sets the frequency division ratio to 1/4, 1/2 or 1/1 when MCK is generated from the signal input to the FSTI pin. See the description of $3E for XT1D.

	XT1D	XT2D	XT4D	Frequency division ratio
*	0	0	0	According to XTSL
	1	—	—	1/1
	0	1	—	1/2
	0	0	1	1/4

*: preset, —: don't care

DRR2 to DRR0: Partially clears the Data RAM values (0 write).
The following values are cleared when set to 1 (on) respectively; default = 0
DRR2: M08, M09, M0A
DRR1: M00, M01, M02
DRR0: M00, M01, M02 only when LOCK = low
Note) Set DRR1 and DRR0 on for 50µs or more.

ASFG: When vibration detection is performed during anti-shock circuit operation, FCS servo filter is forcibly set to gain normal status.
On when set to 1; default = 0

LPAS: Built-in analog buffer low-current consumption mode
This mode reduces the total analog buffer current consumption for the VC, TE, SE and FE input analog buffers by using a single operational amplifier.
On when set to 1; default = 0
Note) When using this mode, first check whether each error signal is properly A/D converted using the SRO1 and SRO0 commands of $3F.

SRO1, SRO0: These commands are used to output various data externally continuously which have been specified with the $39 command. (However, D15 (DAC) of $39 must be set to 1.)
Digital output (SOCK, XOLT and SOUT) can be obtained from three specified pins by setting these commands to 1 respectively. The default is 0, 0. (no readout)

The output pins for each case are shown below.

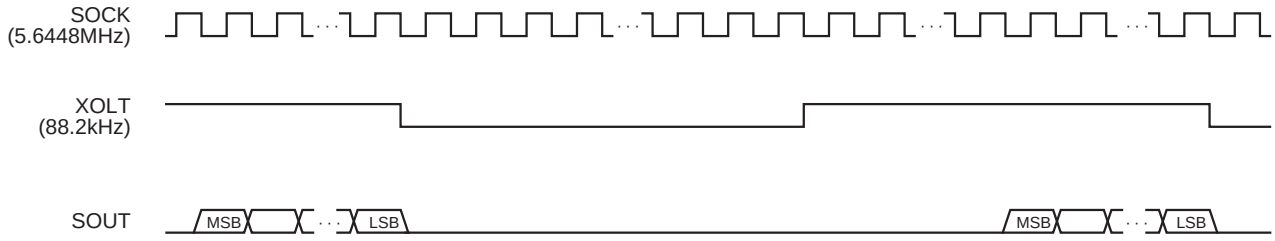
	SRO1 = 1	SRO0 = 1
SOCK	DA13 pin	DA10 pin
XOLT	DA12 pin	DA09 pin
SOUT	DA14 pin	DA11 pin

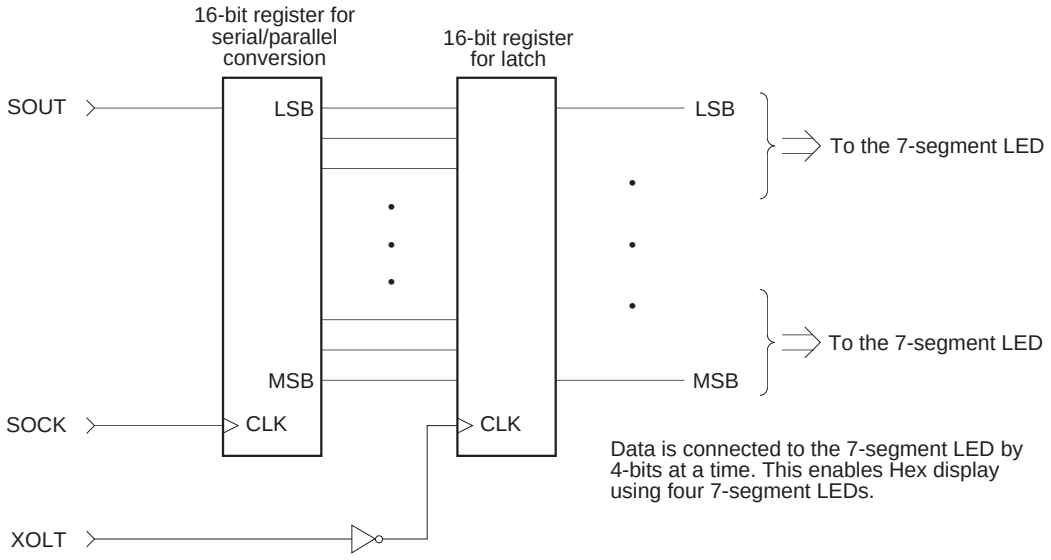
(See "Description of Data Readout" on the following page.)

AGHF: This halves the frequency of the internally generated sine wave during AGC.

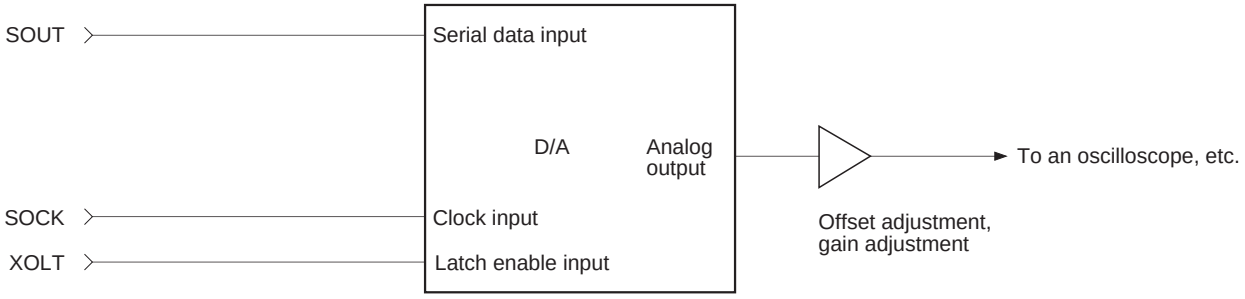
FTQ: The slope of the output during focus search is a quarter of the conventional output slope.

Description of Data Readout





Data is connected to the 7-segment LED by 4-bits at a time. This enables Hex display using four 7-segment LEDs.



Waveforms can be monitored with an oscilloscope using a serial input-type D/A converter as shown above.

§5-20. List of Servo Filter Coefficients

<Coefficient Preset Value Table (1)>

ADDRESS	DATA	CONTENTS
K00	E0	SLED INPUT GAIN
K01	81	SLED LOW BOOST FILTER A-H
K02	23	SLED LOW BOOST FILTER A-L
K03	7F	SLED LOW BOOST FILTER B-H
K04	6A	SLED LOW BOOST FILTER B-L
K05	10	SLED OUTPUT GAIN
K06	14	FOCUS INPUT GAIN
K07	30	SLED AUTO GAIN
K08	7F	FOCUS HIGH CUT FILTER A
K09	46	FOCUS HIGH CUT FILTER B
K0A	81	FOCUS LOW BOOST FILTER A-H
K0B	1C	FOCUS LOW BOOST FILTER A-L
K0C	7F	FOCUS LOW BOOST FILTER B-H
K0D	58	FOCUS LOW BOOST FILTER B-L
K0E	82	FOCUS PHASE COMPENSATE FILTER A
K0F	7F	FOCUS DEFECT HOLD GAIN
K10	4E	FOCUS PHASE COMPENSATE FILTER B
K11	32	FOCUS OUTPUT GAIN
K12	20	ANTI SHOCK INPUT GAIN
K13	30	FOCUS AUTO GAIN
K14	80	HPTZC / Auto Gain HIGH PASS FILTER A
K15	77	HPTZC / Auto Gain HIGH PASS FILTER B
K16	80	ANTI SHOCK HIGH PASS FILTER A
K17	77	HPTZC / Auto Gain LOW PASS FILTER B
K18	00	Fix*
K19	F1	TRACKING INPUT GAIN
K1A	7F	TRACKING HIGH CUT FILTER A
K1B	3B	TRACKING HIGH CUT FILTER B
K1C	81	TRACKING LOW BOOST FILTER A-H
K1D	44	TRACKING LOW BOOST FILTER A-L
K1E	7F	TRACKING LOW BOOST FILTER B-H
K1F	5E	TRACKING LOW BOOST FILTER B-L
K20	82	TRACKING PHASE COMPENSATE FILTER A
K21	44	TRACKING PHASE COMPENSATE FILTER B
K22	18	TRACKING OUTPUT GAIN
K23	30	TRACKING AUTO GAIN
K24	7F	FOCUS GAIN DOWN HIGH CUT FILTER A
K25	46	FOCUS GAIN DOWN HIGH CUT FILTER B
K26	81	FOCUS GAIN DOWN LOW BOOST FILTER A-H
K27	3A	FOCUS GAIN DOWN LOW BOOST FILTER A-L
K28	7F	FOCUS GAIN DOWN LOW BOOST FILTER B-H
K29	66	FOCUS GAIN DOWN LOW BOOST FILTER B-L
K2A	82	FOCUS GAIN DOWN PHASE COMPENSATE FILTER A
K2B	44	FOCUS GAIN DOWN DEFECT HOLD GAIN
K2C	4E	FOCUS GAIN DOWN PHASE COMPENSATE FILTER B
K2D	1B	FOCUS GAIN DOWN OUTPUT GAIN
K2E	00	NOT USED
K2F	00	NOT USED

* Fix indicates that normal preset values should be used.

<Coefficient Preset Value Table (2)>

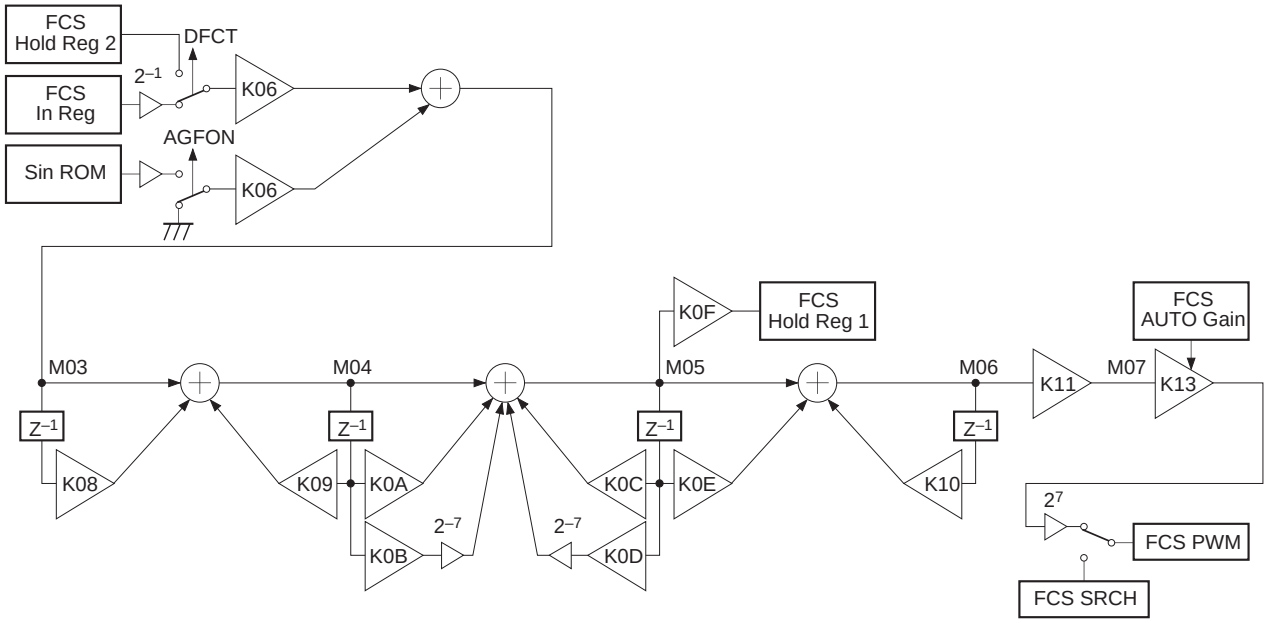
ADDRESS	DATA	CONTENTS
K30	80	SLED INPUT GAIN (Only when TRK Gain Up2 is accessed with SFSK = 1.)
K31	66	ANTI SHOCK LOW PASS FILTER B
K32	00	NOT USED
K33	7F	ANTI SHOCK HIGH PASS FILTER B-H
K34	6E	ANTI SHOCK HIGH PASS FILTER B-L
K35	20	ANTI SHOCK FILTER COMPARATE GAIN
K36	7F	TRACKING GAIN UP2 HIGH CUT FILTER A
K37	3B	TRACKING GAIN UP2 HIGH CUT FILTER B
K38	80	TRACKING GAIN UP2 LOW BOOST FILTER A-H
K39	44	TRACKING GAIN UP2 LOW BOOST FILTER A-L
K3A	7F	TRACKING GAIN UP2 LOW BOOST FILTER B-H
K3B	77	TRACKING GAIN UP2 LOW BOOST FILTER B-L
K3C	86	TRACKING GAIN UP PHASE COMPENSATE FILTER A
K3D	0D	TRACKING GAIN UP PHASE COMPENSATE FILTER B
K3E	57	TRACKING GAIN UP OUTPUT GAIN
K3F	00	NOT USED
K40	04	TRACKING HOLD FILTER INPUT GAIN
K41	7F	TRACKING HOLD FILTER A-H
K42	7F	TRACKING HOLD FILTER A-L
K43	79	TRACKING HOLD FILTER B-H
K44	17	TRACKING HOLD FILTER B-L
K45	6D	TRACKING HOLD FILTER OUTPUT GAIN
K46	00	TRACKING HOLD FILTER INPUT GAIN (Only when TRK Gain Up2 is accessed with THSK = 1.)
K47	00	NOT USED
K48	02	FOCUS HOLD FILTER INPUT GAIN
K49	7F	FOCUS HOLD FILTER A-H
K4A	7F	FOCUS HOLD FILTER A-L
K4B	79	FOCUS HOLD FILTER B-H
K4C	17	FOCUS HOLD FILTER B-L
K4D	54	FOCUS HOLD FILTER OUTPUT GAIN
K4E	00	NOT USED
K4F	00	NOT USED

§5-21. Filter Composition

The internal filter composition is shown below.

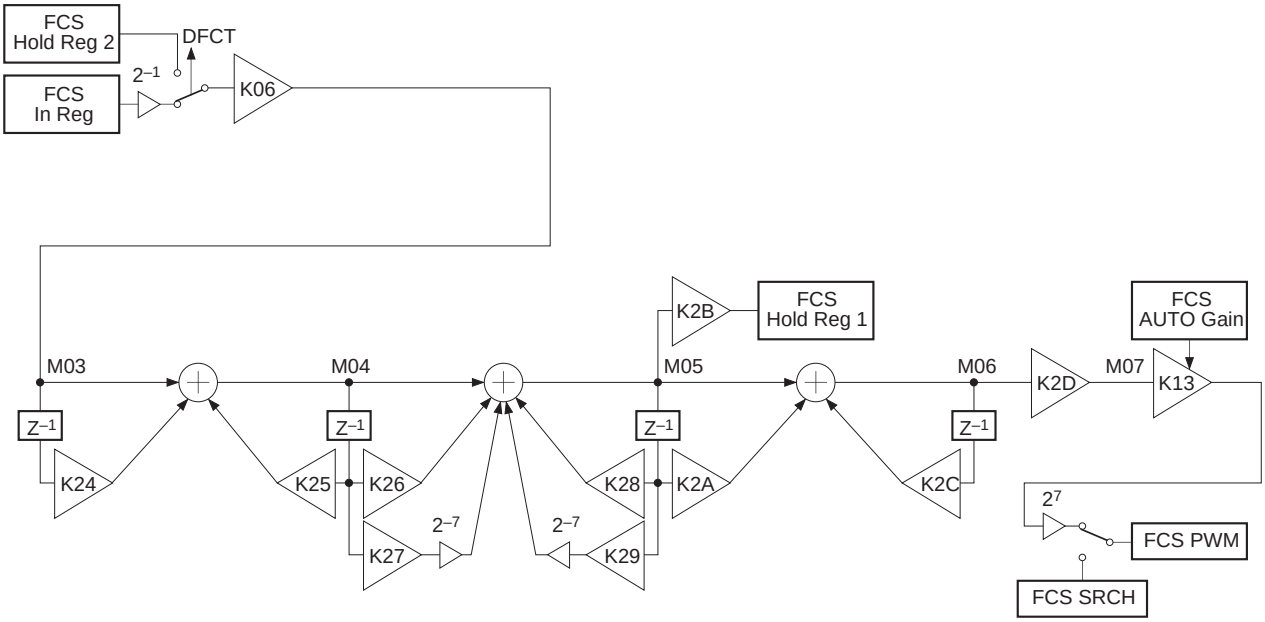
K∗∗ and M∗∗ indicate coefficient RAM and Data RAM address values respectively.

FCS Servo Gain Normal fs = 88.2kHz



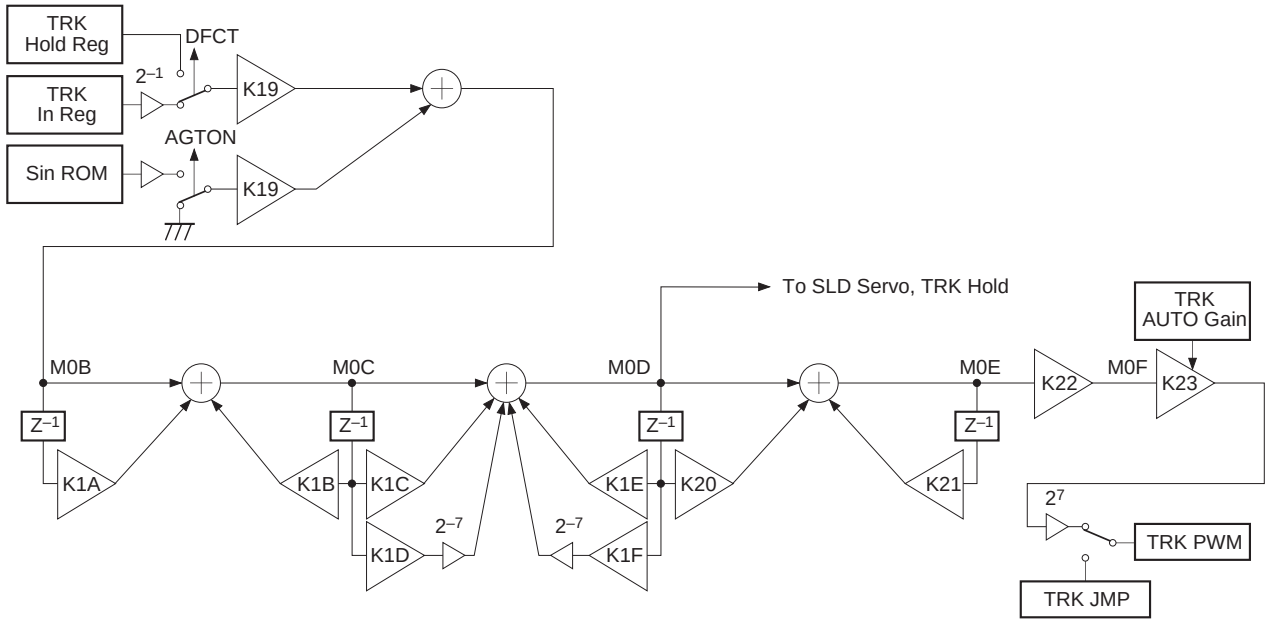
Note) Set the MSB bit of the K0B and K0D coefficients to 0.

FCS Servo Gain Down fs = 88.2kHz



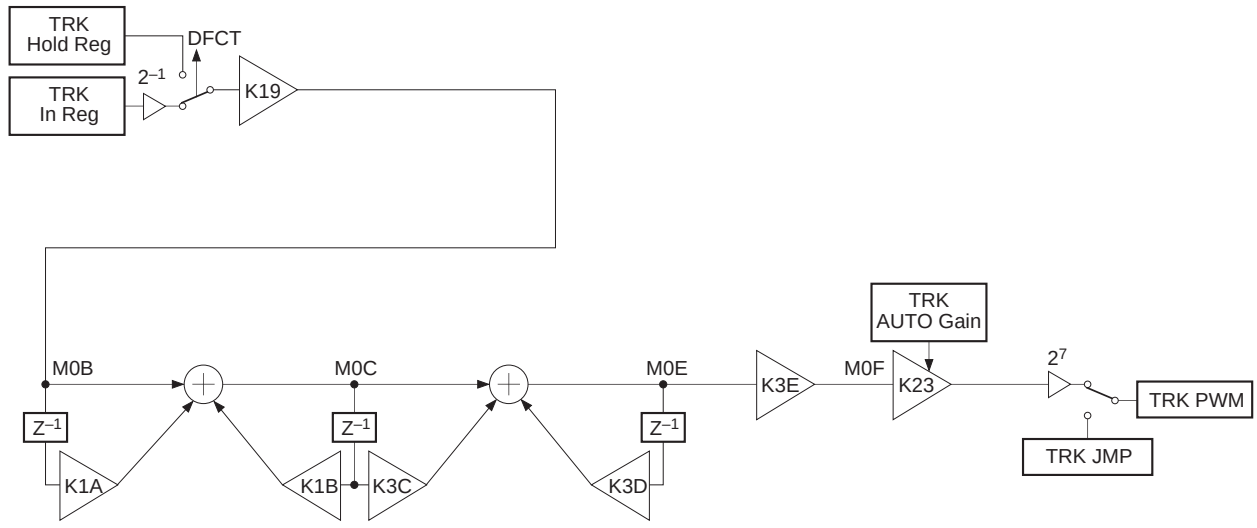
Note) Set the MSB bit of the K27 and K29 coefficients to 0.

TRK Servo Gain Normal fs = 88.2kHz

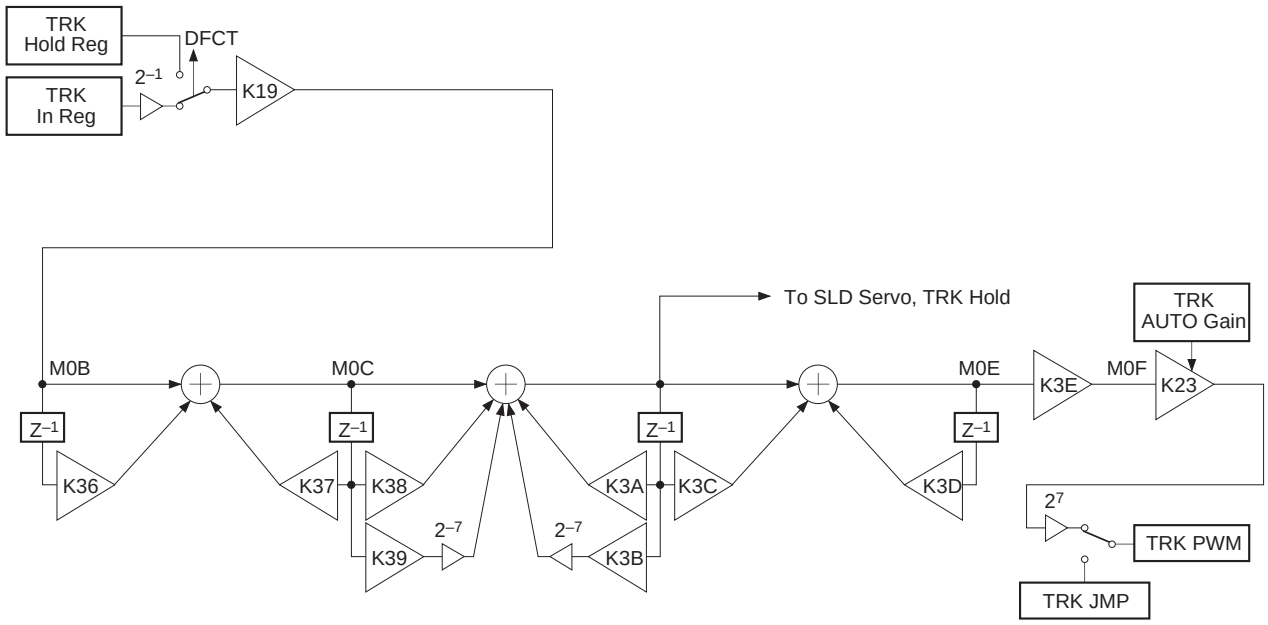


Note) Set the MSB bit of the K1D and K1F coefficients to 0.

TRK Servo Gain Up 1 fs = 88.2kHz

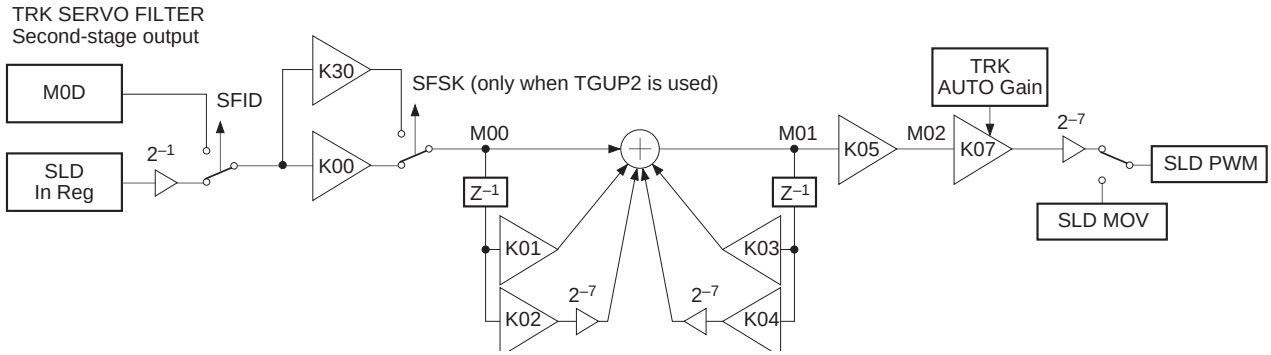


TRK Servo Gain Up 2 fs = 88.2kHz



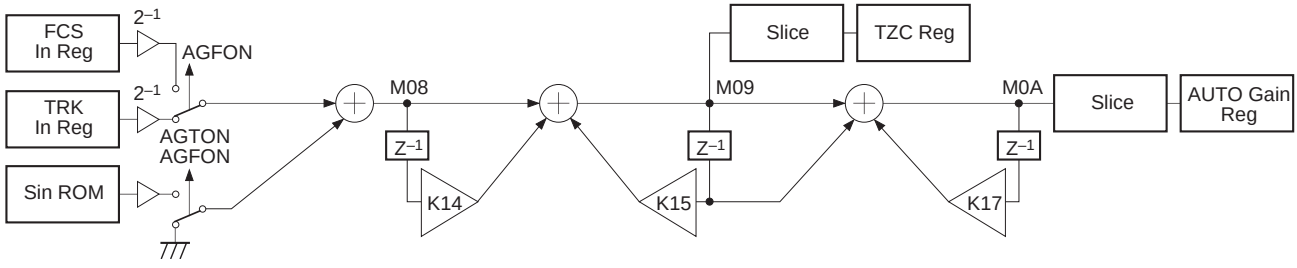
Note) Set the MSB bit of the K39 and K3B coefficients to 0.

SLD Servo fs = 345Hz

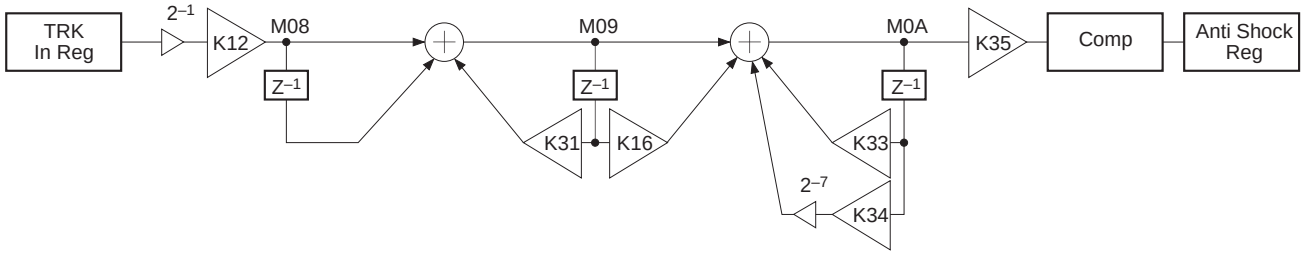


Note) Set the MSB bit of the K02 and K04 coefficients to 0.

HPTZC/Auto Gain fs = 88.2kHz

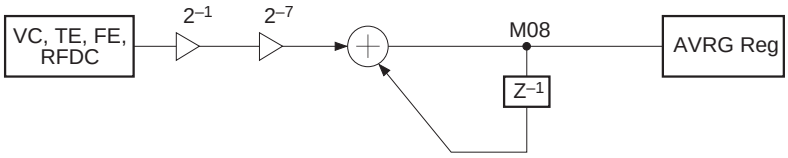


Anti Shock fs = 88.2kHz

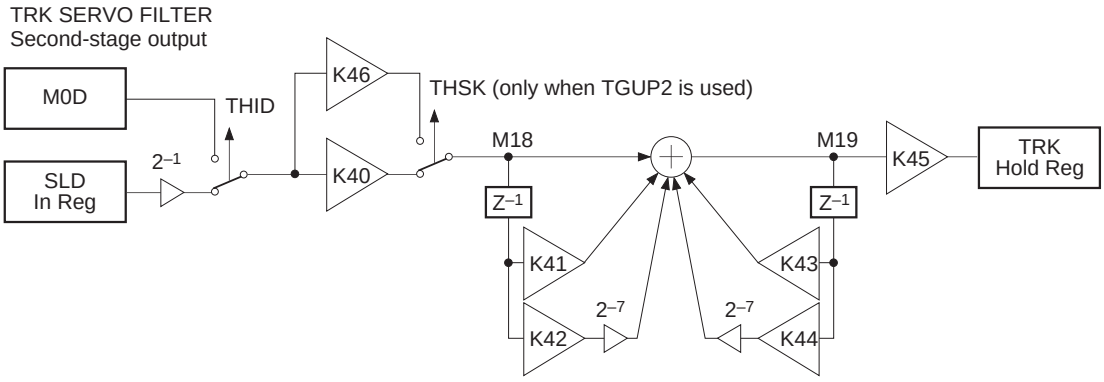


Note) Set the MSB bit of the K34 coefficient to 0.
The comparator input is 1/16 the maximum amplitude of the comparator input.

AVRG fs = 88.2kHz

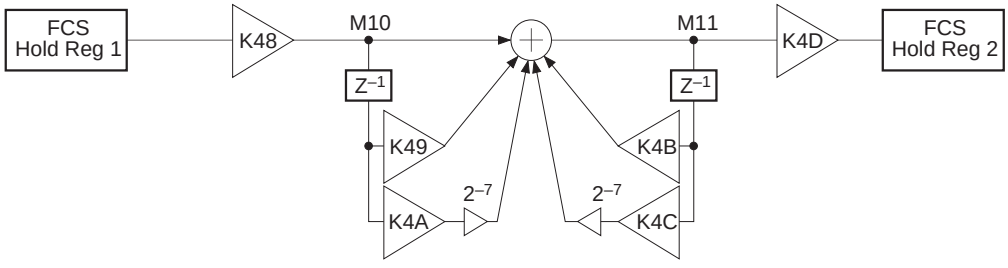


TRK Hold fs = 345Hz



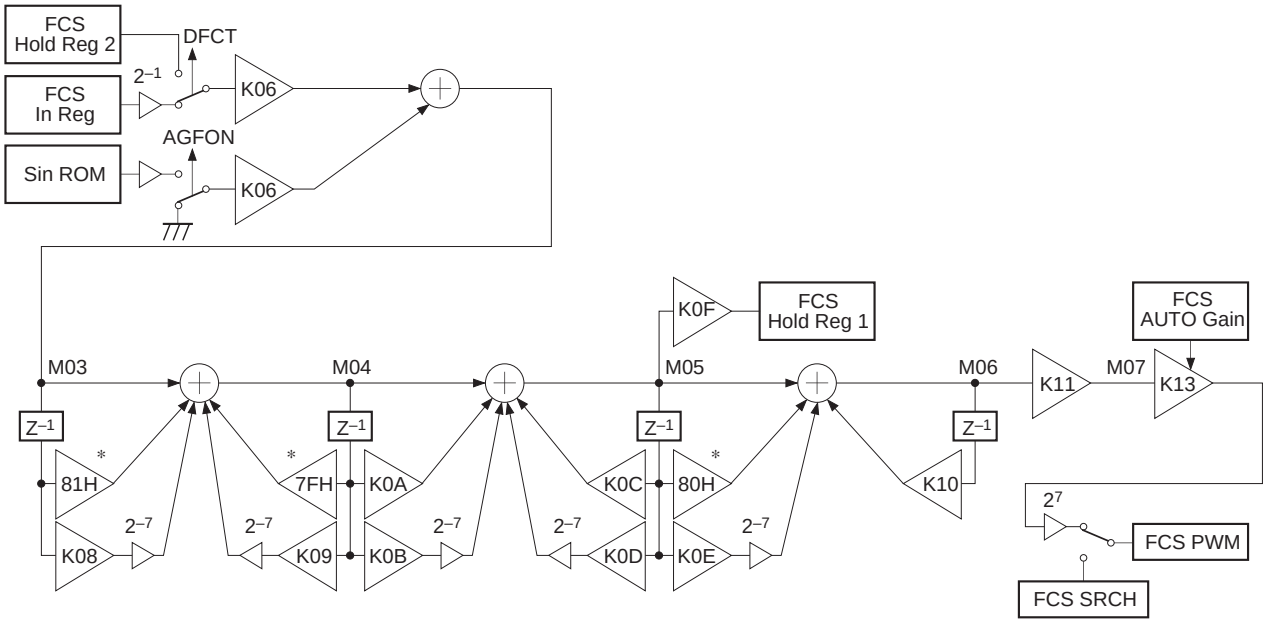
Note) Set the MSB bit of the K42 and K44 coefficients to 0.

FCS Hold fs = 345Hz



Note) Set the MSB bit of the K4A and K4C coefficients to 0.

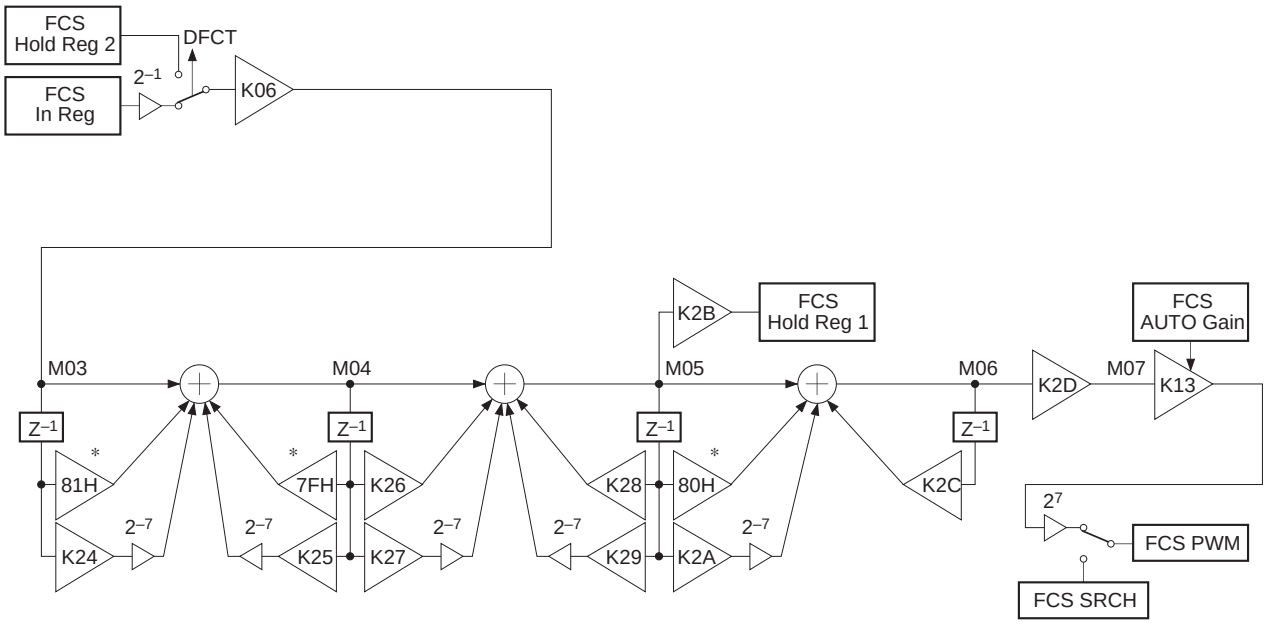
FCS Servo Gain Normal; Fs = 88.2kHz, during quasi double accuracy (Ex.: $3EAXX0)



* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K0B and K0D coefficients during normal operation, and of the K08, K09 and K0E coefficients during quasi double accuracy to 0.

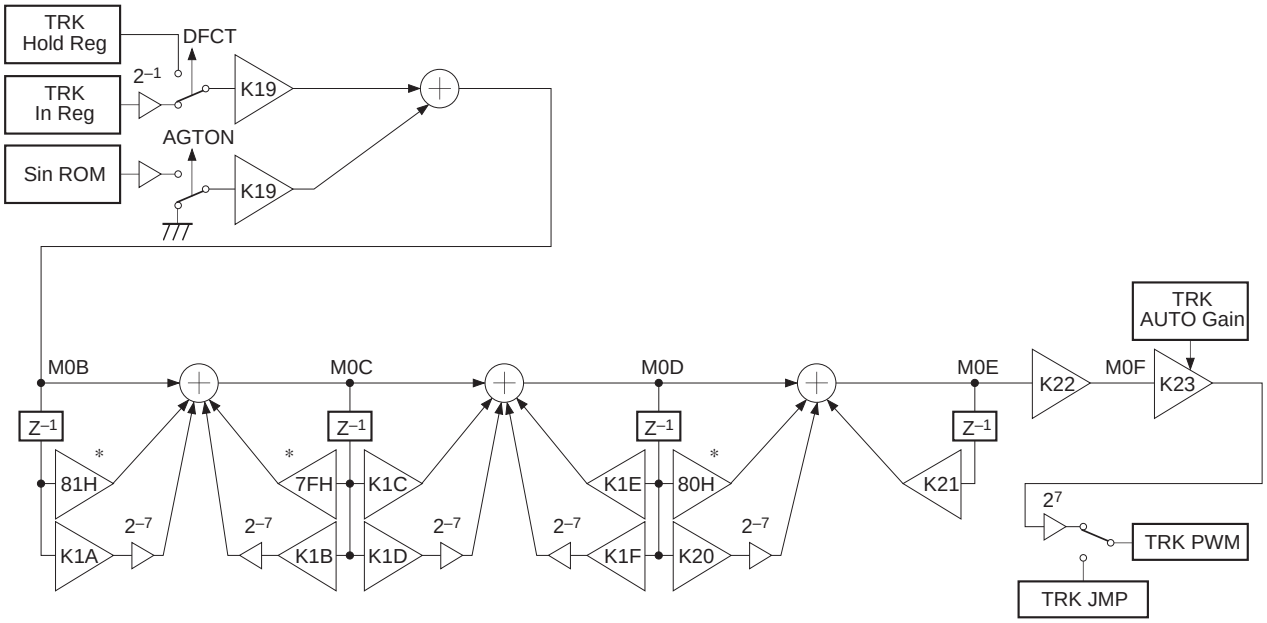
FCS Servo Gain Down; Fs = 88.2kHz, during quasi double accuracy (Ex.: $3E5XX0)



* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K27 and K29 coefficients during normal operation, and of the K24, K25 and K2A coefficients during quasi double accuracy to 0.

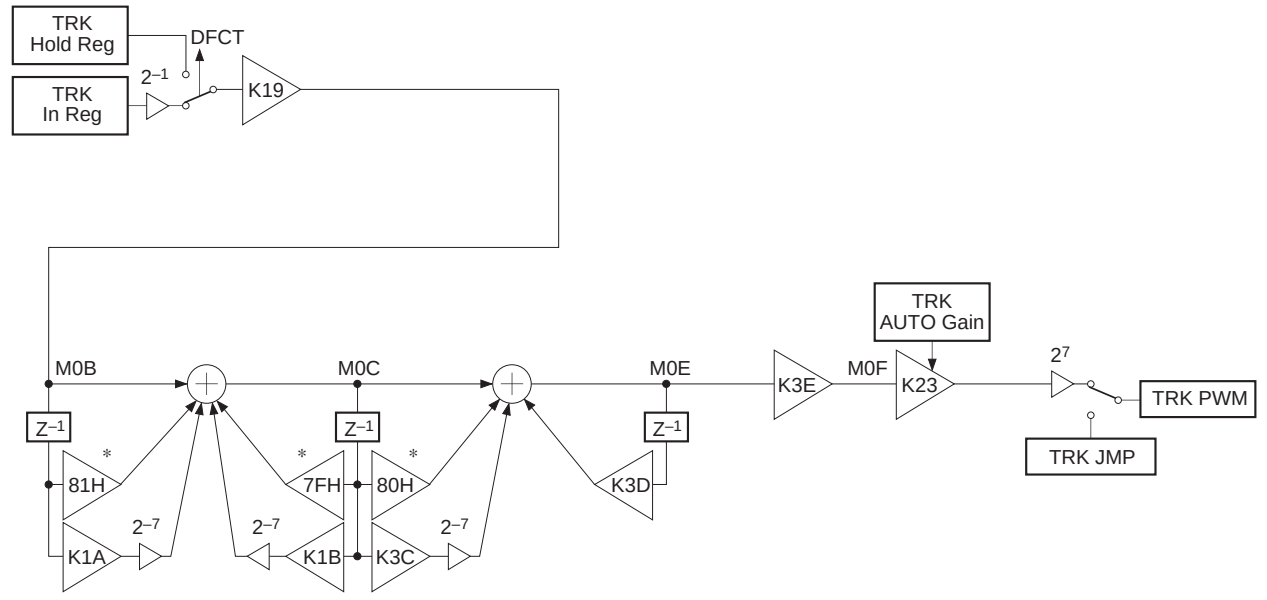
TRK Servo Gain Normal; Fs = 88.2kHz, during quasi double accuracy (Ex.: $3EXAX0)



* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K1D and K1F coefficients during normal operation, and of the K1A, K1B and K20 coefficients during quasi double accuracy to 0.

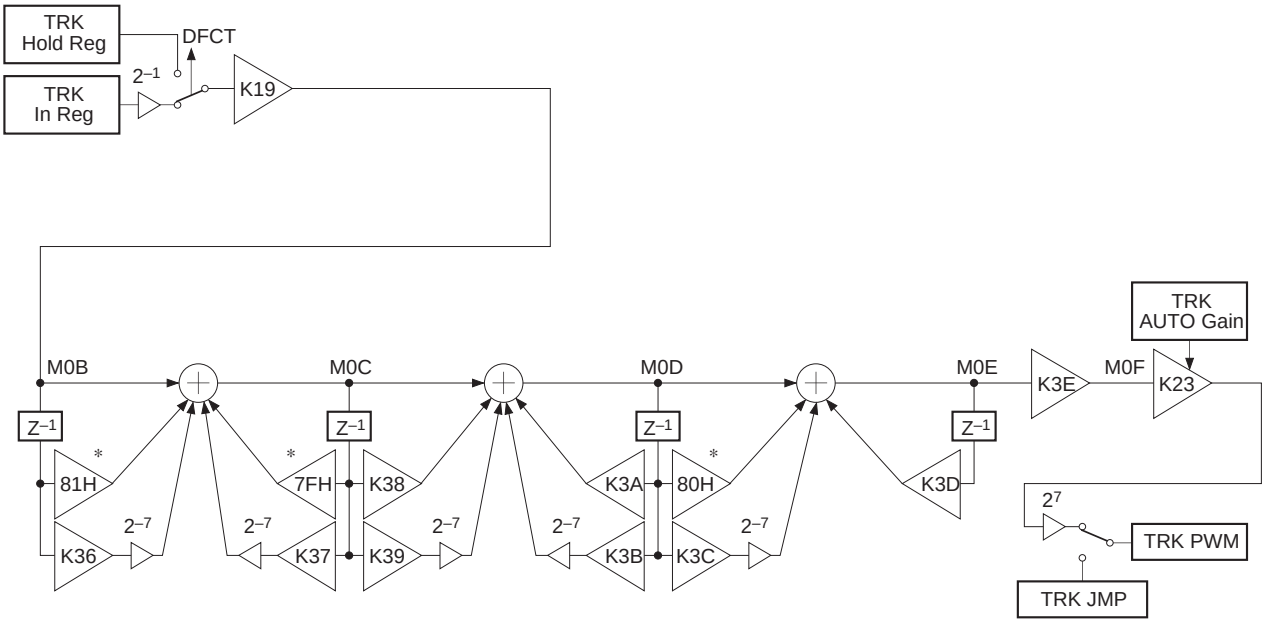
TRK Servo Gain up 1; Fs = 88.2kHz, during quasi double accuracy (Ex.: $3EX5X0)



* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K1A, K1B and K3C coefficients during quasi double accuracy to 0.

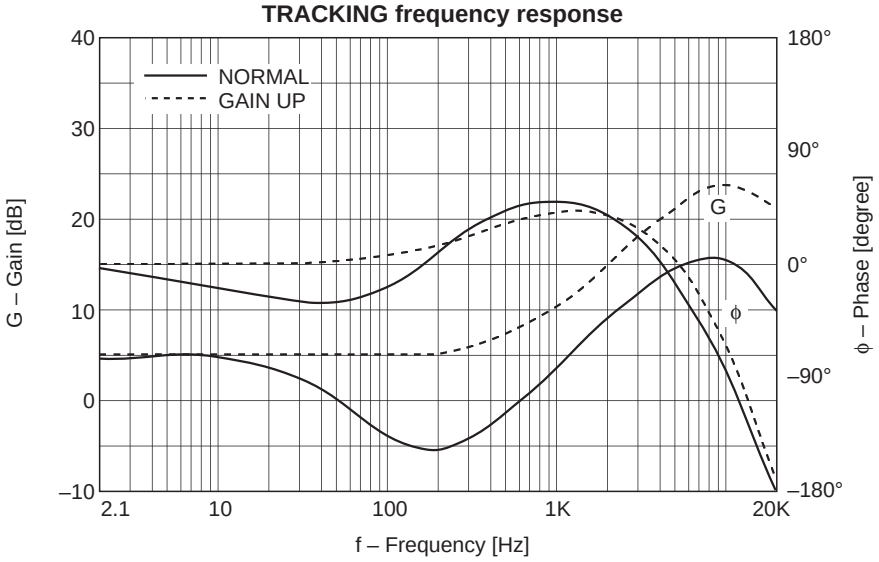
TRK Servo Gain up 2; Fs = 88.2kHz, during quasi double accuracy (Ex.: $3EX5X0)

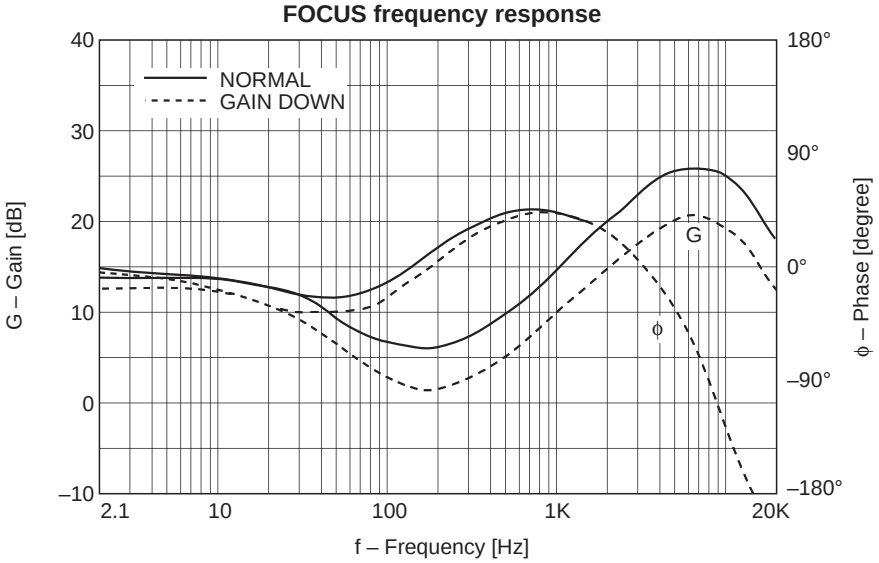


* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

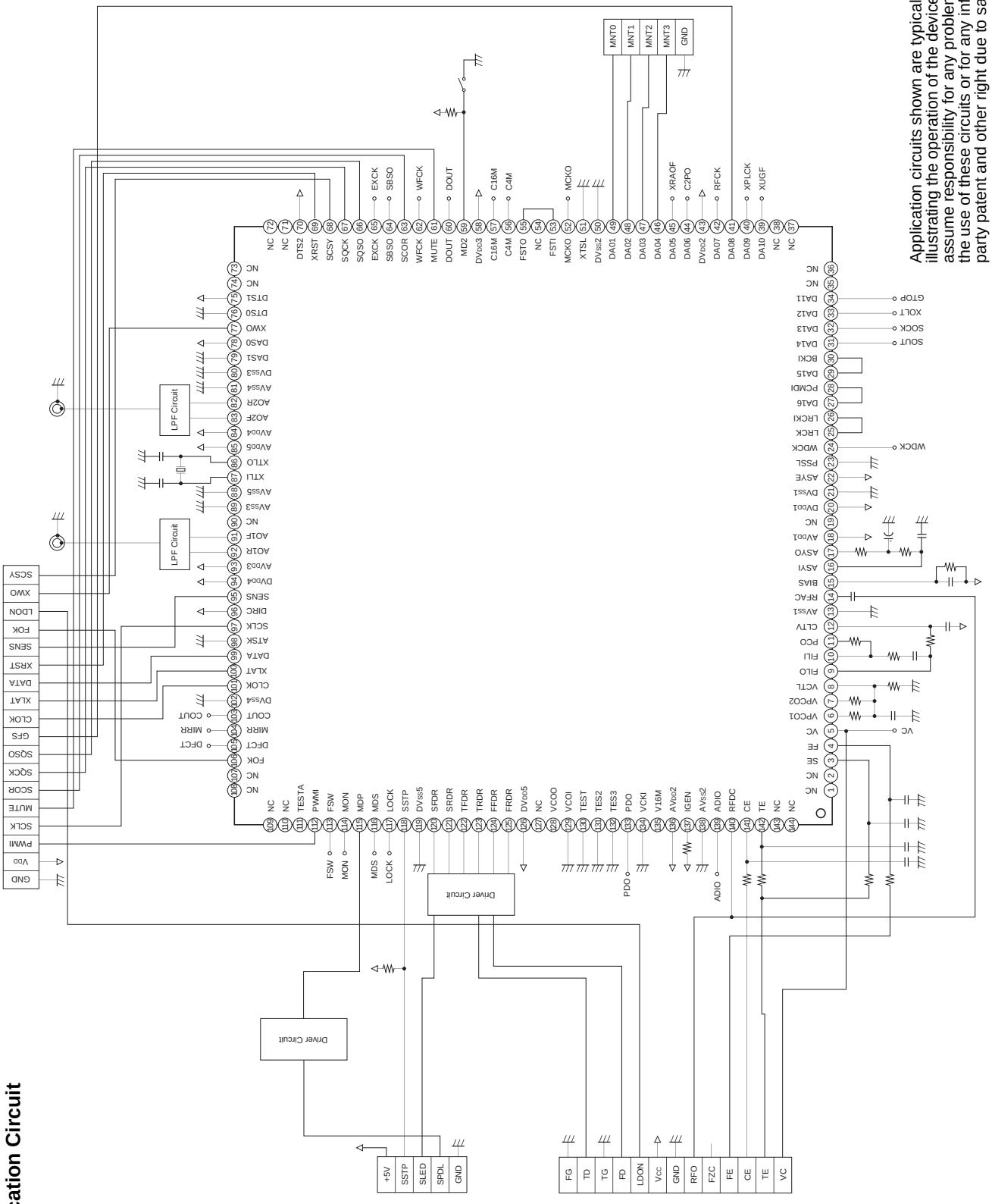
Note) Set the MSB bit of the K39 and K3B coefficients during normal operation, and of the K36, K37 and K3C coefficients during quasi double accuracy to 0.

§5-22. TRACKING and FOCUS Frequency Response



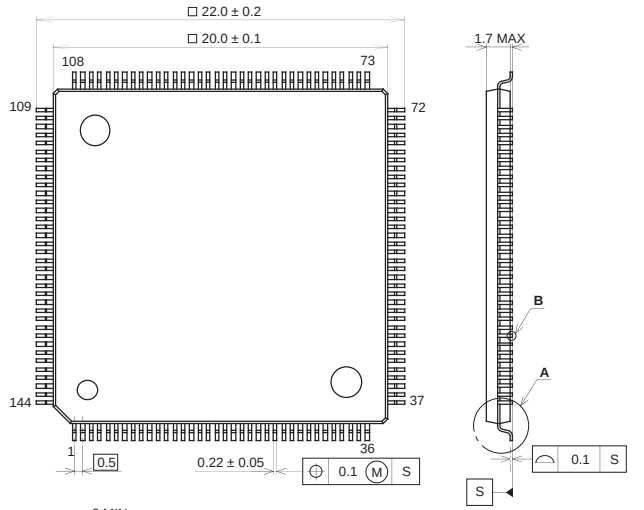


[6] Application Circuit



Package Outline Unit: mm

144PIN LQFP (PLASTIC)

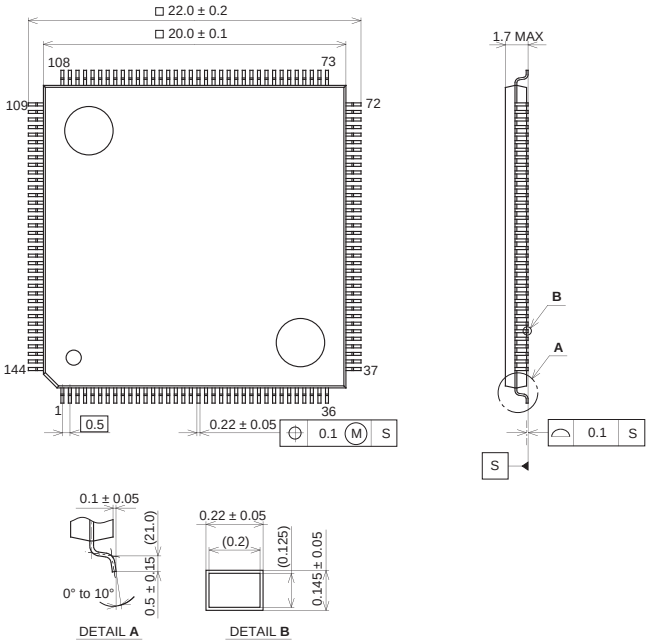


SONY CODE	LQFP-144P-L01
EIAJ CODE	LQFP144-P-2020-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.3 g

144PIN LQFP(PLASTIC)



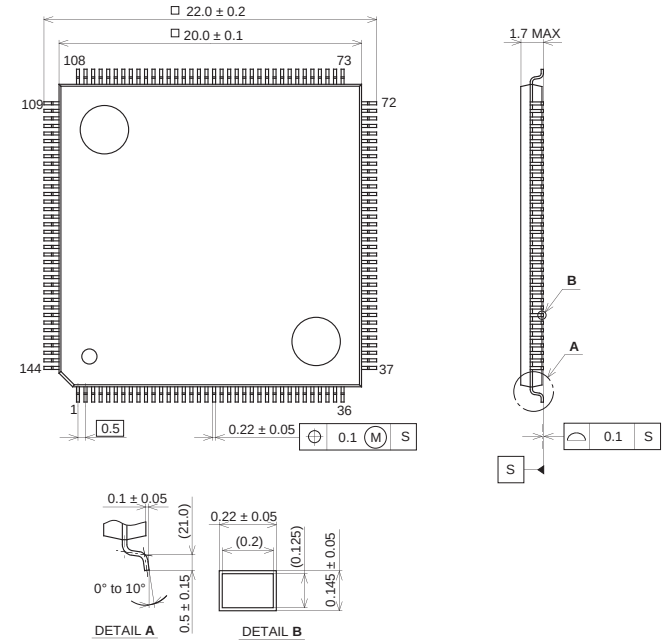
SONY CODE	LQFP-144P-L021
EIAJ CODE	LQFP144-P-2020
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.3g

Package Outline Unit: mm

144PIN LQFP(PLASTIC)

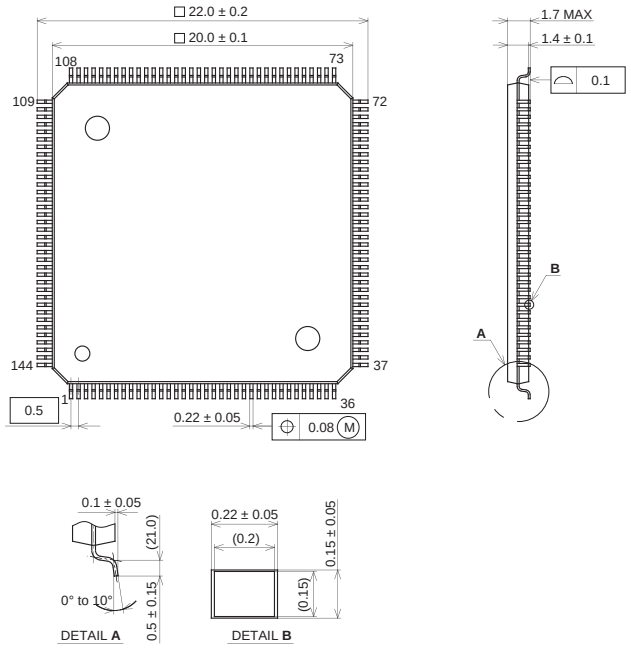


PACKAGE STRUCTURE

SONY CODE	LQFP-144P-L022
EIAJ CODE	LQFP144-P-2020
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	1.3g

144PIN LQFP(PLASTIC)



PACKAGE STRUCTURE

SONY CODE	LQFP-144P-L051
EIAJ CODE	LQFP144-P-2020
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.3g