Triple Phase and Sinx/x Equalized, Low-Pass Video Filter

GENERAL DESCRIPTION

The ML6421 monolithic BiCMOS 6th-order filter provides fixed frequency low pass filtering for video applications. This triple phase-equalized filter with Sinx/x correction is designed for reconstruction filtering at the output of a Video DAC.

Cut-off frequencies are either 5.5, 8.0, or 3.0MHz. Each channel incorporates a 6th-order lowpass filter, a first order all-pass filter, a gain boost circuit, and a 75Ω coax cable driver. A control pin (Range) is provided to allow the inputs to swing from 0 to 1V, or 0.5 to 1.5V, by providing a 0.5V offset to the input.

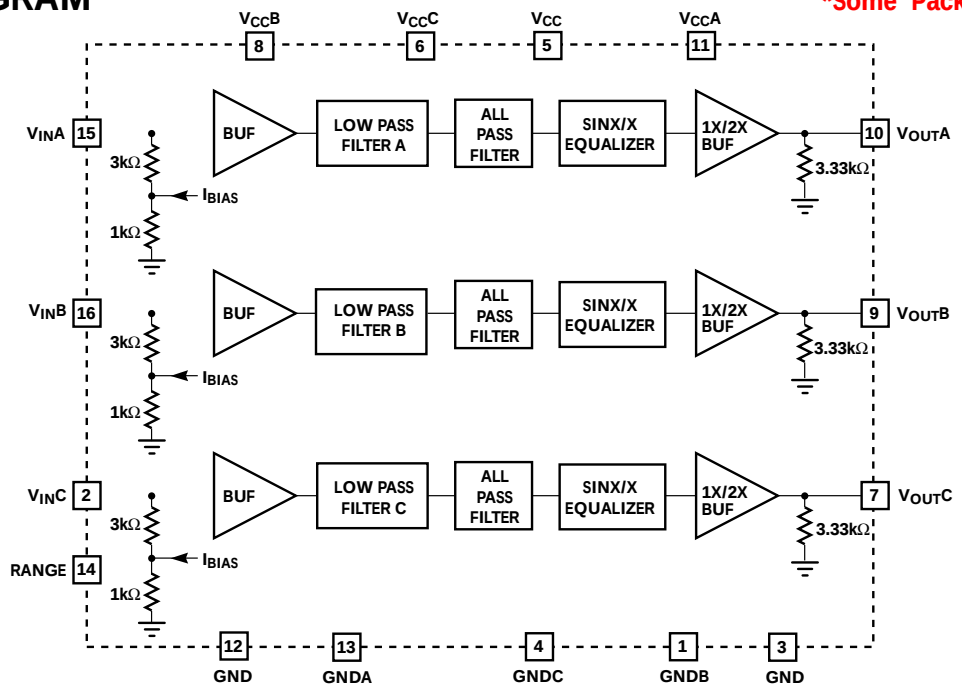
The unity gain filters are powered from a single 5V supply, and can drive $1V_{P-P}$ over 75Ω (0.5V to 1.5V), or $2V_{P-P}$ over 150Ω (0.5V to 2.5V) with the internal coax drivers.

FEATURES

- 5.5, 8.0, 9.3, or 3.0MHz bandwidth
- 1x or 2x gain
- 6th-order filter with phase and amplitude equalizer
- >40dB stopband rejection
- No external components or clocks
- ±10% frequency accuracy over maximum supply and temperature variation
- <2% differential gain <2° differential phase
- <25ns group delay variation
- Drives $1V_{P-P}$ into 75Ω, or $2V_{P-P}$ into 150Ω
- 5V ±10% operation

BLOCK DIAGRAM

*Some Packages Are Obsolete

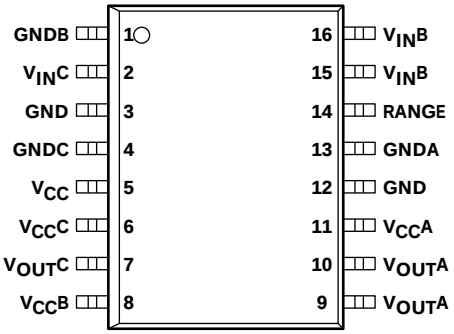


	1x GAIN			2x GAIN	
	ML6221-1	ML6421-3	ML6421-4	ML6421-5	ML6421-7
FilterA	5.5MHz	8.0MHz	8.0MHz	5.5MHz	9.3MHz
Filter B	5.5MHz	8.0MHz	3.0MHz	5.5MHz	9.3MHz
Filter C	5.5MHz	8.0MHz	3.0MHz	5.5MHz	9.3MHz

Triple Input/Anti-aliasing Video Filter

PIN CONFIGURATION

ML6421
16-Pin Wide SOIC (S16W)



TOP VIEW

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	GNDB	Ground pin for filter B.
2	$V_{IN}C$	Signal input to filter C. Input impedance is 4kΩ.
3	GND	Power and logic ground.
4	GNDC	Ground pin for filter C.
5	V_{CC}	Positive supply.
6	$V_{CC}C$	Power supply for filter C.
7	$V_{OUT}C$	Output of filter C. Drive is $1V_{P-P}$ into 75Ω (0.5V to 1.5V), or $2V_{P-P}$ into 150Ω (0.5V to 2.5V).
8	$V_{CC}B$	Power supply for filter B: 4.5V to 5.5V.
9	$V_{OUT}B$	Output of filter B. Drive is $1V_{P-P}$ into 75Ω (0.5V to 1.5V), or $2V_{P-P}$ into 150Ω (0.5V to 2.5V).
10	$V_{OUT}A$	Output of filter A. Drive is $1V_{P-P}$ into 75Ω (0.5V to 1.5V), or $2V_{P-P}$ into 150Ω (0.5V to 2.5V).
11	$V_{CC}A$	Power supply for filter A.
12	GND	Power and logic ground.
13	GNDA	Ground pin for filter A.
14	RANGE	Input signal range select. For –1 to –4; when RANGE is low (0), the input signal range is 0.5V to 2.5V, with an output range of 0.5V to 2.5V. When RANGE is high (1), the input signal range is 0V to 2V, with an output range of 0.5V to 2.5V. For –5 to –7; when RANGE is low (0), the input signal range is 0.5V to 1.5V, with an output range of 0.5V to 2.5V. When RANGE is high (1), the input signal range is 0V to 1V, with an output range of 0.5V to 2.5V.
15	$V_{IN}A$	Signal input to filter A. Input impedance is 4kΩ.
16	$V_{IN}B$	Signal input to filter B. Input impedance is 4kΩ.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (V_{CC}) ..... –5.5MHz0.3 to +7V
GND ..... –0.3 to V_{CC} +0.3V
Logic Inputs ..... –0.3 to V_{CC} +0.3V
Input Current per Pin ..... ±25mA
Storage Temperature ..... –65° to 150°C

Package Dissipation at T_A = 25°C 1W
Lead Temperature (Soldering 10 sec) ..... 260°C
Thermal Resistance (θ_{JA}) ..... 65°C/W

OPERATING CONDITIONS

TSupply Voltage ..... 5V ± 10%
Temperature Range ..... 0°C < to < 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified V_{CC} = 5V ± 10% and $T_A = T_{MIN}$ to T_{MAX}, R_L =75Ω or 150Ω, $V_{OUT} = 2V_{P-P}$ for 150Ω Load and $V_{OUT} = 1V_{P-P}$ for 75Ω Load (Note 1)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL							
R_{IN}	Input Impedance			3	4	5	kΩ
DR/R_{IN}	Input R Matching					±2	%
I_{BIAS}	Input Current	V_{IN} = 0.5V,	ML6421(–1 to –4)		–80		µA
		range = low	ML6421(–5 to –7)		45		µA
		V_{IN} = 0.0V,	ML6421(–1 to –4)		–125		µA
		range = high	ML6421(–5 to –7)		–210		µA
	Small Signal Gain	V_{IN} = 100mV_{P-P}	ML6421(–1 to –4)	–0.5	0	0.5	dB
		at 100kHz	ML6421(–5 to –7)	5.5	6	6.5	dB
	Differential Gain	V_{IN} = 1.1V to 2.5V at 3.58 & 4.43 MHz	ML6421(–1 to –4)		1		%
		V_{IN} = 0.8V to 1.5V at 3.58 & 4.43 MHz	ML6421(–5 to –7)		1		%
	Differential Phase	V_{IN} = 1.1V to 2.5V at 3.58 & 4.43 MHz	ML6421(–1 to –4)		1		deg
		V_{IN} = 0.8V to 1.5V at 3.58 & 4.43 MHz	ML6421(–5 to –7)		1		deg
V_{IN}	Input Range	Range = 0	ML6421(–1 to –4)	0.5	2.5	V	
			ML6421(–5 to –7)	0.5		1.5	V
		Range = 1	ML6421(–1 to –4)	0.0		2.0	V
		ML6421(-5 to -8)		0.0		1	V
	Peak Overshoot	2T, 0.7V_{P-P} pulse		2.0		%	
	Crosstalk Rejection	f_{IN} = 3.58,	ML6421(–1 to –4)	50			dB
		f_{IN} = 4.43MHz (Note 6)	ML6421(–5 to –7)	45			dB
	Channel to Channel Group Delay Matching (f_C = 5.5MHz)	f_{IN} = 100kHz			±10		ns
	Channel to Channel Group Matching	f_{IN} = 100kHz			±2		%

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL (Continued)							
	Output Current	RL = 0 (short circuit)			175		mA
C_L	Load Capacitance					35	pF
	Composite Chroma	f_C = 5.5MHz	ML6421(–1 to –4)		±15		ns
	/Luma delay		ML6421(–5 to –7)		±15		ns
		f_C = 8.0MHz/9.3MHz			±8		ns
5.50MHZ FILTER (ML6421-1, -5)							
	Bandwidth	–0.75dB (Note 5)	ML6421(–1 to –4)	4.95	5.50	6.05	MHz
	(monotonic passband)	–0.55dB (Note 5)	ML6421(–5 to –7)	4.95	5.50	6.05	MHz
	Subcarrier Frequency Gain	f_{IN} = 3.58MHz	ML6421(–1 to –4)	–0.3	0.2	0.7	dB
	ML6421-1		ML6421(–5 to –7)	–0.9	1.4	1.9	dB
		f_{IN} = 4.43MHz	ML6421(–1 to –4)	–0.35	0.1	0.65	dB
			ML6421(–5 to –7)	1.1	1.6	2.1	dB
	Attenuation	f_{IN} = 10MHz	ML6421(–1 to –4)	16	18		dB
			ML6421(–5 to –7)	20	25		dB
		f_{IN} = 50MHz		40	45		dB
	Output Noise	BW = 30MHz (Note 6)				1000	μV_{RMS}
	Group Delay				145		ns
8.0MHZ FILTER							
	Bandwidth (monotonic passband)	–3dB (Note 5)		7.2	8	8.8	MHz
	Subcarrier Frequency Gain	f_{IN} = 3.58MHz		–0.25	0.25	0.75	dB
	ML6421-3 or ML6421 4/ML6421-7	f_{IN} = 4.43MHz		–0.11	0.39	0.89	dB
	Attenuation	f_{IN} = 17MHz		20	25		dB
		f_{IN} = 85MHz		40	42		dB
	Output Noise	BW = 30MHz (Note 6)				1000	μV_{RMS}
	Group Delay				120		ns
9.3MHZ FILTER							
	Bandwidth (monotonic passband)	–2dB (Note 5)		8.4	9.3	10.2	MHz
	Subcarrier Frequency Gain	f_{IN} = 3.58MHz		–0.01	0.4	0.9	dB
	ML6421-3 or ML6421 4/ML6421-7	f_{IN} = 4.43MHz		–0.1	0.6	1.1	dB
	Attenuation	f_{IN} = 17MHz		20	25		dB
		f_{IN} = 85MHz		40	42		dB
	Output Noise	BW = 30MHz (Note 6)				1000	μV_{RMS}
	Group Delay				120		ns

ELECTRICAL CHARACTERISTICS (CONTINUED)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
3.0MHZ FILTER						
	Bandwidth (monotonic passband)	–2.5dB (Note 5)	2.7	3	3.3	MHz
	Attenuation	f_{IN} = 9.82MHz	30	33		dB
		f_{IN} = 60MHz	43	50		dB
	Output Noise	BW = 30MHz (Note 6)			700	μV_{RMS}
	Bandwidth (monotonic passband)	–2dB (Note 5)	3	3.3	3.6	MHz
	Attenuation	f_{IN} = 9.82MHz	30	33		dB
	f_{IN} = 60MHz		43	50		dB
	Output Noise	BW = 30MHz (Note 6)			700	μV_{RMS}
DIGITAL AND DC						
V_{IL}	Logic Input Low	Range			0.8	V
V_{IH}	Logic Input High	Range	V_{CC} – 0.8			V
I_{IL}	Logic Input Low	V_{IN} = GND	–1			µA
I_{IH}	Logic Input High	V_{IN} = V_{CC}			1	µA
I_{CC}	Supply Current	V_{IN} = 0.5V (Note 4)		110	135	mA
	R_L = 75Ω	V_{IN} = 1.5V		140	175	mA

Note 1: Limits are guaranteed by 100% testing, sampling or correlation with worst case test conditions.

Note 2: Maximum resistance on the outputs is 500Ω in order to improve step response.

Note 3: Connect all ground pins to the ground plane via the shortest path.

Note 4: Power dissipation: $P_D = (I_{CC} \times V_{CC}) - [3(V_{OUT}^2/RL)]$

Note 5: The bandwidth is the –3dB frequency of the unboosted filter. This represents the attenuation that results from boosting the gain from the –3dB point at the specified frequency.

Note 6: These parameters are guaranteed by characterization only.

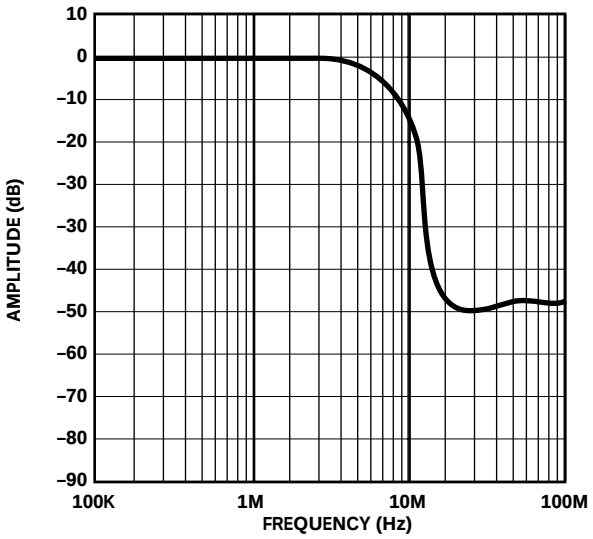


Figure 1. Stop-Band Amplitude vs Frequency (f_C = 5.5MHz).

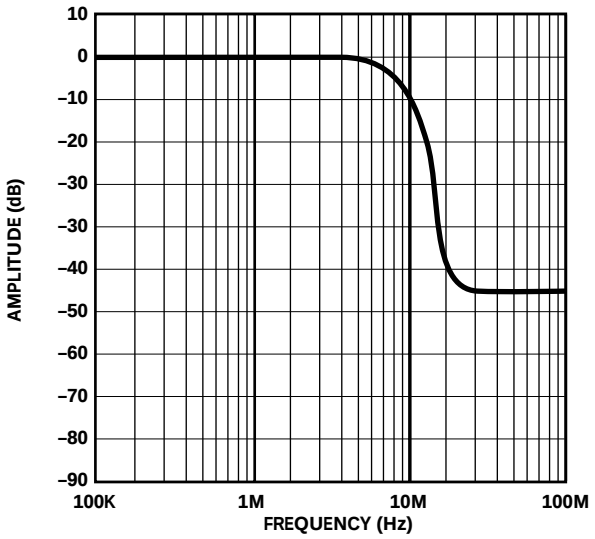


Figure 2. Stop-Band Amplitude vs Frequency (f_C = 8.0MHz).

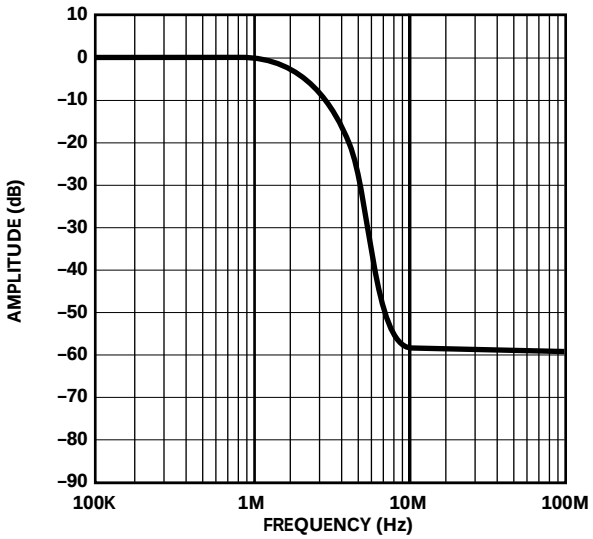


Figure 3. Stop-Band Amplitude vs Frequency (f_C = 3.0MHz).

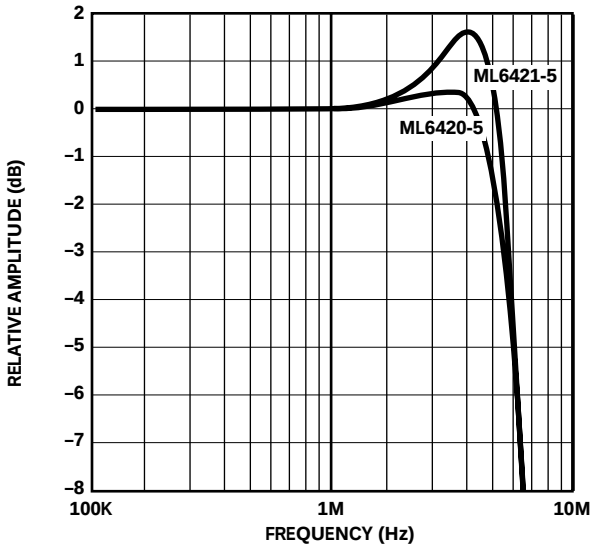


Figure 4. Pass-Band Amplitude vs Frequency (f_C = 5.5MHz).

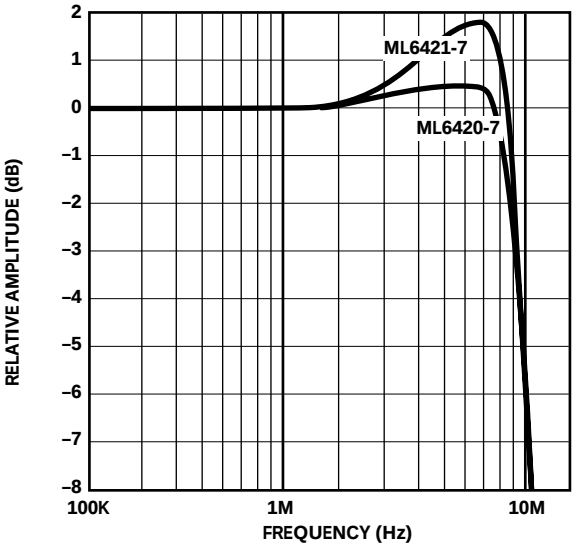


Figure 5. Pass-Band Amplitude vs Frequency (f_C = 9.3MHz).

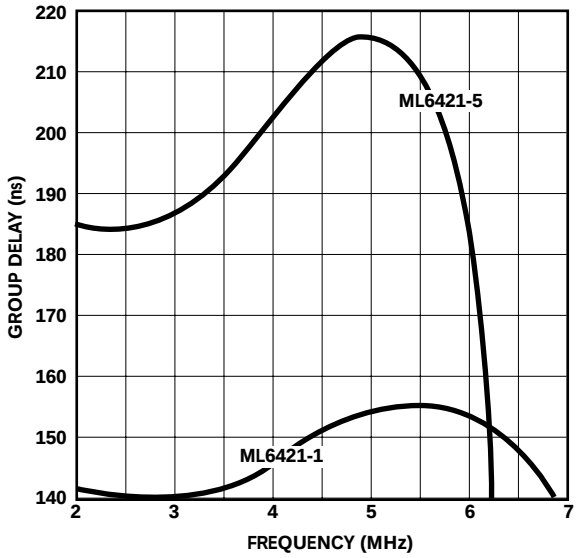


Figure 6. Group Delay vs Frequency (f_C = 5.5MHz).

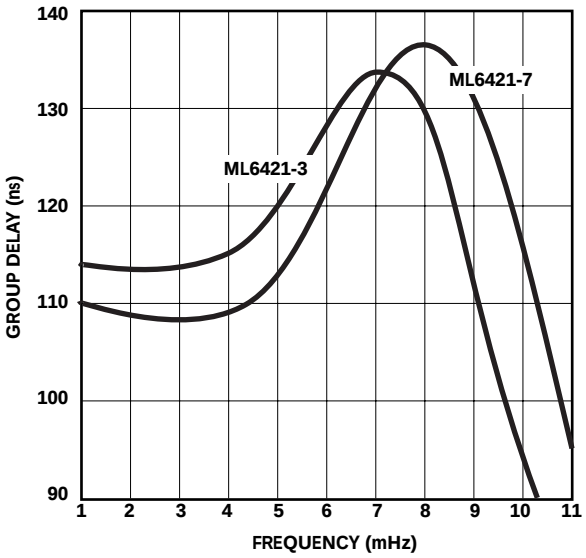


Figure 7. Group Delay vs Frequency (f_C = 8.0MHz).

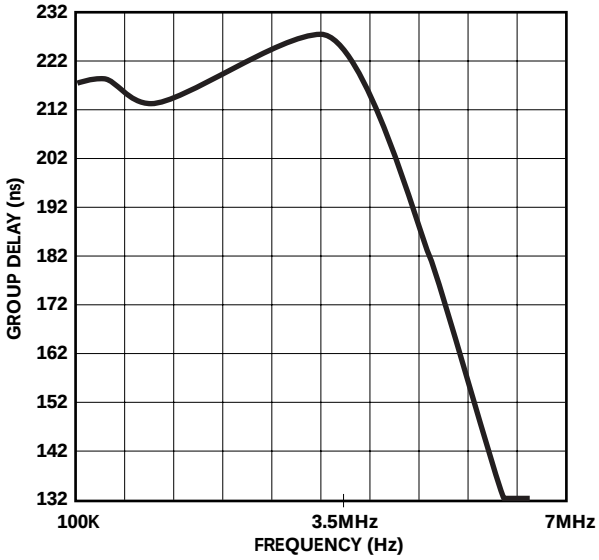


Figure 8. Group Delay vs Frequency (f_C = 3.0MHz).

FUNCTIONAL DESCRIPTION

The ML6421 single-chip Triple Video Filter IC is intended for consumer and low cost professional video applications. Each of the three channels incorporates an input buffer amplifier, a sixth order lowpass filter, a first order allpass equalizer, Sinx/x equalizer and an output amplifier capable of driving 75Ω to ground.

The ML6421 can be driven by a DAC with Range down to 0V. When Range is low the input and output signal range is 0.5V to 2.5V. When the input signal includes 0V, Range should be tied high. In this case, an offset is added to the input so that the output swing is kept between 0.5V to 2.5V. The output amplifier is capable of driving up to 24mA of peak current; therefore the output voltage should not exceed 1.8V when driving 75Ω to ground.

APPLICATION GUIDELINES

OUTPUT CONSIDERATIONS

The triple filters have unity gain. The circuit has unity gain (0dB) when connected to a 150Ω load, and a –6dB gain when driving a 75Ω load via a 75Ω series output resistor. The output may be either AC or DC coupled. For AC coupling, the –3dB point should be 5Hz or less. There must also be a DC path of -500Ω to ground for output biasing.

INPUT CONSIDERATIONS

The input resistance is 4kΩ. The input may be either DC or AC coupled. (Note that each input sources 80 to 125µA of bias current). The ML6421 is designed to be directly driven by a DAC. For current output video DACs, a 75Ω or 150Ω resistor to ground may need to be added to the DAC output (filter input).

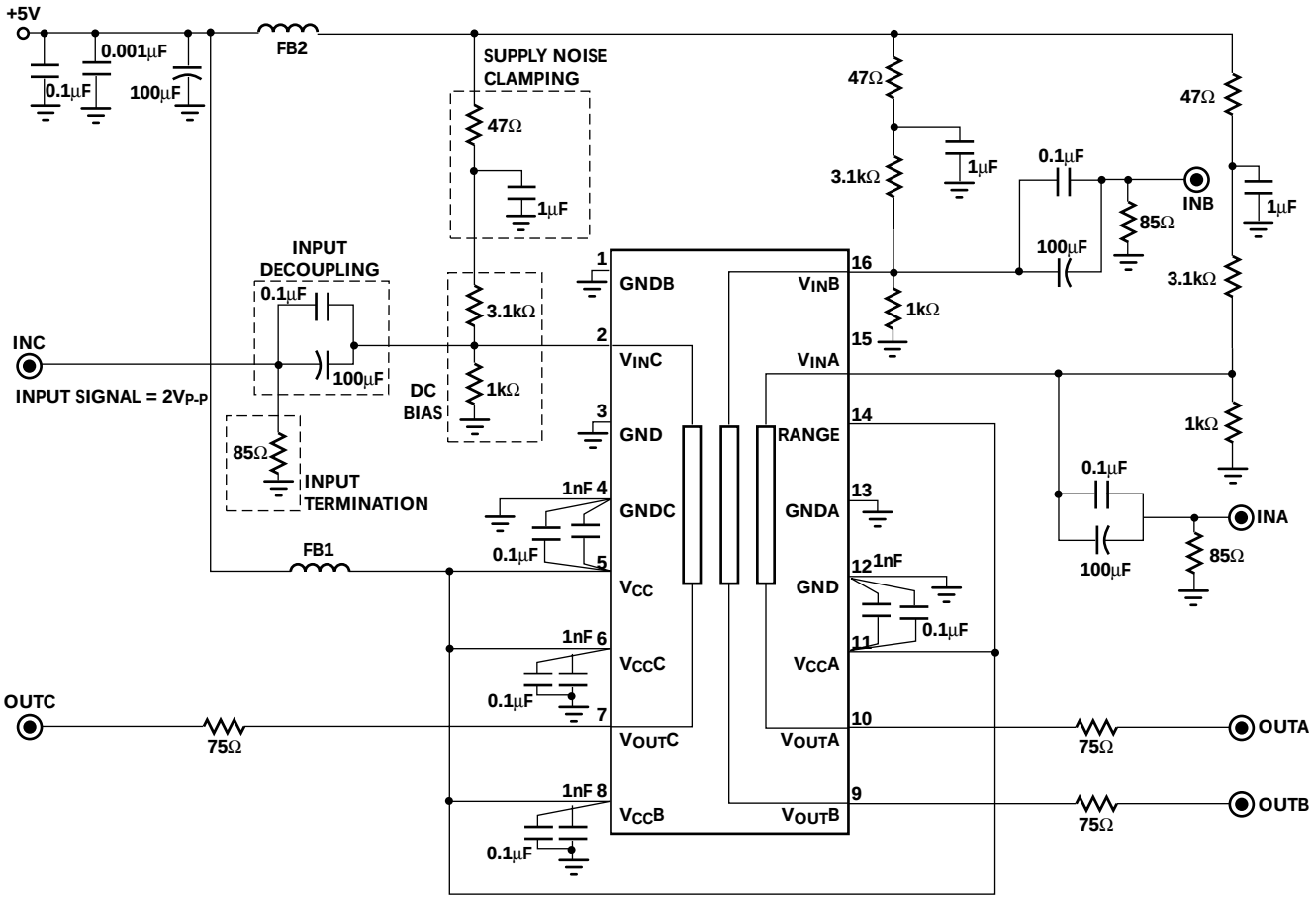


Figure 9. ML6421 AC Coupled DC Bias Test Circuit

LAYOUT CONSIDERATIONS

In order to obtain full performance from these triple filters, layout is very important. Good high frequency decoupling is required between each power supply and ground. Otherwise, oscillations and/or excessive crosstalk may occur. A ground plane is recommended.

Each filter has its own supply and ground pins. In the test circuit, 0.1µF capacitors are connected in parallel with 1nF capacitors on V_{CC}, $V_{CC}C$, $V_{CC}B$ and $V_{CC}A$ for maximum noise rejection (Figure 9).

Further noise reduction is achieved by using series ferrite beads. In typical applications, this degree of bypassing may not be necessary.

Since there are three filters in one package, space the signal leads away from each other as much as possible.

Power Considerations

The ML6421 power dissipation follows the formula:

$$P_D = (I_{CC} \times V_{CC}) - \left[\left(\frac{V_{OUT}{}^2}{RL} \times 3\right)\right] \quad (1)$$

This is a measure of the amount of current the part sinks (current in – current out to the load).

Under worst case conditions:

$$P_D = (0.175 \times 5.5) - \left[\left(\frac{15^2}{75} \times 3\right)\right] = 872.5\text{mW}$$

ML6421 VIDEO LOW PASS FILTER

Filter Selection: The ML6421 provides several choices in filter cut-off frequencies depending on the application.

RGB: When the BW of each signal is the same, then the ML6421-1 (5.5MHz) or ML6421-3 (8MHz) are appropriate depending on the sampling rate.

YUV: When the luminance bandwidth is different from the color bandwidth, the ML6421-4 with the 8.0, and two 3.0MHz filters are most appropriate.

S-Video: For Y/C (S-video) and Y/C + CV (Composite Video) systems the 5.5MHz or 8MHz filters are appropriate. In NTSC the C signal occupies the bandwidth from about 2.6MHz to about 4.6MHz, while in PAL the C signal occupies the bandwidth from about 3.4MHz to about 5.4MHz. In both cases, a 5.5MHz low pass filter provides adequate rejection for both sampling and reconstruction. In addition, using the same filter for both Y/C and CV maintains identical signal timing without adjustments.

Composite: When one or more composite signals need to be filtered, then the 5.5MHz and 8MHz filters permit filtering of one, two or three composite signals.

NTSC/PAL: A 5.5MHz cut-off frequency provides good filtering for 4.2MHz, 5.0MHz and 5.5MHz signals without the need to change filters on a production basis.

Sinx/x: For digital video system with output D/A converters, there is a fall-off in response with frequency

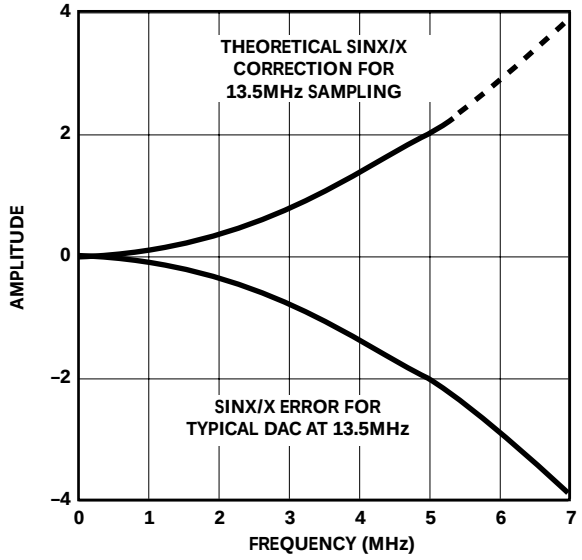


Figure 10. Sinx/x Frequency Response

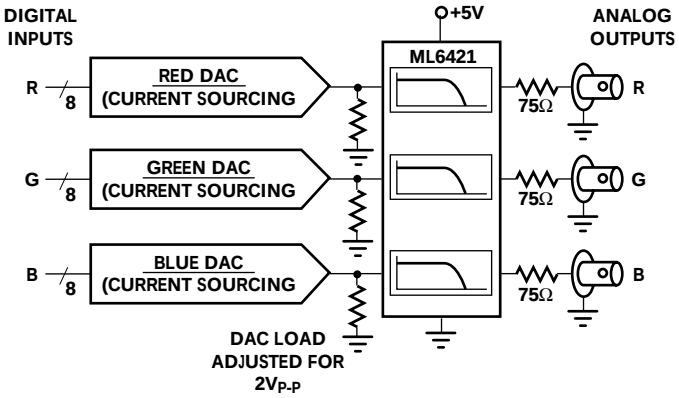


Figure 11. Typical ML6421 Reconstruction Application

ML6421 VIDEO LOW PASS FILTER (CONTINUED

due to discrete sampling. The fall-off follows a sinx/x response. The ML6421 filters have a complementary boost to provide a flatter overall response. The boost is designed for 13.5MHz Y/C and CV sampling and 6.75MHz U/V sampling. Note: The ML6421 has the same pin-out as the ML6420.

In a typical application the ML6421 is used as the final output device in a video processing chain. In this case, inputs to the ML6421 are supplied by DAC outputs with their associated load resistors (typically 75Ω or 150Ω). Resistance values should be adjusted to provide $2V_{P-P}$ at the input of the ML6421.

The ML6421 will drive 75Ω source termination resistors (making the total load 150Ω) so that no external drivers or amplifiers are required.

FILTER PERFORMANCE

The reconstruction performance of a filter is based on its ability to remove the high band spectral artifacts (that result from the sampling process) without distorting the valid signal spectral contents within the passband. For video signals, the effect of these artifacts is a variation of the amplitude of small detail elements in the picture (such as highlights or fine pattern details) as the elements move relative to the sampling clock. The result is similar to the aliasing problem and causes a “winking” of details as they move in the picture.

Figure 12 shows the problem in the frequency domain. Curve A shows the amplitude response of the ML6421 filter, while Curve B shows the signal spectrum as it is distorted by the sampling process. Curve C shows the composite of the two curves which is the result of passing the sampled waveform through the ML6421 filter. It is clear that the distortion artifacts are reduced significantly.

Ultimately it is the time domain signal that is viewed on a TV monitor, so the effect of the reconstruction filter on the time domain signal is important. Figure 13 shows the sampling artifacts in the time domain. Curve A is the original signal, Curve B. is the result of CCIR601 sampling, and Curve C. is the same signal filtered through the ML6421. Again the distortions in the signal are essentially removed by the filter.

In an effort to measure the time domain effectiveness of a reconstruction filter, Figure 14 was generated from a swept frequency waveform. Curves A, B, and C are generated as in Figure 13, but additional curves D and E help quantify the effect of filtering in the time domain. Curve D and Curve E represent the envelopes (instantaneous amplitudes) of Curves B and C. Again it is evident in Curve D that the envelope varies significantly due to the sampling process. In Curve E, filtering with the ML6421 removes these artifacts and generates an analog output signal that rivals the oversampled (and more ideal) signal waveforms. The ML6421 reduces the amplitude variation from over 6% to less than 1%.

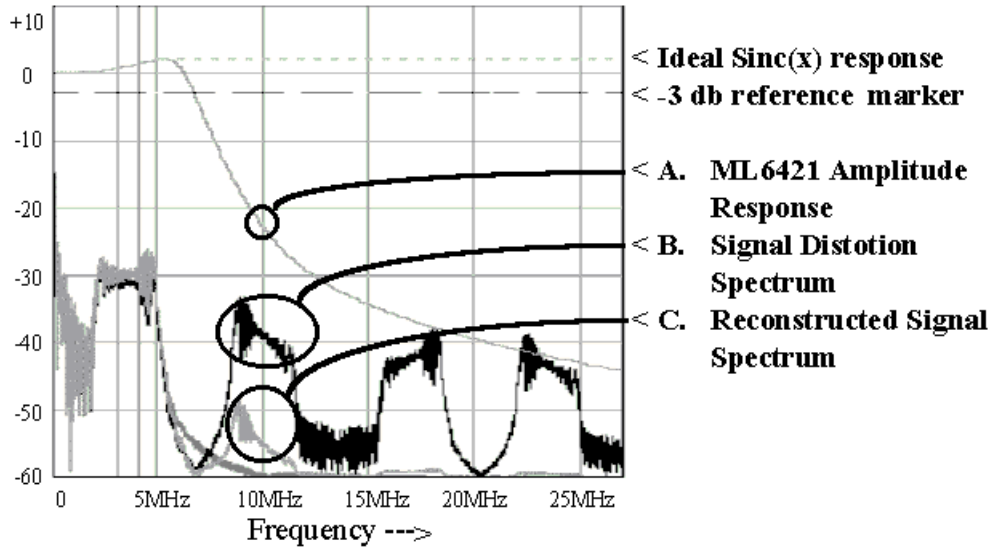


Figure 12. ML6421 Reconstruction Performance in the Frequency Domain

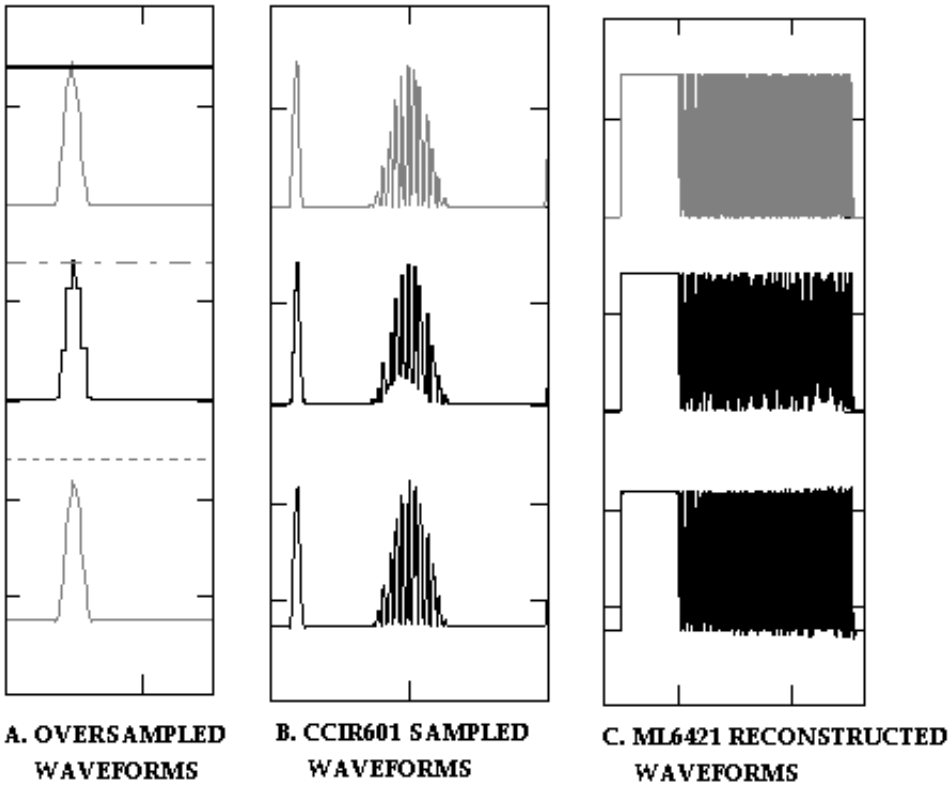


Figure 13. ML6421 Reconstruction Performance in the Time Domain

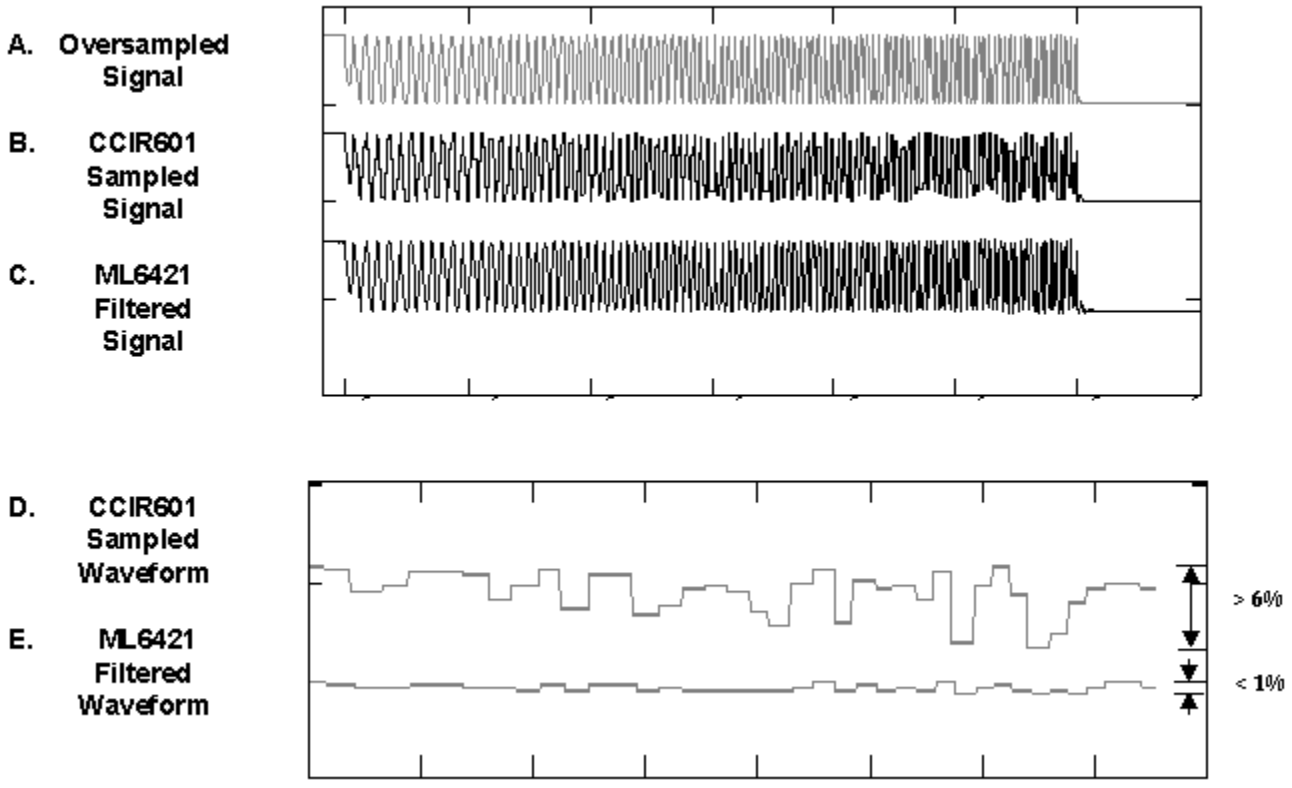
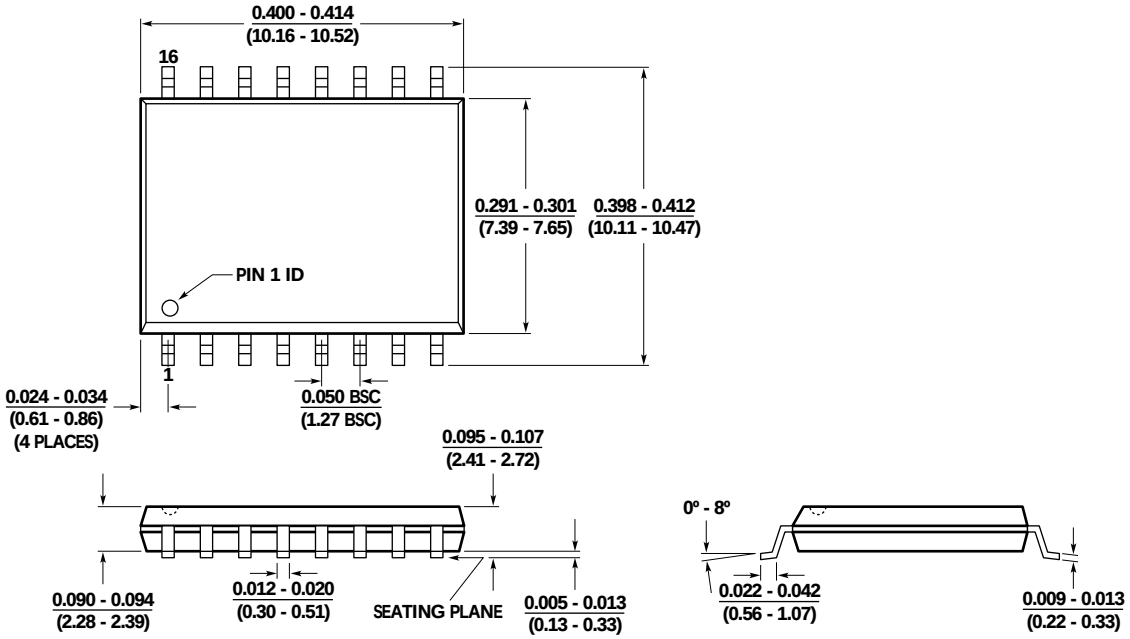


Figure 14. Amplitude Ripple of Reconstructed Swept Pulses

PHYSICAL DIMENSIONS

Package: S16W
16-Pin Wide SOIC



ORDERING INFORMATION

PART NUMBER	BW (MHZ)	GAIN	TEMPERATURE RANGE	PACKAGE
ML6421CS-1	5.5/5.5/5.5	1X	0°C to 70°C	16-pin SOIC wide (S16W)
ML6421CS-3	8.0/8.0/8.0	1X	0°C to 70°C	16-pin SOIC wide (S16W)
ML6421CS-4	8.0/3.0/3.0	1X	0°C to 70°C	16-pin SOIC wide (S16W)(OBS)
ML6421CS-5	5.5/5.5/2.5	2X	0°C to 70°C	16-pin SOIC wide (S16W)
ML6421CS-7	9.3/9.3/9.3	2X	0°C to 70°C	16-pin SOIC wide (S16W)

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Products described herein may be covered by one or more of the following U.S. patents: 4,897,611; 4,964,026; 5,027,116; 5,281,862; 5,283,483; 5,418,502; 5,508,570; 5,510,727; 5,523,940; 5,546,017; 5,559,470; 5,565,761; 5,592,128; 5,594,376; 5,652,479; 5,661,427; 5,663,874; 5,672,959; 5,689,167; 5,714,897; 5,717,798; 5,742,151; 5,747,977; 5,754,012; 5,757,174; 5,767,653; 5,777,514; 5,793,168; 5,798,635; 5,804,950; 5,808,455; 5,811,999; 5,818,207; 5,818,669; 5,825,165; 5,825,223; 5,838,723; 5.844,378; 5,844,941. Japan: 2,598,946; 2,619,299; 2,704,176; 2,821,714. Other patents are pending.

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