

## TLV902x and TLV903x High-Precision Dual and Quad Comparators

### 1 Features

- 1.65 V to 5.5 V supply range
- Precision input offset voltage 300  $\mu$ V
- Power-On Reset (POR) for known start-up
- Rail-to-Rail input with fault-tolerance
- 100ns Typ propagation delay
- Low quiescent current 16  $\mu$ A per channel
- Low input bias current 5 pA
- Open-drain output option (TLV902x)
- Push-pull output option (TLV903x)
- Full -40°C to +125°C temp range
- 2 kV ESD protection

### 2 Applications

- [Appliances](#)
- [Building automation](#)
- [Factory automation & control](#)
- [Motor drives](#)
- [Infotainment & cluster](#)

### 3 Description

The TLV902x and TLV903x are a family of dual and quad channel comparators. The family offers low input offset voltage, integrated Power-On Reset (POR) circuitry, and fault-tolerant inputs with an excellent speed-to-power combination with a propagation delay of 100 ns. Operating voltage range of 1.65 V to 5.5 V with a quiescent supply current of 18 $\mu$ A per channel.

This device family also includes a Power On Reset (POR) feature that ensures the output is in a known state until the minimum supply voltage has been reached and a small time period passed before the output starts responding to the inputs. This prevents output transients during system power-up and power-down.

These comparators also feature no output phase inversion with fault-tolerant inputs that can go up to 6V without damage. This makes this family of comparators well suited for precision voltage monitoring in harsh, noisy environments.

The TLV902x comparators have an open-drain output stage that can be pulled below or beyond the supply voltage, making it appropriate for low voltage logic and level translators.

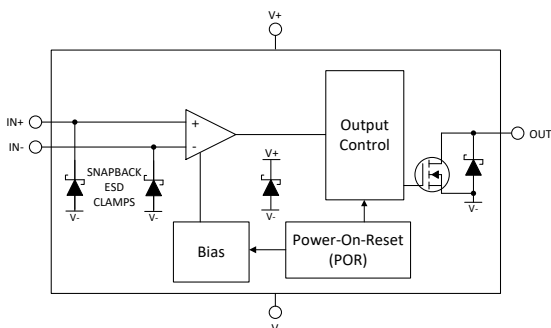
The TLV903x comparators have a push-pull output stage capable of sinking and sourcing milliamps of current when controlling an LED or driving a capacitive load such as a MOSFET gate.

The TLV902x and TLV903x are specified for the Industrial temperature range of -40°C to +125°C and are available in a standard leaded and leadless packages.

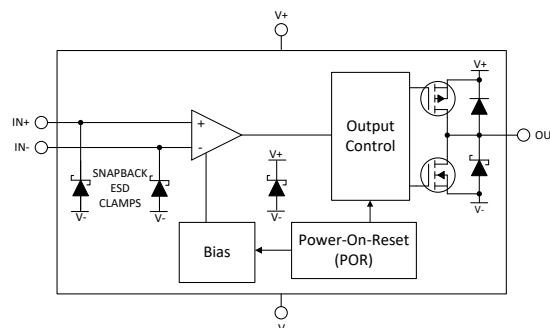
#### Device Information (1)

| PART NUMBER                   | PACKAGE          | BODY SIZE (NOM)   |
|-------------------------------|------------------|-------------------|
| TLV9022,<br>TLV9032<br>(Dual) | SOIC (8)         | 3.91 mm × 4.90 mm |
|                               | TSSOP (8)        | 3.00 mm × 4.40 mm |
|                               | VSSOP (8)        | 3.00 mm × 3.00 mm |
|                               | WSON (8)         | 2.00 mm × 2.00 mm |
|                               | SOT-23 (8)       | 1.60 mm × 2.90 mm |
| TLV9024,<br>TLV9034<br>(Quad) | SOIC (14)        | 3.91 mm × 8.65 mm |
|                               | TSSOP (14)       | 4.40 mm × 5.00 mm |
|                               | SOT-23-THIN (14) | 4.20 mm × 2.00 mm |
|                               | WQFN (16)        | 3.00 mm × 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.



TLV9022 and TLV9024 Block Diagram



TLV9032 and TLV9034 Block Diagram



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

|                                                                                                       |             |
|-------------------------------------------------------------------------------------------------------|-------------|
| <b>Changes from Revision * (June 2020) to Revision A (September 2020)</b>                             | <b>Page</b> |
| • Initial release.....                                                                                | <b>1</b>    |
| • Updated the numbering format for tables, figures, and cross-references throughout the document..... | <b>1</b>    |
| • Added Typical Graphs.....                                                                           | <b>11</b>   |
| <b>Changes from Revision A (September 2020) to Revision B (November 2020)</b>                         | <b>Page</b> |
| • Added Quad Devices.....                                                                             | <b>1</b>    |
| • Updated tables for Quad.....                                                                        | <b>5</b>    |

## 5 Pin Configuration and Functions

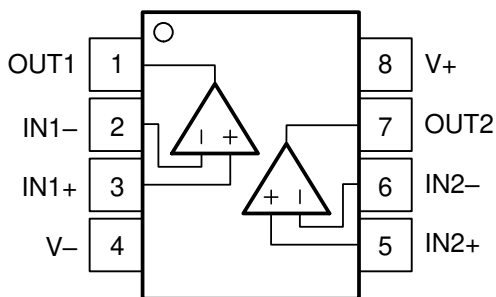
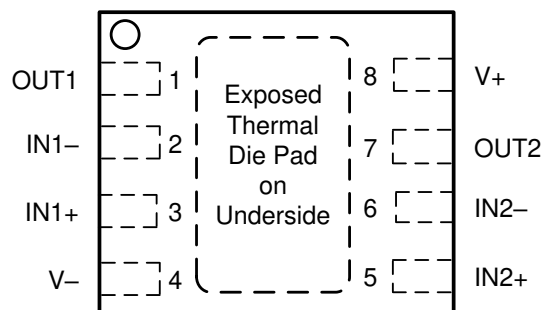


**Figure 5-1. D, DGK, PW, DDF Packages  
8-Pin SOIC, VSSOP, TSSOP, SOT-23-8  
Top View**



NOTE: Connect exposed thermal pad directly to V- pin.

**Figure 5-2. DSG Package,  
8-Pad WSON With Exposed Thermal Pad,  
Top View**

### Pin Functions: TLV90x2

| PIN         |     | I/O | DESCRIPTION                            |
|-------------|-----|-----|----------------------------------------|
| NAME        | NO. |     |                                        |
| OUT1        | 1   | O   | Output pin of the comparator 1         |
| IN1–        | 2   | I   | Inverting input pin of comparator 1    |
| IN1+        | 3   | I   | Noninverting input pin of comparator 1 |
| V–          | 4   | —   | Negative (low) supply                  |
| IN2+        | 5   | I   | Noninverting input pin of comparator 2 |
| IN2–        | 6   | I   | Inverting input pin of comparator 2    |
| OUT2        | 7   | O   | Output pin of the comparator 2         |
| V+          | 8   | —   | Positive supply                        |
| Thermal Pad | —   | —   | Connect directly to V- pin             |

## Pin Functions: TLV90x4

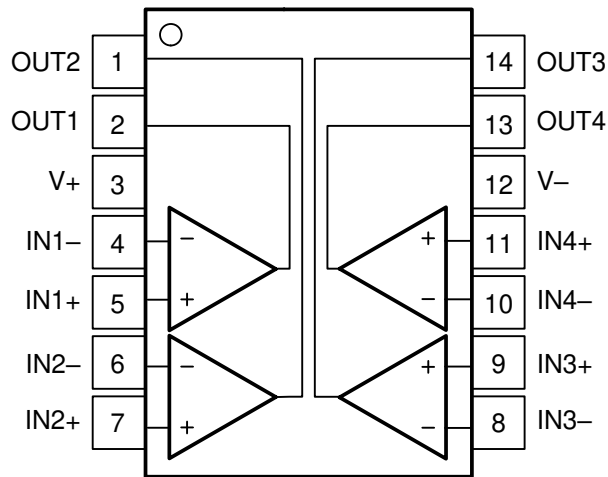
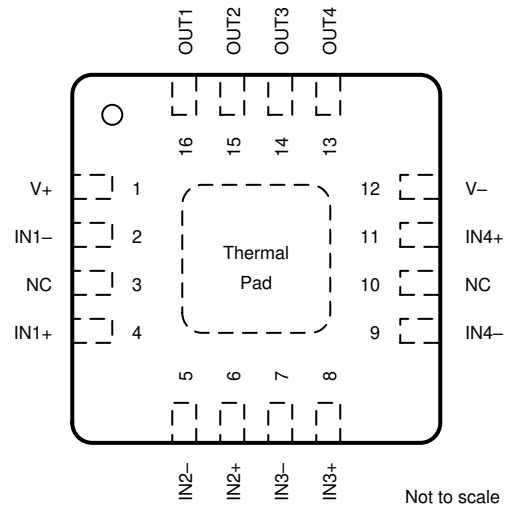


**Figure 5-3. D, PW, DYY Package,  
14-Pin SOIC, TSSOP, SOT-23,  
Top View**



NOTE: Connect exposed thermal pad directly to V- pin.

**Figure 5-4. RTE Package,  
16-Pad WQFN With Exposed Thermal Pad,  
Top View**

## Pin Functions: TLV90x4

| NAME <sup>(1)</sup> | PIN  |      | I/O    | DESCRIPTION                                    |
|---------------------|------|------|--------|------------------------------------------------|
|                     | SOIC | WQFN |        |                                                |
| OUT2                | 1    | 15   | Output | Output pin of the comparator 2                 |
| OUT1                | 2    | 16   | Output | Output pin of the comparator1                  |
| V+                  | 3    | 1    | —      | Positive supply                                |
| IN1-                | 4    | 2    | Input  | Negative input pin of the comparator 1         |
| IN1+                | 5    | 4    | Input  | Positive input pin of the comparator 1         |
| IN2-                | 6    | 5    | Input  | Negative input pin of the comparator 2         |
| IN2+                | 7    | 6    | Input  | Positive input pin of the comparator 2         |
| IN3-                | 8    | 7    | Input  | Negative input pin of the comparator 3         |
| IN3+                | 9    | 8    | Input  | Positive input pin of the comparator 3         |
| IN4-                | 10   | 9    | Input  | Negative input pin of the comparator 4         |
| IN4+                | 11   | 11   | Input  | Positive input pin of the comparator 4         |
| V-                  | 12   | 12   | —      | Negative supply                                |
| OUT4                | 13   | 13   | Output | Output pin of the comparator 4                 |
| OUT3                | 14   | 14   | Output | Output pin of the comparator 3                 |
| NC                  | —    | 3    | —      | No Internal Connection - Leave floating or GND |
| NC                  | —    | 10   | —      | No Internal Connection - Leave floating or GND |
| Thermal Pad         | —    | PAD  | —      | Connect directly to V- pin.                    |

- (1) Some manufacturers transpose the names of channels 1 & 2. Electrically the pinouts are identical, just a difference in channel naming convention.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                                         | MIN  | MAX          | UNIT |
|---------------------------------------------------------|------|--------------|------|
| Supply voltage: $V_S = (V+) - (V-)$                     | -0.3 | 6            | V    |
| Input pins (IN+, IN-) from $V-$ <sup>(2)</sup>          | -0.3 | 6            | V    |
| Current into Input pins (IN+, IN-)                      | -10  | 10           | mA   |
| Output (OUT) from $V-$ , open drain only <sup>(3)</sup> | -0.3 | 6            | V    |
| Output (OUT) from $V-$ , push-pull only                 | -0.3 | $(V+) + 0.3$ | V    |
| Output short circuit duration <sup>(4)</sup>            |      | 10           | s    |
| Junction temperature, $T_J$                             |      | 150          | °C   |
| Storage temperature, $T_{stg}$                          | -65  | 150          | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input terminals are diode-clamped to  $(V-)$ . Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less. Additionally, Inputs (IN+, IN-) can be greater than  $V+$  and OUT as long as it is within the -0.3 V to 6 V range
- (3) Output (OUT) for open drain can be greater than  $V+$  and inputs (IN+, IN-) as long as it is within the -0.3 V to 6 V range
- (4) Short-circuit to  $V-$  or  $V+$ . Short circuits from outputs can cause excessive heating and eventual destruction.

### 6.2 ESD Ratings

|             |                         |                                                                                | VALUE | UNIT |
|-------------|-------------------------|--------------------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|             |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1000 |      |

- (1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                                            | MIN  | MAX | UNIT |
|--------------------------------------------|------|-----|------|
| Supply voltage: $V_S = (V+) - (V-)$        | 1.65 | 5.5 | V    |
| Input voltage range (IN+, IN-) from $(V-)$ | -0.2 | 5.7 | V    |
| Ambient temperature, $T_A$                 | -40  | 125 | °C   |

## 6.4 Thermal Information, TLV90x2

| THERMAL METRIC <sup>(1)</sup> |                                              | TLV90x2  |            |             |            |              | UNIT |
|-------------------------------|----------------------------------------------|----------|------------|-------------|------------|--------------|------|
|                               |                                              | D (SOIC) | PW (TSSOP) | DGK (VSSOP) | DSG (WSON) | DDF (SOT-23) |      |
|                               |                                              | 8 PINS   | 8 PINS     | 8 PINS      | 8 PINS     | 8 PINS       |      |
| R <sub>qJA</sub>              | Junction-to-ambient thermal resistance       | 167.7    | 221.7      | –           | 175.2      | –            | °C/W |
| R <sub>qJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 107.0    | 109.1      | –           | 178.1      | –            | °C/W |
| R <sub>qJB</sub>              | Junction-to-board thermal resistance         | 111.2    | 152.5      | –           | 139.5      | –            | °C/W |
| Y <sub>JT</sub>               | Junction-to-top characterization parameter   | 53.1     | 36.4       | –           | 47.2       | –            | °C/W |
| Y <sub>JB</sub>               | Junction-to-board characterization parameter | 110.4    | 150.7      | –           | 138.9      | –            | °C/W |
| R <sub>qJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | –        | –          | –           | 127.3      | –            | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Thermal Information, TLV90x4

| THERMAL METRIC <sup>(1)</sup> |                                              | TLV90x4  |            |            |              | UNIT |
|-------------------------------|----------------------------------------------|----------|------------|------------|--------------|------|
|                               |                                              | D (SOIC) | PW (TSSOP) | RTE (WQFN) | DYY (SOT-23) |      |
|                               |                                              | 14 PINS  | 14 PINS    | 16 PINS    | 14 PINS      |      |
| R <sub>qJA</sub>              | Junction-to-ambient thermal resistance       | 136.0    | 155.0      | 134.1      | –            | °C/W |
| R <sub>qJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 91.2     | 82.0       | 122.6      | –            | °C/W |
| R <sub>qJB</sub>              | Junction-to-board thermal resistance         | 92.0     | 98.5       | 109.3      | –            | °C/W |
| Y <sub>JT</sub>               | Junction-to-top characterization parameter   | 46.9     | 25.7       | 30.9       | –            | °C/W |
| Y <sub>JB</sub>               | Junction-to-board characterization parameter | 91.6     | 97.6       | 108.3      | –            | °C/W |
| R <sub>qJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | –        | –          | 98.7       | –            | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.6 Electrical Characteristics, TLV90x2

For  $V_S$  (Total Supply Voltage) =  $(V+) - (V-) = 5\text{ V}$ ,  $V_{CM} = (V-)$  at  $T_A = 25^\circ\text{C}$  (Unless otherwise noted)

| PARAMETER                  |                                                 | TEST CONDITIONS                                                                                                                 | MIN          | TYP       | MAX          | UNIT                         |
|----------------------------|-------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|--------------|-----------|--------------|------------------------------|
| <b>OFFSET VOLTAGE</b>      |                                                 |                                                                                                                                 |              |           |              |                              |
| $V_{OS}$                   | Input offset voltage                            | $V_S = 1.8\text{ V}$ and $5\text{ V}_x$                                                                                         | -1.5         | $\pm 0.3$ | 1.5          | mV                           |
| $V_{OS}$                   | Input offset voltage                            | $V_S = 1.8\text{ V}$ and $5\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                       | -2           |           | 2            |                              |
| $dV_{IO}/dT$               | Input offset voltage drift                      | $V_S = 1.8\text{ V}$ and $5\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                       |              | $\pm 0.5$ |              | $\mu\text{V}/^\circ\text{C}$ |
| <b>POWER SUPPLY</b>        |                                                 |                                                                                                                                 |              |           |              |                              |
| $I_Q$                      | Quiescent current per comparator                | $V_S = 1.8\text{ V}$ and $5\text{ V}$ , No Load, Output Low                                                                     |              | 16        | 30           | $\mu\text{A}$                |
| $I_Q$                      | Quiescent current per comparator                | $V_S = 1.8\text{ V}$ and $5\text{ V}$ , No Load, Output Low, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                  |              |           | 35           |                              |
| PSRR                       | Power-supply rejection ratio                    | $V_S = 1.8\text{ V}$ to $5\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , (push-pull version)                  | 75           | 95        |              | dB                           |
| PSRR                       | Power-supply rejection ratio                    | $V_S = 1.8\text{ V}$ to $5\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ (open drain version)                   | 80           | 95        |              | dB                           |
| <b>INPUT BIAS CURRENT</b>  |                                                 |                                                                                                                                 |              |           |              |                              |
| $I_B$                      | Input bias current                              | $V_{CM} = V_S/2$                                                                                                                |              | 5         |              | pA                           |
| $I_{OS}$                   | Input offset current                            | $V_{CM} = V_S/2$                                                                                                                |              | 1         |              | pA                           |
| <b>INPUT CAPACITANCE</b>   |                                                 |                                                                                                                                 |              |           |              |                              |
| $C_{ID}$                   | Input Capacitance, Differential                 | $V_{CM} = V_S/2$                                                                                                                |              | 2         |              | pF                           |
| $C_{IC}$                   | Input Capacitance, Common Mode                  | $V_{CM} = V_S/2$                                                                                                                |              | 3         |              | pF                           |
| <b>INPUT VOLTAGE RANGE</b> |                                                 |                                                                                                                                 |              |           |              |                              |
| $V_{CM\text{-Range}}$      | Common-mode voltage range                       | $V_S = 1.8\text{ V}$ and $5\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                       | $(V-) - 0.2$ |           | $(V+) + 0.2$ | V                            |
| CMRR                       | Common-mode rejection ratio                     | $V_S = 5\text{ V}$ , $(V-) - 0.2\text{ V} < V_{CM} < (V+) + 0.2\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$   | 60           | 70        |              | dB                           |
| CMRR                       | Common-mode rejection ratio                     | $V_S = 1.8\text{ V}$ , $(V-) - 0.2\text{ V} < V_{CM} < (V+) + 0.2\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | 50           | 60        |              | dB                           |
| <b>OPEN-LOOP GAIN</b>      |                                                 |                                                                                                                                 |              |           |              |                              |
| $A_{VD}$                   | Large signal differential voltage amplification | For push-pull version only                                                                                                      | 50           | 200       |              | V/mV                         |
| <b>OUTPUT</b>              |                                                 |                                                                                                                                 |              |           |              |                              |
| $V_{OL}$                   | Voltage swing from $(V-)$                       | $I_{SINK} = 4\text{ mA}$ , $T_A = 25^\circ\text{C}$                                                                             |              | 75        | 125          | mV                           |
| $V_{OL}$                   | Voltage swing from $(V-)$                       | $I_{SINK} = 4\text{ mA}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                                    |              |           | 175          | mV                           |
| $V_{OH}$                   | Voltage swing from $(V+)$                       | $I_{SOURCE} = 4\text{ mA}$ , $T_A = 25^\circ\text{C}$ (push-pull only)                                                          |              | 75        | 125          | mV                           |
| $V_{OH}$                   | Voltage swing from $(V+)$                       | $I_{SOURCE} = 4\text{ mA}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ (push-pull only)                                 |              |           | 175          | mV                           |
| $I_{LKG}$                  | Open-drain output leakage current               | $V_{PULLUP} = (V+)$ , $T_A = 25^\circ\text{C}$ (open drain only)                                                                |              | 100       |              | pA                           |
| $I_{SC}$                   | Short-circuit current                           | $V_S = 5\text{ V}$ , Sinking                                                                                                    | 90           | 100       |              | mA                           |
| $I_{SC}$                   | Short-circuit current                           | $V_S = 5\text{ V}$ , Sourcing (push-pull only)                                                                                  | 90           | 100       |              | mA                           |

## 6.7 Switching Characteristics, TLV90x2

For  $V_S$  (Total Supply Voltage) =  $(V+) - (V-) = 5\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $C_L = 15\text{ pF}$  at  $T_A = 25^\circ\text{C}$  (Unless otherwise noted)

| PARAMETER            |                                     | TEST CONDITIONS                                                                                                                                                                                                         | MIN | TYP | MAX | UNIT          |
|----------------------|-------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|---------------|
| <b>OUTPUT</b>        |                                     |                                                                                                                                                                                                                         |     |     |     |               |
| $T_{PD-HL}$          | Propagation delay time, high-to-low | $V_{ID} = -100\text{ mV}$ ; Delay from mid-point of input to mid-point of output ( $R_P = 2.5\text{ K}\Omega$ for open drain only)                                                                                      |     | 100 |     | ns            |
| $T_{PD-LH}$          | Propagation delay time, low-to-high | $V_{ID} = 100\text{ mV}$ ; Delay from mid-point of input to mid-point of output (for push-pull only)                                                                                                                    |     | 115 |     | ns            |
| $T_{PD-LH}$          | Propagation delay time, low-to-high | $V_{ID} = 100\text{ mV}$ ; Delay from mid-point of input to mid-point of output ( $R_P = 2.5\text{ K}\Omega$ for open drain only)                                                                                       |     | 150 |     | ns            |
| $T_{FALL}$           | 5V Output Fall Time, 80% to 20%     | $V_{ID} = -100\text{ mV}$                                                                                                                                                                                               |     | 3   |     | ns            |
| $T_{RISE}$           | 5V Output Rise Time, 20% to 80%     | $V_{ID} = 100\text{ mV}$ (for push-pull only)                                                                                                                                                                           |     | 3   |     | ns            |
| $F_{TOGGLE}$         | 5V, Toggle Frequency                | $V_{ID} = 100\text{ mV}$ ( $R_P = 2.5\text{ K}\Omega$ for open drain only)                                                                                                                                              |     | 3   |     | MHz           |
| <b>POWER ON TIME</b> |                                     |                                                                                                                                                                                                                         |     |     |     |               |
| $P_{ON}$             | Power on-time                       | $V_S = 1.8\text{ V}$ and $5\text{ V}$ , $V_{CM} = (V-)$ , $V_{ID} = -0.1\text{ V}$ , $V_{PULL-UP} = V_S / 2$ , Delay from $V_S / 2$ to $V_{OUT} = 0.1 \times V_S / 2$ ( $R_P = 2.5\text{ K}\Omega$ for open drain only) |     | 20  |     | $\mu\text{s}$ |

## 6.8 Electrical Characteristics, TLV90x4

For  $V_S$  (Total Supply Voltage) =  $(V+) - (V-) = 5\text{ V}$ ,  $V_{CM} = (V-)$  at  $T_A = 25^\circ\text{C}$  (Unless otherwise noted)

| PARAMETER                  |                                                 | TEST CONDITIONS                                                                                                                 | MIN          | TYP       | MAX          | UNIT                         |
|----------------------------|-------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|--------------|-----------|--------------|------------------------------|
| <b>OFFSET VOLTAGE</b>      |                                                 |                                                                                                                                 |              |           |              |                              |
| $V_{OS}$                   | Input offset voltage                            | $V_S = 1.8\text{ V}$ and $5\text{ V}_x$                                                                                         | -1.5         | $\pm 0.3$ | 1.5          | mV                           |
| $V_{OS}$                   | Input offset voltage                            | $V_S = 1.8\text{ V}$ and $5\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                       | -2           |           | 2            |                              |
| $dV_{IO}/dT$               | Input offset voltage drift                      | $V_S = 1.8\text{ V}$ and $5\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                       |              | $\pm 0.5$ |              | $\mu\text{V}/^\circ\text{C}$ |
| <b>POWER SUPPLY</b>        |                                                 |                                                                                                                                 |              |           |              |                              |
| $I_Q$                      | Quiescent current per comparator                | $V_S = 1.8\text{ V}$ and $5\text{ V}$ , No Load, Output Low                                                                     |              | 16        | 30           | $\mu\text{A}$                |
| $I_Q$                      | Quiescent current per comparator                | $V_S = 1.8\text{ V}$ and $5\text{ V}$ , No Load, Output Low, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                  |              |           | 35           |                              |
| PSRR                       | Power-supply rejection ratio                    | $V_S = 1.8\text{ V}$ to $5\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , (push-pull version)                  |              |           | 177.8        | $\mu\text{V}/\text{V}$       |
| PSRR                       | Power-supply rejection ratio                    | $V_S = 1.8\text{ V}$ to $5\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , (push-pull version)                  | 75           | 95        |              | dB                           |
| PSRR                       | Power-supply rejection ratio                    | $V_S = 1.8\text{ V}$ to $5\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , (open drain version)                 |              |           | 100          | $\mu\text{V}/\text{V}$       |
| PSRR                       | Power-supply rejection ratio                    | $V_S = 1.8\text{ V}$ to $5\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , (open drain version)                 | 80           | 95        |              | dB                           |
| <b>INPUT BIAS CURRENT</b>  |                                                 |                                                                                                                                 |              |           |              |                              |
| $I_B$                      | Input bias current                              | $V_{CM} = V_S/2$                                                                                                                |              | 5         |              | pA                           |
| $I_{OS}$                   | Input offset current                            | $V_{CM} = V_S/2$                                                                                                                |              | 1         |              | pA                           |
| <b>INPUT CAPACITANCE</b>   |                                                 |                                                                                                                                 |              |           |              |                              |
| $C_{ID}$                   | Input Capacitance, Differential                 | $V_{CM} = V_S/2$                                                                                                                |              | 2         |              | pF                           |
| $C_{IC}$                   | Input Capacitance, Common Mode                  | $V_{CM} = V_S/2$                                                                                                                |              | 3         |              | pF                           |
| <b>INPUT VOLTAGE RANGE</b> |                                                 |                                                                                                                                 |              |           |              |                              |
| $V_{CM\text{-Range}}$      | Common-mode voltage range                       | $V_S = 1.8\text{ V}$ and $5\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                       | $(V-) - 0.2$ |           | $(V+) + 0.2$ | V                            |
| CMRR                       | Common-mode rejection ratio                     | $V_S = 5\text{ V}$ , $(V-) - 0.2\text{ V} < V_{CM} < (V+) + 0.2\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$   | 60           | 70        |              | dB                           |
| CMRR                       | Common-mode rejection ratio                     | $V_S = 1.8\text{ V}$ , $(V-) - 0.2\text{ V} < V_{CM} < (V+) + 0.2\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | 50           | 60        |              | dB                           |
| <b>OPEN-LOOP GAIN</b>      |                                                 |                                                                                                                                 |              |           |              |                              |
| $A_{VD}$                   | Large signal differential voltage amplification | For push-pull version only                                                                                                      | 50           | 200       |              | V/mV                         |
| <b>OUTPUT</b>              |                                                 |                                                                                                                                 |              |           |              |                              |
| $V_{OL}$                   | Voltage swing from $(V-)$                       | $I_{SINK} = 4\text{ mA}$ , $T_A = 25^\circ\text{C}$                                                                             |              | 75        | 125          | mV                           |
| $V_{OL}$                   | Voltage swing from $(V-)$                       | $I_{SINK} = 4\text{ mA}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                                    |              |           | 175          | mV                           |
| $V_{OH}$                   | Voltage swing from $(V+)$                       | $I_{SOURCE} = 4\text{ mA}$ , $T_A = 25^\circ\text{C}$ (push-pull only)                                                          |              | 75        | 125          | mV                           |
| $V_{OH}$                   | Voltage swing from $(V+)$                       | $I_{SOURCE} = 4\text{ mA}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ (push-pull only)                                 |              |           | 175          | mV                           |
| $I_{LKG}$                  | Open-drain output leakage current               | $V_{PULLUP} = (V+)$ , $T_A = 25^\circ\text{C}$ (open drain only)                                                                |              | 100       |              | pA                           |
| $I_{SC}$                   | Short-circuit current                           | $V_S = 5\text{ V}$ , Sinking                                                                                                    | 90           | 100       |              | mA                           |
| $I_{SC}$                   | Short-circuit current                           | $V_S = 5\text{ V}$ , Sourcing (push-pull only)                                                                                  | 90           | 100       |              | mA                           |

## 6.9 Switching Characteristics, TLV90x4

For  $V_S$  (Total Supply Voltage) =  $(V+) - (V-) = 5\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $C_L = 15\text{ pF}$  at  $T_A = 25^\circ\text{C}$  (Unless otherwise noted)

| PARAMETER            | TEST CONDITIONS                                                                                                                                                                                                                          | MIN | TYP | MAX | UNIT          |
|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|---------------|
| <b>OUTPUT</b>        |                                                                                                                                                                                                                                          |     |     |     |               |
| $T_{PD-HL}$          | Propagation delay time, high-to-low<br>$V_{ID} = -100\text{ mV}$ ; Delay from mid-point of input to mid-point of output ( $R_P = 2.5\text{ K}\Omega$ for open drain only)                                                                |     | 100 |     | ns            |
| $T_{PD-LH}$          | Propagation delay time, low-to-high<br>$V_{ID} = 100\text{ mV}$ ; Delay from mid-point of input to mid-point of output (for push-pull only)                                                                                              |     | 115 |     | ns            |
| $T_{PD-LH}$          | Propagation delay time, low-to-high<br>$V_{ID} = 100\text{ mV}$ ; Delay from mid-point of input to mid-point of output ( $R_P = 2.5\text{ K}\Omega$ for open drain only)                                                                 |     | 150 |     | ns            |
| $T_{FALL}$           | 5V Output Fall Time, 80% to 20%<br>$V_{ID} = -100\text{ mV}$                                                                                                                                                                             |     | 3   |     | ns            |
| $T_{RISE}$           | 5V Output Rise Time, 20% to 80%<br>$V_{ID} = 100\text{ mV}$ , for push-pull only                                                                                                                                                         |     | 3   |     | ns            |
| $F_{TOGGLE}$         | 5V, Toggle Frequency<br>$V_{ID} = 100\text{ mV}$ ( $R_P = 2.5\text{ K}\Omega$ for open drain only)                                                                                                                                       |     | 3   |     | MHz           |
| <b>POWER ON TIME</b> |                                                                                                                                                                                                                                          |     |     |     |               |
| $P_{ON}$             | Power on-time<br>$V_S = 1.8\text{ V}$ and $5\text{ V}$ , $V_{CM} = (V-)$ , $V_{ID} = -0.1\text{ V}$ , $V_{PULL-UP} = V_S / 2$ , Delay from $V_S / 2$ to $V_{OUT} = 0.1 \times V_S / 2$ ( $R_P = 2.5\text{ K}\Omega$ for open drain only) |     | 30  |     | $\mu\text{s}$ |

## 6.10 Typical Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_{\text{PULLUP}} = 2.5\text{ k}\Omega$ ,  $C_L = 15\text{ pF}$ ,  $V_{\text{CM}} = 0\text{ V}$ ,  $V_{\text{UNDERDRIVE}} = 100\text{ mV}$ ,  $V_{\text{OVERDRIVE}} = 100\text{ mV}$  unless otherwise noted.

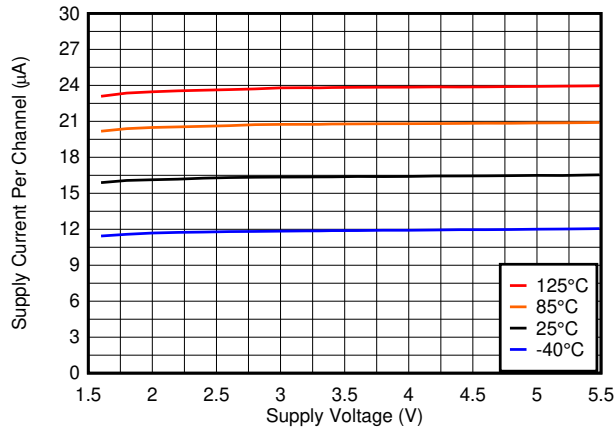


Figure 6-1. Supply Current vs. Supply Voltage

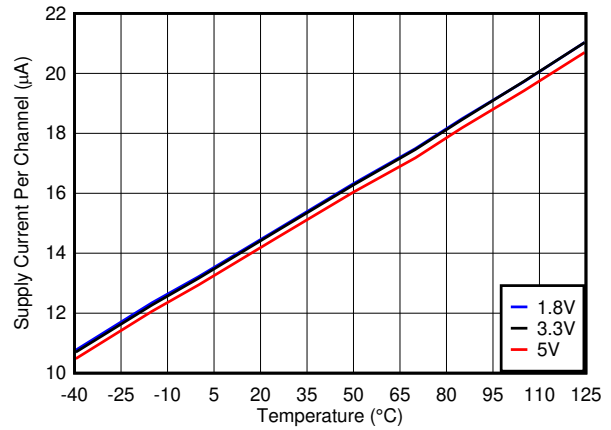


Figure 6-2. Supply Current vs. Temperature

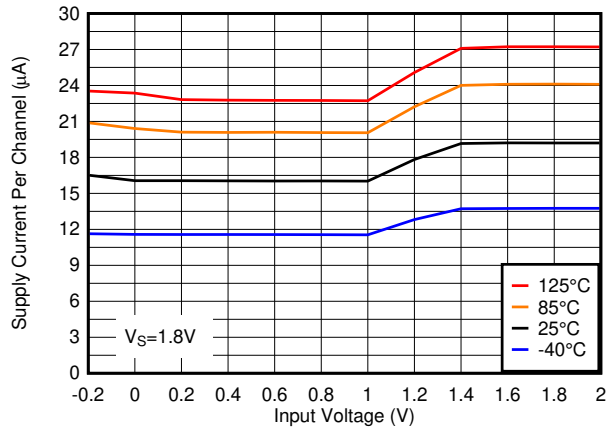


Figure 6-3. Supply Current vs. Input Voltage, 1.8V

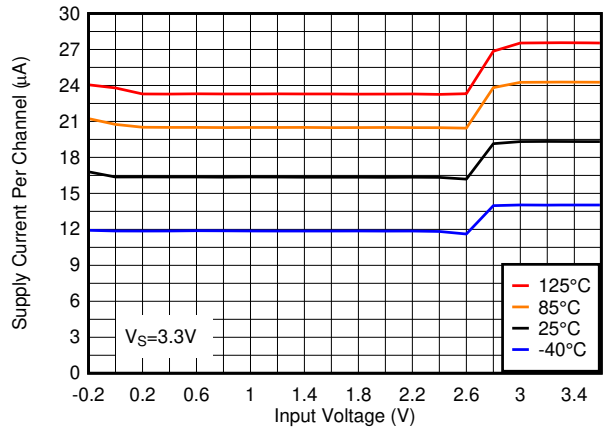


Figure 6-4. Supply Current vs. Input Voltage, 3.3V

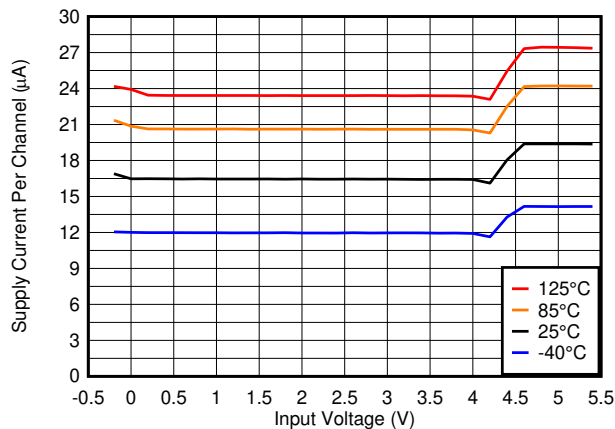


Figure 6-5. Supply Current vs. Input Voltage, 5V

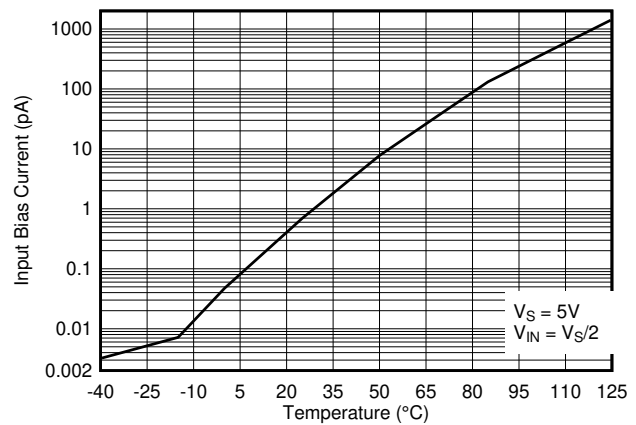


Figure 6-6. Input Bias Current vs. Temperature

## 6.10 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_{\text{PULLUP}} = 2.5\text{ k}\Omega$ ,  $C_L = 15\text{ pF}$ ,  $V_{\text{CM}} = 0\text{ V}$ ,  $V_{\text{UNDERDRIVE}} = 100\text{ mV}$ ,  $V_{\text{OVERDRIVE}} = 100\text{ mV}$  unless otherwise noted.

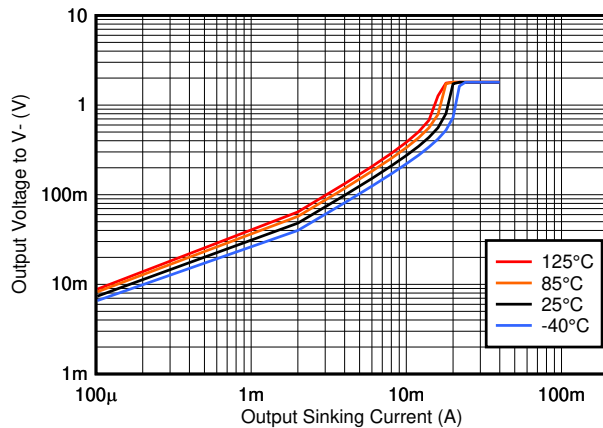


Figure 6-7. Output Sinking Current vs. Output Voltage, 1.8V

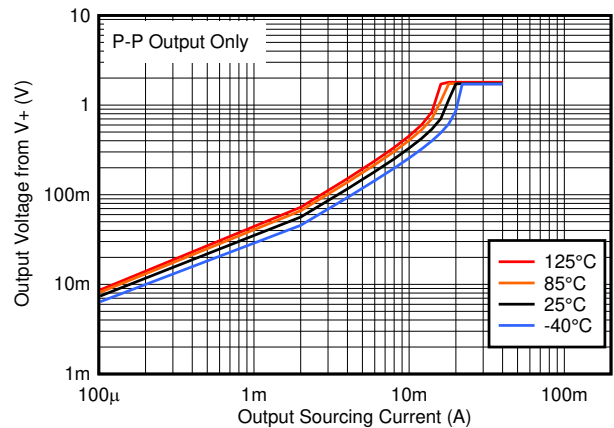


Figure 6-8. Output Sourcing Current vs. Output Voltage, 1.8V

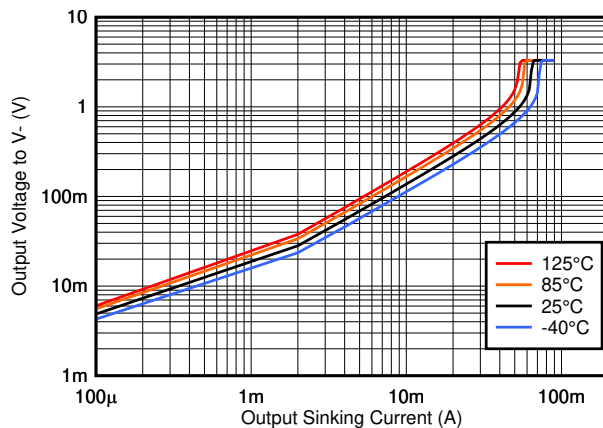


Figure 6-9. Output Sinking Current vs. Output Voltage, 3.3V

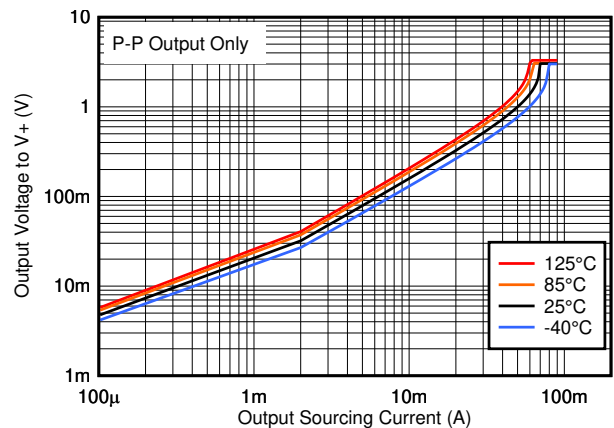


Figure 6-10. Output Sourcing Current vs. Output Voltage, 3.3V

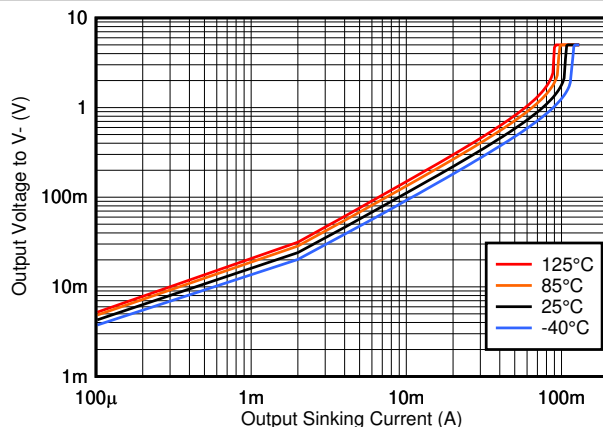


Figure 6-11. Output Sinking Current vs. Output Voltage, 5V

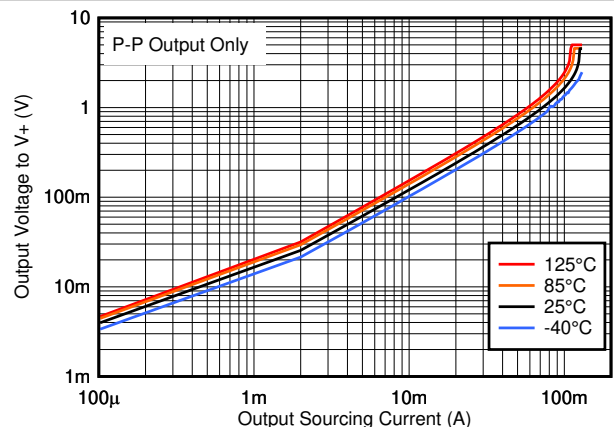


Figure 6-12. Output Sourcing Current vs. Output Voltage, 5V

## 6.10 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_{\text{PULLUP}} = 2.5\text{ k}\Omega$ ,  $C_L = 15\text{ pF}$ ,  $V_{\text{CM}} = 0\text{ V}$ ,  $V_{\text{UNDERDRIVE}} = 100\text{ mV}$ ,  $V_{\text{OVERDRIVE}} = 100\text{ mV}$  unless otherwise noted.

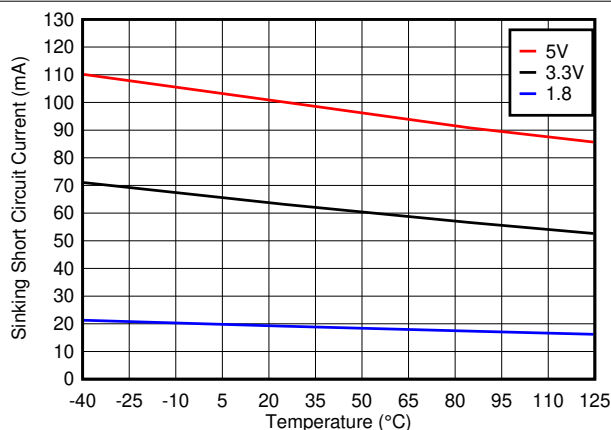


Figure 6-13. Sinking Short Circuit Current vs. Temperature

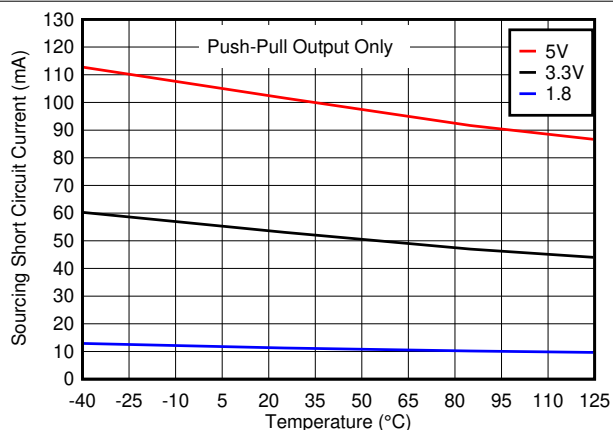


Figure 6-14. Sourcing Short Circuit Current vs. Temperature

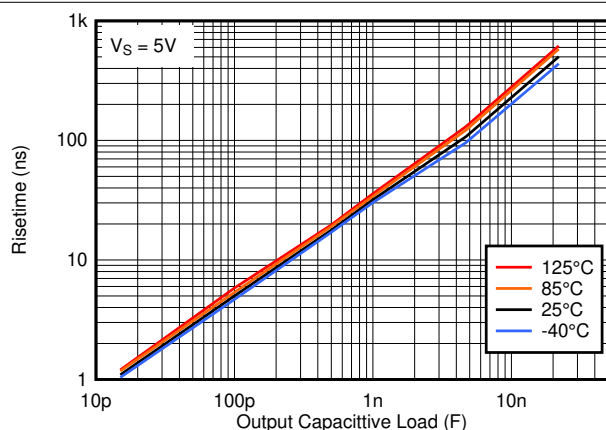


Figure 6-15. Risettime vs. Capacitive Load

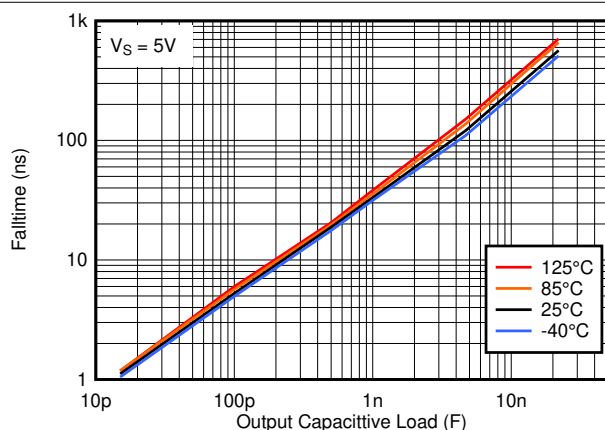


Figure 6-16. Falltime vs. Capacitive Load

## 6.10 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_{\text{PULLUP}} = 2.5\text{ k}\Omega$ ,  $C_L = 15\text{ pF}$ ,  $V_{\text{CM}} = 0\text{ V}$ ,  $V_{\text{UNDERDRIVE}} = 100\text{ mV}$ ,  $V_{\text{OVERDRIVE}} = 100\text{ mV}$  unless otherwise noted.

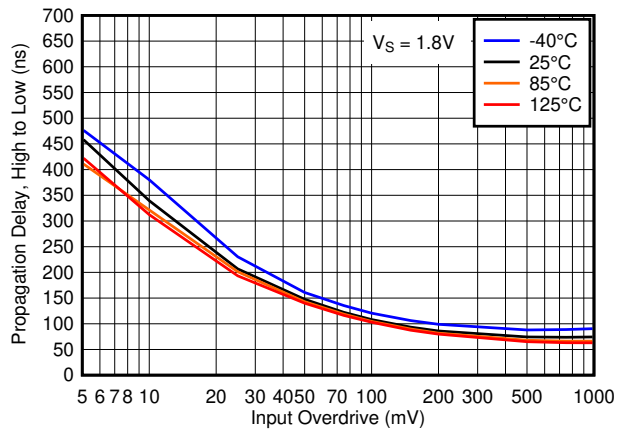


Figure 6-17. Propagation Delay, High to Low, 1.8V

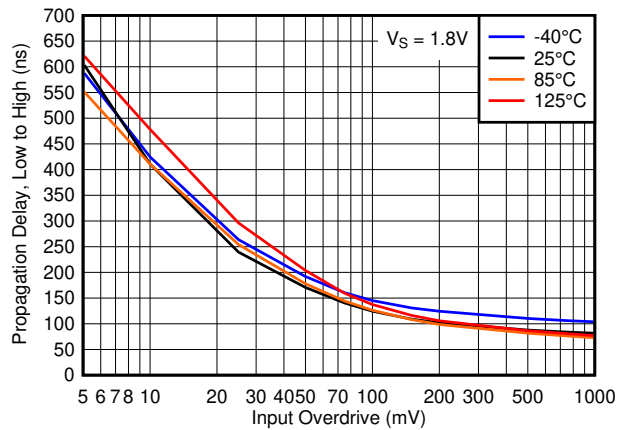


Figure 6-18. Propagation Delay, Low to High, 1.8V

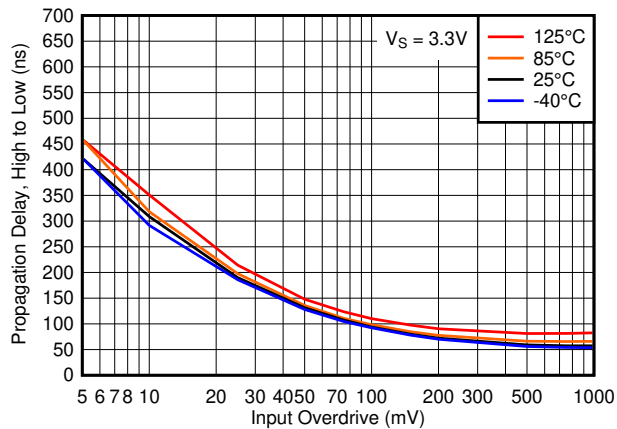


Figure 6-19. Propagation Delay, High to Low, 3.3V

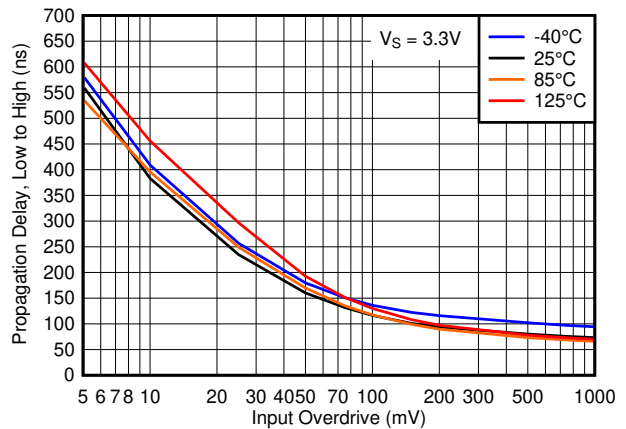


Figure 6-20. Propagation Delay, Low to High, 3.3V

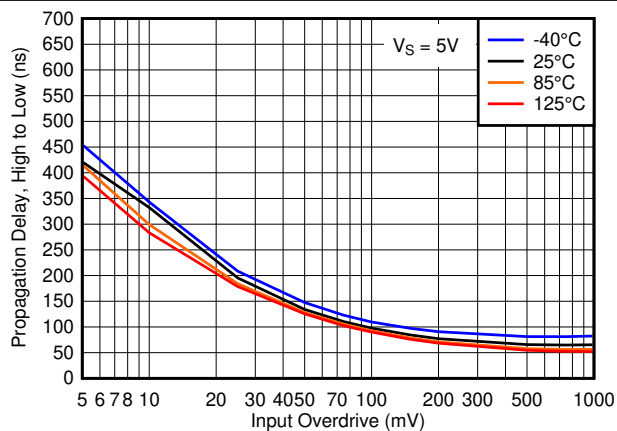


Figure 6-21. Propagation Delay, High to Low, 5V

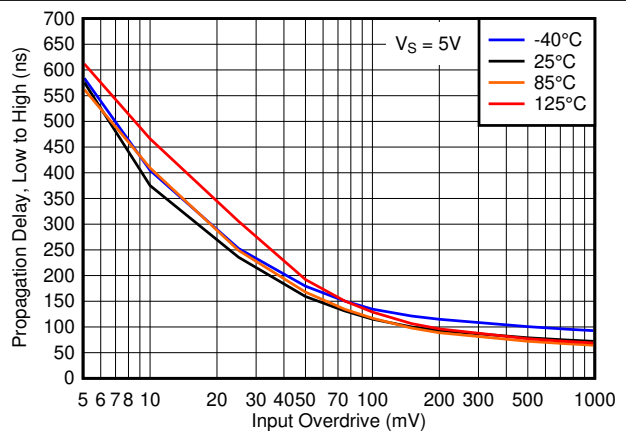


Figure 6-22. Propagation Delay, Low to High, 5V

## 6.10 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_{\text{PULLUP}} = 2.5\text{ k}\Omega$ ,  $C_L = 15\text{ pF}$ ,  $V_{\text{CM}} = 0\text{ V}$ ,  $V_{\text{UNDERDRIVE}} = 100\text{ mV}$ ,  $V_{\text{OVERDRIVE}} = 100\text{ mV}$  unless otherwise noted.

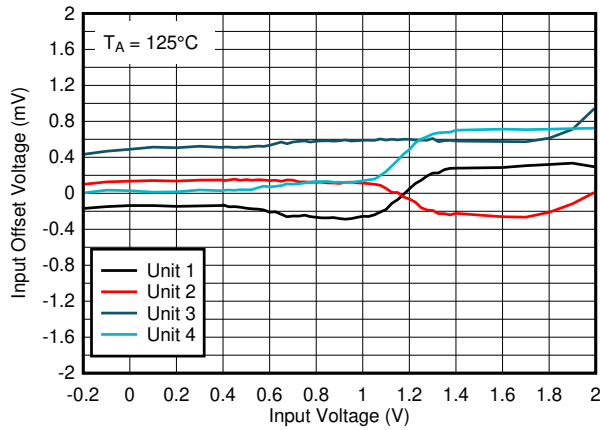


Figure 6-23. Offset Voltage vs. Input Voltage at  $125^\circ\text{C}$ , 1.8V

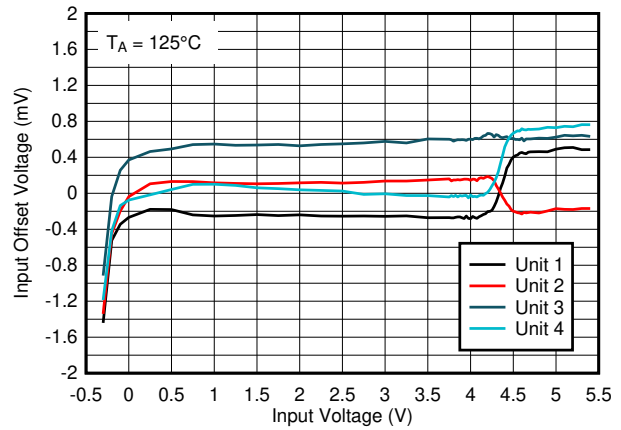


Figure 6-24. Offset Voltage vs. Input Voltage at  $125^\circ\text{C}$ , 5V

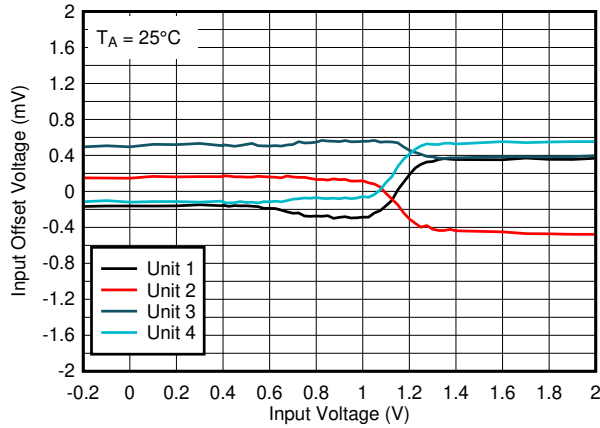


Figure 6-25. Offset Voltage vs. Input Voltage at  $25^\circ\text{C}$ , 1.8V

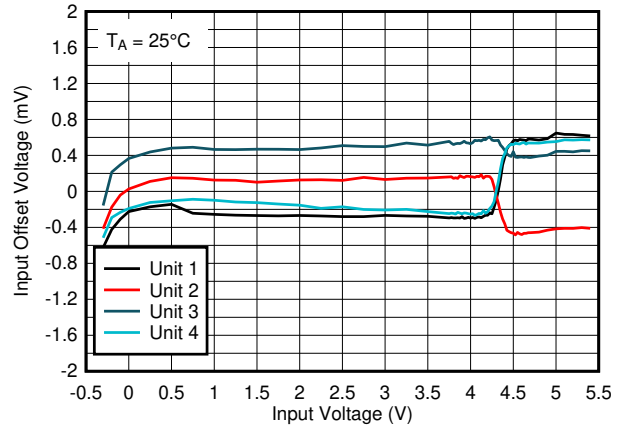


Figure 6-26. Offset Voltage vs. Input Voltage at  $25^\circ\text{C}$ , 5V

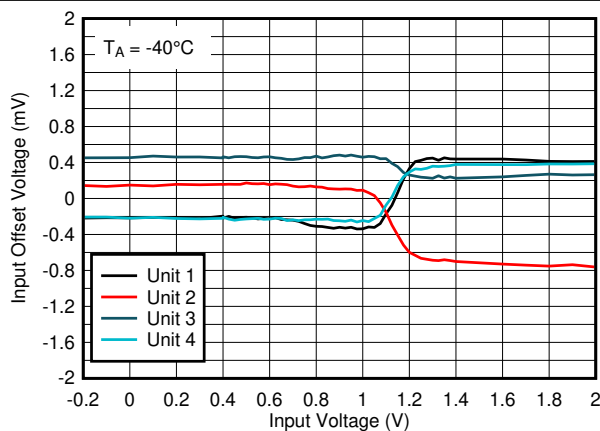


Figure 6-27. Offset Voltage vs. Input Voltage at  $-40^\circ\text{C}$ , 1.8V

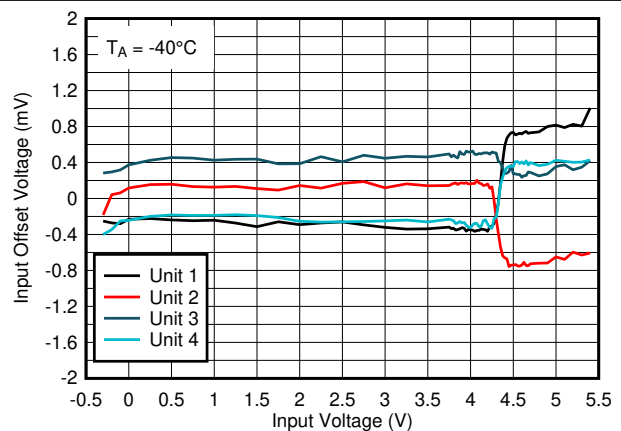


Figure 6-28. Offset Voltage vs. Input Voltage at  $-40^\circ\text{C}$ , 5V

## 6.10 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_{\text{PULLUP}} = 2.5\text{ k}\Omega$ ,  $C_L = 15\text{ pF}$ ,  $V_{\text{CM}} = 0\text{ V}$ ,  $V_{\text{UNDERDRIVE}} = 100\text{ mV}$ ,  $V_{\text{OVERDRIVE}} = 100\text{ mV}$  unless otherwise noted.

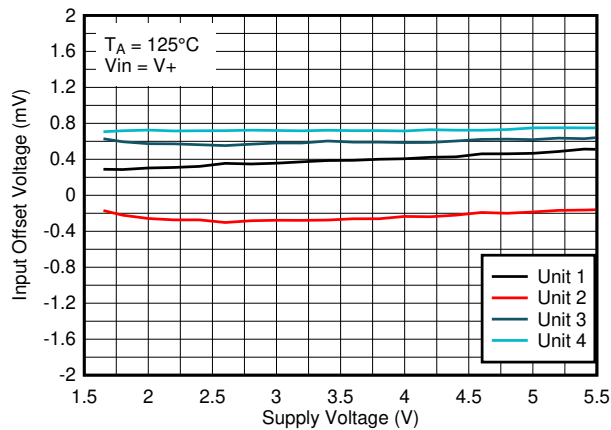


Figure 6-29. Offset Voltage vs. Supply Voltage at  $125^\circ\text{C}$ ,  $V_{\text{IN}}=V_+$

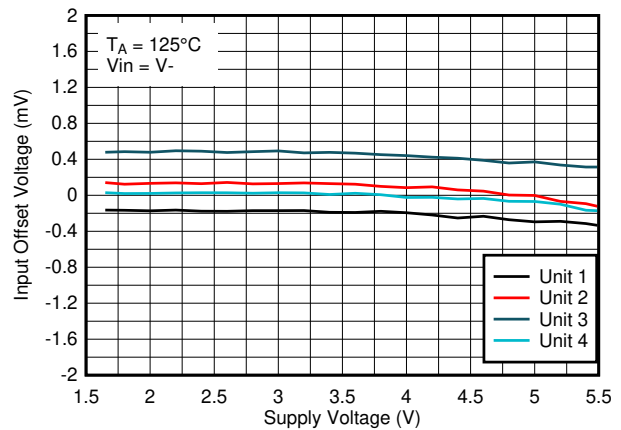


Figure 6-30. Offset Voltage vs. Supply Voltage at  $125^\circ\text{C}$ ,  $V_{\text{IN}}=V_-$

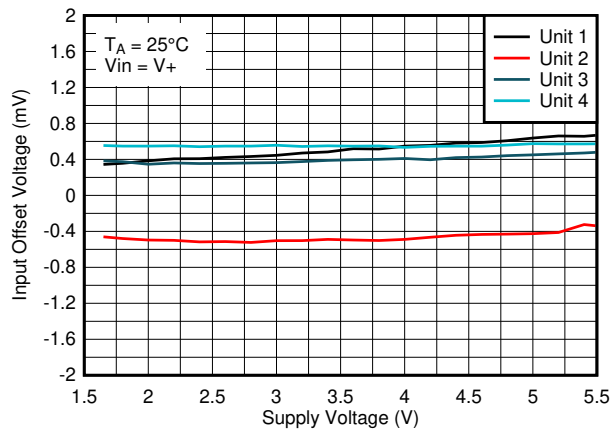


Figure 6-31. Offset Voltage vs. Supply Voltage at  $25^\circ\text{C}$ ,  $V_{\text{IN}}=V_+$

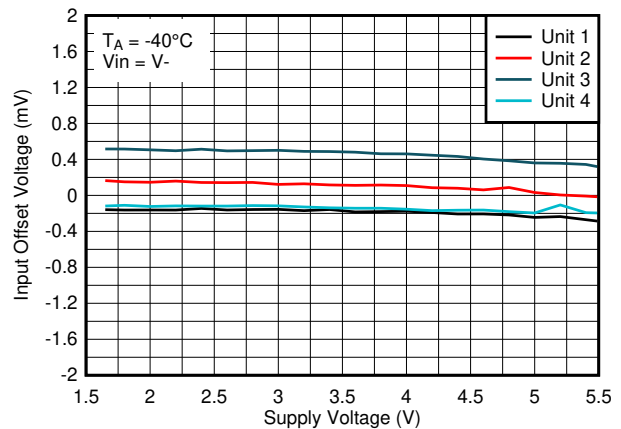


Figure 6-32. Offset Voltage vs. Supply Voltage at  $25^\circ\text{C}$ ,  $V_{\text{IN}}=V_-$

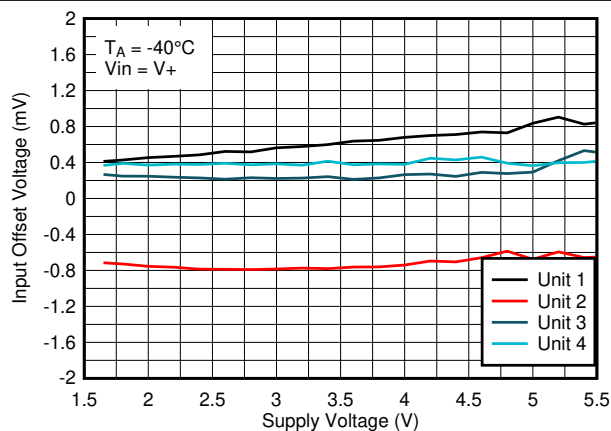


Figure 6-33. Offset Voltage vs. Supply Voltage at  $-40^\circ\text{C}$ ,  $V_{\text{IN}}=V_+$

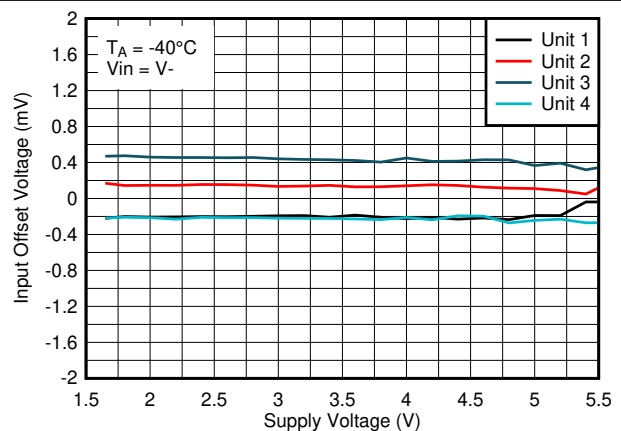


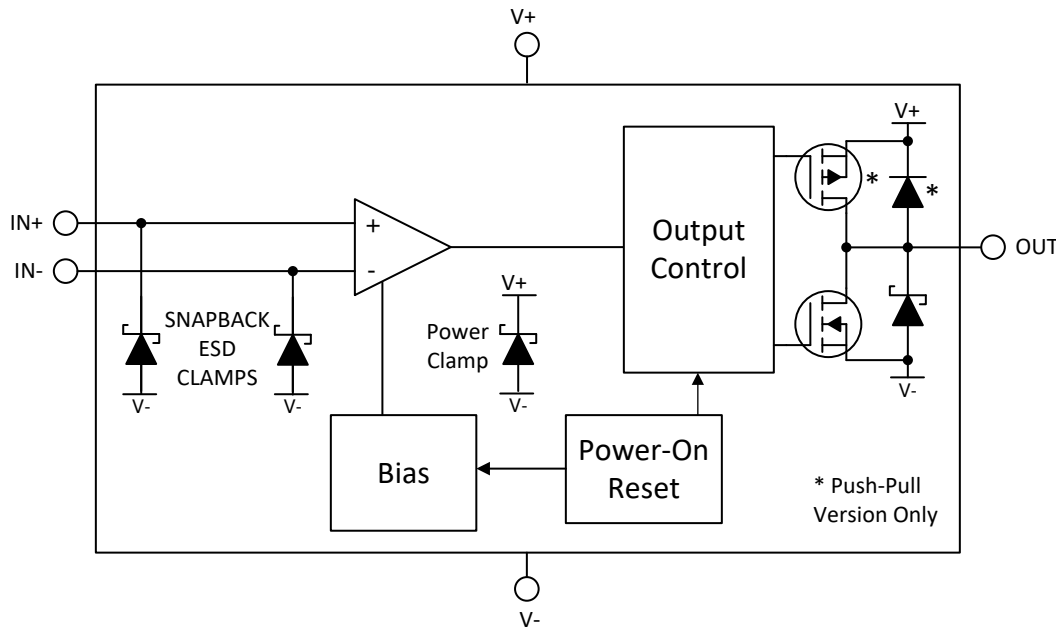
Figure 6-34. Offset Voltage vs. Supply Voltage at  $-40^\circ\text{C}$ ,  $V_{\text{IN}}=V_-$

## 7 Detailed Description

### 7.1 Overview

The TLV902x and TLV903x devices are dual-channel, micro-power comparators with push-pull and open-drain outputs and low input offset voltage. Operating down to 1.65 V while only consuming only 16  $\mu$ A per channel, the TLV902x and TLV903x are ideally suited for portable, automotive and industrial applications. An internal power-on reset circuit ensures that the output remains in a known state during power-up and power-down while fail-safe inputs can tolerate input transients without damage or false outputs.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

The TLV902x (open-drain output) and TLV903x (push-pull output) devices are micro-power comparators that have low input offset voltages and are capable of operating at low voltages. The TLV90xx family feature a rail-to-rail input stage capable of operating up to 200 mV beyond the power supply rails. The comparators also feature push-pull and open-drain output stage options and Power On Reset for known start-up conditions.

### 7.4 Device Functional Modes

#### 7.4.1 Outputs

##### 7.4.1.1 TLV9022 and TLV9024 Open Drain Output

The TLV902x features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage from 0 V up to 5.5 V, independent of the comparator supply voltage ( $V_S$ ). The open-drain output also allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to between 100 $\mu$ A and 1mA. Lower pull-up resistor values will help increase the rising edge risetime, but at the expense of increasing  $V_{OL}$  and higher power dissipation. The risetime will be dependant on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1 M $\Omega$ ) will create an exponential rising edge due to the RC time constant and increase the risetime.

Unused open drain outputs should be left floating, or can be tied to the V- pin if floating pins are not allowed. While an individual output can typically sink up to 125 mA, the total combined current for all channels must be less than 200 mA.

### 7.4.1.2 TLV9032 and TLV9034 Push-Pull Output

The TLV903x features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Unused push-pull outputs should be left floating, and never tied to a supply, ground, or another output. While an individual output can typically sink and source up to 100mA, the total combined current for all channels must be less than 200 mA.

### 7.4.2 Power-On Reset (POR)

The TLV90xx has an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply ( $V_S$ ) is ramping up or ramping down, the POR circuitry will be activated for up to 30 $\mu$ s after the minimum supply voltage threshold of 1.5V is crossed, or immediately when the supply voltage drops below 1.5V. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input ( $V_{ID}$ ).

The POR circuit will keep the output high impedance (HI-Z) during the POR period ( $t_{ON}$ ).

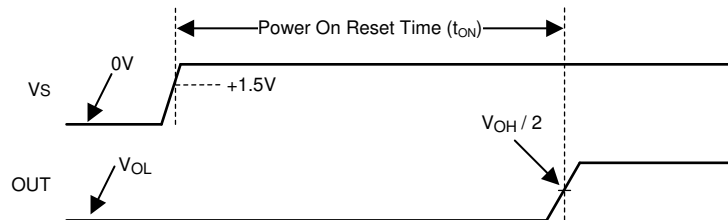


**Figure 7-1. Power-On Reset Timing Diagram**

Note that it the nature of an open collector output that the output will rise with the pull-up voltage during the POR period.

For the TL903x push-pull output devices, the output is "floating" during the POR period. A light pull-up (to V+) or pull-down (to V-) resistor can be used to pre-bias the output condition to prevent the output from floating. If output high is the desired start-up condition, then use the open collector TL902x, since a pull-up resistor is already required.

### 7.4.3 Inputs

#### 7.4.3.1 Rail to Rail Input

The TLV90xx input voltage range extends from 200mV below V- to 200 mV above V+. The differential input voltage ( $V_{ID}$ ) can be any voltage within these limits. No phase-inversion of the comparator output will occur when the input pins exceed V+ or V-.

#### 7.4.3.2 Fault Tolerant Inputs

The TLV90xx inputs are fault tolerant up to 5.5V independent of  $V_S$ . Fault tolerant is defined as maintaining the same high input impedance when  $V_S$  is unpowered or within the recommended operating ranges.

The fault tolerant inputs can be any value between 0 V and 5.5 V, even while  $V_S$  is zero or ramping up or down. This feature avoids power sequencing issues as long as the input voltage range and supply voltage are within the specified ranges. This is possible since the inputs are not clamped to V+ and the input current maintains its value even when a higher voltage is applied to the inputs.

As long as one of the input pins remains within the valid input range, and the supply voltage is valid and not in POR, the output state will be correct.

The following is a summary of input voltage excursions and their outcomes:

1. When both IN- and IN+ are within the specified input voltage range:
  - a. If IN- is higher than IN+ and the offset voltage, the output is low.

- b. If IN- is lower than IN+ and the offset voltage, the output is high.
2. When IN- is outside the specified input voltage range and IN+ is within the specified voltage range, the output is low.
3. When IN+ is higher than the specified input voltage range and IN- is within the specified input voltage range, the output is high
4. When IN- and IN+ are both outside the specified input voltage range, the output is **indeterminate** (random).  
*Do not* operate in this region.

Even with the fault tolerant feature, TI *strongly* recommends keeping the inputs within the specified input voltage range during normal system operation to maintain datasheet specifications. Operating outside the specified input range can cause changes in specifications such as propagation delay and input bias current, which can lead to unpredictable behavior.

#### 7.4.3.3 Input Protection

The input bias current is typically 5 pA for input voltages between V+ and V-. The comparator inputs are protected from reverse voltage by the internal ESD diodes connected to V-. As the input voltage goes under V-, or above the input Absolute Maximum ratings the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current typically doubles for each 10°C temperature increase.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents should the clamps conduct. The current should be limited 10 mA or less. This series resistance can be part of any resistive input dividers or networks.

#### 7.4.4 ESD Protection

The TLV90xx family incorporates internal ESD protection circuits on all pins. The inputs, and the open-drain output, use a proprietary "snapback" type ESD clamp from each pin to V-, which allows the pins to exceed the supply voltage (V+). While shown as Zener diodes, snapback "short" and go low impedance (like an SCR) when the threshold is exceeded, as opposed to clamping to a defined voltage like a Zener.

The TLV902x open-drain output protection also consists of a ESD clamp between the output and V- to allow the output to be pulled above V+ to a maximum of 5.5V.

The TLV903x push-pull output protection consists of a ESD clamp between the output and V-, but also includes a ESD diode clamp to V+, as the output should not exceed the supply rails.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents should the clamps conduct. The current should be limited 10 mA or less. This series resistance can be part of any resistive input dividers or networks. TI does not specify the performance of the ESD clamps and external clamping should be added if the inputs or output could exceed the maximum ratings as part of normal operation.

#### 7.4.5 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs should be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even V+ as long as the input is directly connected to the V+ pin to avoid transients).

#### 7.4.6 Hysteresis

The TLV90xx family does not have internal hysteresis. Due to the wide effective bandwidth and low input offset voltage, it is possible for the output to "chatter" (oscillate) when the absolute differential voltage near zero as the comparator triggers on it's own internal wideband noise. This is normal comparator behavior and is expected. TI recommends that the user add external hysteresis if slow moving signals are expected. See [Section 8.1.2](#) in the following section.



voltage can influence the propagation delay ( $t_p$ ). The smaller the overdrive voltage, the longer the propagation delay, particularly when  $<100\text{mV}$ . If the fastest speeds are desired, it is recommended to apply the highest amount of overdrive possible.

The risetime ( $t_r$ ) and falltime ( $t_f$ ) is the time from the 20% and 80% points of the output waveform.

### 8.1.2 Hysteresis

The basic comparator configuration may oscillate or produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator.

This problem can be prevented by the addition of hysteresis or positive feedback.

The hysteresis transfer curve is shown in [Figure 8-2](#). This curve is a function of three components:  $V_{TH}$ ,  $V_{OS}$ , and  $V_{HYST}$ :

- $V_{TH}$  is the actual set voltage or threshold trip voltage.
- $V_{OS}$  is the internal offset voltage between  $V_{IN+}$  and  $V_{IN-}$ . This voltage is added to  $V_{TH}$  to form the actual trip point at which the comparator must respond to change output states.
- $V_{HYST}$  is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

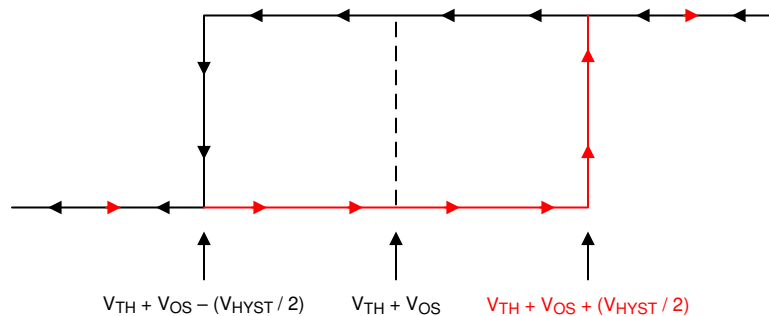


**Figure 8-2. Hysteresis Transfer Curve**

For more information, please see Application Note SBOA219 "[Comparator with and without hysteresis circuit](#)".

#### 8.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage ( $V_+$ ), as shown in [Figure 8-3](#).

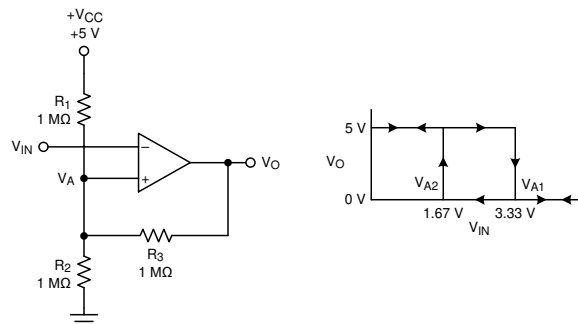


**Figure 8-3. TLV903xin an Inverting Configuration With Hysteresis**

The equivalent resistor networks when the output is high and low are shown in [Figure 8-3](#).

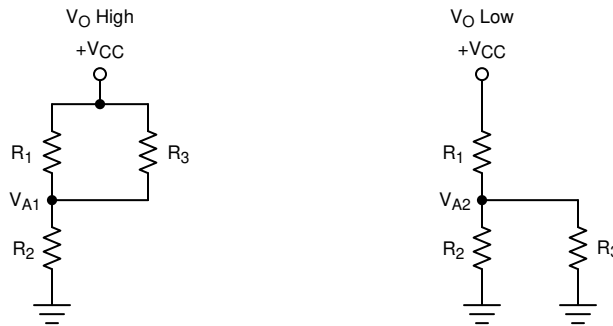


**Figure 8-4. Inverting Configuration Resistor Equivalent Networks**

When  $V_{IN}$  is less than  $V_A$ , the output voltage is high (for simplicity, assume  $V_O$  switches as high as  $V_{CC}$ ). The three network resistors can be represented as  $R1 \parallel R3$  in series with  $R2$ , as shown in [Figure 8-4](#).

[Equation 1](#) below defines the high-to-low trip voltage ( $V_{A1}$ ).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \quad (1)$$

When  $V_{IN}$  is greater than  $V_A$ , the output voltage is low. In this case, the three network resistors can be presented as  $R2 \parallel R3$  in series with  $R1$ , as shown in [Equation 2](#).

Use [Equation 2](#) to define the low to high trip voltage ( $V_{A2}$ ).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \quad (2)$$

[Equation 3](#) defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \quad (3)$$

### 8.1.2.2 Non-Inverting Comparator With Hysteresis

A noninverting comparator with hysteresis requires a two-resistor network and a voltage reference ( $V_{REF}$ ) at the inverting input, as shown in [Figure 8-5](#),

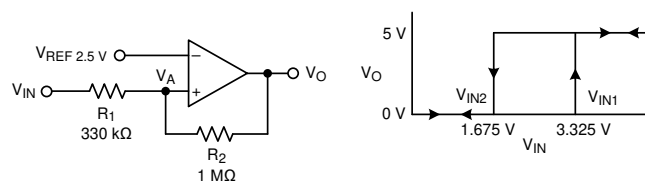


**Figure 8-5. TLV903x in a Non-Inverting Configuration With Hysteresis**

The equivalent resistor networks when the output is high and low are shown in [Figure 8-6](#).

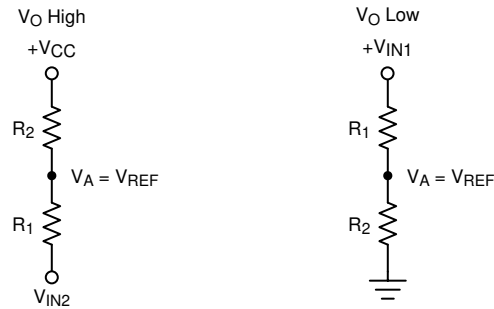


**Figure 8-6. Non-Inverting Configuration Resistor Networks**

When  $V_{IN}$  is less than  $V_{REF}$ , the output is low. For the output to switch from low to high,  $V_{IN}$  must rise above the  $V_{IN1}$  threshold. Use Equation 4 to calculate  $V_{IN1}$ .

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \quad (4)$$

When  $V_{IN}$  is greater than  $V_{REF}$ , the output is high. For the comparator to switch back to a low state,  $V_{IN}$  must drop below  $V_{IN2}$ . Use Equation 5 to calculate  $V_{IN2}$ .

$$V_{IN2} = \frac{V_{REF} (R1 + R2) - V_{CC} \times R1}{R2} \quad (5)$$

The hysteresis of this circuit is the difference between  $V_{IN1}$  and  $V_{IN2}$ , as shown in Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \quad (6)$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

### 8.1.2.3 Inverting and Non-Inverting Hysteresis using Open-Drain Output

It is also possible to use an open drain output device, such as the TLV902x, but the output pull-up resistor must also be taken into account in the calculations. The pull-up resistor is seen in series with the feedback resistor when the output is high. Thus, the feedback resistor is actually seen as  $R2 + R_{PULLUP}$ . TI recommends that the pull-up resistor be at least 10 times less than the feedback resistor value.

## 8.2 Typical Applications

### 8.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. Figure 8-7 shows a simple window comparator circuit. Window comparators require open drain outputs (TLV902x) if the outputs are directly connected together.

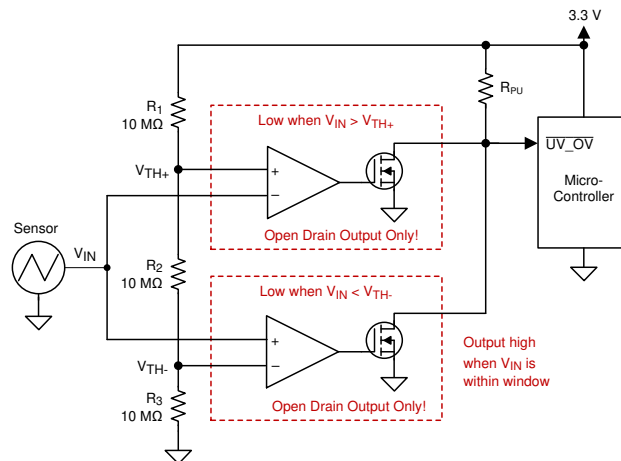


**Figure 8-7. Window Comparator**

### 8.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1 V
- Alert (logic low output) when an input signal is greater than 2.2 V
- Alert signal is active low
- Operate from a 3.3-V power supply

### 8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in [Figure 8-7](#). Connect  $V_{CC}$  to a 3.3-V power supply and  $V_{EE}$  to ground. Make  $R_1$ ,  $R_2$  and  $R_3$  each 10-M $\Omega$  resistors. These three resistors are used to create the positive and negative thresholds for the window comparator ( $V_{TH+}$  and  $V_{TH-}$ ).

With each resistor being equal,  $V_{TH+}$  is 2.2 V and  $V_{TH-}$  is 1.1 V. Large resistor values such as 10-M $\Omega$  are used to minimize power consumption. The resistor values may be recalculated to provide the desired trip point values.

The sensor output voltage is applied to the inverting and noninverting inputs of the two comparators. Using two open-drain output comparators allows the two comparator outputs to be Wire-OR'ed together.

The respective comparator outputs will be low when the sensor is less than 1.1 V or greater than 2.2 V. The respective comparator outputs will be high when the sensor is in the range of 1.1 V to 2.2 V (within the "window"), as shown in [Figure 8-8](#).

### 8.2.1.3 Application Curve

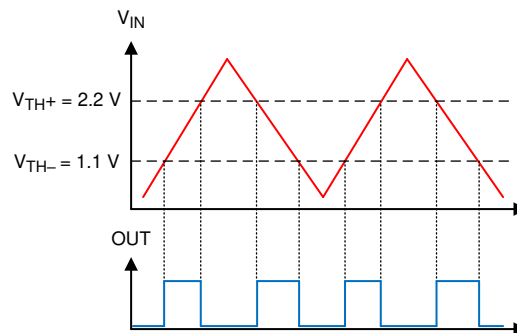


**Figure 8-8. Window Comparator Results**

For more information, please see Application note SBOA221 "[Window comparator circuit](#)".

## 8.2.2 Square-Wave Oscillator

Square-wave oscillator can be used as low cost timing reference or system supervisory clock source. A push-pull output (TLV903x) is recommended for best symmetry.

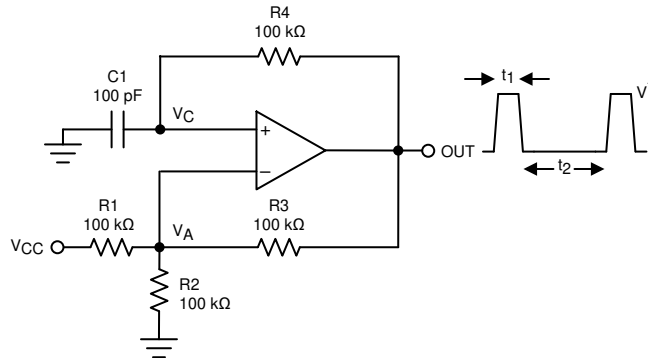


**Figure 8-9. Square-Wave Oscillator**

### 8.2.2.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor  $C_1$  and resistor  $R_4$ . The maximum frequency is limited by propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which may help to reduce BOM cost and board space.  $R_4$  should be over several kilo-ohms to minimize loading the output.

### 8.2.2.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following calculation provides details of the steps.

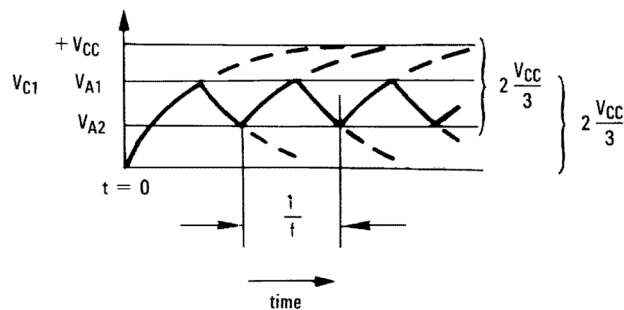


**Figure 8-10. Square-Wave Oscillator Timing Thresholds**

First consider the output of Figure [Figure 8-9](#) as high, which indicates the inverted input  $V_C$  is lower than the noninverting input ( $V_A$ ). This causes the  $C_1$  to be charged through  $R_4$ , and the voltage  $V_C$  increases until it is equal to the noninverting input. The value of  $V_A$  at the point is calculated by [Equation 7](#).

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \parallel R_3} \quad (7)$$

if  $R_1 = R_2 = R_3$ , then  $V_{A1} = 2 V_{CC} / 3$

At this time the comparator output trips pulling down the output to the negative rail. The value of  $V_A$  at this point is calculated by [Equation 8](#).

$$V_{A2} = \frac{V_{CC}(R_2 \parallel R_3)}{R_1 + R_2 \parallel R_3} \quad (8)$$

if  $R_1 = R_2 = R_3$ , then  $V_{A2} = V_{CC}/3$

The  $C_1$  now discharges through the  $R_4$ , and the voltage  $V_{CC}$  decreases until it reaches  $V_{A2}$ . At this point, the output switches back to the starting state. The oscillation period equals to the time duration from for  $C_1$  from  $2V_{CC}/3$  to  $V_{CC}/3$  then back to  $2V_{CC}/3$ , which is given by  $R_4 C_1 \times \ln 2$  for each trip. Therefore, the total time duration is calculated as  $2 R_4 C_1 \times \ln 2$ .

The oscillation frequency can be obtained by Equation 9:

$$f = 1 / (2 R_4 \times C_1 \times \ln 2) \quad (9)$$

### 8.2.2.3 Application Curve

Figure 8-11 shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100 \text{ k}\Omega$
- $C_1 = 100 \text{ pF}$ ,  $C_L = 20 \text{ pF}$
- $V_+ = 5 \text{ V}$ ,  $V_- = \text{GND}$
- $C_{\text{stray}}$  (not shown) from  $V_A$  TO GND =  $10 \text{ pF}$

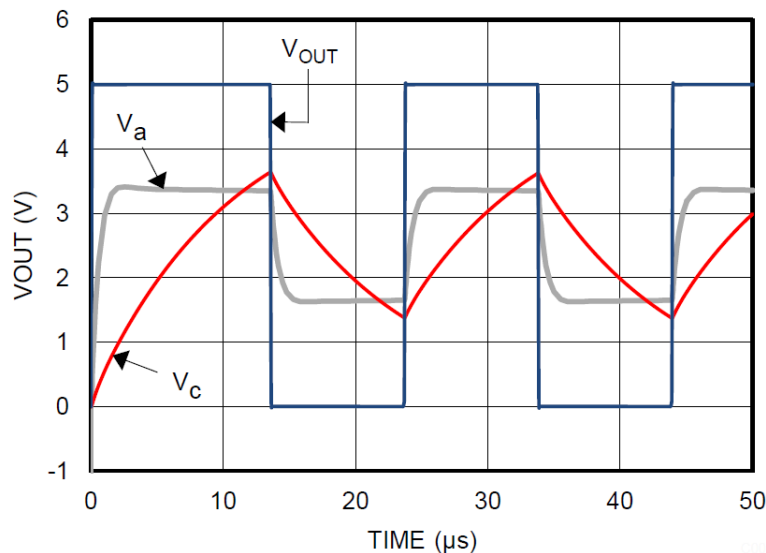


Figure 8-11. Square-Wave Oscillator Output Waveform

### 8.2.3 Adjustable Pulse Width Generator

Figure 8-12 is a variation on the square wave oscillator that allows adjusting the pulse widths.

$R_4$  and  $R_5$  provide separate charge and discharge paths for the capacitor  $C$  depending on the output state.

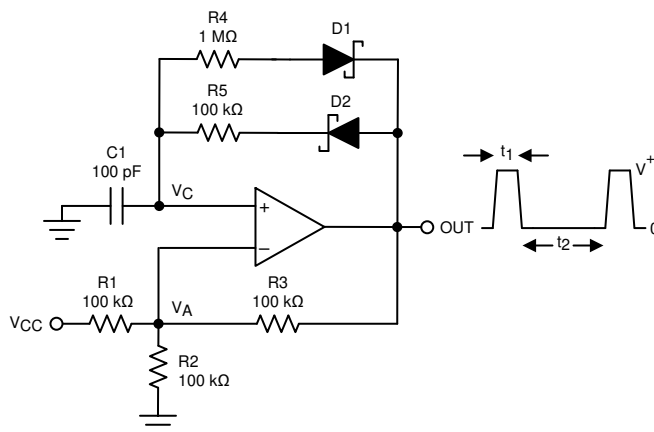


**Figure 8-12. Adjustable Pulse Width Generator**

The charge path is set through  $R_5$  and  $D_2$  when the output is high. Similarly, the discharge path for the capacitor is set by  $R_4$  and  $D_1$  when the output is low.

The pulse width  $t_1$  is determined by the RC time constant of  $R_5$  and  $C$ . Thus, the time  $t_2$  between the pulses can be changed by varying  $R_4$ , and the pulse width can be altered by  $R_5$ . The frequency of the output can be changed by varying both  $R_4$  and  $R_5$ . At low voltages, the effects of the diode forward drop (0.8 V, or 0.15 V for Schottky) must be taken into account by altering output high and low voltages in the calculations.

#### 8.2.4 Time Delay Generator

The circuit shown in [Figure 8-13](#) provides output signals at a prescribed time interval from a time reference and automatically resets the output low when the input returns to 0V. This is useful for sequencing a "power on" signal to trigger a controlled start-up of power supplies.

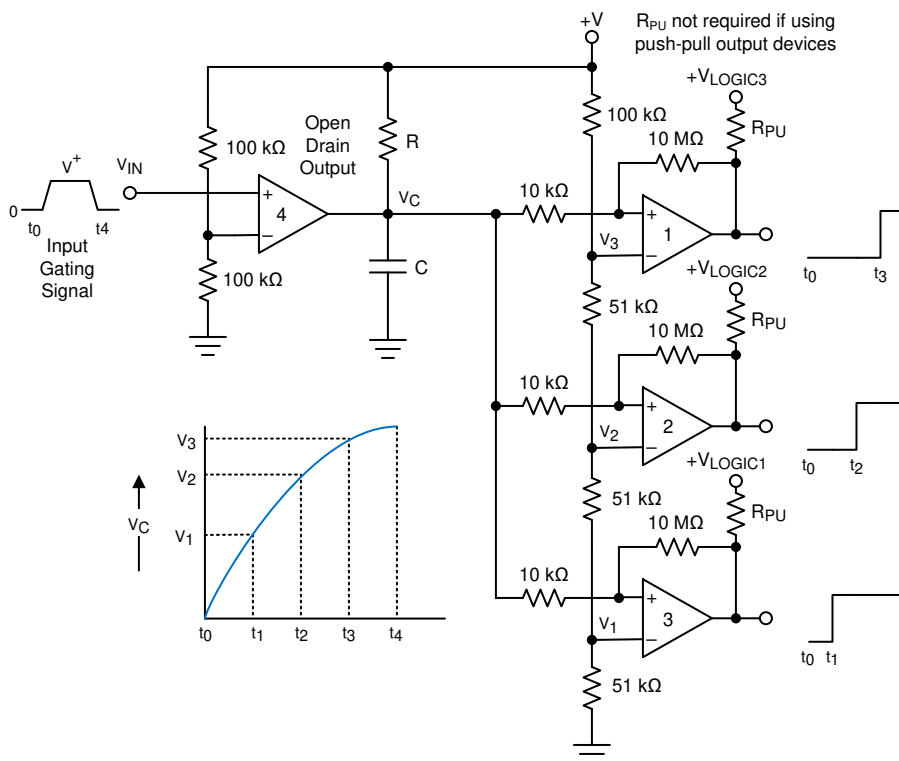


**Figure 8-13. Time Delay Generator**

Consider the case of  $V_{IN} = 0$ . The output of comparator 4 is also at ground, "shorting" the capacitor and holding it at 0V. This implies that the outputs of comparators 1, 2, and 3 are also at 0V. When an input signal is applied, the output of open drain comparator 4 goes High-Z and C charges exponentially through R. This is indicated in the graph. The output voltages of comparators 1, 2, and 3 switch to the high state in sequence when  $V_C$  rises above the reference voltages  $V_1$ ,  $V_2$  and  $V_3$ . A small amount of hysteresis has been provided by the 10 k $\Omega$  and 10 M $\Omega$  resistors to insure fast switching when the RC time constant is chosen to give long delay times. A good starting point is  $R = 100$  k $\Omega$  and  $C = 0.01$   $\mu$ F to 1  $\mu$ F.

All outputs will immediately go low when  $V_{IN}$  falls to 0V, due to the comparator output going low and immediately discharging the capacitor.

Comparator 4 must be a open-drain type output (TLV902x), whereas comparators 1 though 3 may be either open drain or push-pull output, depending on system requirements.  $R_{PU}$  is not required for push-pull output devices.

### 8.2.5 Logic Level Shifter

The output of the TLV902x is the uncommitted drain of the output transistor. Many open-drain outputs can be tied together to provide an output OR'ing function if desired.

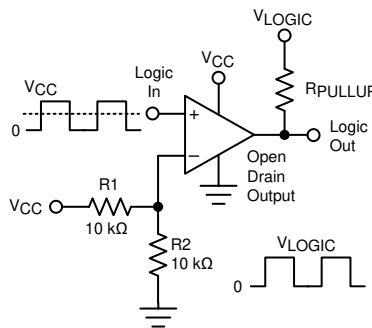


**Figure 8-14. Universal Logic Level Shifter**

The two 10 k $\Omega$  resistors bias the input to half of the input logic supply level to set the threshold in the mid-point of the input logic levels. Only one shared output pull-up resistor is needed and may be connected to any pull-up voltage between 0 V and 5.5 V. The pullup voltage should match the driven logic input "high" level.

### 8.2.6 One-Shot Multivibrator

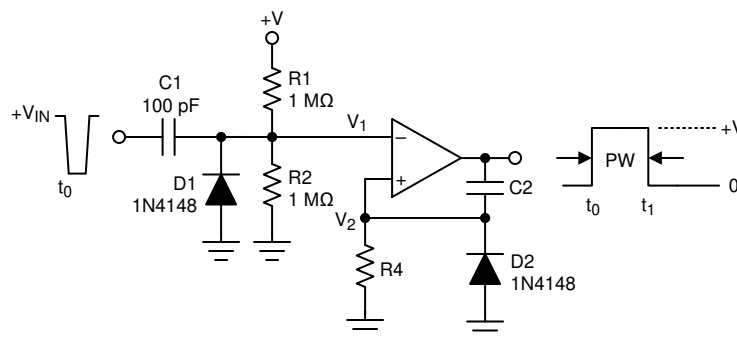


**Figure 8-15. One-Shot Multivibrator**

A monostable multivibrator has one stable state in which it can remain indefinitely. It can be triggered externally to another quasi-stable state. A monostable multivibrator can thus be used to generate a pulse of desired width.

The desired pulse width is set by adjusting the values of  $C_2$  and  $R_4$ . The resistor divider of  $R_1$  and  $R_2$  can be used to determine the magnitude of the input trigger pulse. The output will change state when  $V_1 < V_2$ . Diode  $D_2$  provides a rapid discharge path for capacitor  $C_2$  to reset at the end of the pulse. The diode also prevents the non-inverting input from being driven below ground.

## 8.2.7 Bi-Stable Multivibrator

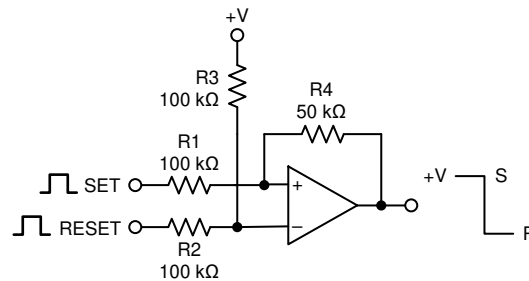


**Figure 8-16. Bi-Stable Multivibrator**

A bi-stable multivibrator has two stable states. The reference voltage is set up by the voltage divider of  $R_2$  and  $R_3$ . A pulse applied to the SET terminal will switch the output of the comparator high. The resistor divider of  $R_1$ ,  $R_4$ , and  $R_5$  now clamps the non-inverting input to a voltage greater than the reference voltage. A pulse applied to RESET will now toggle the output low.

## 8.2.8 Zero Crossing Detector

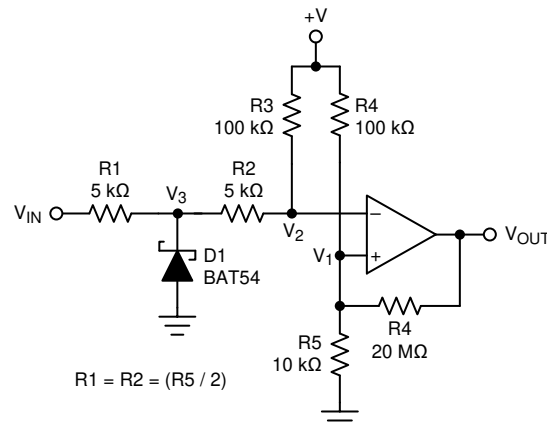


**Figure 8-17. Zero Crossing Detector**

A voltage divider of  $R_4$  and  $R_5$  establishes a reference voltage  $V_1$  at the non-inverting input. By making the series resistance of  $R_1$  and  $R_2$  equal to  $R_5$ , the comparator will switch when  $V_{IN} = 0$ . Diode  $D_1$  insures that  $V_3$  clamps near ground. The voltage divider of  $R_2$  and  $R_3$  then prevents  $V_2$  from going below ground. A small amount of hysteresis is setup to ensure rapid output voltage transitions.

## 8.2.9 Pulse Slicer

A Pulse Slicer is a variation of the Zero Crossing Detector and is used to detect the zero crossings on an input signal with a varying baseline level. This circuit works best with symmetrical waveforms. The RC network of  $R_1$  and  $C_1$  establishes an mean reference voltage  $V_{REF}$ , which tracks the mean amplitude of the  $V_{IN}$  signal. The noninverting input is directly connected to  $V_{REF}$  through  $R_2$ .  $R_2$  and  $R_3$  are used to produce hysteresis to keep transitions free of spurious toggles. The time constant is a tradeoff between long-term symmetry and response time to changes in amplitude.

If the waveform is data, it is recommended that the data be encoded in NRZ (Non-Return to Zero) format to maintain proper average baseline. Asymmetrical inputs may suffer from timing distortions caused by the changing  $V_{REF}$  average voltage.

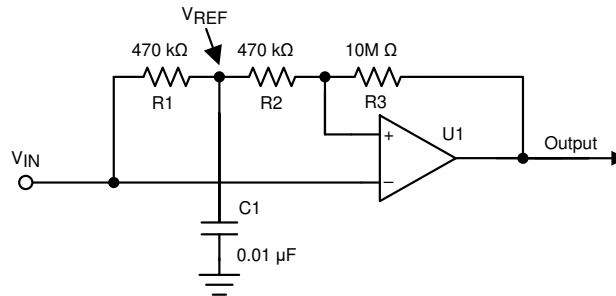


**Figure 8-18. Pulse Slicer using TLV903x**

For this design, follow these design requirements:

- The RC constant value ( $R_2$  and  $C_1$ ) must support the targeted data rate in order to maintain a valid tripping threshold.
- The hysteresis introduced with  $R_2$  and  $R_{43}$  helps to avoid spurious output toggles.

The TLV902x may also be used, but with the addition of a pull-up resistor on the output (not shown for clarity).

Figure 8-19 shows the results of a 9600 baud data signal riding on a varying baseline.

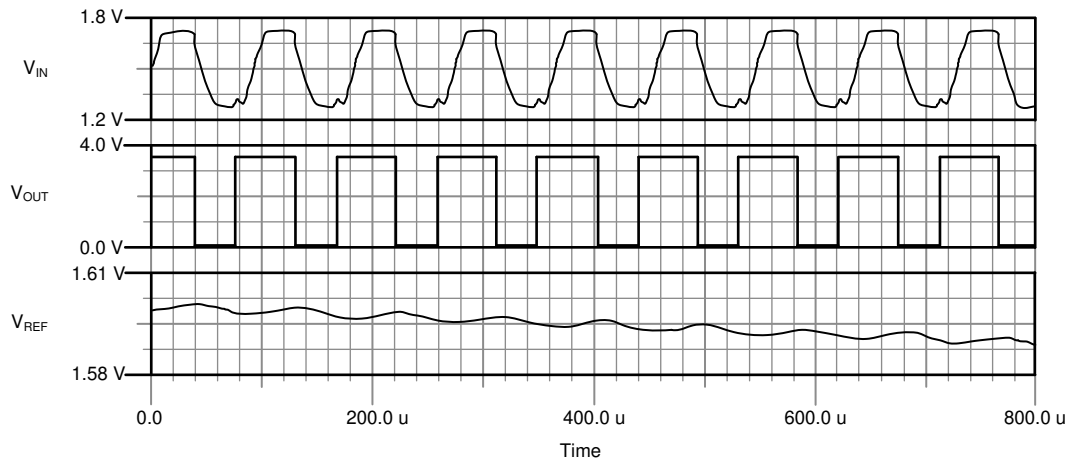


**Figure 8-19. Pulse Slicer Waveforms**

### 8.3 Power Supply Recommendations

Due to the fast output edges, it is critical to have bypass capacitors on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1  $\mu$ F ceramic bypass capacitor directly between  $V_{CC}$  pin and ground pins. Narrow, peak currents will be drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device may be powered from either "split" supplies ( $V+$ ,  $V-$  & GND), or a "single" supply ( $V+$  and GND), with GND applied to the  $V-$  pin.

Input signals must stay within the specified input range (between  $V+$  and  $V-$ ) for either type.

Note that on "split" supplies, the output will now swing "low" ( $V_{OL}$ ) to  $V-$  potential and not GND.

## 9 Layout

### 9.1 Layout Guidelines

For accurate comparator applications it is important maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and should be treated as high speed logic devices. The bypass capacitor should be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the  $V_{CC}$  and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a  $V_{CC}$  or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100 ohms) resistor may also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations should be used when routing long distances.

### 9.2 Layout Example

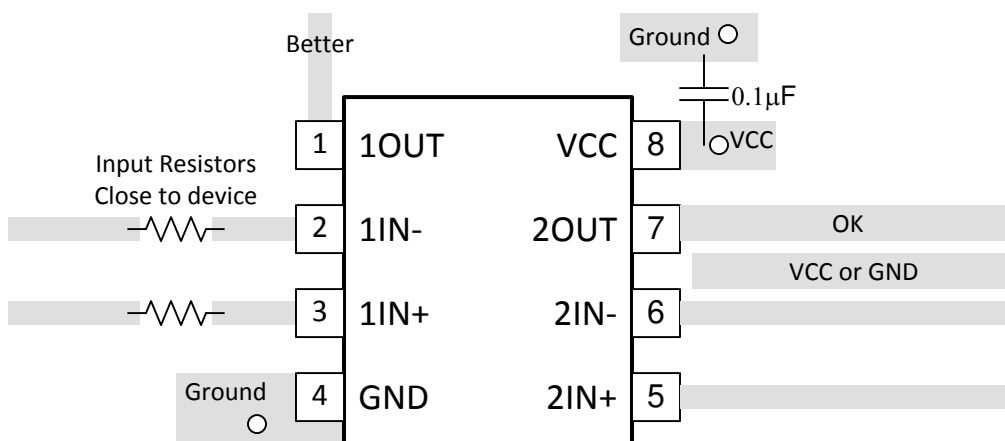


**Figure 9-1. Dual Layout Example**

## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

*Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137*

*Precision Design, Comparator with Hysteresis Reference Design— TIDU020*

*Window comparator circuit - SBOA221*

*Reference Design, Window Comparator Reference Design— TIPD178*

*Comparator with and without hysteresis circuit - SBOA219*

*Inverting comparator with hysteresis circuit - SNOA997*

*Non-Inverting Comparator With Hysteresis Circuit - SBOA313*

*Zero crossing detection using comparator circuit - SNOA999*

*PWM generator circuit - SBOA212*

*How to Implement Comparators for Improving Performance of Rotary Encoder in Industrial Drive Applications - SNOAA41*

*A Quad of Independently Func Comparators - SNOA654*

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV9022DR        | ACTIVE        | SOIC         | D                  | 8    | 2500           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | TL9022                  | <a href="#">Samples</a> |
| TLV9024RTER      | PREVIEW       | WQFN         | RTE                | 16   | 3000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | TL9024                  |                         |
| TLV9032DR        | ACTIVE        | SOIC         | D                  | 8    | 2500           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | TL9032                  | <a href="#">Samples</a> |
| TLV9034RTER      | PREVIEW       | WQFN         | RTE                | 16   | 3000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | TL9034                  |                         |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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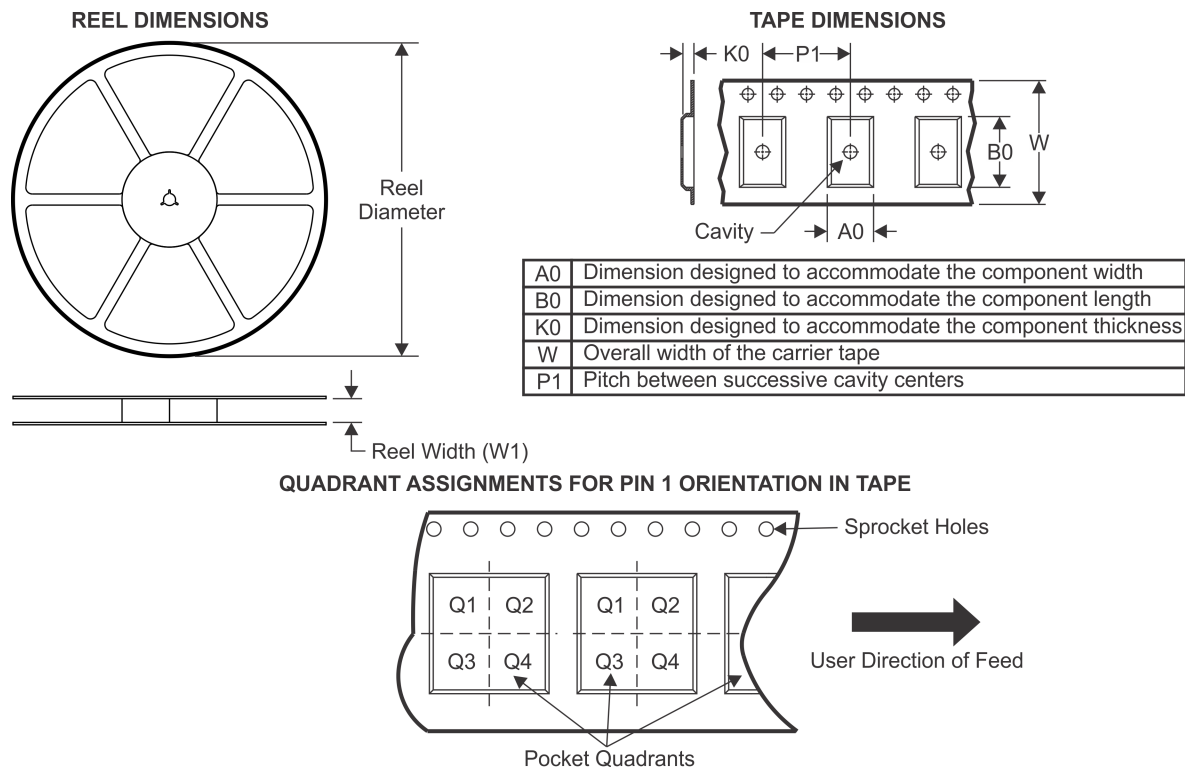
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLV9022, TLV9032 :**

- Automotive: [TLV9022-Q1](#), [TLV9032-Q1](#)

**NOTE: Qualified Version Definitions:**

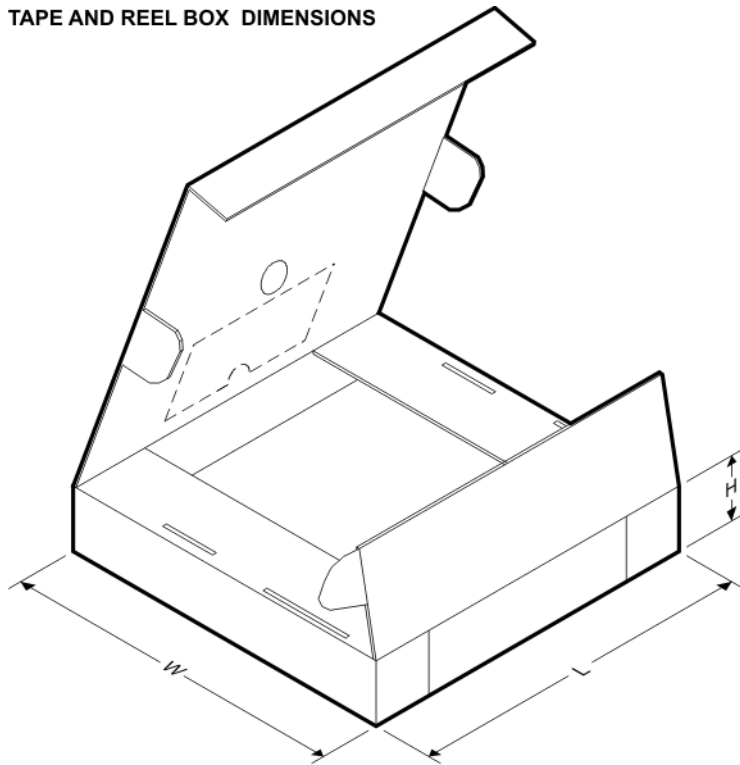
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device    | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV9022DR | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TLV9032DR | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device    | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV9022DR | SOIC         | D               | 8    | 2500 | 853.0       | 449.0      | 35.0        |
| TLV9032DR | SOIC         | D               | 8    | 2500 | 853.0       | 449.0      | 35.0        |



## PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



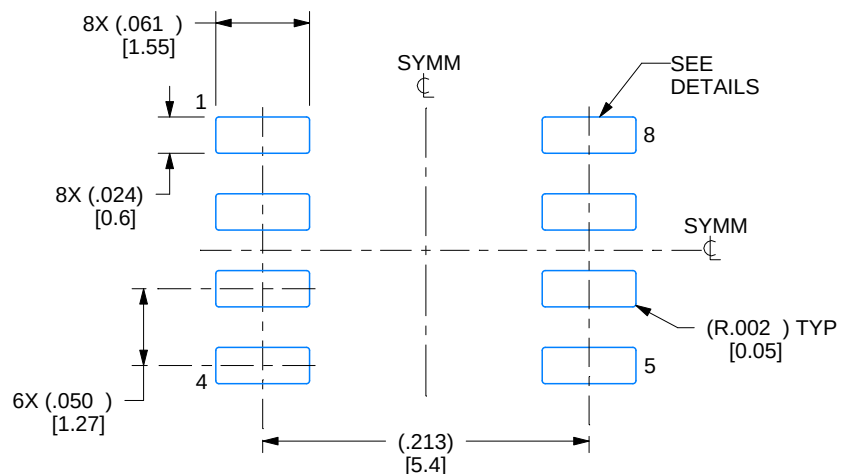
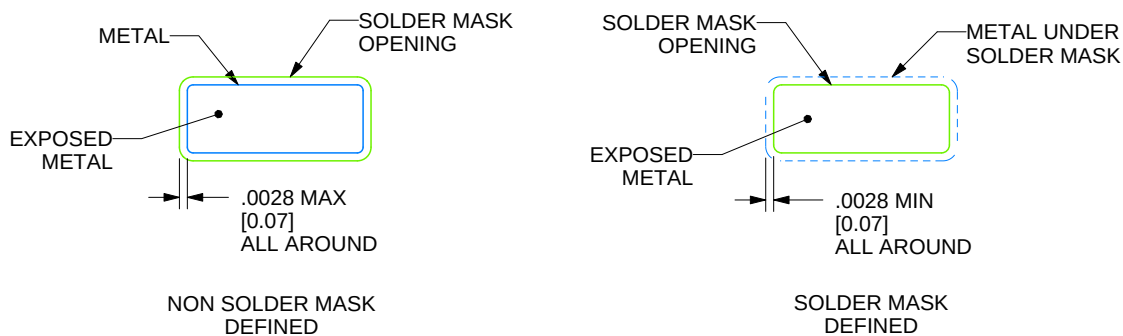
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

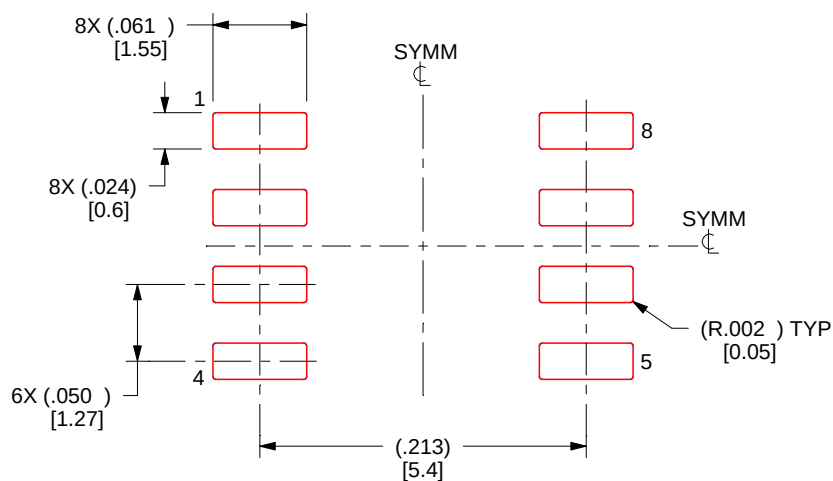
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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