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NTE797
Integrated Circuit
TV Chroma Processor

DISCONTINUED

Features;

- Phase–Locked Subcarrier Regeneration Utilizes Sample–And–Hold Techniques
- Automatic Chrominance Control (ACC)/Killer Detector Employs Sample–And–Hold Techniques
- Supplementary ACC with an Overload Detector to Prevent Oversaturation of this Picture Tube
- Sinusoidal Subcarrier Output
- Keyed Chroma Output
- Emitter–Follower Buffered Outputs for Low Output Impedance
- Linear DC Saturation Control

Absolute Maximum Ratings: (T_A = +25°C unless otherwise specified)

Device Dissipation ($T_A \le$ +55°C) 750mW
  Derate Linearly Above T_A = +55°C . . . . . 7.9mW/°C
DC Supply Voltage (Across Pin5 and Pin12, Note 1) Δ 13.2V
DC Current:
  Into Pin12 . . . . . 38mA
  Into Pin14 . . . . . 20mA
DC Voltage (Pin9)
  Negative Rating . . . . . –5V
  Positive Rating 3V
Operating Ambient Temperature Range, T_A . . . . . –40° to +85°C
Storage Temperature range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 1/32 in (0.79mm) from case, 10sec max.), T_L . . . . . +265°C

Note 1. This rating does not apply when using the internal zener reference in conjunction with an external pass transistor.

Electrical Characteristics: (T_A = +25°C, chroma control at maximum position for all characteristics test except for chroma output test. For this test, control should be set at minimum position.)

Characteristic	Test Measurement & Symbol	Switch S1	Pos. S2	Chroma Input TP1	Min	Typ	Max	Unit
Static Characteristics								
Voltage Regulator	V_{12}	2	2	0	10.1	11.2	12.1	V
Supply Current								
Dynamic Characteristics (Note 2)								
Pull−In Range (Note 3)	V_8	Note 3	2	$0.5V_{p-p}$	±250	−	−	Hz
Oscillator Output	V_8	2	2	0	0.6	1.0	−	V_{p-p}
100% Chroma Output	V_{15}	1	2	$0.5V_{p-p}$	1.4	2.7	−	V_{p-p}
Overload Detector	V_{15}	1	1	$0.5V_{p-p}$	0.4	−	0.7	V_{p-p}
Minimum Chroma Output	V_{15}	1	2	$0.5V_{p-p}$	−	−	20	mV_{p-p}
200% Chroma Output	V_{15}	1	2	$1V_{p-p}$	70	100	140	% of 100%
20% Chroma Output	V_{15}	1	2	$0.1V_{p-p}$	40	−	105	reading
Kill Level	V_{TP1}	1	2	vary	5	−	60	mV_{p-p}

Note 2. Except for pull−in range testing, tune oscillator trimmer capacitor for free−running frequency of 3.579545 MHz ± 10Hz.

Note 3. Set Switch 1 to Position 2, detune oscillator ±250Hz, set Switch to Position 1, and check for oscillator pull−in.

Circuit Description:

The chroma input is applied to Pin1 through the desired band−shaping network. A 2,450−ohm resistor should be placed in series with Pin1 to minimize oscillator pickup in the first chroma amplifier. This amplifier supplies signals to the second chroma amplifier and to the ACC and AFPC detectors. The first chroma amplifier is gain−controlled by the ACC amplifier. A horizontal keying pulse is applied to Pin9. This pulse must be present to ensure proper operation of the oscillator circuit. The subcarrier burst is sampled during the keying interval in the AFPC detector. The error voltage, produced at Pin2 and proportional to the burst phase, is compared to the quiescent bias voltage at Pin3 by the sample−and−hold circuitry. This “compared” voltage controls the phase−shifting network in the phase−locked loop. The operation of the AFPC loop is independent of any external adjustments or voltages except for an initial capacitor adjustment to set the free−running frequency. The regenerated oscillator signal at Pin8 is applied internally to the AFPC and ACC detectors through +45 − and −45 −degree phase−shifter networks to establish the proper phase relationship for these detectors. The ACC detectors, which also samples the burst during the keying interval, produces a correction voltage proportional to the burst amplitude. The correction voltage is compared to the quiescent bias level using sample−and−hold circuitry similar to that used in the AFPC portion of the circuit. The “compared” voltage is applied internally to the ACC amplifier and killer amplifier. Because the amplifier gains and killer threshold are determined by the ratios of the internal resistors, these functions are independent of external voltages or controls.

The attenuated chroma signal is fed to the second chroma amplifier, where the burst is removed by keyer action. The killer amplifier, the chroma gain control, and the overload detector control the action of the second chroma amplifier, whose gain is proportional to the DC voltage at Pin16. The overload detector (Pin13) receives a sample of the chroma output (Pin15) and detects the peak of the signal. The detected voltage is stored in an external capacitor connected to Pin16. This stored voltage on Pin16 affects the gain of the second chroma in the same manner as the chroma gain control.

Pin Connection Diagram



