**Freescale**
Data Sheet: Technical Data

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# MPC5561 Microcontroller Data Sheet

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5561 microcontroller device. For functional characteristics, refer to the *MPC5561 Microcontroller Reference Manual*.

## 1 Overview

The MPC5561 microcontroller (MCU) is a member of the MPC5500 family of microcontrollers built on the Power Architecture® embedded technology. This family of parts has many new features coupled with high performance CMOS technology to provide substantial reduction of cost per feature and significant performance improvement over the MPC500 family.

The host processor core of this device complies with the Power Architecture embedded category that is 100% user-mode compatible (including floating point library) with the original PowerPC instruction set.The embedded architecture enhancements improve the performance in embedded applications. The core also has additional instructions, including digital signal processing (DSP) instructions, beyond the original PowerPC instruction set.

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The MPC5500 family of parts contains many new features coupled with high performance CMOS technology to provide significant performance improvement over the MPC565.

The host processor core of the MPC5561 also includes an instruction set enhancement allowing variable length encoding (VLE). This allows optional encoding of mixed 16- and 32-bit instructions. With this enhancement, it is possible to significantly reduce the code size footprint.

The MPC5561 has two levels of memory hierarchy. The fastest accesses are to the 32-kilobytes (KB) unified cache. The next level in the hierarchy contains the 192-KB on-chip internal SRAM and one megabyte (MB) internal flash memory. The internal SRAM and flash memory hold instructions and data. The external bus interface is designed to support most of the standard memories used with the MPC5*xx* family.

The less complex timer functions of the MPC5561 are performed by the enhanced modular input/output system (eMIOS). The eMIOS' 24 hardware channels are capable of single-action, double-action, pulse-width modulation (PWM), and modulus-counter operations. Motor control capabilities include edge-aligned and center-aligned PWM.

Off-chip communication is performed by a suite of serial protocols including controller area networks (FlexCANs), enhanced deserial/serial peripheral interfaces (DSPIs), and enhanced serial communications interfaces (eSCIs).

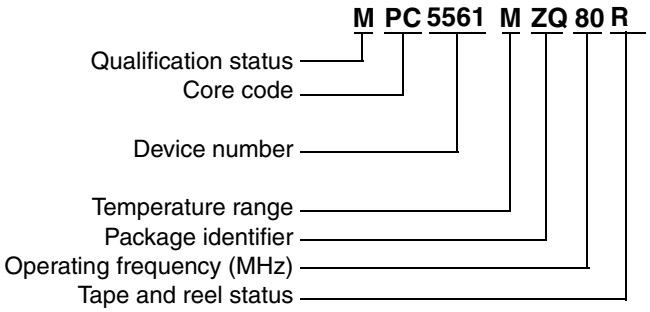
The Parallel Digital Interface (PDI) block provides a glueless interface from the MPC5500 family of devices to high speed external parallel devices such as Analog to Digital Convertors (ADCs) and image sensors. The PDI module, with its internal Direct Memory Access (DMA) engine, moves external parallel data into system memory with minimum intervention from the host processor. The host processor can also read data from the PDI via an interrupt directly.

The MCU has an on-chip enhanced queued dual analog-to-digital converter (eQADC).324 s 40-channels.

The system integration unit (SIU) performs several chip-wide configuration functions. Pad configuration and general-purpose input and output (GPIO) are controlled from the SIU. External interrupts and reset control are also determined by the SIU. The internal multiplexer submodule provides multiplexing of eQADC trigger sources and external interrupt signal multiplexing.

The FlexRay controller provides functional node networking, with static and dynamic host access, to develop highly dependable automotive control systems that require the full implementation of the FlexRay protocol, as published in *FlexRay Protocol Specification 2.0*. The FlexRay module uses fault-tolerant, time-triggered events and clock synchronization mechanisms to maintain the global time of the functional nodes. Bus guardian operations are available for each channel in a multi- or redundant-channel configuration.

# 2 Ordering Information




**Temperature Range**
M = –40° C to 125° C

**Package Identifier**
ZQ = 324PBGA SnPb
VZ = 324PBGA Pb-free

**Operating Frequency**
80 = 80 MHz
112 = 112 MHz
132 = 132 MHz

**Tape and Reel Status**
R = Tape and reel
(blank) = Trays

**Qualification Status**
P = Pre qualification
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

**Note:** Not all options are available on all devices. Refer to Table 1.

**Figure 1. MPC5500 Family Part Number Example**

Unless noted in this data sheet, all specifications apply from $T_L$ to $T_H$.

**Table 1. Orderable Part Numbers**

| Freescale Part Number[1] | Package Description | Speed (MHz) | | Operating Temperature [2] | |
|---|---|---|---|---|---|
| | | Nominal | Max. [3] ($f_{MAX}$) | Min. ($T_L$) | Max. ($T_H$) |
| MPC5561MVZ132 | MPC5561 324 package Lead-free (PbFree) | 132 | 135 | –40° C | 125° C |
| MPC5561MVZ112 | | 112 | 114 | | |
| MPC5561MVZ80 | | 80 | 82 | | |
| MPC5561MZQ132 | MPC5561 324 package Leaded (SnPb) | 132 | 135 | –40° C | 125° C |
| MPC5561MZQ112 | | 112 | 114 | | |
| MPC5561MZQ80 | | 80 | 82 | | |

1 All devices are PPC5561, rather than MPC5561 or SPC5561, until product qualifications are complete. Not all configurations are available in the PPC parts.

2 The lowest ambient operating temperature is referenced by $T_L$; the highest ambient operating temperature is referenced by $T_H$.

3 Speed is the nominal maximum frequency. Max. speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; and 135 MHz parts allow for 132 MHz system clock + 2% FM.

# 3 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MCU.

## 3.1 Maximum Ratings

**Table 2. Absolute Maximum Ratings [1]**

| Spec | Characteristic | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|
| 1 | 1.5 V core supply voltage [2] | $V_{DD}$ | –0.3 | 1.7 | V |
| 2 | Flash program/erase voltage | $V_{PP}$ | –0.3 | 6.5 | V |
| 4 | Flash read voltage | $V_{FLASH}$ | –0.3 | 4.6 | V |
| 5 | SRAM standby voltage | $V_{STBY}$ | –0.3 | 1.7 | V |
| 6 | Clock synthesizer voltage | $V_{DDSYN}$ | –0.3 | 4.6 | V |
| 7 | 3.3 V I/O buffer voltage | $V_{DD33}$ | –0.3 | 4.6 | V |
| 8 | Voltage regulator control input voltage | $V_{RC33}$ | –0.3 | 4.6 | V |
| 9 | Analog supply voltage (reference to $V_{SSA}$) | $V_{DDA}$ | –0.3 | 5.5 | V |
| 10 | I/O supply voltage (fast I/O pads) [3] | $V_{DDE}$ | –0.3 | 4.6 | V |
| 11 | I/O supply voltage (slow and medium I/O pads) [3] | $V_{DDEH}$ | –0.3 | 6.5 | V |
| 12 | DC input voltage [4]<br>$V_{DDEH}$ powered I/O pads<br>$V_{DDE}$ powered I/O pads | $V_{IN}$ | <br>–1.0 [5]<br>–1.0 [5] | <br>6.5 [6]<br>4.6 [7] | V |
| 13 | Analog reference high voltage (reference to $V_{RL}$) | $V_{RH}$ | –0.3 | 5.5 | V |
| 14 | $V_{SS}$ to $V_{SSA}$ differential voltage | $V_{SS} – V_{SSA}$ | –0.1 | 0.1 | V |
| 15 | $V_{DD}$ to $V_{DDA}$ differential voltage | $V_{DD} – V_{DDA}$ | $–V_{DDA}$ | $V_{DD}$ | V |
| 16 | $V_{REF}$ differential voltage | $V_{RH} – V_{RL}$ | –0.3 | 5.5 | V |
| 17 | $V_{RH}$ to $V_{DDA}$ differential voltage | $V_{RH} – V_{DDA}$ | –5.5 | 5.5 | V |
| 18 | $V_{RL}$ to $V_{SSA}$ differential voltage | $V_{RL} – V_{SSA}$ | –0.3 | 0.3 | V |
| 19 | $V_{DDEH}$ to $V_{DDA}$ differential voltage | $V_{DDEH} – V_{DDA}$ | $–V_{DDA}$ | $V_{DDEH}$ | V |
| 20 | $V_{DDF}$ to $V_{DD}$ differential voltage | $V_{DDF} – V_{DD}$ | –0.3 | 0.3 | V |
| 21 | $V_{RC33}$ to $V_{DDSYN}$ differential voltage spec has been moved to Table 9 DC Electrical Specifications, Spec 43a. | | | | |
| 22 | $V_{SSSYN}$ to $V_{SS}$ differential voltage | $V_{SSSYN} – V_{SS}$ | –0.1 | 0.1 | V |
| 23 | $V_{RCVSS}$ to $V_{SS}$ differential voltage | $V_{RCVSS} – V_{SS}$ | –0.1 | 0.1 | V |
| 24 | Maximum DC digital input current [8]<br>(per pin, applies to all digital pins) [4] | $I_{MAXD}$ | –2 | 2 | mA |
| 25 | Maximum DC analog input current [9]<br>(per pin, applies to all analog pins) | $I_{MAXA}$ | –3 | 3 | mA |
| 26 | Maximum operating temperature range [10]<br>Die junction temperature | $T_J$ | $T_L$ | 150.0 | °C |
| 27 | Storage temperature range | $T_{STG}$ | –55.0 | 150.0 | °C |

**Table 2. Absolute Maximum Ratings [1] (continued)**

| Spec | Characteristic | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|
| 28 | Maximum solder temperature [11]<br>Lead free (Pb-free)<br>Leaded (SnPb) | $T_{SDR}$ | —<br>— | 260.0<br>245.0 | °C |
| 29 | Moisture sensitivity level [12] | MSL | — | 3 | |

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond any of the listed maxima can affect device reliability or cause permanent damage to the device.

2 1.5 V ± 10% for proper operation. This parameter is specified at a maximum junction temperature of 150 °C.

3 All functional non-supply I/O pins are clamped to $V_{SS}$ and $V_{DDE}$, or $V_{DDEH}$.

4 AC signal overshoot and undershoot of up to ± 2.0 V of the input voltages is permitted for an accumulative duration of 60 hours over the complete lifetime of the device (injection current not limited for this duration).

5 Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met. Keep the negative DC voltage greater than –0.6 V on SINB during the internal power-on reset (POR) state.

6 Internal structures hold the input voltage less than the maximum voltage on all pads powered by $V_{DDEH}$ supplies, if the maximum injection current specification is met (2 mA for all pins) and $V_{DDEH}$ is within the operating voltage specifications.

7 Internal structures hold the input voltage less than the maximum voltage on all pads powered by $V_{DDE}$ supplies, if the maximum injection current specification is met (2 mA for all pins) and $V_{DDE}$ is within the operating voltage specifications.

8 Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

9 Total injection current for all analog input pins must not exceed 15 mA.

10 Lifetime operation at these specification limits is not guaranteed.

11 Moisture sensitivity profile per IPC/JEDEC J-STD-020D.

12 Moisture sensitivity per JEDEC test method A112.

## 3.2 Thermal Characteristics

The shaded rows in the following table indicate information specific to a four-layer board.

**Table 3. MPC5561 Thermal Characteristics (Preliminary Values)**

| Spec | MPC5561 Thermal Characteristic | Symbol | 324 PBGA | Unit |
|---|---|---|---|---|
| 1 | Junction to ambient [1, 2], natural convection (one-layer board) | $R_{\theta JA}$ | 29 | °C/W |
| 2 | Junction to ambient [1, 3], natural convection (four-layer board 2s2p) | $R_{\theta JA}$ | 19 | °C/W |
| 3 | Junction to ambient (@200 ft./min., one-layer board) | $R_{\theta JMA}$ | 22 | °C/W |
| 4 | Junction to ambient (@200 ft./min., four-layer board 2s2p) | $R_{\theta JMA}$ | 16 | °C/W |
| 5 | Junction to board (four-layer board 2s2p) [4] | $R_{\theta JB}$ | 10 | °C/W |
| 6 | Junction to case [5] | $R_{\theta JC}$ | 7 | °C/W |
| 7 | Junction to package top, natural convection [6] | $\Psi_{JT}$ | 2 | °C/W |

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

### 3.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the device junction temperature, $T_J$, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

$T_A$ = ambient temperature for the package ($^oC$)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

$P_D$ = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 $W/cm^2$

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$T_J$ = junction temperature ($^oC$)

$T_B$ = board temperature at the package perimeter ($^oC/W$)

$R_{\theta JB}$ = junction-to-board thermal resistance ($^oC/W$) per JESD51-8

$P_D$ = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction-to-case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case-to-ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter ($\Psi_{JT}$) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$T_T$ = thermocouple temperature on top of the package ($^oC$)

$\Psi_{JT}$ = thermal characterization parameter ($^oC/W$)

$P_D$ = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

### References:

Semiconductor Equipment and Materials International
3081 Zanker Rd.
San Jose, CA., 95134
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the web at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

## 3.3 Package

The MPC5561 is available in packaged form. Read the package options in Section 2, “Ordering Information.” Refer to Section 4, “Mechanicals,” for pinouts and package drawings.

## 3.4 EMI (Electromagnetic Interference) Characteristics

**Table 4. EMI Testing Specifications [1]**

| Spec | Characteristic | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| 1 | Scan range | 0.15 | — | 1000 | MHz |
| 2 | Operating frequency | — | — | $f_{MAX}$ | MHz |
| 3 | $V_{DD}$ operating voltages | — | 1.5 | — | V |
| 4 | $V_{DDSYN}$, $V_{RC33}$, $V_{DD33}$, $V_{FLASH}$, $V_{DDE}$ operating voltages | — | 3.3 | — | V |
| 5 | $V_{PP}$, $V_{DDEH}$, $V_{DDA}$ operating voltages | — | 5.0 | — | V |
| 6 | Maximum amplitude | — | — | 14 [2]<br>32 [3] | dBuV |
| 7 | Operating temperature | — | — | 25 | °C |

1 EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03. Qualification testing was performed on the MPC5554 and applied to the MPC5500 family as generic EMI performance data.

2 Measured with the single-chip EMI program.

3 Measured with the expanded EMI program.

## 3.5 ESD (Electromagnetic Static Discharge) Characteristics

**Table 5. ESD Ratings [1, 2]**

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| ESD for human body model (HBM) | | 2000 | V |
| HBM circuit description | R1 | 1500 | Ω |
| | C | 100 | pF |
| ESD for field induced charge model (FDCM) | | 500 (all pins)<br>750 (corner pins) | V |
| Number of pulses per pin:<br>Positive pulses (HBM)<br>Negative pulses (HBM) | <br>—<br>— | <br>1<br>1 | <br>—<br>— |
| Interval of pulses | — | 1 | second |

1 All ESD testing conforms to CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 Device failure is defined as: 'If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature.

## 3.6 Voltage Regulator Controller ($V_{RC}$) and Power-On Reset (POR) Electrical Specifications

The following table lists the $V_{RC}$ and POR electrical specifications:

**Table 6. $V_{RC}$ and POR Electrical Specifications**

| Spec | Characteristic | | Symbol | Min. | Max. | Units |
|---|---|---|---|---|---|---|
| 1 | 1.5 V ($V_{DD}$) POR [1] | Negated (ramp up)<br>Asserted (ramp down) | $V_{POR15}$ | 1.1<br>1.1 | 1.35<br>1.35 | V |
| 2 | 3.3 V ($V_{DDSYN}$) POR [1] | Asserted (ramp up)<br>Negated (ramp up)<br>Asserted (ramp down)<br>Negated (ramp down) | $V_{POR33}$ | 0.0<br>2.0<br>2.0<br>0.0 | 0.30<br>2.85<br>2.85<br>0.30 | V |
| 3 | $\overline{\text{RESET}}$ pin supply ($V_{DDEH6}$) POR [1, 2] | Negated (ramp up)<br>Asserted (ramp down) | $V_{POR5}$ | 2.0<br>2.0 | 2.85<br>2.85 | V |
| 4 | $V_{RC33}$ voltage | Before $V_{RC}$ allows the pass transistor to start turning on | $V_{TRANS_START}$ | 1.0 | 2.0 | V |
| 5 | | When $V_{RC}$ allows the pass transistor to completely turn on [3, 4] | $V_{TRANS_ON}$ | 2.0 | 2.85 | V |
| 6 | | When the voltage is greater than the voltage at which the $V_{RC}$ keeps the 1.5 V supply in regulation [5, 6] | $V_{VRC33REG}$ | 3.0 | — | V |
| 7 | Current can be sourced by $V_{RCCTL}$ at Tj: | –40° C<br>25° C<br>150° C | $I_{VRCCTL}$ [7] | 11.0<br>9.0<br>7.5 | —<br>—<br>— | mA<br>mA<br>mA |
| 8 | Voltage differential during power up such that: $V_{DD33}$ can lag $V_{DDSYN}$ or $V_{DDEH6}$ before $V_{DDSYN}$ and $V_{DDEH6}$ reach the $V_{POR33}$ and $V_{POR5}$ minimums respectively. | | $V_{DD33_LAG}$ | — | 1.0 | V |

**Table 6. $V_{RC}$ and POR Electrical Specifications (continued)**

| Spec | Characteristic | | Symbol | Min. | Max. | Units |
|---|---|---|---|---|---|---|
| 9 | Absolute value of slew rate on power supply pins | | — | — | 50 | V/ms |
| 10 | Required gain at Tj: $I_{DD} \div I_{VRCCTL}$ (@ $f_{sys} = f_{MAX}$) 6, 7, 8, 9 | – 40° C | BETA[10] | 60 | — | — |
| | | 25° C | | 65 | — | — |
| | | 150° C | | 85 | 500 | — |

1 The internal POR signals are $V_{POR15}$, $V_{POR33}$, and $V_{POR5}$. On power up, assert $\overline{\text{RESET}}$ before the internal POR negates. $\overline{\text{RESET}}$ must remain asserted until the power supplies are within the operating conditions as specified in Table 9 DC Electrical Specifications. On power down, assert $\overline{\text{RESET}}$ before any power supplies fall outside the operating conditions and until the internal POR asserts.

2 $V_{IL_S}$ (Table 9, Spec15) is guaranteed to scale with $V_{DDEH6}$ down to $V_{POR5}$.

3 Supply full operating current for the 1.5 V supply when the 3.3 V supply reaches this range.

4 It is possible to reach the current limit during ramp up—do not treat this event as short circuit current.

5 At peak current for device.

6 Requires compliance with Freescale's recommended board requirements and transistor recommendations. Board signal traces/routing from the $V_{RCCTL}$ package signal to the base of the external pass transistor and between the emitter of the pass transistor to the $V_{DD}$ package signals must have a maximum of 100 nH inductance and minimal resistance (less than 1 Ω). $V_{RCCTL}$ must have a nominal 1 μF phase compensation capacitor to ground. $V_{DD}$ must have a 20 μF (nominal) bulk capacitor (greater than 4 μF over all conditions, including lifetime). Place high-frequency bypass capacitors consisting of eight 0.01 μF, two 0.1 μF, and one 1 μF capacitors around the package on the $V_{DD}$ supply signals.

7 $I_{VRCCTL}$ is measured at the following conditions: $V_{DD}$ = 1.35 V, $V_{RC33}$ = 3.1 V, $V_{VRCCTL}$ = 2.2 V.

8 Refer to Table 1 for the maximum operating frequency.

9 Values are based on $I_{DD}$ from high-use applications as explained in the $I_{DD}$ Electrical Specification.

10 Represents the worst-case external transistor BETA. It is measured on a per-part basis and calculated as ($I_{DD} \div I_{VRCCTL}$).

## 3.7 Power-Up/Down Sequencing

Power sequencing between the 1.5 V power supply and $V_{DDSYN}$ or the $\overline{\text{RESET}}$ power supplies is required if using an external 1.5 V power supply with $V_{RC33}$ tied to ground (GND). To avoid power-sequencing, $V_{RC33}$ must be powered up within the specified operating range, even if the on-chip voltage regulator controller is not used. Refer to Section 3.7.2, "Power-Up Sequence (VRC33 Grounded)," and Section 3.7.3, "Power-Down Sequence (VRC33 Grounded)."

Power sequencing requires that $V_{DD33}$ must reach a certain voltage where the values are read as ones before the POR signal negates. Refer to Section 3.7.1, "Input Value of Pins During POR Dependent on VDD33."

Although power sequencing is not required between $V_{RC33}$ and $V_{DDSYN}$ during power up, $V_{RC33}$ must not lead $V_{DDSYN}$ by more than 600 mV or lag by more than 100 mV for the $V_{RC}$ stage turn-on to operate within specification. Higher spikes in the emitter current of the pass transistor occur if $V_{RC33}$ leads or lags $V_{DDSYN}$ by more than these amounts. The value of that higher spike in current depends on the board power supply circuitry and the amount of board level capacitance.

Furthermore, when all of the PORs negate, the system clock starts to toggle, adding another large increase of the current consumed by $V_{RC33}$. If $V_{RC33}$ lags $V_{DDSYN}$ by more than 100 mV, the increase in current consumed can drop $V_{DD}$ low enough to assert the 1.5 V POR again. Oscillations are possible when the

1.5 V POR asserts and stops the system clock, causing the voltage on $V_{DD}$ to rise until the 1.5 V POR negates again. All oscillations stop when $V_{RC33}$ is powered sufficiently.

When powering down, $V_{RC33}$ and $V_{DDSYN}$ have no delta requirement to each other, because the bypass capacitors internal and external to the device are already charged. When not powering up or down, no delta between $V_{RC33}$ and $V_{DDSYN}$ is required for the $V_{RC}$ to operate within specification.

There are no power up/down sequencing requirements to prevent issues such as latch-up, excessive current spikes, and so on. Therefore, the state of the I/O pins during power up and power down varies depending on which supplies are powered.

Table 7 gives the pin state for the sequence cases for all pins with pad type pad_fc (fast type).

**Table 7. Pin Status for Fast Pads During the Power Sequence**

| $V_{DDE}$ | $V_{DD33}$ | $V_{DD}$ | POR | Pin Status for Fast Pad Output Driver pad_fc (fast) |
|---|---|---|---|---|
| Low | — | — | Asserted | Low |
| $V_{DDE}$ | Low | Low | Asserted | High |
| $V_{DDE}$ | Low | $V_{DD}$ | Asserted | High |
| $V_{DDE}$ | $V_{DD33}$ | Low | Asserted | High impedance (Hi-Z) |
| $V_{DDE}$ | $V_{DD33}$ | $V_{DD}$ | Asserted | Hi-Z |
| $V_{DDE}$ | $V_{DD33}$ | $V_{DD}$ | Negated | Functional |

Table 8 gives the pin state for the sequence cases for all pins with pad type pad_mh (medium type) and pad_sh (slow type).

**Table 8. Pin Status for Medium and Slow Pads During the Power Sequence**

| $V_{DDEH}$ | $V_{DD}$ | POR | Pin Status for Medium and Slow Pad Output Driver pad_mh (medium) pad_sh (slow) |
|---|---|---|---|
| Low | — | Asserted | Low |
| $V_{DDEH}$ | Low | Asserted | High impedance (Hi-Z) |
| $V_{DDEH}$ | $V_{DD}$ | Asserted | Hi-Z |
| $V_{DDEH}$ | $V_{DD}$ | Negated | Functional |

The values in Table 7 and Table 8 do not include the effect of the weak-pull devices on the output pins during power up.

Before exiting the internal POR state, the voltage on the pins go to a high-impedance state until POR negates. When the internal POR negates, the functional state of the signal during reset applies and the weak-pull devices
(up or down) are enabled as defined in the device reference manual. If $V_{DD}$ is too low to correctly propagate the logic signals, the weak-pull devices can pull the signals to $V_{DDE}$ and $V_{DDEH}$.

To avoid this condition, minimize the ramp time of the $V_{DD}$ supply to a time period less than the time required to enable the external circuitry connected to the device outputs.

During initial power ramp-up, when $V_{stby}$ is 0.6v or above. a typical current of 1-3mA and maximum of 4mA may be seen until $V_{DD}$ is applied. This current will not reoccur until $V_{stby}$ is lowered below $V_{stby}$ min. specification.

Figure 2 shows an approximate interpolation of the $I_{STBY}$ worst-case specification to estimate values at different voltages and temperatures. The vertical lines shown at 25 °C, 60 °C, and 150 °C in Figure 2 are the actual $I_{DD_STBY}$ specifications (27d) listed in Table 9.

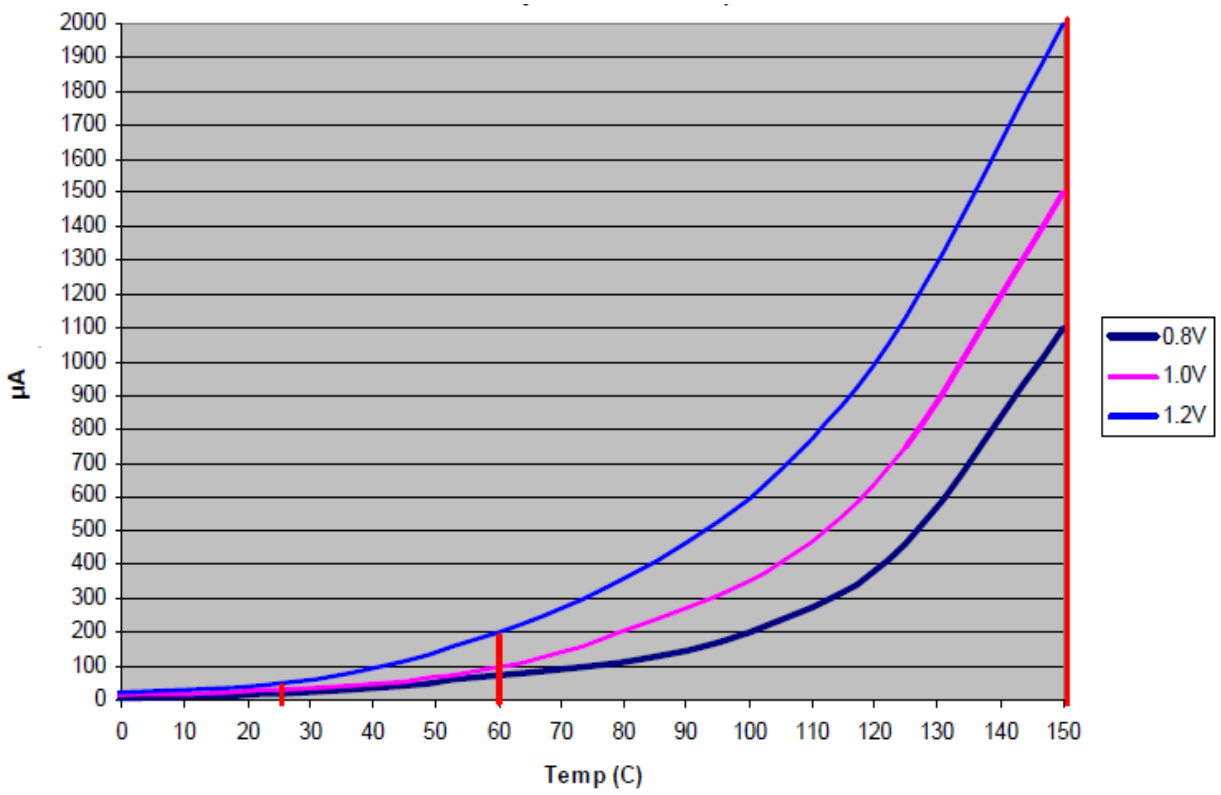



**Figure 2. $fI_{STBY}$ Worst-case Specifications**

### 3.7.1 Input Value of Pins During POR Dependent on $V_{DD33}$

When powering up the device, $V_{DD33}$ must not lag the latest $V_{DDSYN}$ *or* $\overline{\text{RESET}}$ power pin ($V_{DDEH6}$) by more than the $V_{DD33}$ lag specification listed in Table 6, spec 8. This avoids accidentally selecting the bypass clock mode because the internal versions of PLLCFG[0:1] and $\overline{\text{RSTCFG}}$ are not powered and therefore cannot read the default state when POR negates. $V_{DD33}$ can lag $V_{DDSYN}$ *or* the $\overline{\text{RESET}}$ power pin ($V_{DDEH6}$), but cannot lag both by more than the $V_{DD33}$ lag specification. This $V_{DD33}$ lag specification applies during power up only. $V_{DD33}$ has no lead or lag requirements when powering down.

### 3.7.2 Power-Up Sequence ($V_{RC33}$ Grounded)

The 1.5 V $V_{DD}$ power supply must rise to 1.35 V before the 3.3 V $V_{DDSYN}$ power supply and the $\overline{\text{RESET}}$ power supply rises above 2.0 V. This ensures that digital logic in the PLL for the 1.5 V power supply does not begin to operate below the specified operation range lower limit of 1.35 V. Because the internal 1.5 V POR is disabled, the internal 3.3 V POR or the $\overline{\text{RESET}}$ power POR must hold the device in reset. Since they can negate as low as 2.0 V, $V_{DD}$ must be within specification before the 3.3 V POR and the $\overline{\text{RESET}}$ POR negate.

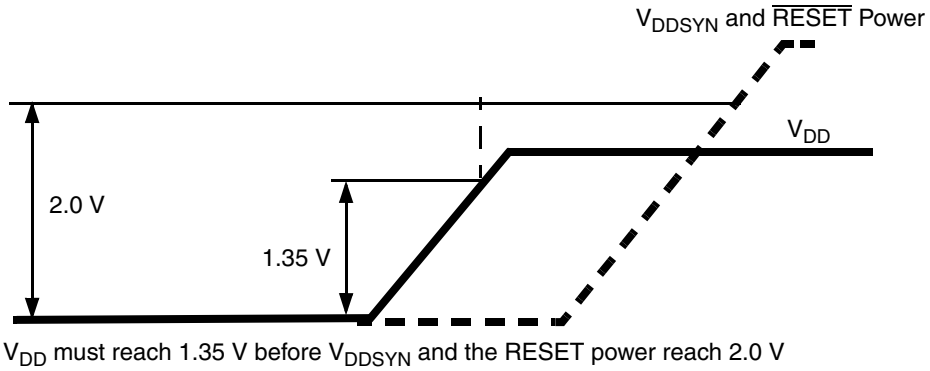



**Figure 3. Power-Up Sequence ($V_{RC33}$ Grounded)**

### 3.7.3 Power-Down Sequence ($V_{RC33}$ Grounded)

The only requirement for the power-down sequence with $V_{RC33}$ grounded is if $V_{DD}$ decreases to less than its operating range, $V_{DDSYN}$ or the $\overline{\text{RESET}}$ power must decrease to less than 2.0 V before the $V_{DD}$ power increases to its operating range. This ensures that the digital 1.5 V logic, which is reset only by an ORed POR and can cause the 1.5 V supply to decrease less than its specification value, resets correctly. See Table 6, footnote 1.

## 3.8 DC Electrical Specifications

**Table 9. DC Electrical Specifications ($T_A = T_L$ to $T_H$)**

| Spec | Characteristic | Symbol | Min | Max. | Unit |
|---|---|---|---|---|---|
| 1 | Core supply voltage (average DC RMS voltage) | $V_{DD}$ | 1.35 | 1.65 | V |
| 2 | Input/output supply voltage (fast input/output) [1] | $V_{DDE}$ | 1.62 | 3.6 | V |
| 3 | Input/output supply voltage (slow and medium input/output) | $V_{DDEH}$ | 3.0 | 5.25 | V |
| 4 | 3.3 V input/output buffer voltage | $V_{DD33}$ | 3.0 | 3.6 | V |
| 5 | Voltage regulator control input voltage | $V_{RC33}$ | 3.0 | 3.6 | V |
| 6 | Analog supply voltage [2] | $V_{DDA}$ | 4.5 | 5.25 | V |
| 8 | Flash programming voltage [3] | $V_{PP}$ | 4.5 | 5.25 | V |
| 9 | Flash read voltage | $V_{FLASH}$ | 3.0 | 3.6 | V |
| 10 | SRAM standby voltage [4] | $V_{STBY}$ | 0.8 | 1.2 | V |
| 11 | Clock synthesizer operating voltage | $V_{DDSYN}$ | 3.0 | 3.6 | V |
| 12 | Fast I/O input high voltage | $V_{IH_F}$ | $0.65 \times V_{DDE}$ | $V_{DDE} + 0.3$ | V |
| 13 | Fast I/O input low voltage | $V_{IL_F}$ | $V_{SS} - 0.3$ | $0.35 \times V_{DDE}$ | V |
| 14 | Medium and slow I/O input high voltage | $V_{IH_S}$ | $0.65 \times V_{DDEH}$ | $V_{DDEH} + 0.3$ | V |
| 15 | Medium and slow I/O input low voltage | $V_{IL_S}$ | $V_{SS} - 0.3$ | $0.35 \times V_{DDEH}$ | V |
| 16 | Fast input hysteresis | $V_{HYS_F}$ | $0.1 \times V_{DDE}$ | | V |
| 17 | Medium and slow I/O input hysteresis | $V_{HYS_S}$ | $0.1 \times V_{DDEH}$ | | V |
| 18 | Analog input voltage | $V_{INDC}$ | $V_{SSA} - 0.3$ | $V_{DDA} + 0.3$ | V |
| 19 | Fast output high voltage ($I_{OH_F}$ = –2.0 mA) | $V_{OH_F}$ | $0.8 \times V_{DDE}$ | — | V |
| 20 | Slow and medium output high voltage<br>$I_{OH_S}$ = –2.0 mA<br>$I_{OH_S}$ = –1.0 mA | $V_{OH_S}$ | $0.80 \times V_{DDEH}$<br>$0.85 \times V_{DDEH}$ | — | V |
| 21 | Fast output low voltage ($I_{OL_F}$ = 2.0 mA) | $V_{OL_F}$ | — | $0.2 \times V_{DDE}$ | V |
| 22 | Slow and medium output low voltage<br>$I_{OL_S}$ = 2.0 mA<br>$I_{OL_S}$ = 1.0 mA | $V_{OL_S}$ | — | <br>$0.20 \times V_{DDEH}$<br>$0.15 \times V_{DDEH}$ | V |
| 23 | Load capacitance (fast I/O) [5]<br>DSC (SIU_PCR[8:9]) = 0b00<br>= 0b01<br>= 0b10<br>= 0b11 | $C_L$ | <br>—<br>—<br>—<br>— | <br>10<br>20<br>30<br>50 | <br>pF<br>pF<br>pF<br>pF |
| 24 | Input capacitance (digital pins) | $C_{IN}$ | — | 7 | pF |
| 25 | Input capacitance (analog pins) | $C_{IN_A}$ | — | 10 | pF |
| 26 | Input capacitance:<br>(Shared digital and analog pins AN[12]_MA[0]_$\overline{SDS}$, AN[13]_MA[1]_SDO, AN[14]_MA[2]_SDI, and AN[15]_FCK) | $C_{IN_M}$ | — | 12 | pF |

**Table 9. DC Electrical Specifications ($T_A = T_L$ to $T_H$) (continued)**

| Spec | Characteristic | Symbol | Min | Max. | Unit |
|---|---|---|---|---|---|
| 27a | Operating current 1.5 V supplies @ 135 MHz: [6]<br>8-way cache [7]<br>$V_{DD}$ (including $V_{DDF}$ max current) @1.65 V typical use [8, 9]<br>$V_{DD}$ (including $V_{DDF}$ max current) @1.35 V typical use [8, 9]<br>$V_{DD}$ (including $V_{DDF}$ max current) @1.65 V high use [9, 10]<br>$V_{DD}$ (including $V_{DDF}$ max current) @1.35 V high use [9, 10]<br>4-way cache [11]<br>$V_{DD}$ (including $V_{DDF}$ max current) @1.65 V high use [9, 10]<br>$V_{DD}$ (including $V_{DDF}$ max current) @1.35 V high use [9, 10] | <br><br>$I_{DD}$<br>$I_{DD}$<br>$I_{DD}$<br>$I_{DD}$<br><br>$I_{DD}$<br>$I_{DD}$ | <br><br>—<br>—<br>—<br>—<br><br>—<br>— | <br><br>620<br>440<br>670<br>490<br><br>610<br>430 | <br><br>mA<br>mA<br>mA<br>mA<br><br>mA<br>mA |
| 27b | Operating current 1.5 V supplies @ 114 MHz: [6]<br>8-way cache [7]<br>$V_{DD}$ (including $V_{DDF}$ max current) @1.65 V typical use [8, 9]<br>$V_{DD}$ (including $V_{DDF}$ max current) @1.35 V typical use [8, 9]<br>$V_{DD}$ (including $V_{DDF}$ max current) @1.65 V high use [9, 10]<br>$V_{DD}$ (including $V_{DDF}$ max current) @1.35 V high use [9, 10]<br>4-way cache [11]<br>$V_{DD}$ (including $V_{DDF}$ max current) @1.65 V high use [9, 10]<br>$V_{DD}$ (including $V_{DDF}$ max current) @1.35 V high use [9, 10] | <br><br>$I_{DD}$<br>$I_{DD}$<br>$I_{DD}$<br>$I_{DD}$<br><br>$I_{DD}$<br>$I_{DD}$ | <br><br>—<br>—<br>—<br>—<br><br>—<br>— | <br><br>590<br>395<br>580<br>390<br><br>550<br>385 | <br><br>mA<br>mA<br>mA<br>mA<br><br>mA<br>mA |
| 27c | Operating current 1.5 V supplies @ 82 MHz: [6]<br>8-way cache [7]<br>$V_{DD}$ (including $V_{DDF}$ max current) @1.65 V typical use [8, 9]<br>$V_{DD}$ (including $V_{DDF}$ max current) @1.35 V typical use [8, 9]<br>$V_{DD}$ (including $V_{DDF}$ max current) @1.65 V high use [9, 10]<br>$V_{DD}$ (including $V_{DDF}$ max current) @1.35 V high use [9, 10]<br>4-way cache [11]<br>$V_{DD}$ (including $V_{DDF}$ max current) @1.65 V high use [9, 10]<br>$V_{DD}$ (including $V_{DDF}$ max current) @1.35 V high use [9, 10] | <br><br>$I_{DD}$<br>$I_{DD}$<br>$I_{DD}$<br>$I_{DD}$<br><br>$I_{DD}$<br>$I_{DD}$ | <br><br>—<br>—<br>—<br>—<br><br>—<br>— | <br><br>485<br>320<br>470<br>315<br><br>400<br>310 | <br><br>mA<br>mA<br>mA<br>mA<br><br>mA<br>mA |
| 27d | RAM standby current.[12]<br>$I_{DD_STBY}$ @ 25° C<br>$V_{STBY}$ @ 0.8 V<br>$V_{STBY}$ @ 1.0 V<br>$V_{STBY}$ @ 1.2 V<br><br>$I_{DD_STBY}$ @ 60° C<br>$V_{STBY}$ @ 0.8 V<br>$V_{STBY}$ @ 1.0 V<br>$V_{STBY}$ @ 1.2 V<br><br>$I_{DD_STBY}$ @ 150° C (Tj)<br>$V_{STBY}$ @ 0.8 V<br>$V_{STBY}$ @ 1.0 V<br>$V_{STBY}$ @ 1.2 V | <br><br>$I_{DD_STBY}$<br>$I_{DD_STBY}$<br>$I_{DD_STBY}$<br><br><br>$I_{DD_STBY}$<br>$I_{DD_STBY}$<br>$I_{DD_STBY}$<br><br><br>$I_{DD_STBY}$<br>$I_{DD_STBY}$<br>$I_{DD_STBY}$ | <br><br>—<br>—<br>—<br><br><br>—<br>—<br>—<br><br><br>—<br>—<br>— | <br><br>20<br>30<br>50<br><br><br>70<br>100<br>200<br><br><br>1200<br>1500<br>2000 | <br><br>µA<br>µA<br>µA<br><br><br>µA<br>µA<br>µA<br><br><br>µA<br>µA<br>µA |
| 28 | Operating current 3.3 V supplies @ $f_{MAX}$ MHz<br>$V_{DD33}$ [13]<br><br><br><br>$V_{FLASH}$<br>$V_{DDSYN}$ | <br>$I_{DD_33}$<br><br><br><br>$I_{VFLASH}$<br>$I_{DDSYN}$ | <br>—<br><br><br><br>—<br>— | <br>2 + (values derived from procedure of footnote [13])<br><br><br><br>10<br>15 | <br>mA<br><br><br><br>mA<br>mA |

**Table 9. DC Electrical Specifications ($T_A = T_L$ to $T_H$) (continued)**

| Spec | Characteristic | Symbol | Min | Max. | Unit |
|---|---|---|---|---|---|
| 29 | Operating current 5.0 V supplies (12 MHz ADCLK):<br>$V_{DDA}$ ($V_{DDA0}$ + $V_{DDA1}$)<br>Analog reference supply current ($V_{RH}$, $V_{RL}$)<br>$V_{PP}$ | <br>$I_{DD_A}$<br>$I_{REF}$<br>$I_{PP}$ | <br>—<br>—<br>— | <br>20.0<br>1.0<br>25.0 | <br>mA<br>mA<br>mA |
| 30 | Operating current $V_{DDE}$ supplies: [14]<br>$V_{DDEH1}$<br>$V_{DDE2}$<br>$V_{DDE3}$<br>$V_{DDEH4}$<br>$V_{DDE5}$<br>$V_{DDEH6}$<br>$V_{DDE7}$<br>$V_{DDEH8}$<br>$V_{DDEH9}$ | <br>$I_{DD1}$<br>$I_{DD2}$<br>$I_{DD3}$<br>$I_{DD4}$<br>$I_{DD5}$<br>$I_{DD6}$<br>$I_{DD7}$<br>$I_{DD8}$<br>$I_{DD9}$ | <br>—<br>—<br>—<br>—<br>—<br>—<br>—<br>—<br>— | <br>Refer to footnote [14] | <br>mA<br>mA<br>mA<br>mA<br>mA<br>mA<br>mA<br>mA<br>mA |
| 31 | Fast I/O weak pullup current [15]<br>1.62–1.98 V<br>2.25–2.75 V<br>3.00–3.60 V | $I_{ACT_F}$ | <br>10<br>20<br>20 | <br>110<br>130<br>170 | <br>µA<br>µA<br>µA |
| | Fast I/O weak pulldown current [15]<br>1.62–1.98 V<br>2.25–2.75 V<br>3.00–3.60 V | | <br>10<br>20<br>20 | <br>100<br>130<br>170 | <br>µA<br>µA<br>µA |
| 32 | Slow and medium I/O weak pullup/down current [15]<br>3.0–3.6 V<br>4.5–5.5 V | $I_{ACT_S}$ | <br>10<br>20 | <br>150<br>170 | <br>µA<br>µA |
| 33 | I/O input leakage current [16] | $I_{INACT_D}$ | –2.5 | 2.5 | µA |
| 34 | DC injection current (per pin) | $I_{IC}$ | –2.0 | 2.0 | mA |
| 35 | Analog input current, channel off [17] | $I_{INACT_A}$ | –150 | 150 | nA |
| 35a | Analog input current, shared analog / digital pins (AN[12], AN[13], AN[14], AN[15]) | $I_{INACT_AD}$ | –2.5 | 2.5 | µA |
| 36 | $V_{SS}$ to $V_{SSA}$ differential voltage [18] | $V_{SS} - V_{SSA}$ | –100 | 100 | mV |
| 37 | Analog reference low voltage | $V_{RL}$ | $V_{SSA}$ – 0.1 | $V_{SSA}$ + 0.1 | V |
| 38 | $V_{RL}$ differential voltage | $V_{RL} - V_{SSA}$ | –100 | 100 | mV |
| 39 | Analog reference high voltage | $V_{RH}$ | $V_{DDA}$ – 0.1 | $V_{DDA}$ + 0.1 | V |
| 40 | $V_{REF}$ differential voltage | $V_{RH} - V_{RL}$ | 4.5 | 5.25 | V |
| 41 | $V_{SSSYN}$ to $V_{SS}$ differential voltage | $V_{SSSYN} - V_{SS}$ | –50 | 50 | mV |
| 42 | $V_{RCVSS}$ to $V_{SS}$ differential voltage | $V_{RCVSS} - V_{SS}$ | –50 | 50 | mV |
| 43 | $V_{DDF}$ to $V_{DD}$ differential voltage | $V_{DDF} - V_{DD}$ | –100 | 100 | mV |
| 43a | $V_{RC33}$ to $V_{DDSYN}$ differential voltage | $V_{RC33} - V_{DDSYN}$ | –0.1 | 0.1 [19] | V |
| 44 | Analog input differential signal range (with common mode 2.5 V) | $V_{IDIFF}$ | –2.5 | 2.5 | V |

**Table 9. DC Electrical Specifications ($T_A = T_L$ to $T_H$) (continued)**

| Spec | Characteristic | Symbol | Min | Max. | Unit |
|---|---|---|---|---|---|
| 45 | Operating temperature range, ambient (packaged) | $T_A = (T_L$ to $T_H)$ | $T_L$ | $T_H$ | °C |
| 46 | Slew rate on power-supply pins | — | — | 50 | V/ms |

1 $V_{DDE2}$ and $V_{DDE3}$ are limited to 2.25–3.6 V only if SIU_ECCR[EBTS] = 0; $V_{DDE2}$ and $V_{DDE3}$ have a range of 1.6–3.6 V if SIU_ECCR[EBTS] = 1.

2 $| V_{DDA0} - V_{DDA1} |$ must be < 0.1 V.

3 $V_{PP}$ can drop to 3.0 V during read operations.

4 If standby operation is not required, connect $V_{STBY}$ to ground.

5 Applies to CLKOUT, external bus pins, and Nexus pins.

6 Maximum average RMS DC current.

7 Eight-way cache enabled (L1CSR0[CORG] = 0b0).

8 Average current measured on automotive benchmark.

9 Peak currents can be higher on specialized code.

10 High-use current measured while running optimized SPE assembly code with all code and data 100% locked in cache (0% miss rate) with all channels of the eMIOS running autonomously, plus the eDMA transferring data continuously from SRAM to SRAM. Higher currents are possible if an ‘idle’ loop that crosses cache lines is run from cache. Write code to avoid this condition.

11 Four-way cache enabled (L1CSR0[CORG] = 0b1) or (L1CSR0[CORG] = 0b0 with L1CSR0[WAM] = 0b1, L1CSR0[WID] = 0b1111, L1CSR0[WDD] = 0b1111, L1CSR0[AWID] = 0b1, and L1CSR0[AWDD] = 0b1).

12 The current specification relates to average standby operation after SRAM has been loaded with data. For power up current see Section 3.7, “Power-Up/Down Sequencing”, Figure 2.

13 Power requirements for the $V_{DD33}$ supply depend on the frequency of operation, load of all I/O pins, and the voltages on the I/O segments. Refer to Table 11 for values to calculate the power dissipation for a specific operation.

14 Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. Refer to Table 10 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.

15 Absolute value of current, measured at $V_{IL}$ and $V_{IH}$.

16 Weak pullup/down inactive. Measured at $V_{DDE}$ = 3.6 V and $V_{DDEH}$ = 5.25 V. Applies to pad types: pad_fc, pad_sh, and pad_mh.

17 Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 °C to 12 °C, in the ambient temperature range of 50 °C to 125 °C. Applies to pad types: pad_a and pad_ae.

18 $V_{SSA}$ refers to both $V_{SSA0}$ and $V_{SSA1}$. $| V_{SSA0} - V_{SSA1} |$ must be < 0.1 V.

19 Up to 0.6 V during power up and power down.

### 3.8.1 I/O Pad Current Specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a segment. The output pin current can be calculated from Table 10 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 10.

**Table 10. I/O Pad Average DC Current ($T_A = T_L$ to $T_H$)[1]**

| Spec | Pad Type | Symbol | Frequency (MHz) | Load[2] (pF) | Voltage (V) | Drive Select / Slew Rate Control Setting | Current (mA) |
|---|---|---|---|---|---|---|---|
| 1 | Slow | $I_{DRV_SH}$ | 25 | 50 | 5.25 | 11 | 8.0 |
| 2 | | | 10 | 50 | 5.25 | 01 | 3.2 |
| 3 | | | 2 | 50 | 5.25 | 00 | 0.7 |
| 4 | | | 2 | 200 | 5.25 | 00 | 2.4 |
| 5 | Medium | $I_{DRV_MH}$ | 50 | 50 | 5.25 | 11 | 17.3 |
| 6 | | | 20 | 50 | 5.25 | 01 | 6.5 |
| 7 | | | 3.33 | 50 | 5.25 | 00 | 1.1 |
| 8 | | | 3.33 | 200 | 5.25 | 00 | 3.9 |
| 9 | Fast | $I_{DRV_FC}$ | 66 | 10 | 3.6 | 00 | 2.8 |
| 10 | | | 66 | 20 | 3.6 | 01 | 5.2 |
| 11 | | | 66 | 30 | 3.6 | 10 | 8.5 |
| 12 | | | 66 | 50 | 3.6 | 11 | 11.0 |
| 13 | | | 66 | 10 | 1.98 | 00 | 1.6 |
| 14 | | | 66 | 20 | 1.98 | 01 | 2.9 |
| 15 | | | 66 | 30 | 1.98 | 10 | 4.2 |
| 16 | | | 66 | 50 | 1.98 | 11 | 6.7 |
| 17 | | | 56 | 10 | 3.6 | 00 | 2.4 |
| 18 | | | 56 | 20 | 3.6 | 01 | 4.4 |
| 19 | | | 56 | 30 | 3.6 | 10 | 7.2 |
| 20 | | | 56 | 50 | 3.6 | 11 | 9.3 |
| 21 | | | 56 | 10 | 1.98 | 00 | 1.3 |
| 22 | | | 56 | 20 | 1.98 | 01 | 2.5 |
| 23 | | | 56 | 30 | 1.98 | 10 | 3.5 |
| 24 | | | 56 | 50 | 1.98 | 11 | 5.7 |
| 25 | | | 40 | 10 | 3.6 | 00 | 1.7 |
| 26 | | | 40 | 20 | 3.6 | 01 | 3.1 |
| 27 | | | 40 | 30 | 3.6 | 10 | 5.1 |
| 28 | | | 40 | 50 | 3.6 | 11 | 6.6 |
| 29 | | | 40 | 10 | 1.98 | 00 | 1.0 |
| 30 | | | 40 | 20 | 1.98 | 01 | 1.8 |
| 31 | | | 40 | 30 | 1.98 | 10 | 2.5 |
| 32 | | | 40 | 50 | 1.98 | 11 | 4.0 |

1 These values are estimates from simulation and are not tested. Currents apply to output pins only.

2 All loads are lumped.

### 3.8.2 I/O Pad $V_{DD33}$ Current Specifications

The power consumption of the $V_{DD33}$ supply dependents on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin $V_{DD33}$ currents for all I/O segments. The output pin $V_{DD33}$ current can be calculated from Table 11 based on the voltage, frequency, and load on all fast (pad_fc) pins. The input pin $V_{DD33}$ current can be calculated from Table 11 based on the voltage, frequency, and load on all pad_sh and pad_mh pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 11.

**Table 11. $V_{DD33}$ Pad Average DC Current ($T_A = T_L$ to $T_H$) [1]**

| Spec | Pad Type | Symbol | Frequency (MHz) | Load [2] (pF) | $V_{DD33}$ (V) | $V_{DDE}$ (V) | Drive Select | Current (mA) |
|---|---|---|---|---|---|---|---|---|
| **Inputs** | | | | | | | | |
| 1 | Slow | $I_{33_SH}$ | 66 | 0.5 | 3.6 | 5.5 | NA | 0.003 |
| 2 | Medium | $I_{33_MH}$ | 66 | 0.5 | 3.6 | 5.5 | NA | 0.003 |
| **Outputs** | | | | | | | | |
| 3 | Fast | $I_{33_FC}$ | 66 | 10 | 3.6 | 3.6 | 00 | 0.35 |
| 4 | | | 66 | 20 | 3.6 | 3.6 | 01 | 0.53 |
| 5 | | | 66 | 30 | 3.6 | 3.6 | 10 | 0.62 |
| 6 | | | 66 | 50 | 3.6 | 3.6 | 11 | 0.79 |
| 7 | | | 66 | 10 | 3.6 | 1.98 | 00 | 0.35 |
| 8 | | | 66 | 20 | 3.6 | 1.98 | 01 | 0.44 |
| 9 | | | 66 | 30 | 3.6 | 1.98 | 10 | 0.53 |
| 10 | | | 66 | 50 | 3.6 | 1.98 | 11 | 0.70 |
| 11 | | | 56 | 10 | 3.6 | 3.6 | 00 | 0.30 |
| 12 | | | 56 | 20 | 3.6 | 3.6 | 01 | 0.45 |
| 13 | | | 56 | 30 | 3.6 | 3.6 | 10 | 0.52 |
| 14 | | | 56 | 50 | 3.6 | 3.6 | 11 | 0.67 |
| 15 | | | 56 | 10 | 3.6 | 1.98 | 00 | 0.30 |
| 16 | | | 56 | 20 | 3.6 | 1.98 | 01 | 0.37 |
| 17 | | | 56 | 30 | 3.6 | 1.98 | 10 | 0.45 |
| 18 | | | 56 | 50 | 3.6 | 1.98 | 11 | 0.60 |
| 19 | | | 40 | 10 | 3.6 | 3.6 | 00 | 0.21 |
| 20 | | | 40 | 20 | 3.6 | 3.6 | 01 | 0.31 |
| 21 | | | 40 | 30 | 3.6 | 3.6 | 10 | 0.37 |
| 22 | | | 40 | 50 | 3.6 | 3.6 | 11 | 0.48 |
| 23 | | | 40 | 10 | 3.6 | 1.98 | 00 | 0.21 |
| 24 | | | 40 | 20 | 3.6 | 1.98 | 01 | 0.27 |
| 25 | | | 40 | 30 | 3.6 | 1.98 | 10 | 0.32 |
| 26 | | | 40 | 50 | 3.6 | 1.98 | 11 | 0.42 |

1 These values are estimated from simulation and not tested. Currents apply to output pins for the fast pads only and to input pins for the slow and medium pads only.

2 All loads are lumped.

## 3.9 Oscillator and FMPLL Electrical Characteristics

**Table 12. FMPLL Electrical Specifications**

**($V_{DDSYN}$ = 3.0–3.6 V; $V_{SS}$ = $V_{SSSYN}$ = 0.0 V; $T_A$ = $T_L$ to $T_H$)**

| Spec | Characteristic | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| 1 | PLL reference frequency range: [1]<br>Crystal reference (20)[2]<br>Crystal reference (40)[3]<br>External reference (20)[2]<br>External reference (40)[3]<br>Dual controller (1:1 mode) | <br>$f_{ref_crystal}$<br>$f_{ref_crystal}$<br>$f_{ref_ext}$<br>$f_{ref_ext}$<br>$f_{ref_1:1}$ | <br>8<br>> 20<br>8<br>> 20<br>24 | <br>≤ 20<br>40<br>≤ 20<br>40<br>$f_{sys} \div 2$ | MHz |
| 2 | System frequency [4] | $f_{sys}$ | $f_{ICO(MIN)} \div 2^{RFD}$ | $f_{MAX}$ [5] | MHz |
| 3 | System clock period | $t_{CYC}$ | — | $1 \div f_{sys}$ | ns |
| 4 | Loss of reference frequency [6] | $f_{LOR}$ | 100 | 1000 | kHz |
| 5 | Self-clocked mode (SCM) frequency [7] | $f_{SCM}$ | 7.4 | 17.5 | MHz |
| 6 | EXTAL input high voltage crystal mode [8]<br><br>All other modes<br>[dual controller (1:1), bypass, external reference] | $V_{IHEXT}$<br><br>$V_{IHEXT}$ | $V_{XTAL}$ + 0.4 V<br><br>$(V_{DDE5} \div 2)$ + 0.4 V | —<br><br>— | V<br><br>V |
| 7 | EXTAL input low voltage crystal mode [9]<br><br>All other modes<br>[dual controller (1:1), bypass, external reference] | $V_{ILEXT}$<br><br>$V_{ILEXT}$ | —<br><br>— | $V_{XTAL}$ – 0.4 V<br><br>$(V_{DDE5} \div 2)$ – 0.4 V | V<br><br>V |
| 8 | XTAL current [10] | $I_{XTAL}$ | 2 | 6 | mA |
| 9 | Total on-chip stray capacitance on XTAL | $C_{S_XTAL}$ | — | 1.5 | pF |
| 10 | Total on-chip stray capacitance on EXTAL | $C_{S_EXTAL}$ | — | 1.5 | pF |
| 11 | Crystal manufacturer's recommended capacitive load | $C_L$ | Refer to crystal specification | Refer to crystal specification | pF |
| 12 | Discrete load capacitance to connect to EXTAL | $C_{L_EXTAL}$ | — | $(2 \times C_L) - C_{S_EXTAL} - C_{PCB_EXTAL}$ [11] | pF |
| 13 | Discrete load capacitance to connect to XTAL | $C_{L_XTAL}$ | — | $(2 \times C_L) - C_{S_XTAL} - C_{PCB_XTAL}$ [11] | pF |
| 14 | PLL lock time [12] | $t_{lpll}$ | — | 750 | µs |
| 15 | Dual controller (1:1) clock skew (between CLKOUT and EXTAL) [13, 14] | $t_{skew}$ | –2 | 2 | ns |
| 16 | Duty cycle of reference | $t_{DC}$ | 40 | 60 | % |
| 17 | Frequency unLOCK range | $f_{UL}$ | –4.0 | 4.0 | % $f_{SYS}$ |
| 18 | Frequency LOCK range | $f_{LCK}$ | –2.0 | 2.0 | % $f_{SYS}$ |

**Table 12. FMPLL Electrical Specifications (continued)**

**($V_{DDSYN}$ = 3.0–3.6 V; $V_{SS}$ = $V_{SSSYN}$ = 0.0 V; $T_A$ = $T_L$ to $T_H$)**

| Spec | Characteristic | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| 19 | CLKOUT period jitter, measured at $f_{SYS}$ max: [15, 16]<br>Peak-to-peak jitter (clock edge to clock edge)<br>Long term jitter (averaged over a 2 ms interval) | $C_{JITTER}$ | <br>—<br>— | <br>5.0<br>0.01 | %<br>$f_{CLKOUT}$ |
| 20 | Frequency modulation range limit [17]<br>(do not exceed $f_{sys}$ maximum) | $C_{MOD}$ | 0.8 | 2.4 | $\%f_{SYS}$ |
| 21 | ICO frequency<br>$f_{ico} = [f_{ref_crystal} \times (MFD + 4)] \div (PREDIV + 1)$ [18]<br>$f_{ico} = [f_{ref_ext} \times (MFD + 4)] \div (PREDIV + 1)$ | $f_{ico}$ | 48 | $f_{MAX}$ | MHz |
| 22 | Predivider output frequency (to PLL) | $f_{PREDIV}$ | 4 | 20 [19] | MHz |

1 Nominal crystal and external reference values are worst-case not more than 1%. The device operates correctly if the frequency remains within ± 5% of the specification limit. This tolerance range allows for a slight frequency drift of the crystals over time. The designer must thoroughly understand the drift margin of the source clock.

2 The 8–20 MHz crystal or external reference values have PLLCFG[2] pulled low.

3 The 20–40 MHz crystal and external reference values have PLLCFG[2] pulled high, and the minimum frequency must be greater than 20 MHz. Use the 8–20 MHz setting (PLLCFG[2] pulled low) if a 20 MHz crystal or external reference is required.
To exit $\overline{\text{RESET}}$ when using 40 MHz, set PLLCFG[2] to 1.

4 All internal registers retain data at 0 Hz.

5 Up to the maximum frequency rating of the device (refer to Table 1).

6 Loss of reference frequency is defined as the reference frequency detected internally, which transitions the PLL into self-clocked mode.

7 The PLL operates at self-clocked mode (SCM) frequency when the reference frequency falls below $f_{LOR}$. SCM frequency is measured on the CLKOUT ball with the divider set to divide-by-two of the system clock.
NOTE: In SCM, the MFD and PREDIV have no effect and the RFD is bypassed.

8 Use the EXTAL input high voltage parameter when using the FlexCAN oscillator in crystal mode (no quartz crystals or resonators). ($V_{extal} - V_{xtal}$) must be ≥ 400 mV for the oscillator's comparator to produce the output clock.

9 Use the EXTAL input low voltage parameter when using the FlexCAN oscillator in crystal mode (no quartz crystals or resonators). ($V_{xtal} - V_{extal}$) must be ≥ 400 mV for the oscillator's comparator to produce the output clock.

10 $I_{xtal}$ is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

11 $C_{PCB_EXTAL}$ and $C_{PCB_XTAL}$ are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

12 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, the lock time also includes the crystal startup time.

13 PLL is operating in 1:1 PLL mode.

14 $V_{DDE}$ = 3.0–3.6 V.

15 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{sys}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via $V_{DDSYN}$ and $V_{SSSYN}$ and variation in crystal oscillator frequency increase the jitter percentage for a given interval. CLKOUT divider is set to divide-by-two.

16 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of (jitter + Cmod).

17 Modulation depth selected must not result in $f_{sys}$ value greater than the $f_{sys}$ maximum specified value.

18 $f_{sys} = f_{ico} \div (2^{RFD})$.

19 Maximum value for dual controller (1:1) mode is ($f_{MAX} \div 2$) with the predivider set to 1 (FMPLL_SYNCR[PREDIV] = 0b001).

## 3.10 eQADC Electrical Characteristics

**Table 13. eQADC Conversion Specifications ($T_A = T_L$ to $T_H$)**

| Spec | Characteristic | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| 1 | ADC clock (ADCLK) frequency [1] | $F_{ADCLK}$ | 1 | 12 | MHz |
| 2 | Conversion cycles<br>Differential<br>Single ended | CC | <br>13 + 2 (15)<br>14 + 2 (16) | <br>13 + 128 (141)<br>14 + 128 (142) | ADCLK cycles |
| 3 | Stop mode recovery time [2] | $T_{SR}$ | 10 | — | µs |
| 4 | Resolution [3] | — | 1.25 | — | mV |
| 5 | INL: 6 MHz ADC clock | INL6 | –4 | 4 | Counts [3] |
| 6 | INL: 12 MHz ADC clock | INL12 | –8 | 8 | Counts |
| 7 | DNL: 6 MHz ADC clock | DNL6 | –3 [4] | 3 [4] | Counts |
| 8 | DNL: 12 MHz ADC clock | DNL12 | –6 [4] | 6 [4] | Counts |
| 9 | Offset error with calibration | OFFWC | –4 [5] | 4 [5] | Counts |
| 10 | Full-scale gain error with calibration | GAINWC | –8 [6] | 8 [6] | Counts |
| 11 | Disruptive input injection current [7, 8, 9, 10] | $I_{INJ}$ | –1 | 1 | mA |
| 12 | Incremental error due to injection current. All channels are 10 kΩ < Rs <100 kΩ<br>Channel under test has Rs = 10 kΩ,<br>$I_{INJ} = I_{INJMAX}$, $I_{INJMIN}$ | $E_{INJ}$ | –4 | 4 | Counts |
| 13 | Total unadjusted error (TUE) for single ended conversions with calibration [11, 12, 13, 14, 15] | TUE | –4 | 4 | Counts |

[1] Conversion characteristics vary with $F_{ADCLK}$ rate. Reduced conversion accuracy occurs at maximum $F_{ADCLK}$ rate. The maximum value is based on 800 KS/s and the minimum value is based on 20 MHz oscillator clock frequency divided by a maximum 16 factor.

[2] Stop mode recovery time begins when the ADC control register enable bits are set until the ADC is ready to perform conversions.

[3] At $V_{RH} - V_{RL}$ = 5.12 V, one least significant bit (LSB) = 1.25, mV = one count.

[4] Guaranteed 10-bit mono tonicity.

[5] The absolute value of the offset error without calibration ≤ 100 counts.

[6] The absolute value of the full scale gain error without calibration ≤ 120 counts.

[7] Below disruptive current conditions, the channel being stressed has conversion values of: 0x3FF for analog inputs greater than $V_{RH}$, and 0x000 for values less than $V_{RL}$. This assumes that $V_{RH} \leq V_{DDA}$ and $V_{RL} \geq V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.

[8] Exceeding the limit can cause a conversion error on both stressed and unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

[9] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA}$ + 0.5 V and $V_{NEGCLAMP}$ = – 0.3 V, then use the larger of the calculated values.

[10] This condition applies to two adjacent pads on the internal pad.

[11] The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to canceling errors.

[12] TUE does not apply to differential conversions.

[13] Measured at 6 MHz ADC clock. TUE with a 12 MHz ADC clock is: –16 counts < TUE < 16 counts.

[14] TUE includes all internal device errors such as internal reference variation (75% Ref, 25% Ref).

[15] Depending on the input impedance, the analog input leakage current (Table 9. DC Electrical Specifications, spec 35a) can affect the actual TUE measured on analog channels AN[12], AN[13], AN[14], AN[15].

## 3.11 H7Fa Flash Memory Electrical Characteristics

**Table 14. Flash Program and Erase Specifications ($T_A = T_L$ to $T_H$)**

| Spec | Flash Program Characteristic | Symbol | Min. | Typical [1] | Initial Max. [2] | Max. [3] | Unit |
|---|---|---|---|---|---|---|---|
| 3 | Doubleword (64 bits) program time [4] | $T_{dwprogram}$ | — | 10 | — | 500 | µs |
| 4 | Page program time [4] | $T_{pprogram}$ | — | 22 | 44 [5] | 500 | µs |
| 7 | 16 KB block pre-program and erase time | $T_{16kpperase}$ | — | 265 | 400 | 5000 | ms |
| 9 | 48 KB block pre-program and erase time | $T_{48kpperase}$ | — | 345 | 400 | 5000 | ms |
| 10 | 64 KB block pre-program and erase time | $T_{64kpperase}$ | — | 415 | 500 | 5000 | ms |
| 8 | 128 KB block pre-program and erase time | $T_{128kpperase}$ | — | 500 | 1250 | 7500 | ms |
| 11 | Minimum operating frequency for program and erase operations [6] | — | 25 | — | — | — | MHz |

1 Typical program and erase times are calculated at 25 °C operating temperature using nominal supply values.

2 Initial factory condition: ≤ 100 program/erase cycles, 25 °C, using a typical supply voltage measured at a minimum system frequency of 80 MHz.

3 The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

5 Page size is 256 bits (8 words).

6 The read frequency of the flash can range up to the maximum operating frequency. There is no minimum read frequency condition.

**Table 15. Flash EEPROM Module Life ($T_A = T_L$ to $T_H$)**

| Spec | Characteristic | Symbol | Min. | Typical [1] | Unit |
|---|---|---|---|---|---|
| 1a | Number of program/erase cycles per block for 16 KB, 48 KB, and 64 KB blocks over the operating temperature range ($T_J$) | P/E | 100,000 | — | cycles |
| 1b | Number of program/erase cycles per block for 128 KB blocks over the operating temperature range ($T_J$) | P/E | 1000 | 100,000 | cycles |
| 2 | Data retention<br>Blocks with 0–1,000 P/E cycles<br>Blocks with 1,001–100,000 P/E cycles | Retention | <br>20<br>5 | <br>—<br>— | years |

1 Typical endurance is evaluated at 25° C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of typical endurance, refer to engineering bulletin EB619 Typical Endurance for Nonvolatile Memory.

Table 16 shows the FLASH_BIU settings versus frequency of operation. Refer to the device reference manual for definitions of these bit fields.

**Table 16. FLASH_BIU Settings vs. Frequency of Operation [1]**

| Maximum Frequency (MHz) | APC | RWSC | WWSC | DPFEN [2] | IPFEN [2] | PFLIM [3] | BFEN [4] |
|---|---|---|---|---|---|---|---|
| Up to and including 82 MHz [5] | 0b001 | 0b001 | 0b01 | 0b00<br>0b01<br>0b11 | 0b00<br>0b01<br>0b11 | 0b000<br>to<br>0b110 | 0b0<br>0b1 |
| Up to and including 102 MHz [6] | 0b001 | 0b010 | 0b01 | 0b00<br>0b01<br>0b11 | 0b00<br>0b01<br>0b11 | 0b000<br>to<br>0b110 | 0b0<br>0b1 |
| Up to and including 135 MHz [7] | 0b010 | 0b011 | 0b01 | 0b00<br>0b01<br>0b11 | 0b00<br>0b01<br>0b11 | 0b000<br>to<br>0b110 | 0b0<br>0b1 |
| Default setting after reset | 0b111 | 0b111 | 0b11 | 0b00 | 0b00 | 0b000 | 0b0 |

1 Illegal combinations exist. Use entries from the same row in this table.
2 For maximum flash performance, set to 0b11.
3 For maximum flash performance, set to 0b110.
4 For maximum flash performance, set to 0b1.
5 82 MHz parts allow for 80 MHz system clock + 2% frequency modulation (FM).
6 102 MHz parts allow for 100 MHz system clock + 2% FM.
7 135 MHz parts allow for 132 MHz system clock + 2% FM.

## 3.12 AC Specifications

### 3.12.1 Pad AC Specifications

**Table 17. Pad AC Specifications ($V_{DDEH}$ = 5.0 V, $V_{DDE}$ = 1.8 V) [1]**

| Spec | Pad | SRC / DSC (binary) | Out Delay [2, 3, 4] (ns) | Rise / Fall [4, 5] (ns) | Load Drive (pF) |
|---|---|---|---|---|---|
| 1 | Slow high voltage (SH) | 11 | 26 | 15 | 50 |
| | | | 82 | 60 | 200 |
| | | 01 | 75 | 40 | 50 |
| | | | 137 | 80 | 200 |
| | | 00 | 377 | 200 | 50 |
| | | | 476 | 260 | 200 |
| 2 | Medium high voltage (MH) | 11 | 16 | 8 | 50 |
| | | | 43 | 30 | 200 |
| | | 01 | 34 | 15 | 50 |
| | | | 61 | 35 | 200 |
| | | 00 | 192 | 100 | 50 |
| | | | 239 | 125 | 200 |

**Table 17. Pad AC Specifications ($V_{DDEH}$ = 5.0 V, $V_{DDE}$ = 1.8 V) [1] (continued)**

| Spec | Pad | SRC / DSC (binary) | Out Delay [2, 3, 4] (ns) | Rise / Fall [4, 5] (ns) | Load Drive (pF) |
|---|---|---|---|---|---|
| 3 | Fast | 00 | 3.1 | 2.7 | 10 |
| | | 01 | | 2.5 | 20 |
| | | 10 | | 2.4 | 30 |
| | | 11 | | 2.3 | 50 |
| 4 | Pullup/down (3.6 V max) | — | — | 7500 | 50 |
| 5 | Pullup/down (5.5 V max) | — | — | 9000 | 50 |

1 These are worst-case values that are estimated from simulation (not tested). The values in the table are simulated at: $V_{DD}$ = 1.35–1.65 V; $V_{DDE}$ = 1.62–1.98 V; $V_{DDEH}$ = 4.5–5.25 V; $V_{DD33}$ and $V_{DDSYN}$ = 3.0–3.6 V; and $T_A = T_L$ to $T_H$.

2 This parameter is supplied for reference and is guaranteed by design (not tested).

3 The output delay is shown in Figure 4. To calculate the output delay with respect to the system clock, add a maximum of one system clock to the output delay.

4 The output delay and rise and fall are measured to 20% or 80% of the respective signal.

5 This parameter is guaranteed by characterization rather than 100% tested.

**Table 18. Derated Pad AC Specifications ($V_{DDEH}$ = 3.3 V, $V_{DDE}$ = 3.3 V) [1]**

| Spec | Pad | SRC/DSC (binary) | Out Delay [2, 3, 4] (ns) | Rise / Fall [3, 5] (ns) | Load Drive (pF) |
|---|---|---|---|---|---|
| 1 | Slow high voltage (SH) | 11 | 39 | 23 | 50 |
| | | | 120 | 87 | 200 |
| | | 01 | 101 | 52 | 50 |
| | | | 188 | 111 | 200 |
| | | 00 | 507 | 248 | 50 |
| | | | 597 | 312 | 200 |
| 2 | Medium high voltage (MH) | 11 | 23 | 12 | 50 |
| | | | 64 | 44 | 200 |
| | | 01 | 50 | 22 | 50 |
| | | | 90 | 50 | 200 |
| | | 00 | 261 | 123 | 50 |
| | | | 305 | 156 | 200 |
| 3 | Fast | 00 | 3.2 | 2.4 | 10 |
| | | 01 | | 2.2 | 20 |
| | | 10 | | 2.1 | 30 |
| | | 11 | | 2.1 | 50 |
| 4 | Pullup/down (3.6 V max) | — | — | 7500 | 50 |
| 5 | Pullup/down (5.5 V max) | — | — | 9500 | 50 |

1 These are worst-case values that are estimated from simulation (not tested). The values in the table are simulated at: $V_{DD}$ = 1.35–1.65 V; $V_{DDE}$ = 3.0–3.6 V; $V_{DDEH}$ = 3.0–3.6 V; $V_{DD33}$ and $V_{DDSYN}$ = 3.0–3.6 V; and $T_A = T_L$ to $T_H$.

2 This parameter is supplied for reference and guaranteed by design (not tested).

3 The output delay, and the rise and fall, are calculated to 20% or 80% of the respective signal.

4 The output delay is shown in Figure 4. To calculate the output delay with respect to the system clock, add a maximum of one system clock to the output delay.

5 This parameter is guaranteed by characterization rather than 100% tested.

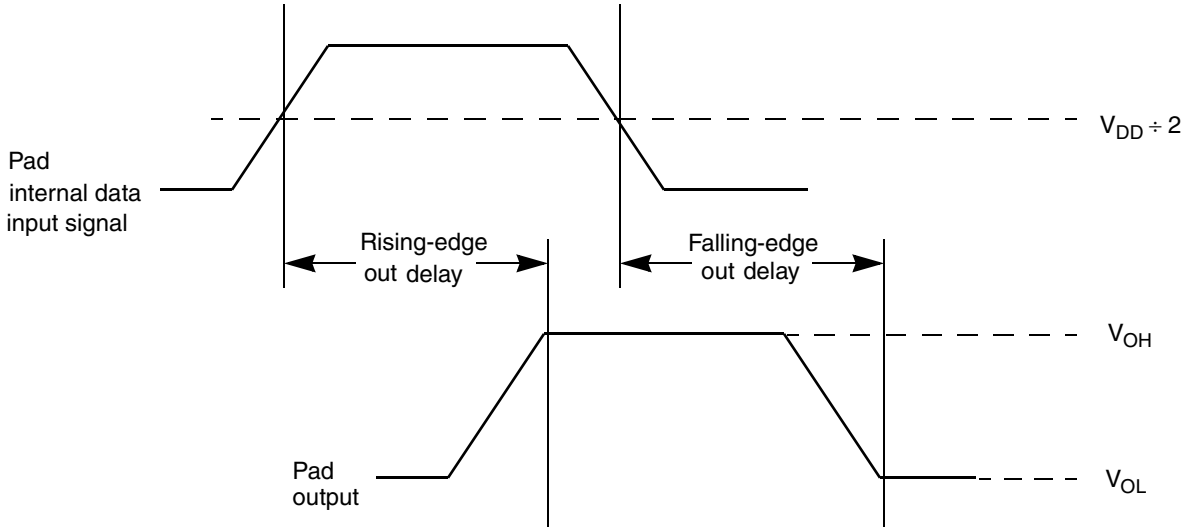



**Figure 4. Pad Output Delay**

## 3.13 AC Timing

### 3.13.1 Reset and Configuration Pin Timing

**Table 19. Reset and Configuration Pin Timing [1]**

| Spec | Characteristic | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|
| 1 | $\overline{\text{RESET}}$ pulse width | $t_{RPW}$ | 10 | — | $t_{CYC}$ |
| 2 | $\overline{\text{RESET}}$ glitch detect pulse width | $t_{GPW}$ | 2 | — | $t_{CYC}$ |
| 3 | PLLCFG, BOOTCFG, WKPCFG, $\overline{\text{RSTCFG}}$ setup time to $\overline{\text{RSTOUT}}$ valid | $t_{RCSU}$ | 10 | — | $t_{CYC}$ |
| 4 | PLLCFG, BOOTCFG, WKPCFG, $\overline{\text{RSTCFG}}$ hold time from $\overline{\text{RSTOUT}}$ valid | $t_{RCH}$ | 0 | — | $t_{CYC}$ |

1 Reset timing specified at: $V_{DDEH}$ = 3.0–5.25 V and $T_A = T_L$ to $T_H$.

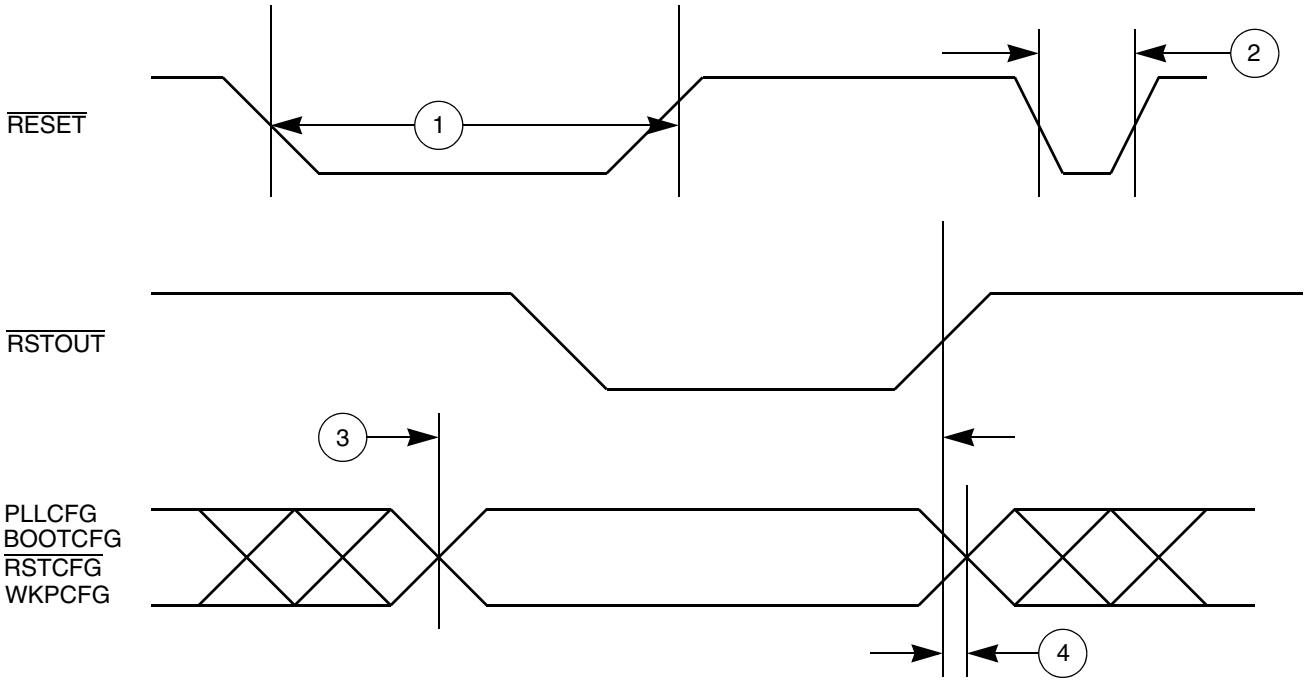



**Figure 5. Reset and Configuration Pin Timing**

## 3.13.2 IEEE 1149.1 Interface Timing

**Table 20. JTAG Pin AC Electrical Characteristics [1]**

| Spec | Characteristic | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|
| 1 | TCK cycle time | $t_{JCYC}$ | 100 | — | ns |
| 2 | TCK clock pulse width (measured at $V_{DDE} \div 2$) | $t_{JDC}$ | 40 | 60 | ns |
| 3 | TCK rise and fall times (40% to 70%) | $t_{TCKRISE}$ | — | 3 | ns |
| 4 | TMS, TDI data setup time | $t_{TMSS}$, $t_{TDIS}$ | 5 | — | ns |
| 5 | TMS, TDI data hold time | $t_{TMSH}$, $t_{TDIH}$ | 25 | — | ns |
| 6 | TCK low to TDO data valid | $t_{TDOV}$ | — | 20 | ns |
| 7 | TCK low to TDO data invalid | $t_{TDOI}$ | 0 | — | ns |
| 8 | TCK low to TDO high impedance | $t_{TDOHZ}$ | — | 20 | ns |
| 9 | JCOMP assertion time | $t_{JCMPPW}$ | 100 | — | ns |
| 10 | JCOMP setup time to TCK low | $t_{JCMPS}$ | 40 | — | ns |
| 11 | TCK falling-edge to output valid | $t_{BSDV}$ | — | 50 | ns |
| 12 | TCK falling-edge to output valid out of high impedance | $t_{BSDVZ}$ | — | 50 | ns |
| 13 | TCK falling-edge to output high impedance (Hi-Z) | $t_{BSDHZ}$ | — | 50 | ns |
| 14 | Boundary scan input valid to TCK rising-edge | $t_{BSDST}$ | 50 | — | ns |
| 15 | TCK rising-edge to boundary scan input invalid | $t_{BSDHT}$ | 50 | — | ns |

[1] These specifications apply to JTAG boundary scan only. JTAG timing specified at: $V_{DDE}$ = 3.0–3.6 V and $T_A = T_L$ to $T_H$. Refer to Table 21 for Nexus specifications.

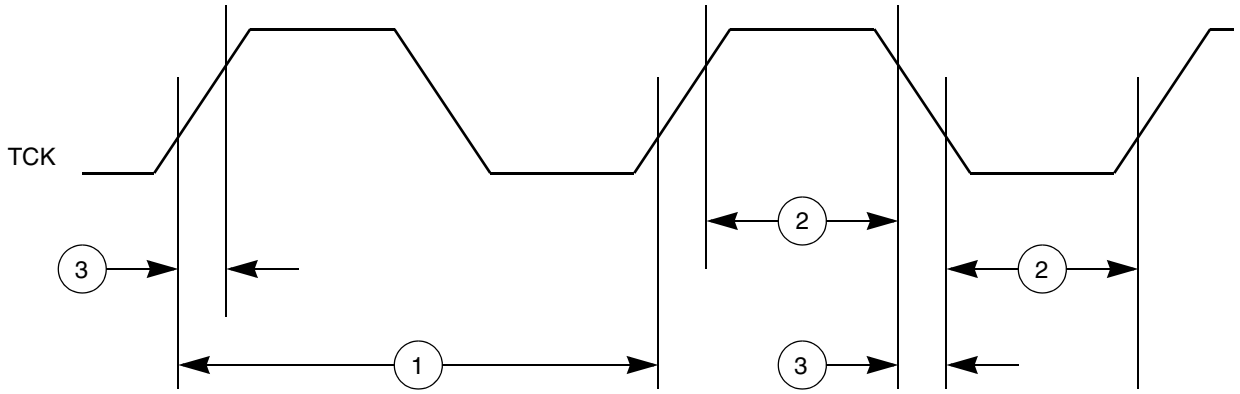



**Figure 6. JTAG Test Clock Input Timing**

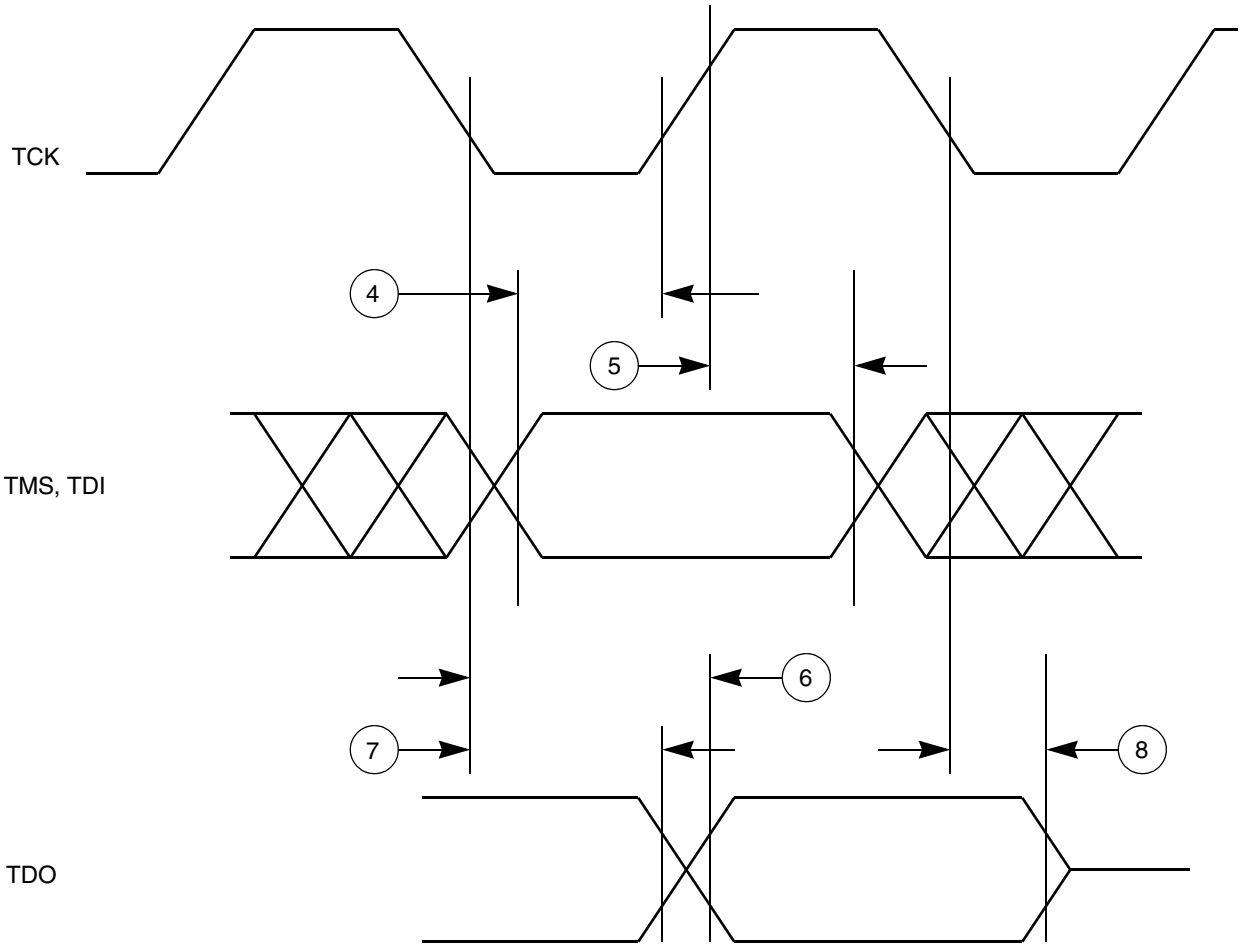



**Figure 7. JTAG Test Access Port Timing**

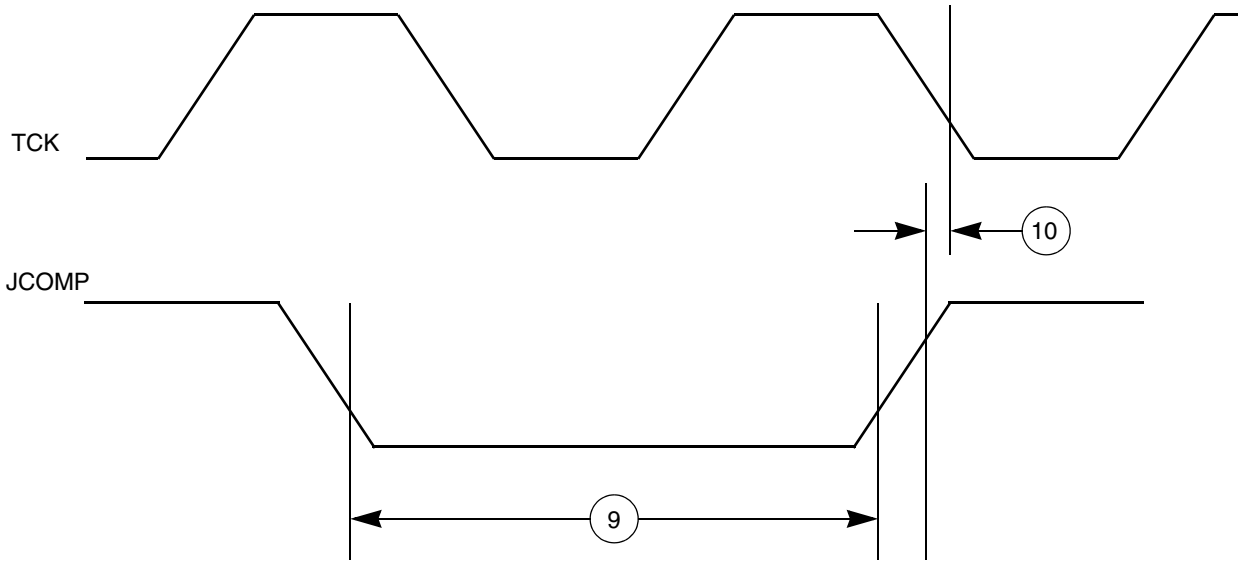



**Figure 8. JTAG JCOMP Timing**

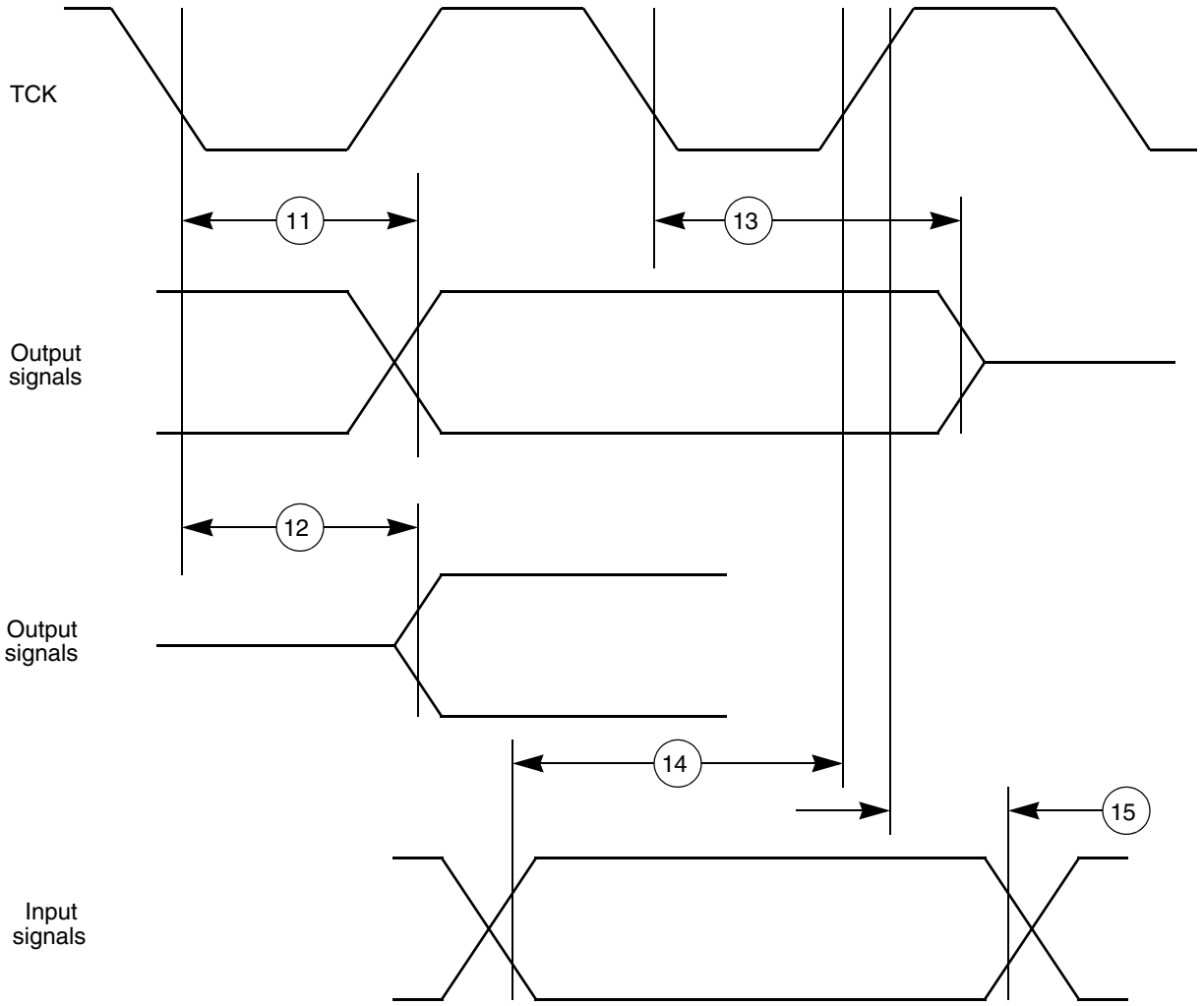



**Figure 9. JTAG Boundary Scan Timing**

## 3.13.3 Nexus Timing

**Table 21. Nexus Debug Port Timing [1]**

| Spec | Characteristic | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|
| 1 | MCKO cycle time | $t_{MCYC}$ | 1 [2] | 8 | $t_{CYC}$ |
| 2 | MCKO duty cycle | $t_{MDC}$ | 40 | 60 | % |
| 3 | MCKO low to MDO data valid [3] | $t_{MDOV}$ | –1.5 | 3.0 | ns |
| 4 | MCKO low to $\overline{\text{MSEO}}$ data valid [3] | $t_{MSEOV}$ | –1.5 | 3.0 | ns |
| 5 | MCKO low to $\overline{\text{EVTO}}$ data valid [3] | $t_{EVTOV}$ | –1.5 | 3.0 | ns |
| 6 | $\overline{\text{EVTI}}$ pulse width | $t_{EVTIPW}$ | 4.0 | — | $t_{TCYC}$ |
| 7 | $\overline{\text{EVTO}}$ pulse width | $t_{EVTOPW}$ | 1 | — | $t_{MCYC}$ |
| 8 | TCK cycle time | $t_{TCYC}$ | 4 [4] | — | $t_{CYC}$ |
| 9 | TCK duty cycle | $t_{TDC}$ | 40 | 60 | % |
| 10 | TDI, TMS data setup time | $t_{NTDIS}$, $t_{NTMSS}$ | 8 | — | ns |
| 11 | TDI, TMS data hold time | $t_{NTDIH}$, $t_{NTMSH}$ | 5 | — | ns |
| 12 | TCK low to TDO data valid<br>$V_{DDE}$ = 2.25–3.0 V<br>$V_{DDE}$ = 3.0–3.6 V | $t_{JOV}$ | <br>0<br>0 | <br>12<br>10 | <br>ns<br>ns |
| 13 | $\overline{\text{RDY}}$ valid to MCKO [5] | — | — | — | — |

1 JTAG specifications apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at $V_{DD}$ = 1.35–1.65 V, $V_{DDE}$ = 2.25–3.6 V, $V_{DD33}$ and $V_{DDSYN}$ = 3.0–3.6 V, $T_A$ = $T_L$ to $T_H$, and CL = 30 pF with DSC = 0b10.

2 The Nexus AUX port runs up to 82 MHz. Set NPC_PCR[MCKO_DIV] to divide-by-two if the system frequency is greater than 82 MHz.

3 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until the next MCKO low cycle occurs.

4 Limit the maximum frequency to approximately 16 MHz ($V_{DDE}$ = 2.25–3.0 V) or 20 MHz ($V_{DDE}$ = 3.0–3.6 V) to meet the timing specification for $t_{JOV}$ of [0.2 x $t_{JCYC}$] as outlined in the IEEE-ISTO 5001-2003 specification.

5 The $\overline{\text{RDY}}$ pin timing is asynchronous to MCKO and is guaranteed by design to function correctly.

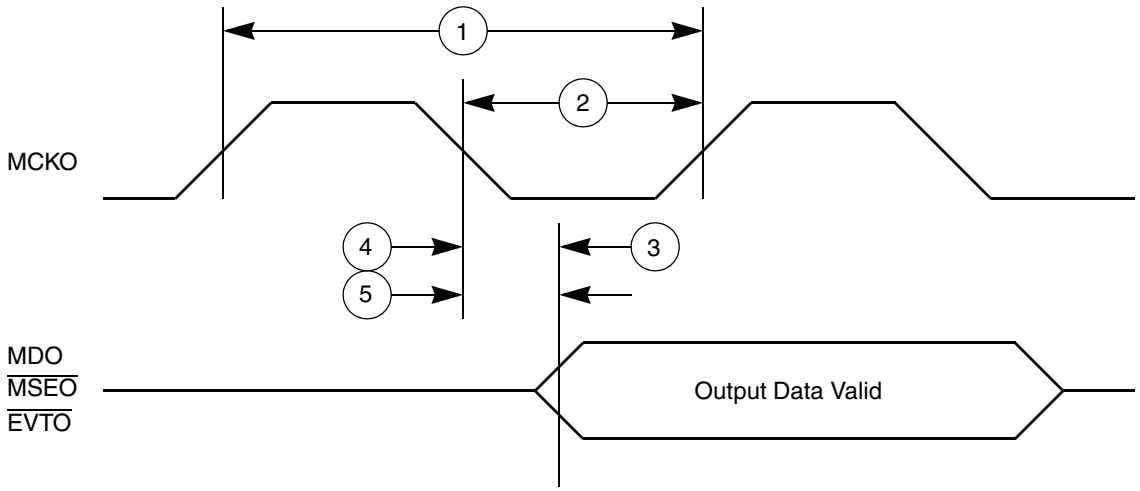



**Figure 10. Nexus Output Timing**

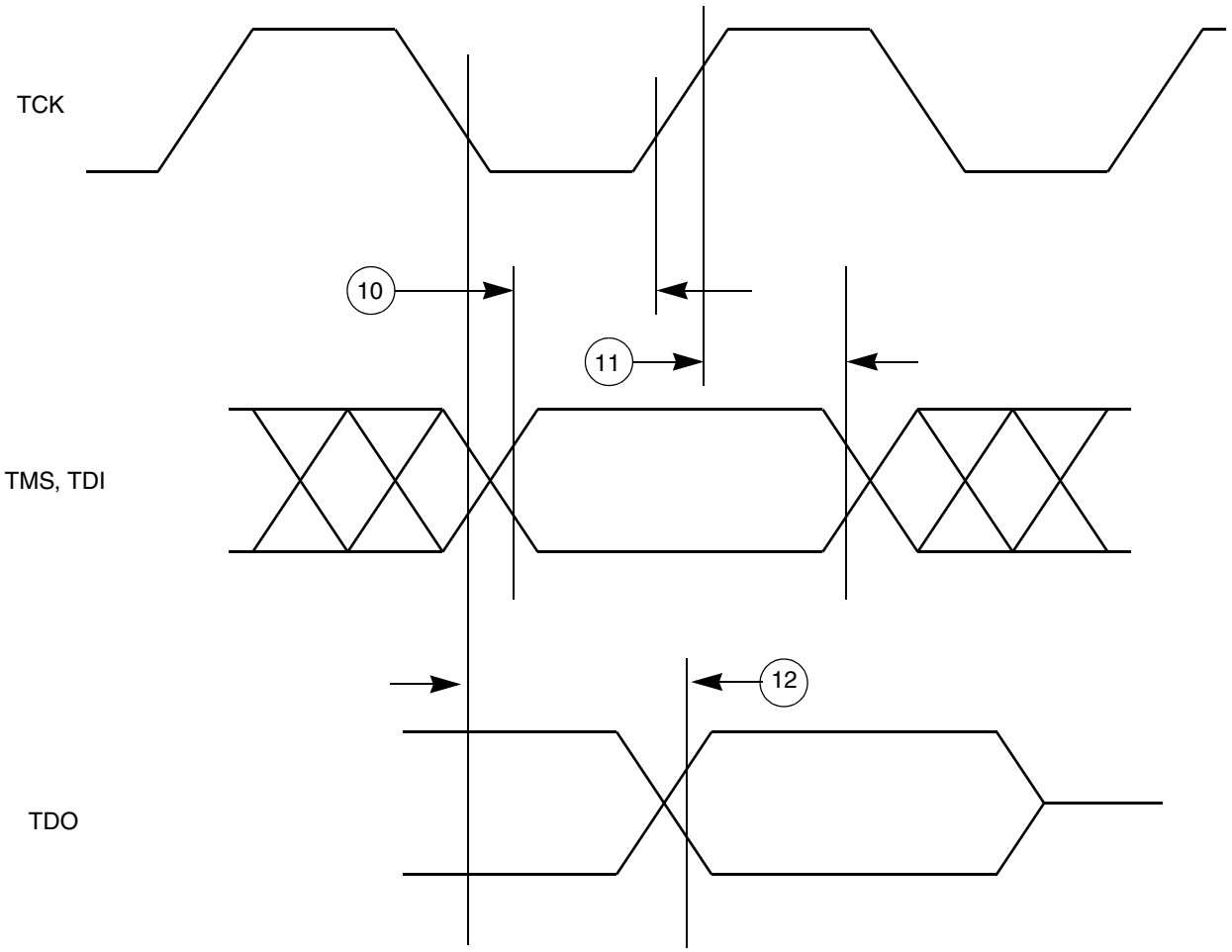



**Figure 11. Nexus TDI, TMS, TDO Timing**

## 3.13.4 External Bus Interface (EBI) Timing

lists the timing information for the external bus interface (EBI).

**Table 22. Bus Operation Timing[1]**

| Spec | Characteristic and Description | Symbol | External Bus Frequency [2, 3] | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 40 MHz | | 56 MHz | | 66 MHz | | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| 1 | CLKOUT period | $T_C$ | 24.4 | — | 17.5 | — | 14.9 | — | ns | Signals are measured at 50% $V_{DDE}$. |
| 2 | CLKOUT duty cycle | $t_{CDC}$ | 45% | 55% | 45% | 55% | 45% | 55% | $T_C$ | |
| 3 | CLKOUT rise time | $t_{CRT}$ | — | —[4] | — | —[4] | — | —[4] | ns | |
| 4 | CLKOUT fall time | $t_{CFT}$ | — | —[4] | — | —[4] | — | —[4] | ns | |
| 5 | CLKOUT positive edge to output signal *invalid* or Hi-Z (hold time)<br><br>External bus interface<br>$\overline{CS}$[0:3]<br>ADDR[8:31]<br>DATA[0:31] [5]<br>$\overline{BDIP}$<br>$\overline{OE}$<br>RD_$\overline{WR}$<br>$\overline{TA}$<br>$\overline{TEA}$ [6]<br>$\overline{TS}$<br>$\overline{WE}$/$\overline{BE}$[0:3] [7] | $t_{COH}$ | 1.0[8]<br><br>1.5 | — | 1.0[8]<br><br>1.5 | — | 1.0[8]<br><br>1.5 | — | ns | EBTS = 0<br><br>EBTS = 1<br><br>Hold time selectable via SIU_ECCR [EBTS] bit. |
| 6 | CLKOUT positive edge to output signal *valid* (output delay)<br><br>External bus interface<br>$\overline{CS}$[0:3]<br>ADDR[8:31]<br>DATA[0:31] [5]<br>$\overline{BDIP}$<br>$\overline{OE}$<br>RD_$\overline{WR}$<br>$\overline{TA}$<br>$\overline{TEA}$ [6]<br>$\overline{TS}$<br>$\overline{WE}$/$\overline{BE}$[0:3] [7] | $t_{COV}$ | — | 10.0[8]<br><br>11.0 | — | 7.5[8]<br><br>8.5 | — | 6.0[8]<br><br>7.0 | ns | EBTS = 0<br><br>EBTS = 1<br><br>Output valid time selectable via SIU_ECCR [EBTS] bit. |

**Table 22. Bus Operation Timing[1] (continued)**

| Spec | Characteristic and Description | Symbol | External Bus Frequency [2, 3] | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 40 MHz | | 56 MHz | | 66 MHz | | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| 7 | Input signal *valid* to CLKOUT positive edge (setup time)<br><br>External bus interface<br>ADDR[8:31]<br>DATA[0:31] [5]<br>RD_$\overline{WR}$<br>$\overline{TA}$<br>$\overline{TEA}$ [6]<br>$\overline{TS}$ | $t_{CIS}$ | 10.0 | — | 7.0 | — | 5.0 | — | ns | |
| 8 | CLKOUT positive edge to input signal *invalid* (hold time)<br><br>External bus interface<br>ADDR[8:31]<br>DATA[0:31] [5]<br>RD_$\overline{WR}$<br>$\overline{TA}$<br>$\overline{TEA}$ [6]<br>$\overline{TS}$ | $t_{CIH}$ | 1.0 | — | 1.0 | — | 1.0 | — | ns | |

1 EBI timing specified at: $V_{DDE}$ = 1.6–3.6 V (unless stated otherwise); $T_A = T_L$ to $T_H$; and CL = 30 pF with DSC = 0b10.

2 Speed is the nominal maximum frequency. Max. speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; and 135 MHz parts allow for 132 MHz system clock + 2% FM.

3 The external bus is limited to half the speed of the internal bus.

4 Refer to fast pad timing in Table 17 and Table 18 (different values for 1.8 V and 3.3 V).

5 Due to pin limitations, the DATA[16:31] signals are not available on the 324 package.

6 Due to pin limitations, the $\overline{TEA}$ signal is not available on the 324 package.

7 Due to pin limitations, the $\overline{WE}$/$\overline{BE}$[2:3] signals are not available on the 324 package.

8 SIU_ECCR[EBTS] = 0 timings are tested and valid at $V_{DDE}$ = 2.25–3.6 V only; SIU_ECCR[EBTS] = 1 timings are tested and valid at $V_{DDE}$ = 1.6–3.6 V.

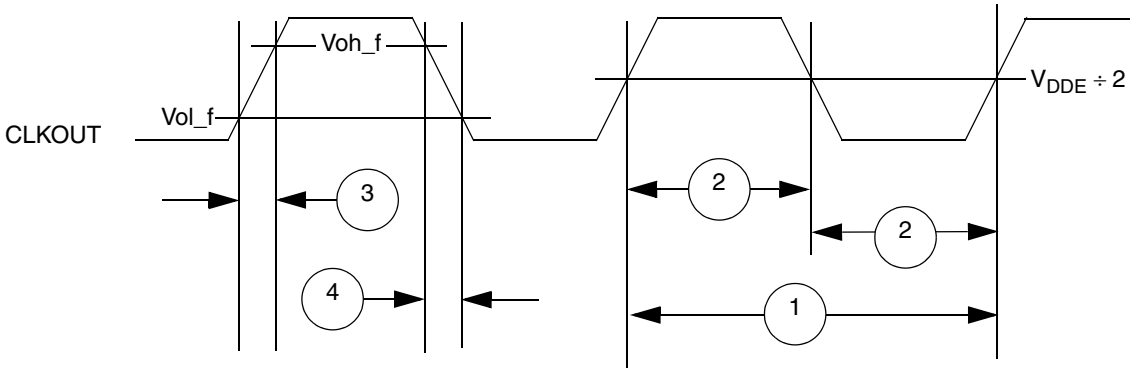



**Figure 12. CLKOUT Timing**

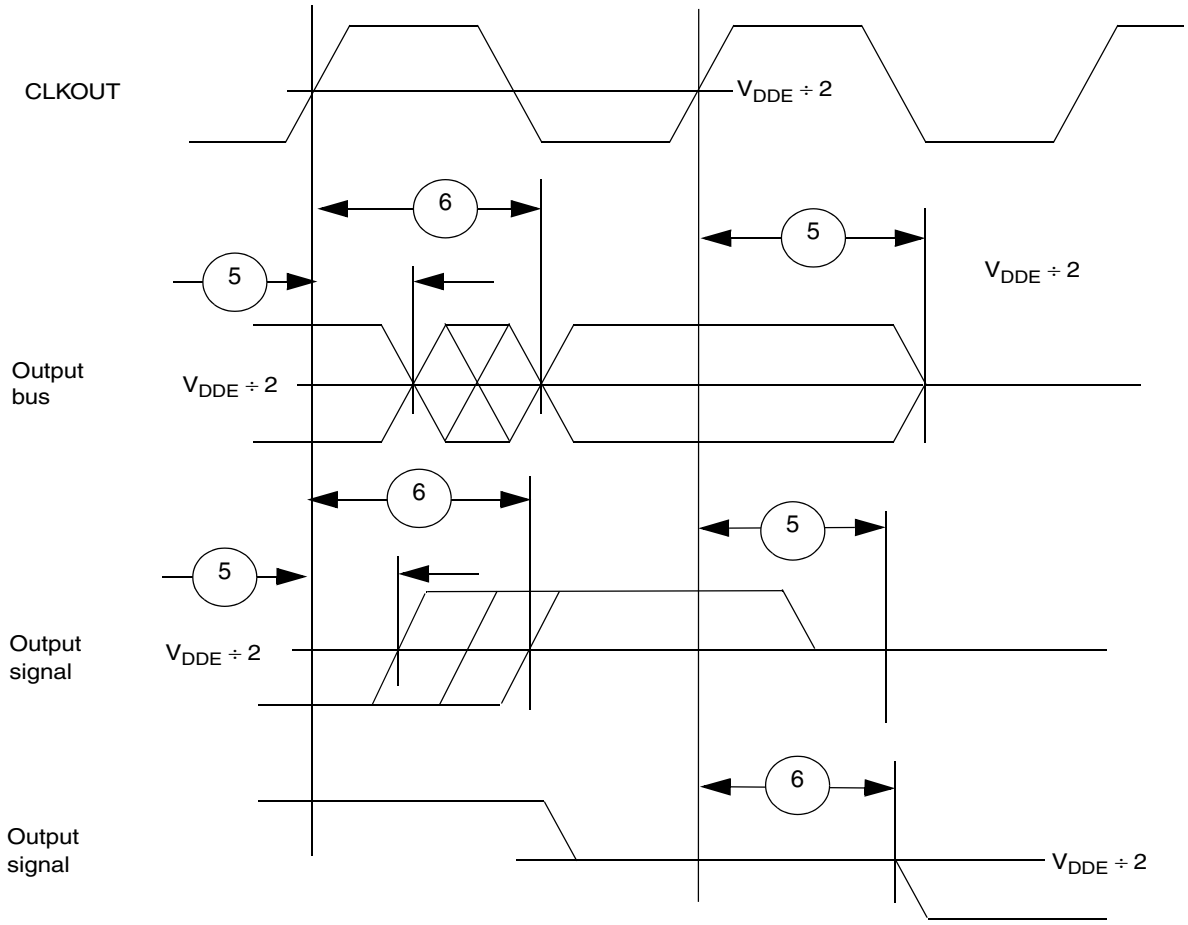



**Figure 13. Synchronous Output Timing**

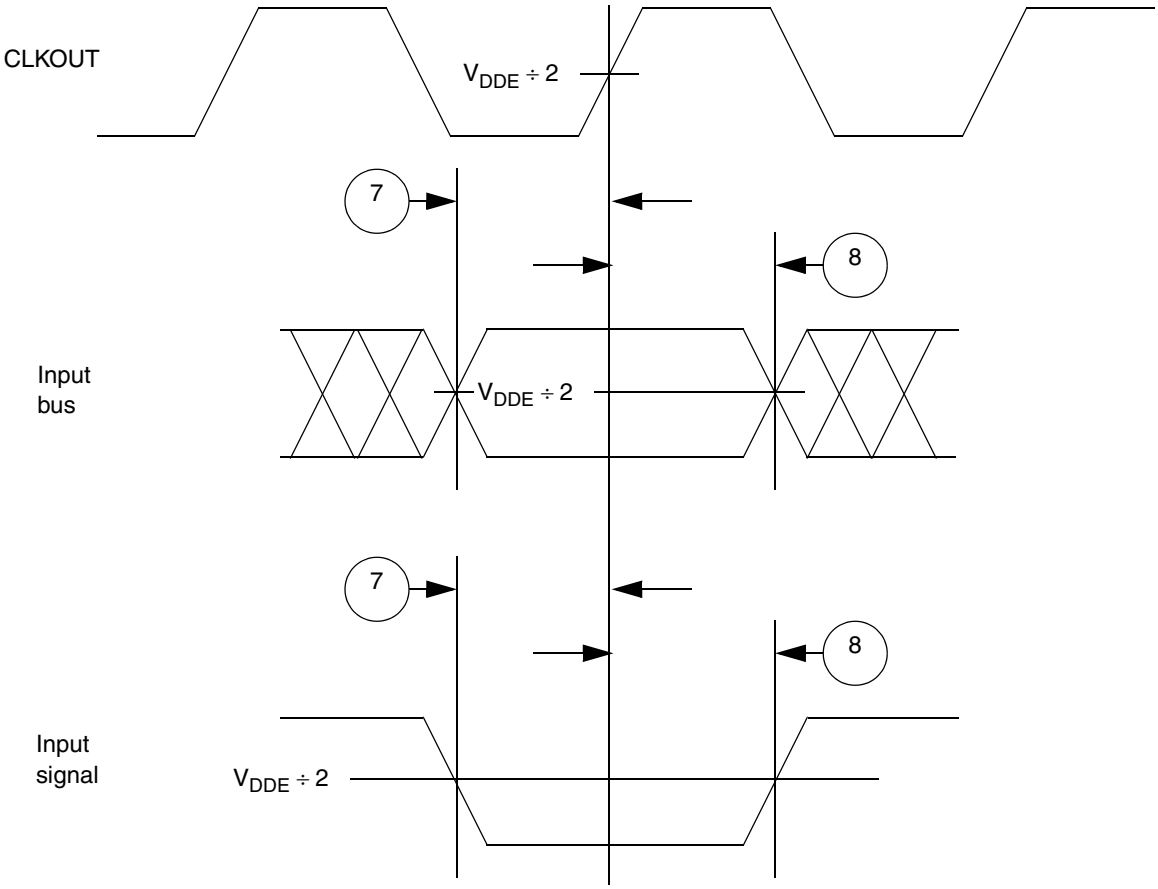



**Figure 14. Synchronous Input Timing**

## 3.13.5 External Interrupt Timing (IRQ Signals)

**Table 23. External Interrupt Timing [1]**

| Spec | Characteristic | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|
| 1 | IRQ pulse-width low | $t_{IPWL}$ | 3 | — | $t_{CYC}$ |
| 2 | IRQ pulse-width high | $T_{IPWH}$ | 3 | — | $t_{CYC}$ |
| 3 | IRQ edge-to-edge time [2] | $t_{ICYC}$ | 6 | — | $t_{CYC}$ |

[1] IRQ timing specified at: $V_{DDEH}$ = 3.0–5.25 V and $T_A = T_L$ to $T_H$.

[2] Applies when IRQ signals are configured for rising-edge or falling-edge events, but not both.

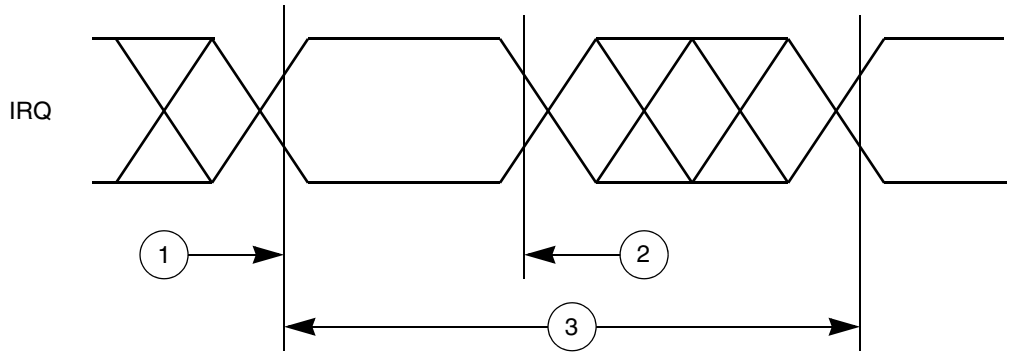



**Figure 15. External Interrupt Timing**

## 3.13.6 eMIOS Timing

**Table 24. eMIOS Timing [1]**

| Spec | Characteristic | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|
| 1 | eMIOS input pulse width | $t_{MIPW}$ | 4 | — | $t_{CYC}$ |
| 2 | eMIOS output pulse width | $t_{MOPW}$ | 1 [2] | — | $t_{CYC}$ |

[1] eMIOS timing specified at: $V_{DDEH}$ = 3.0–5.25 V and $T_A = T_L$ to $T_H$.

[2] This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control field (SRC) in the pad configuration register (PCR).

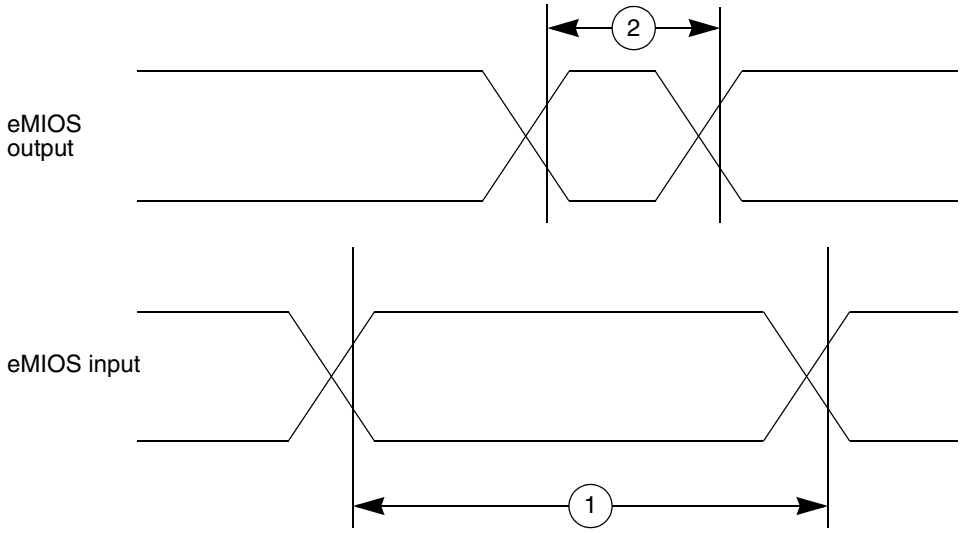



**Figure 16. eMIOS Timing**

## 3.13.7 DSPI Timing

**Table 25. DSPI Timing[1, 2]**

| Spec | Characteristic | Symbol | 80 MHz | | 112 MHz | | 132 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| 1 | SCK cycle time[3, 4] | $t_{SCK}$ | 24.4 ns | 2.9 ms | 17.5 ns | 2.1 ms | 14.8 ns | 1.8 ms | — |
| 2 | PCS to SCK delay[5] | $t_{CSC}$ | 23 | — | 15 | — | 13 | — | ns |
| 3 | After SCK delay[6] | $t_{ASC}$ | 22 | — | 14 | — | 12 | — | ns |
| 4 | SCK duty cycle | $t_{SDC}$ | ($t_{SCK} \div 2$) – 2 ns | ($t_{SCK} \div 2$) + 2 ns | ($t_{SCK} \div 2$) – 2 ns | ($t_{SCK} \div 2$) + 2 ns | ($t_{SCK} \div 2$) – 2 ns | ($t_{SCK} \div 2$) + 2 ns | ns |
| 5 | Slave access time ($\overline{SS}$ active to SOUT driven) | $t_A$ | — | 25 | — | 25 | — | 25 | ns |
| 6 | Slave SOUT disable time ($\overline{SS}$ inactive to SOUT Hi-Z, or invalid) | $t_{DIS}$ | — | 25 | — | 25 | — | 25 | ns |
| 7 | PCS*x* to $\overline{PCSS}$ time | $t_{PCSC}$ | 4 | — | 4 | — | 4 | — | ns |
| 8 | $\overline{PCSS}$ to PCS*x* time | $t_{PASC}$ | 5 | — | 5 | — | 5 | — | ns |
| 9 | Data setup time for inputs<br>Master (MTFE = 0)<br>Slave<br>Master (MTFE = 1, CPHA = 0)[7]<br>Master (MTFE = 1, CPHA = 1) | $t_{SUI}$ | <br>20<br>2<br>–4<br>20 | <br>—<br>—<br>—<br>— | <br>20<br>2<br>3<br>20 | <br>—<br>—<br>—<br>— | <br>20<br>2<br>6<br>20 | <br>—<br>—<br>—<br>— | <br>ns<br>ns<br>ns<br>ns |
| 10 | Data hold time for inputs<br>Master (MTFE = 0)<br>Slave<br>Master (MTFE = 1, CPHA = 0)[7]<br>Master (MTFE = 1, CPHA = 1) | $t_{HI}$ | <br>–4<br>7<br>21<br>–4 | <br>—<br>—<br>—<br>— | <br>–4<br>7<br>14<br>–4 | <br>—<br>—<br>—<br>— | <br>–4<br>7<br>12<br>–4 | <br>—<br>—<br>—<br>— | <br>ns<br>ns<br>ns<br>ns |
| 11 | Data valid (after SCK edge)<br>Master (MTFE = 0)<br>Slave<br>Master (MTFE = 1, CPHA = 0)<br>Master (MTFE = 1, CPHA = 1) | $t_{SUO}$ | <br>—<br>—<br>—<br>— | <br>5<br>25<br>18<br>5 | <br>—<br>—<br>—<br>— | <br>5<br>25<br>14<br>5 | <br>—<br>—<br>—<br>— | <br>5<br>25<br>13<br>5 | <br>ns<br>ns<br>ns<br>ns |
| 12 | Data hold time for outputs<br>Master (MTFE = 0)<br>Slave<br>Master (MTFE = 1, CPHA = 0)<br>Master (MTFE = 1, CPHA = 1) | $t_{HO}$ | <br>–5<br>5.5<br>8<br>–5 | <br>—<br>—<br>—<br>— | <br>–5<br>5.5<br>4<br>–5 | <br>—<br>—<br>—<br>— | <br>–5<br>5.5<br>3<br>–5 | <br>—<br>—<br>—<br>— | <br>ns<br>ns<br>ns<br>ns |

1 All DSPI timing specifications use the fastest slew rate (SRC = 0b11) on pad type M or MH. DSPI signals using pad types of S or SH have an additional delay based on the slew rate. DSPI timing is specified at: $V_{DDEH}$ = 3.0–5.25 V;$T_A = T_L$ to $T_H$; and CL = 50 pF with SRC = 0b11.

2 Speed is the nominal maximum frequency. Max. speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; and 135 MHz parts allow for 132 MHz system clock + 2% FM.

3 The minimum SCK cycle time restricts the baud rate selection for the given system clock rate. These numbers are calculated based on two MPC55xx devices communicating over a DSPI link.

4 The actual minimum SCK cycle time is limited by pad performance.

5 The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].

6 The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].

7 This number is calculated using the SMPL_PT field in DSPI_MCR set to 0b10.

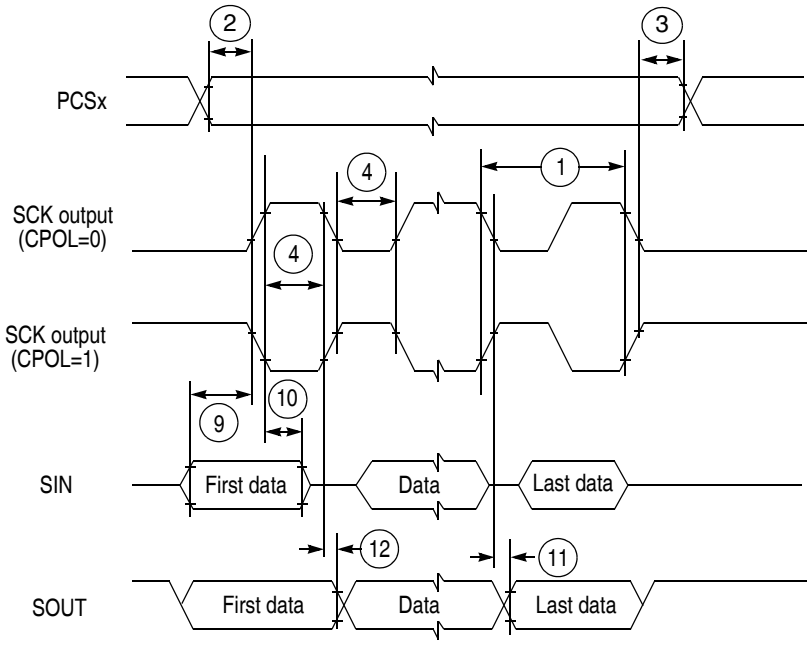



**Figure 17. DSPI Classic SPI Timing—Master, CPHA = 0**

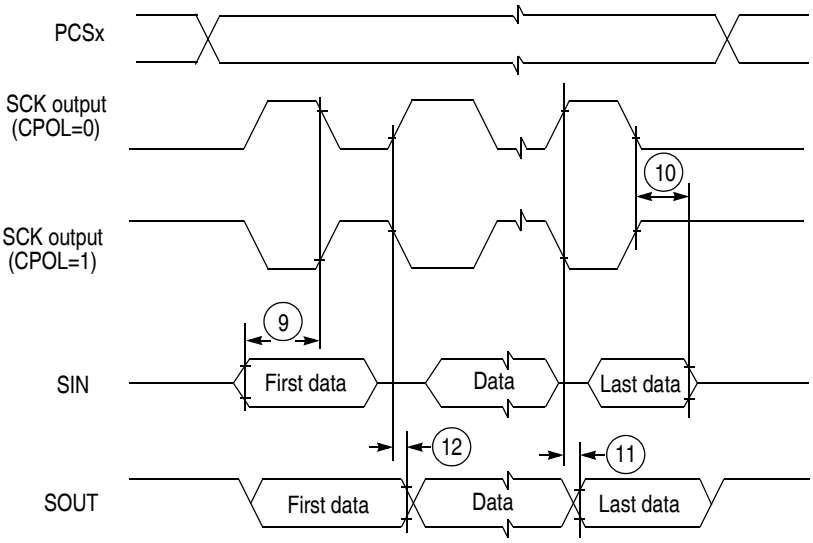



**Figure 18. DSPI Classic SPI Timing—Master, CPHA = 1**

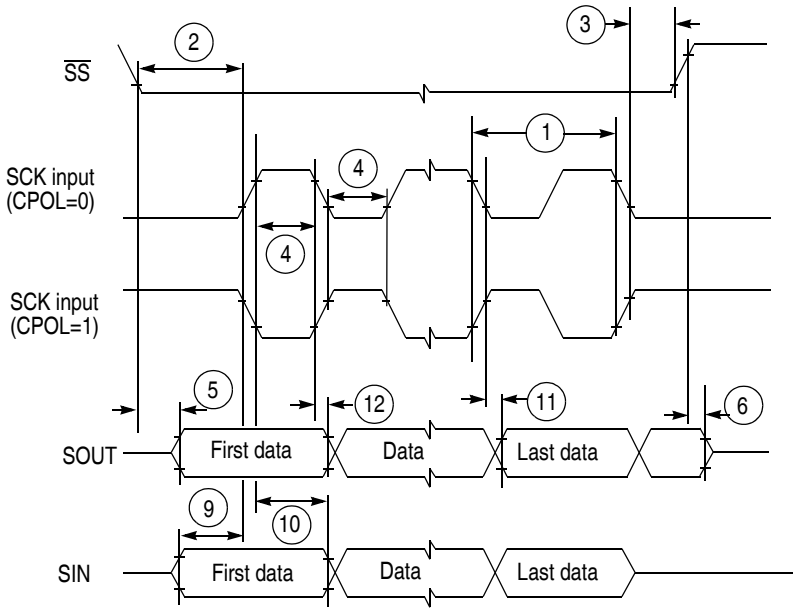



**Figure 19. DSPI Classic SPI Timing—Slave, CPHA = 0**

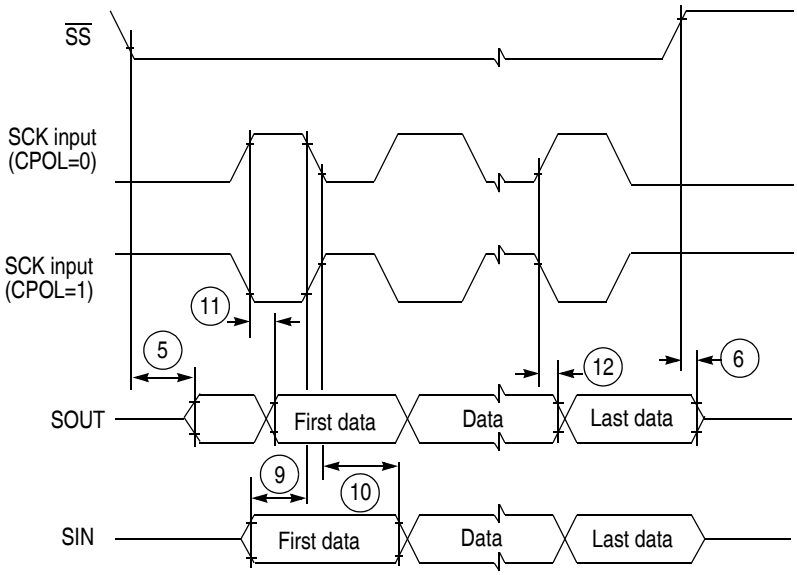



**Figure 20. DSPI Classic SPI Timing—Slave, CPHA = 1**

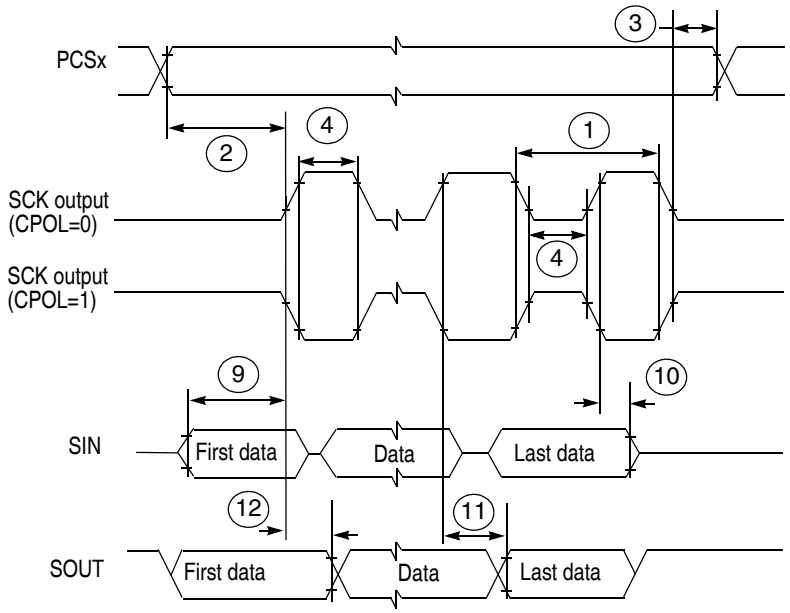



**Figure 21. DSPI Modified Transfer Format Timing—Master, CPHA = 0**

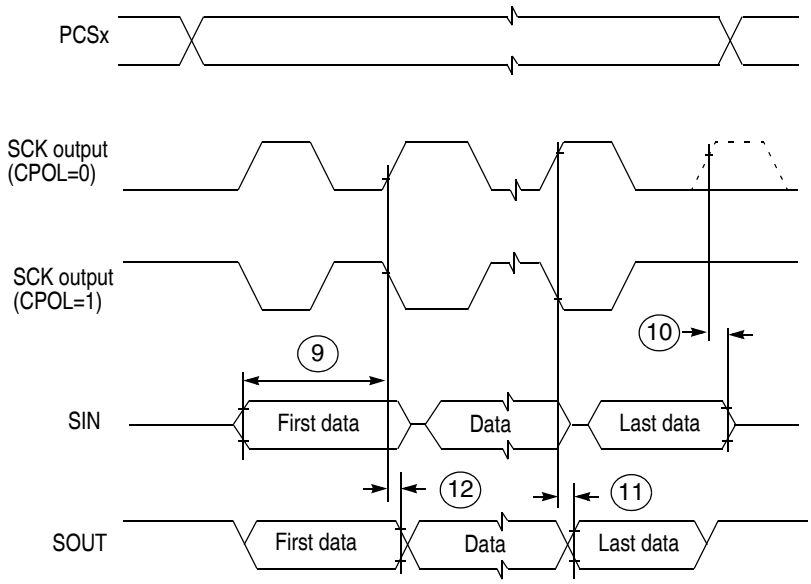



**Figure 22. DSPI Modified Transfer Format Timing—Master, CPHA = 1**

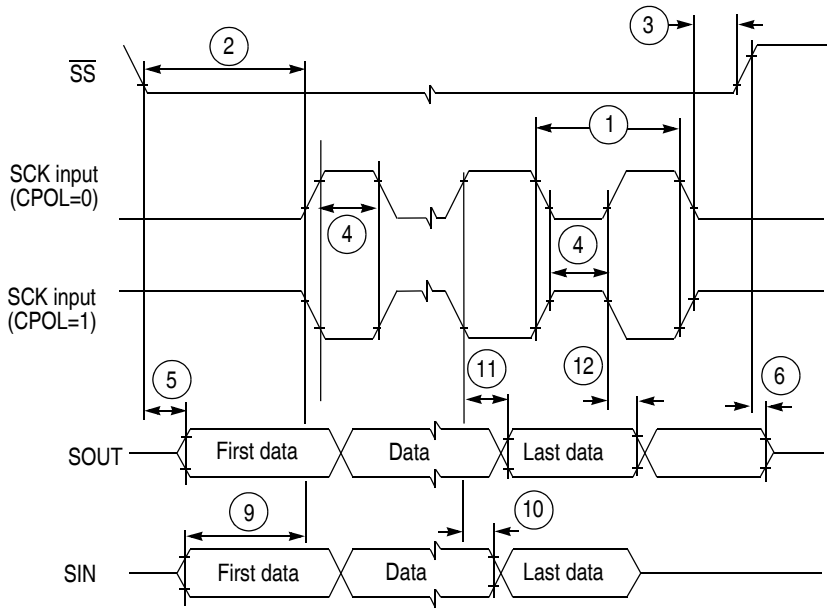



**Figure 23. DSPI Modified Transfer Format Timing—Slave, CPHA = 0**

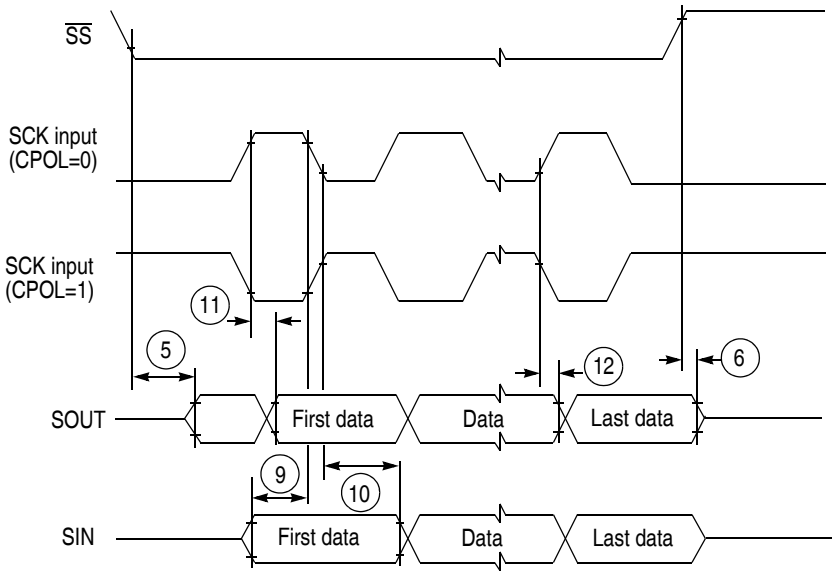



**Figure 24. DSPI Modified Transfer Format Timing—Slave, CPHA = 1**

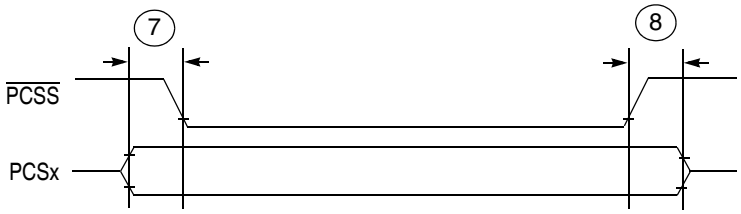



**Figure 25. DSPI PCS Strobe (PCSS) Timing**

## 3.13.8 eQADC SSI Timing

**Table 26. EQADC SSI Timing Characteristics**

| Spec | Rating | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| 2 | FCK period ($t_{FCK} = 1 \div f_{FCK}$) [1, 2] | $t_{FCK}$ | 2 | — | 17 | $t_{SYS_CLK}$ |
| 3 | Clock (FCK) high time | $t_{FCKHT}$ | $t_{SYS_CLK} - 6.5$ | — | $9 \times (t_{SYS_CLK} + 6.5)$ | ns |
| 4 | Clock (FCK) low time | $t_{FCKLT}$ | $t_{SYS_CLK} - 6.5$ | — | $8 \times (t_{SYS_CLK} + 6.5)$ | ns |
| 5 | SDS lead / lag time | $t_{SDS_LL}$ | –7.5 | — | +7.5 | ns |
| 6 | SDO lead / lag time | $t_{SDO_LL}$ | –7.5 | — | +7.5 | ns |
| 7 | EQADC data setup time (inputs) | $t_{EQ_SU}$ | 22 | — | — | ns |
| 8 | EQADC data hold time (inputs) | $t_{EQ_HO}$ | 1 | — | — | ns |

1 $\overline{SS}$ timing specified at $V_{DDEH}$ = 3.0–5.25 V, $T_A = T_L$ to $T_H$, and CL = 25 pF with SRC = 0b11. Maximum operating frequency varies depending on track delays, master pad delays, and slave pad delays.

2 FCK duty cycle is not 50% when it is generated through the division of the system clock by an odd number.

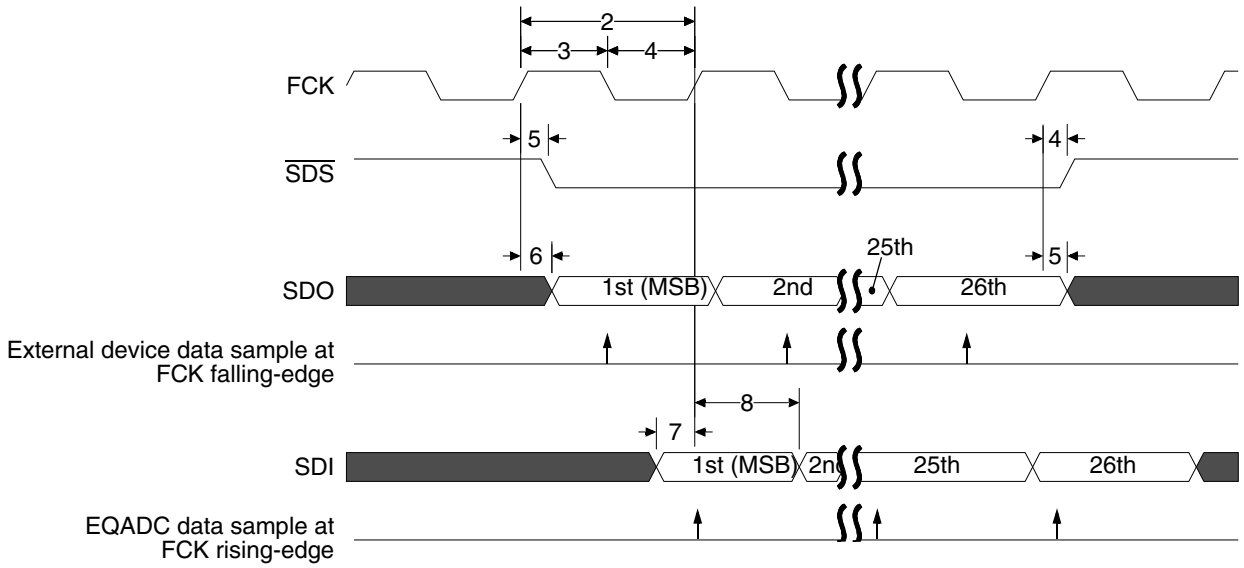



**Figure 26. EQADC SSI Timing**

# 4 Mechanicals

## 4.1 MPC5561 324 PBGA Pinouts

Figure 27 is a pinout for the MPC5561 324 PBGA package.

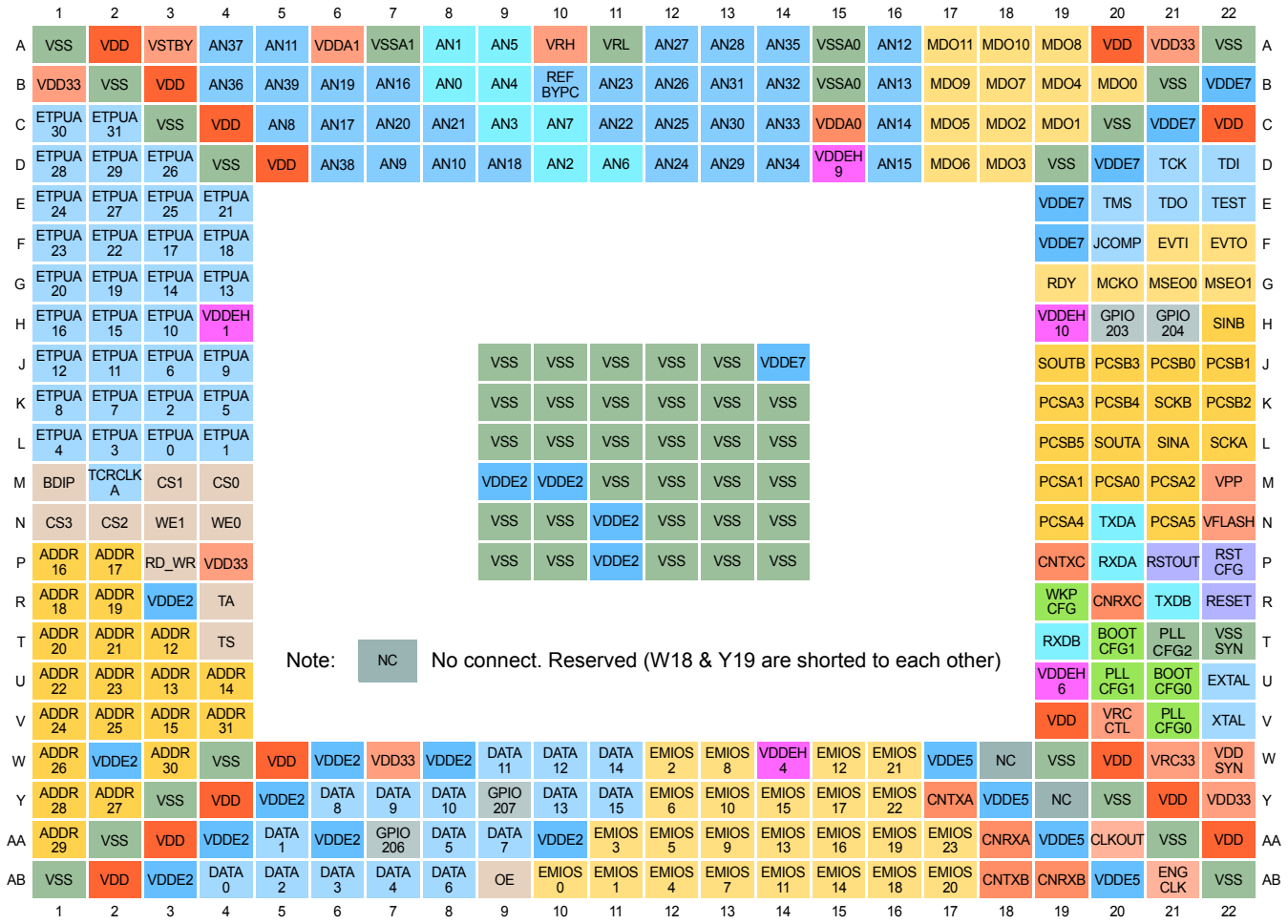



**Figure 27. MPC5561 324 Package**

## 4.2 MPC5561 324-Pin Package Dimensions

The package drawings of the MPC5561 324-pin TEPBGA package are shown in Figure 28.

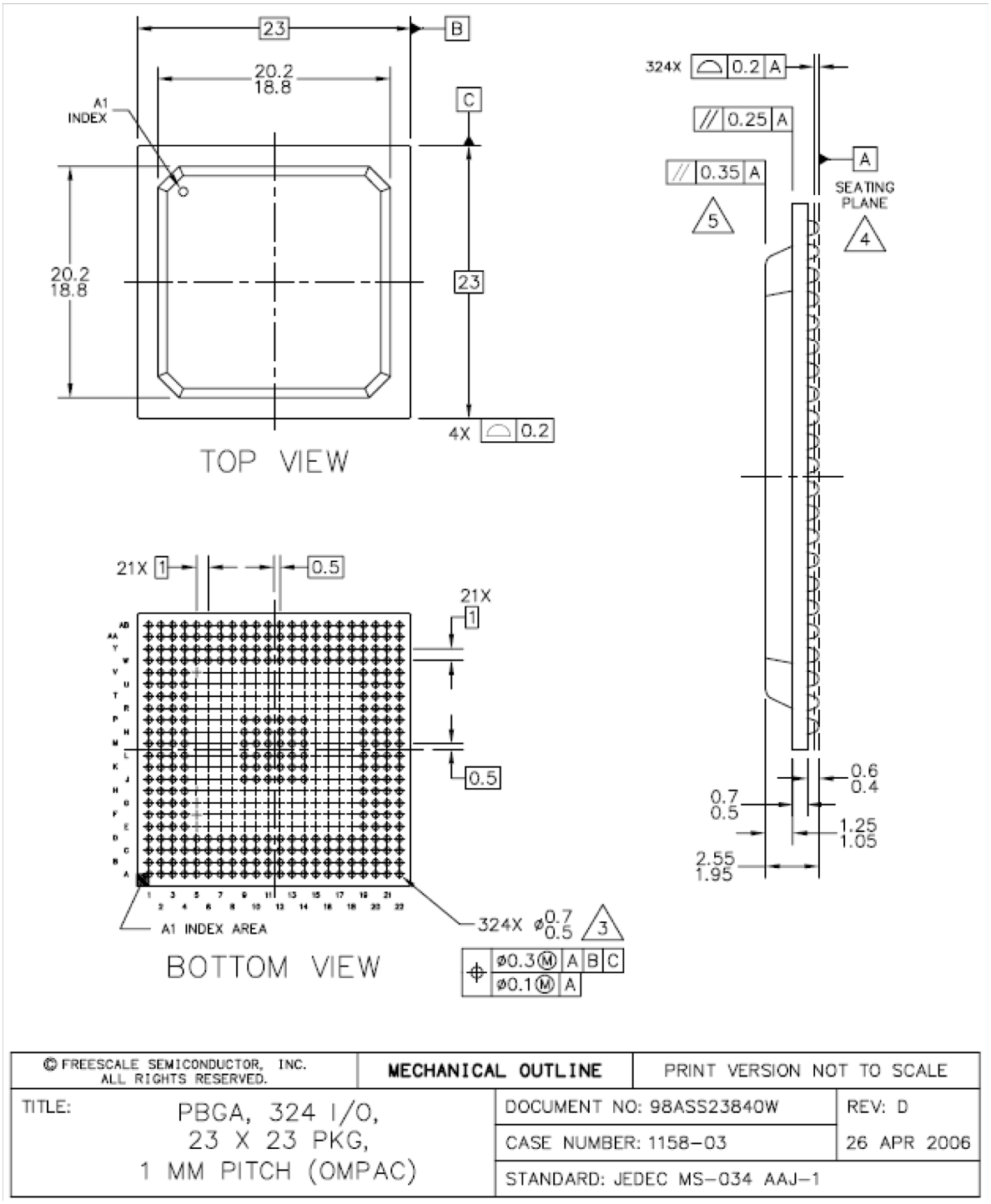



**Figure 28. MPC5561 324 TEPBGA Package**

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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| MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
|---|---|

| TITLE: | DOCUMENT NO: 98ASS23840W | REV: D |
|---|---|---|
| PBGA, 324 I/O,<br>23 X 23 PKG,<br>1 MM PITCH (OMPAC) | CASE NUMBER: 1158–03 | 26 APR 2006 |
| | STANDARD: JEDEC MS–034 AAJ–1 | |

**Figure 28. MPC5561 324 TEPBGA Package (continued)**

# 5 Revision History for the MPC5561 Data Sheet

The history of revisions made to this data sheet are shown in this section. The changes are divided into each revision of this document. The substantive changes incorporated in MPC5561 Data Sheet Rev. 0.0 to produce Rev. 1.0 of this document are grouped as follows:

- Global and text changes
- Table and figure changes

Within each group, the changes are listed in sequential order.

## 5.1 Information Changed Between Revisions 2.0 and 3.0

The following table lists the changes made throughout the document.

**Table 27. Information Changed Between Rev. 2.0 and Rev. 3.0**

| | |
|---|---|
| Section 3.7, "Power-Up/Down Sequencing" | Added the following paragraph in Section 3.7, "Power-Up/Down Sequencing": "During initial power ramp-up, when $V_{stby}$ is 0.6v or above. a typical current of 1-3mA and maximum of 4mA may be seen until VDD is applied. This current will not reoccur until $V_{stby}$ is lowered below Vstby min. specification". |
| | Moved Figure 2 (fISTBY Worst-case Specifications) "ISTBY Worst-case Specifications" to Section 3.7, "Power-Up/Down Sequencing". |
| Section 3.8, "DC Electrical Specifications" | Removed the footnote "Figure 3 shows an illustration of the IDD_STBY values interpolated for these temperature values". |
| | Changed the footnote attached to IDD_STBY to "The current specification relates to average standby operation after SRAM has been loaded with data. For power up current see Section 3.7, "Power-Up/Down Sequencing",Figure 2 (fISTBY Worst-case Specifications)." |
| | In Table 9 (DC Electrical Specifications ($T_A = T_{L\ to}\ T_H$)) the Characteristic "Refer to Figure 3 for an interpolation of this data" changed to "RAM standby current". |

## 5.2 Information Changed Between Revisions 1.0 and 2.0

The following table lists the changes made throughout the document.

**Table 28. Information Changed Between Rev. 1.0 and Rev. 2.0**

| Location | Description of Changes |
|---|---|
| Section 1, "Overview" | |
| | Added new 11th paragraph about FlexRay. Removed discussion in the SIU and DSPI paragraphs about deserialization and serialization, and chaining. Removed reference to SIU_DISR register. |
| Table 6 ($V_{RC}$ and POR Electrical Specifications) *VCR/POR Electrical Specifications*: | |
| | Added to Specs 1, 2 and 3 that reads: On power up, assert $\overline{\text{RESET}}$ before $V_{POR15}$, $V_{POR33}$, and $V_{POR5}$ negate (internal POR). RESET must remain asserted until the power supplies are within the operating conditions as specified in Table 9 *DC Electrical Specifications*. On power down, assert $\overline{\text{RESET}}$ before any power supplies fall outside the operating conditions and until the internal POR asserts. |

**Table 28. Information Changed Between Rev. 1.0 and Rev. 2.0 (continued)**

| Location | Description of Changes |
|---|---|
| Table 9 (DC Electrical Specifications ($T_A = T_{L\ to}\ T_H$)) *DC Electrical Specifications* | • Added footnote that reads: $V_{DDE2}$ and $V_{DDE3}$ are limited to 2.25–3.6 V only if EBTS = 0; $V_{DDE2}$ and $V_{DDE3}$ have a range of 1.6–3.6 V if EBTS =1.<br>• Spec 27a, Operating current 1.5 V supplies @ 135 MHz:<br>-- 8-way 1.65 V typical use: from 630 to 620<br>-- 8-way 1.35 V typical use: from 500 to 440<br>-- 8-way 1.65 V high use: from 785 to 670<br>-- 8-way 1.35 V high use: from 630 to 490<br>-- 4-way 1.65 V high use: from 710 to 620<br>-- 4-way 1.35 V high use: from 550 to 430<br>• Spec 27b, Operating current 1.5 V supplies @ 114 MHz:<br>-- 8-way 1.65 V typical use: from 600 to 590<br>-- 8-way 1.35 V typical use: from 450 to 395<br>-- 8-way 1.65 V high use: from 680 to 580<br>-- 8-way 1.35 V high use: from 500 to 390<br>-- 4-way 1.65 V high use: from 650 to 550<br>-- 4-way 1.35 V high use: from 490 to 385<br>• Spec 27c, Operating current 1.5 V supplies @ 82 MHz:<br>-- 8-way 1.65 V typical use: from 490 to 485<br>-- 8-way 1.35 V typical use: from 360 to 320<br>-- 8-way 1.65 V high use: from 545 to 470<br>-- 8-way 1.35 V high use: from 400 to 315<br>-- 4-way 1.65 V high use: from 530 to 460<br>-- 4-way 1.35 V high use: from 395 to 310<br>• Removed footnote 12 on all these changed values: Preliminary. Specification pending final characterization. |
| Table 17 (Pad AC Specifications (VDDEH = 5.0 V, VDDE = 1.8 V)) *Pad AC Specifications* | • Footnote 1, changed '$V_{DDEH}$ = 4.5–5.5;' to '$V_{DDEH}$ = 4.5–5.25;'<br>• Footnote 1, deleted '$f_{SYS}$ = 132 MHz.'<br>• Footnote 2, changed from 'tested' to '(not tested).'<br>• Footnote 3, changed from 'Out delay. . .' to 'The output delay. . .',<br>• Changed from 'Add a maximum of one system clock to the output delay to get the output delay with respect to the system clock' to 'To calculate the output delay with respect to the system clock, add a maximum of one system clock to the output delay.'<br>• Footnote 4: changed 'Delay' to 'The output delay.'<br>• Footnote 5: deleted 'before qualification.'<br>• Changed from 'This parameter is supplied for reference and is not guaranteed by design and not tested' to 'This parameter is supplied for reference and is guaranteed by design and tested.' |
| *Table 22 (Bus Operation Timing) Bus Operation Timing*: | • External Bus Frequency in the table heading: Added footnote that reads: Speed is the nominal maximum frequency. Max. speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM, and 135 MHz parts allow for 132 MHz system clock + 2% FM.<br>• Spec 1: Changed the values in Min. columns: 40 MHz from 25 to 24.4; 56 MHz from 17.9 to 17.5<br>• Specs 7 and 8: Removed from external bus interface: $\overline{BDIP}$, $\overline{OE}$, TSIZ[0:1], and $\overline{WE}$/$\overline{BE}$[0:3].<br>• Added a footnote each for the DATA[0:31], $\overline{TEA}$, and $\overline{WE}$/$\overline{BE}$[0:3] signals in the table: Due to pin limitations, the DATA[16:31], $\overline{TEA}$, and $\overline{WE}$/$\overline{BE}$[2:3] signals are not available on the 324 package. |

**Table 28. Information Changed Between Rev. 1.0 and Rev. 2.0 (continued)**

| Location | Description of Changes |
|---|---|
| Table 24 (eMIOS Timing) *eMIOS Timing*: | • Footnote 1, changed '$V_{DDEH}$ = 4.5–5.5;' to '$V_{DDEH}$ = 4.5–5.25;'<br>• Deleted (MTS) from the heading, table, and footnotes.<br>• Footnote 1: Deleted '. . .$f_{SYS}$ = 132 MHz. . .', '. . .$V_{DD33}$ and $V_{DDSYN}$ = 3.0–3.6 V. . .' and ' . . .and CL = 200 pF with SRC = 0b11.'<br>• Added Footnote 2: 'This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).' |
| Table 25 (DSPI Timing') *DSPI Timing*: | • Footnote 1, changed '$V_{DDEH}$ = 4.5–5.5;' to '$V_{DDEH}$ = 4.5–5.25;'<br>• Table Title: Added footnote that reads: Speed is the nominal maximum frequency. Max. speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM, and 135 MHz parts allow for 132 MHz system clock + 2% FM. |
| Table 26 (EQADC SSI Timing Characteristics) *EQADC SSI Timing Characteristics*: | • Footnote 1, changed '$V_{DDEH}$ = 4.5–5.5;' to '$V_{DDEH}$ = 4.5–5.25;'<br>• Deleted from table title '(Pads at 3.3 V or 5.0 V)'<br>• Deleted 1st line in table 'CLOAD = 25 pF on all outputs. Pad drive strength set to maximum.'<br>• Spec 1: FCK frequency -- removed.<br>• Combined footnotes 1 and 2, and moved the new footnote to Spec 2. Moved old footnote 3 to Spec 2.<br>• Footnote 1, deleted '$V_{DD}$ = 1.35–1.65 V' and '$V_{DD33}$ and $V_{DDSYN}$ = 3.0–3.6V.'<br>Changed 'CL = 50 pF' to 'CL = 25 pF.'<br>• Footnote 2: added 'cycle' after 'duty' to read: FCK duty cycle is not 50% when . . . . |
| Figure 27 (MPC5561 324 Package) *MPC5561 324 PBGA Pinouts:* | • Changed ball labels on the 324 PBGA to show only signals available on the device:<br>• C1 -> PSCS3, C2 -> PCSC4,<br>• D1 -> PCSC1, D2 -> PCSC2, D3 -> $\overline{IRQ}$14<br>• E1 -> $\overline{IRQ}$12, E2 -> $\overline{IRQ}$15, E3 -> $\overline{IRQ}$13, E4 -> $\overline{IRQ}$9<br>• F1 -> $\overline{IRQ}$11, F2 -> $\overline{IRQ}$10, F3 -> PDI_DATA6, F4 -> PDI_DATA7<br>• G1 -> $\overline{IRQ}$8, G2 -> PDI_DATA8, G3 -> PCSB4, G4 -> PCSB3<br>• H1 -> PDI_DATA5, H2 -> PCSB5, H3 -> PDICHSEL2<br>• J1 -> PCSB1, J2 -> PDI_DATA0, J3 -> FRN_RX, J4 -> PDICHSEL1<br>• K1 -> PDICHSEL0, K2 -> GPIO121, K3 -> PDI_FRAME_VALID, K4 -> FRBTXEN, K19 -> RXDD<br>• L1 -> FRBTX, L2 -> PDISNCLK, L3 -> GPIO114, L4 -> PDILINEVALID, L20 -> PCSC5, L21 -> PCSC2, L22 -> PCSC1<br>• M2 -> IRQ7, M19 -> PCSB2, M20 -> TXDC, M21 -> TXDD<br>• N19 -> RXDC, N21 -> PCSB3<br>• AB18 -> PCSC3, AB19 -> PCSC4 |

## 5.3 Information Changed Between Revisions 0.0 and 1.0

The following table lists the global changes made throughout the document, as well as substantive changes to text that is not in a table of figure.

**Table 29. Global and Text Changes Between Rev. 0.0 and Rev. 1.0**

| Location | Description of Changes |
|---|---|
| Global Changes throughout the document | • Replaced kilobytes with KB.<br>• Replaced megabytes with MB. |
| Section 1, "Overview": | • First paragraph: text changed from ". . . based on the PowerPC Book E architecture" to ". . . built on the Power Architecture embedded technology."<br>• Second paragraph: Changed terminology from PowerPC Book E architecture to Power Architecture terminology.<br>• Added new third paragraph about VLE feature.<br>• Added new eighth paragraph about the parallel digital interface (PDI).<br>• Paragraph nine: changed "the MPC5561 has an on-chip 20-channel enhanced queued analog-to-digital converter (eQADC)" to ". . . has an on-chip 40-channel dual enhanced queued . . ."<br>• Added the sentence preceding Table 1: 'Unless noted in this data sheet, all specifications apply from $T_L$ to $T_H$.' |
| Sections 3.7.1, 3.7.2 and 3.7.3: Reordered sections resulting in the following order and section renumbering: | • Section 3.7.1, "Input Value of Pins During POR Dependent on VDD33," then<br>• Section 3.7.2, "Power-Up Sequence (VRC33 Grounded)," then<br>• Section 3.7.3, "Power-Down Sequence (VRC33 Grounded). |
| Section 3.7.1, "Input Value of Pins During POR Dependent on VDD33," changed: | From: 'To avoid accidentally selecting the bypass clock because PLLCFG[0:1] and RSTCFG are not treated as ones (1s) when POR negates, $V_{DD33}$ must not lag $V_{DDSYN}$ and the RESET pin power ($V_{DDEH6}$) when powering the device by more than the $V_{DD33}$ lag specification in Table 6. $V_{DD33}$ individually can lag either $V_{DDSYN}$ or the RESET power pin ($V_{DDEH6}$) by more than the $V_{DD33}$ lag specification. $V_{DD33}$ can lag one of the $V_{DDSYN}$ or $V_{DDEH6}$ supplies, but cannot lag both by more than the $V_{DD33}$ lag specification. This $V_{DD33}$ lag specification only applies during power up. $V_{DD33}$ has no lead or lag requirements when powering down.'<br>To:<br>'When powering the device, $V_{DD33}$ must not lag $V_{DDSYN}$ and the RESET power pin ($V_{DDEH6}$) by more than the $V_{DD33}$ lag specification listed in Table 6. This avoids accidentally selecting the bypass clock mode because the internal versions of PLLCFG[0:1] and RSTCFG are not powered and therefore cannot read the default state when POR negates. $V_{DD33}$ can lag $V_{DDSYN}$ or the RESET power pin ($V_{DDEH6}$), but cannot lag both by more than the $V_{DD33}$ lag specification. This $V_{DD33}$ lag specification only applies during power up. $V_{DD33}$ has no lead or lag requirements when powering down.' |
| Section 3.7.1, "Input Value of Pins During POR Dependent on VDD33:" | Added the following text directly before this section and after Table 8 *Pin Status for Medium / Slow Pads During the Power-on Sequence*:<br>'The values in Table 7 and Table 8 do not include the effect of the weak pull devices on the output pins during power up.<br><br>Before exiting the internal POR state, the voltage on the pins goes to high-impedance until POR negates. When the internal POR negates, the functional state of the signal during reset applies and the weak pull devices (up or down) are enabled as defined in the device *Reference Manual*. If $V_{DD}$ is too low to correctly propagate the logic signals, the weak-pull devices can pull the signals to $V_{DDE}$ and $V_{DDEH}$.<br><br>To avoid this condition, minimize the ramp time of the $V_{DD}$ supply to a time period less than the time required to enable the external circuitry connected to the device outputs.' |
| Section 3.7.3, "Power-Down Sequence (VRC33 Grounded)" | Deleted the underscore in ORed_POR to become ORed POR. |
| Section 3.13.6, "eTPU Timing" | Deleted entire section, including table and figure, because the MPC5561 does not have the eTPU module. |

The following table describes the changes made to information in tables and figures:

**Table 30. Table and Figure Changes Between Rev. 0.0 and 1.0**

| Location | Description of Changes |
|---|---|
| Figure 1 (MPC5500 Family Part Number Example) *MPC5500 Family Part Numbers*: | • Removed the 2 in the tape and reel designator in both the graphic and in the Tape and Reel Status text.<br>• Changed Qualification Status by adding ‘, general market flow’ to the M designator, and added an ‘S’ designator with the description of ‘Fully spec. qualified, automotive flow.<br>• Changed footnote 1 to read: All devices are PPC5561, rather than MPC5561 or SPC5561, until product qualifications are complete. Not all configurations are available in the PPC parts. |
| Table 1 (Orderable Part Numbers) *Orderable Part Numbers*: | • Increased the frequency values in the Maximum column by 2 ns.<br>• Changed the maximum operating frequency from 132 MHz to 135 MHz.<br>• Reordered rows to group devices by lead-free package types in descending frequency order, and leaded package types.<br>• Footnote 2: added ‘ambient’ between ‘lowest’ and ‘operating’ and ‘highest’ and ‘operating.’<br>• Changed footnote 3 from ‘132 MHz allows only 128 MHz + 2% FM’ to ‘135 MHz allows for 132 MHz + 2% FM’. |
| Table 2 (Absolute Maximum Ratings) *Absolute Maximum Ratings*: | • Deleted Spec 3, “Flash core voltage.”<br>• Spec 12 “DC Input Voltage”: Deleted from second line‘. . .except for eTPUB15 and SINB (DSPI_B_SIN)’ leaving $V_{DDEH}$ powered I/O pads. Deleted third line ‘$V_{DDEH}$ powered by I/O pads (eTPUB15 and SINB), including the min. and max values of -0.3 and 6.5 respectively, and deleted old footnote 7.<br>• Spec 12 “DC Input Voltage”: Added footnote 8 to second line “$V_{DDE}$ powered I/O pads” that reads: ‘Internal structures hold the input voltage less than the maximum voltage on all pads powered by the $V_{DDE}$ supplies, if the maximum injection current specification is met (s mA for all pins) and $V_{DDE}$ is within the operating voltage specifications.<br>• Spec 14, column 2, changed: ‘$V_{SS}$ differential voltage’ to ‘$V_{SS}$ to $V_{SSA}$ differential voltage.’<br>• Spec 15, column 2, changed: ‘$V_{DD}$ differential voltage’ to ‘$V_{DD}$ to $V_{DDA}$ differential voltage.’<br>• Spec 21, Added the name of the spec, ‘*$V_{RC33}$ to $V_{DDSYN}$ differential voltage,’* as well as the name and cross reference to Table 9, *DC Electrical Specification*s, to which the Spec was moved.<br>• Spec 28 “Maximum Solder Temperature”: Added two sublines:<br>Lead free (PbFree) and Leaded (SnPb) with maximum values of 260 C and 245 C respectively.<br>• Footnote 1, added: ‘any of’ between ‘beyond’ and ‘the listed maxima.’<br>• Deleted footnote 2: ‘Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.’Spec 26 “Maximum Operating Temperature Range”: replaced -40 C with $T_L$.<br>• Footnote 6 (now footnote 5): Added the following sentence to the end, “Keep the negative DC voltage greater than -0.6 V on SINB during the internal power-on reset (POR) state.” |
| Table 4 (EMI Testing Specifications) *EMI Testing Specifications*: | • Changed the maximum operating frequency to from 132 to $f_{MAX}$.<br>• Footnote 2: Deleted ‘Refer to Table 1 for the maximum operating frequency.’ |

**Table 30. Table and Figure Changes Between Rev. 0.0 and 1.0 (continued)**

| Location | Description of Changes |
|---|---|
| Table 5 (ESD Ratings ,) *ESD Characteristics*: Added *(Electromagnetic Static Discharge)* in the table title. | |
| Table 6 ($V_{RC}$ and POR Electrical Specifications) *VCR/POR Electrical Specifications*: | • Subscript all symbol names that appear after the first underscore character.<br>• Specs 7 and 10: added 'at Tj 'at the end of the first line in the second column: Characteristic.<br>• Footnote 10: Deleted 'Preliminary value. Final specification pending characterization."<br>• Added to Spec 2:<br>3.3 V ($V_{DDSYN}$) POR negated (ramp down) Min. 0.0 Max. 0.30 V<br>3.3 V ($V_{DDSYN}$) POR asserted (ramp up) Min. 0.0 Max. 0.30 V<br>• Spec 3: Added new footnote 3 for both lines: 'It is possible to reach the current limit during ramp up--do not treat this event as a short circuit current.'<br>• Spec 5: Changed old Footnote 1 (now footnote 2): 'User must be able to supply full operating current for the 1.5V supply when the 3.3V supply reaches this range." to 'Supply full operating current for the 1.5 V supply when the 3.3 V supply reaches this range."<br>• Spec 10:<br>  • Changed the minimum values of: -40 C = 60; 25 C = 65; 150 C = 85.<br>  • Added old footnote 5 as new footnote 6.<br>  • Removed 'Tj 'after '150 C' in the last line, second column: Characteristic.<br>  • Added a new footnote 7, 'Refer to Table 1 for the maximum operating frequency.'<br>  • Rewrote old footnote 7(new footnote 9) to: Represents the worst-case external transistor BETA. It is measured on a per part basis and calculated as ($I_{DD}$ ÷ $I_{VRCCTL}$).<br>  • Added cross-reference to footnote 6: '$I_{VRCCTL}$ is measured at the following conditions: $V_{DD}$ = 1.35 V, $V_{RC33}$ = 3.1 V, $V_{VRCCTL}$ = 2.2 V.' Changed '(@ $V_{DD}$ = 1.35 V, $f_{sys}$ = $f_{MAX}$)' to '(@ $f_{sys}$ = $f_{MAX}$).'<br>• Added new footnote 1 to Spec 3: " $V_{IL_S}$ (Table 9, Spec 15) is guaranteed to scale with $V_{DDEH6}$ down to $V_{POR5}$.<br>• Rewrote old footnote 7(new footnote 9) to: Represents the worst-case external transistor BETA. It is measured on a per part basis and calculated as ($I_{DD}$ ÷ $I_{VRCCTL}$).<br>• Deleted old footnote 8: 'Preliminary value. Final specification pending characterization.' |
| Table 7 (Pin Status for Fast Pads During the Power Sequence) *Power Sequence Pin Status for Fast Pads* | • Changed title to *Pin Status for Fast Pads During the Power Sequence*<br>• Changed preceding paragraph<br>From: Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies depending on power. Prior to exiting POR, the pads are in a high impedance state (Hi-Z).<br>To: There are no power up/down sequencing requirements to prevent issues such as latch-up, excessive current spikes, and so on. Therefore, the state of the I/O pins during power up/down varies depending on which supplies are powered.<br>• Deleted the 'Comment' column.<br>• Added a POR column after the $V_{DD}$ column.<br>• Added row 2:' $V_{DDE}$, Low, Low, Asserted, High' and row 5: $V_{DDE}$, $V_{DD33}$, $V_{DD}$, Asserted, Hi-Z. |
| Table 8 (Pin Status for Medium and Slow Pads During the Power Sequence) *Power Sequence Pin Status for Medium/Slow Pads:* | • Changed title to *Pin Status for Medium and Slow Pads During the Power Sequence*<br>• Updated preceding paragraph.<br>• Deleted the 'Comment' column.<br>• Added a POR column after the $V_{DD}$ column.<br>• Added row 3:' $V_{DDEH}$, $V_{DD}$, Asserted, Hi-Z.' |

**Table 30. Table and Figure Changes Between Rev. 0.0 and 1.0 (continued)**

| Location | Description of Changes |
|---|---|
| Table 9 (DC Electrical Specifications ($T_A = T_{L\ to}\ T_H$)) *DC Electrical Specifications*: | • Spelled out meaning of the slash '/' as 'and' as well as 'I/O' as 'input/output.' Sentence still very confusing. Deleted 'input/output' from the specs to improve clarity.<br>• Spec 20, column 2, *Characteristics*,' Slow and medium output high voltage ($I_{OH_S}$ = –2.0 mA):' Created a left-justified second line and moved '$I_{OH_S}$ = –2.0 mA' from the 1st line to the second line and deleted the parentheses. Created a left-justified third line that reads '$I_{OH_S}$ = –1.0 mA.'<br>• Spec 20, column 4, *Min.*: Added a blank line before and after '0.80 × $V_{DDEH}$' and put '0.85 × $V_{DDEH}$' on the last line.<br>• Spec 22, column 2,'*Slow and medium output low voltage ($I_{OL_S}$ = 2.0 mA)*:' Created a left-justified second line and moved '$I_{OL_S}$ = 2.0 mA.' from the 1st line to the second line and deleted the parentheses. Created a left-justified third line that reads '$I_{OL_S}$ = 1.0 mA.'<br>• Spec 22, column 5, *Max.*: Added a blank line before and after '0.20 × $V_{DDEH}$' and put '0.15 × $V_{DDEH}$' on the last line.<br>• Spec 26: Changed 'AN[12]_MA[1]_SDO' to 'AN[13]_MA[1]_SDO'.<br>• Spec 27a: Changed 132 MHz to 135 MHz. Added maximum values for 8-way cache:<br>1.65 typical = 630<br>1.35 typical = 500<br>1.65 high = 785<br>1.35 high = 630<br>All 8-way cache max values have footnote 11.<br>Added 4-way cache with footnote 10:<br>1.65 high = 685 with footnote 11<br>1.35 high = TBD with footnote 12<br>• Spec 27b, Operating current 1.5 V supplies @ 114 MHz: Added maximum values for 8-way cache:<br>1.65 typical = 600,<br>1.35 typical = 450,<br>1.65 high = 680,<br>1.35 high = 500.<br>All 8-way cache max values have footnote 11.<br>Added 4-way cache with footnote 10:<br>1.65 and 1.35 high = TBD with footnote 12 |
| Table 9 (DC Electrical Specifications ($T_A = T_{L\ to}\ T_H$)) *DC Electrical Specifications*: (continued) | • Spec 27c, Operating current 1.5 V supplies @ 82 MHz: Added maximum values for 8-way cache:<br>1.65 typical = 490,<br>1.35 typical = 360,<br>1.65 high = 520,<br>1.35 high = 390.<br>All 8-way cache max values have footnote 11.<br>Added 4-way cache values<br>1.65 high = TBD and 1.35 high = TBD, both with footnote 12.<br>• Spec 28: Changed 132 MHz to 135 MHz.<br>• Spec 29: Deleted frequency information.<br>• Corrected footnote 3 to read: If standby operation is not required, connect the $V_{STBY}$ to ground.<br>• Combined old footnotes 11 and 12 for new footnote 6 and added to specs 27a, b, and c on the 8-way cache line that reads: Eight-way cache enabled (L1CSR0[CORG] = 0b0).<br>• Added footnote 10 to specs 27a, b, and c on the 4-way cache line that reads: Four-way cache enabled (L1CSR0[CORG] = 0b1) or (L1CSR0[CORG] = 0b0 with L1CSR0[WAM] = 0b1, L1CSR0[WID] = 0b1111, L1CSR0[WDD] = 0b1111, L1CSR0[AWID] = 0b1, and L1CSR0[AWDD] = 0b1).<br>• Added footnote 11 to specs 27a, b, and c on the max numeric values: "Preliminary. Specification pending final characterization."<br>• Added footnote 12 to specs 27a, b, and c on the max TBD values: "Specification pending final characterization." |

**Table 30. Table and Figure Changes Between Rev. 0.0 and 1.0 (continued)**

| Location | Description of Changes |
|---|---|
| Figure 2 (fISTBY Worst-case Specifications) | Added figure to show interpolated $IDD_{STBY}$ values listed in Table 9 (DC Electrical Specifications ($T_A = T_{L\ to}\ T_H$)). |
| Table 12 (FMPLL Electrical Specifications) | *FMPLL Electrical Characteristics*:<br>• Added ($T_A = T_L - T_H$) to the second line of the table title.<br>• Spec 1, footnote 1 in column 2: *'PLL reference frequency range.'*: Changed to read 'Nominal crystal and external reference values are worst-case not more than 1%. The device operates correctly if the frequency remains within ± 5% of the specification limit. This tolerance range allows for a slight frequency drift of the crystals over time. The designer must thoroughly understand the drift margin of the source clock.'<br>• Spec 1, added two more lines to the *PLL reference frequency range*' to read as follows:<br>crystal reference (20) fref_crystal 8 ≤ 20<br>crystal reference (40) fref_crystal > 20 40<br>external reference (20) fref_ext 8 ≤ 20<br>external reference (40) fref_ext > 20 40<br>• Spec 1, footnote 2 in column 2: *'PLL reference frequency range.'*: Changed to: 'The 8–20 MHz crystal or external reference values have PLLCFG[2] pulled low' and applies to spec 1, column 2, crystal reference and external reference.<br>• Spec 1, footnote 2 in column 2: *'PLL reference frequency range,'* Changed to: The 20–40 MHz crystal and external reference values have PLLCFG[2] pulled high, and the minimum frequency must be greater than 20 MHz. Use the 8–20 MHz setting (PLLCFG[2] pulled low) if a 20 MHz crystal or external reference is required. To exit $\overline{\text{RESET}}$ when using 40 MHz, set PLLCFG[2] to 1.<br>• Specs 12 and 13: Grouped (2 x CI).<br>• Spec 21, column 2: Changed $f_{ref_crystal}$ to $f_{ref}$ in ICO frequency equation, and added the same equation but substituted $f_{ref_ext}$ for $f_{ref}$ for the external reference clock, giving:<br>$f_{ico} = [\ f_{ref_crystal} \times (MFD + 4)\ ] \div (PREDIV + 1)$<br>$f_{ico} = [\ f_{ref_ext} \times (MFD + 4)\ ] \div (PREDIV + 1)$<br>• Spec 21, column 4, Max.: Deleted old footnote 18 that reads:<br>The ICO frequency can be higher than the maximum allowable system frequency. For this case, set the CMPLL synthesizer control register reduced frequency divider (FMPLL_SYNCR[RFD]) to divide-by-two (RFD = 0b001). Therefore, for a 40 MHz maximum device (system frequency), program the FMPLL to generate 80 MHz at the ICO output and then divide-by-two the RFD to provide the 40 MHz system clock.'<br>• Spec 21: Changed column 5 from '82 or 66 MHz' to: '150'.<br>• Spec 22: Changed column 4, *Max. Value* from $f_{MAX}$ to 20, and added footnote 20 to read, 'Maximum value for dual controller (1:1) mode is ($f_{MAX} \div 2$) and the predivider set to 1 (FMPLL_SYNCR[PREDIV] = 0b001).' |
| Table 13 (eQADC Conversion Specifications (TA = TL to TH)) | *eQADC Conversion Specifications*: Added ($T_A = T_L - T_H$) to the table title. |
| Table 14 (Flash Program and Erase Specifications ($T_A = T_L$ to $T_H$)) | *Flash Program and Erase Specifications:*<br>• Added ($T_A = T_L - T_H$) to the table title.<br>• Specs 7, 8, 9, and 10:<br>Changed typical values — 48 KB: from 340 to 345; 64 KB: from 400 to 415<br>Spec 8, 128KB block pre-program and erase time, Max. column value from 15,000 to 7,500.<br>• Moved footnote 1 from the table title to directly after the 'Typical' in the column 5 header.<br>• Footnote 2: Changed from: 'Initial factory condition: ≤ 100 program/erase cycles, 25 °C, typical supply voltage, 80 MHz minimum system frequency.' to: 'Initial factory condition: ≤ 100 program/erase cycles, 25 °C, using a typical supply voltage measured at a minimum system frequency of 80 MHz.' |
| Table 15 (Flash EEPROM Module Life ($T_A = T_L$ to $T_H$)) | *Flash EEPROM Module Life*:<br>• Replaced (Full Temperature Range) with ($T_A = T_L - T_H$) in the table title.<br>• Spec 1b, Min. column value changed from 10,000 to 1,000. |

**Table 30. Table and Figure Changes Between Rev. 0.0 and 1.0 (continued)**

| Location | Description of Changes |
|---|---|
| Table 16 (FLASH_BIU Settings vs. Frequency of Operation) *FLASH BIU Settings vs. Frequency of Operations*: | • Changed the Maximum Operating Frequency column entry from: Up to and including132 MHz to: Up to and including134 MHz.<br>• Added footnote 1 to the end of the table title, The footnote reads: 'Illegal combinations exist. Use entries from the same row in this table.'<br>• Moved footnote 2:' For maximum flash performance, set to 0b11' to the 'DPFEN' column header.<br>• Deleted the x-refs in the 'DPFEN' column for the rows.<br>• Created a x-ref for footnote 2 and inserted in the 'IPFEN' column header.<br>• Deleted the x-refs in the 'IPFEN' column for the rows.<br>• Moved footnote 3:' For maximum flash performance, set to 0b110' to the 'PFLIM' column header.<br>• Deleted the x-refs in the 'PFLIM' column for the rows.<br>• Moved footnote 4:' For maximum flash performance, set to 0b1' to the 'BFEN' column header.<br>• Deleted the x-refs in the 'BFEN' column for the rows.<br>• Changed footnote 6 from: 'Allows for 128 MHz system clock with 2% frequency modulation' to: 'Allows for 132 MHz system clock with 2% frequency modulation.' |
| Table 17 (Pad AC Specifications (VDDEH = 5.0 V, VDDE = 1.8 V)) *Pad AC Specifications* and Table 18 (Derated Pad AC Specifications (VDDEH = 3.3 V, VDDE = 3.3 V)) *Derated Pad AC Specifications*: | • Footnote 1, deleted '$f_{SYS}$ = 132 MHz.'<br>• Footnote 2, changed from 'tested' to '(not tested).'<br>• Footnote 3, changed from 'Out delay. . .' to 'The output delay. . .',<br>• Changed from 'Add a maximum of one system clock to the output delay to get the output delay with respect to the system clock' to 'To calculate the output delay with respect to the system clock, add a maximum of one system clock to the output delay.'<br>• Footnote 4: changed 'Delay' to 'The output delay.'<br>• Footnote 5: deleted 'before qualification.'<br>• Changed from 'This parameter is supplied for reference and is not guaranteed by design and not tested' to 'This parameter is supplied for reference and is guaranteed by design and tested.' |
| Table 19 (Reset and Configuration Pin Timing) *Reset and Configuration Pin Timing*: Footnote 1, deleted '$f_{SYS}$ = 132 MHz.' | |
| Table 20 (JTAG Pin AC Electrical Characteristics) *JTAG Pin AC Electrical Characteristics*: | • Footnote 1, deleted: '$f_{SYS}$ = 132 MHz.' and ', and CL = 30 pF with DSC = 0b10, SRC = 0b11'<br>• Footnote 1, changed 'functional' to 'Nexus.' |
| Table 21 (Nexus Debug Port Timing) *Nexus Debug Port Timing*. | • Changed Spec 12, TCK Low to TDO Data Valid: Changed 'VDDE = 3.0 to 3.6 volts' maximum value in column 4 from 9 to 10. Now reads 'VDDE = 3.0–3.6 V' with a max value of 10.<br>• Footnote 5, changed from 'to MCKO. The timing is. . .' to: 'to 'MCKO and is . . .' |
| Table 22 (Bus Operation Timing) *Bus Operation Timing*: | • Changed Spec 1 for the minimum 67 MHz column from: 15.2 to 14.9.<br>• Specs 5 and 6: corrected format to show the bus timing values for various frequencies with EBTS bit = 0 and EBTS bit = 1. |
| Table 23 (External Interrupt Timing) *External Interrupt Timing*: | • Footnote 1: Deleted '$f_{SYS}$ = 132 MHz', '.$V_{DD33}$ and $V_{DDSYN}$ = 3.0–3.6 V' and 'and CL = 200 pF with SRC = 0b11.'<br>• Deleted second figure after table 'External Interrupt Setup Timing.' |

**Table 30. Table and Figure Changes Between Rev. 0.0 and 1.0 (continued)**

| Location | Description of Changes |
|---|---|
| Table 24 *eTPU Timing*, Figure 16 *eTPU Timing* and Figure 17 *eTPU Input/Output Timing:* | Deleted – No eTPU in MPC5561. |
| Table 24 (eMIOS Timing) *eMIOS Timing*: | • Deleted (MTS) from the heading, table, and footnotes.<br>• Footnote 1: Deleted '. . .$f_{SYS}$ = 132 MHz. . .', '. . .$V_{DD33}$ and $V_{DDSYN}$ = 3.0–3.6 V. . .' and ' . . .and CL = 200 pF with SRC = 0b11.'<br>• Added Footnote 2: 'This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).' |
| Figure 16 (eMIOS Timing) *eMIOS Timing* | Added figure. |
| Table 25 (DSPI Timing') *DSPI Timing*: | • Added to beginning of footnote 1 'All DSPI timing specifications use the fastest slew rate (SRC = 0b11) on pad type M or MH. DSPI signals using pad types of S or SH have an additional delay based on the slew rate.'<br>• Footnote 1: Deleted '$V_{DD}$ = 1.35–1.65 V' and '$V_{DD33}$ and $V_{DDSYN}$ = 3.0–3.6 V. |
| Table 26 (EQADC SSI Timing Characteristics) *EQADC SSI Timing Characteristics*: | • Deleted from table title '(Pads at 3.3 V or 5.0 V)'<br>• Deleted 1st line in table 'CLOAD = 25 pF on all outputs. Pad drive strength set to maximum.'<br>• Spec 1: FCK frequency -- removed.<br>• Combined footnotes 1 and 2, and moved the new footnote to Spec 2. Moved old footnote 3 to Spec 2.<br>• Footnote 1, deleted '$V_{DD}$ = 1.35–1.65 V' and '$V_{DD33}$ and $V_{DDSYN}$ = 3.0–3.6V.'<br>Changed 'CL = 50 pF' to 'CL = 25 pF.'<br>• Footnote 2: added 'cycle' after 'duty' to read: FCK duty cycle is not 50% when . . . . |
| Figure 27 (MPC5561 324 Package) *MPC5561 324 Package*: | • Changed ball label T21 from VRCVSS to PLLCFG2.<br>• Deleted the version number and date. |

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