AT30TSE004A

Integrated Temperature Sensor with Serial EEPROM

DATASHEET

Features

- Integrated Temperature Sensor (TS) + 4-Kbit Serial EEPROM
- JEDEC JC42.4 (TSE2004av) DIMM Serial Presence Detect (SPD) + TS compliant
- Low voltage operation
  - Optimized for V_{CC} range of 1.7V to 3.6V
- 2-wire serial interface: I^2C Fast Mode Plus (FM+) compatible
  - 100kHz, 400kHz, and 1MHz compatibility
  - Bus Timeout supported
- Schmitt Trigger, filtered inputs for noise suppression
- Industry standard green (Pb/Halide-free/RoHS compliant) package options
  - 8-pad Ultra Thin DFN (2 x 3 x 0.6mm)
  - 8-pad Very Very Thin DFN (2 x 3 x 0.8mm)

Temperature Sensor Features

- Highly accurate B-grade temp. measurements requiring no external components
  - ±1.0°C accuracy (maximum) over the +75°C to +95°C range
  - ±2.0°C accuracy (maximum) over the +40°C to +125°C range
  - ±3.0°C accuracy (maximum) over the -20°C to +125°C range
- 11-bit ADC temperature-to-digital converter with 0.125°C resolution
- Programmable hysteresis threshold: off, 0°C, 1.5°C, 3°C, and 6°C
- Low operating current
  - Temperature sensor active ~0.2mA (typical)

Serial EEPROM Features

- Integrates 4-Kbits of Serial EEPROM
  - Internally organized into four quadrants of 128-bytes each
- Individual Reversible Software Write Protection on all four 128-byte quadrants
- Supports byte and Page Write operations
- Self-timed write cycle (5ms maximum)
- High-reliability
  - Endurance: 1,000,000 write cycles
  - Data retention: 100 years
- Low operating current
  - Serial EEPROM Write ~1.5mA (typical)
  - Serial EEPROM Read ~0.2mA (typical)

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1. Description

The Atmel® AT30TSE004A is a combination Serial EEPROM and temperature sensor device containing 4096-bits of Serially Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 512-bytes of eight bits each. The Serial EEPROM operation is tailored specifically for DRAM memory modules with Serial Presence Detect (SPD) to store a module's vital product data such as the module's size, speed, voltage, data width, and timing parameters.

The AT30TSE004A is protocol compatible with the legacy JEDEC TSE2002av specification (2-Kbit) devices enabling the AT30TSE004A to be utilized in legacy applications without any software changes. The Serial EEPROM deploys special software commands to allow users to identify and set which half of the memory the internal address counter is located. This special page addressing method used to select the upper or lower half of the Serial EEPROM is the key to the legacy compatibility; however, there is one minor exception to the legacy compatibility as the AT30TSE004A does not support the Permanent Write Protection feature because it was removed from the JEDEC TSE2004a (DDR4) specification.

In addition, the Serial EEPROM incorporates a Reversible Software Write Protection (RSWP) feature enabling the ability to selectively write protect any or all of the four 128-byte quadrants. Once the RSWP is set, it can only be reversed by sending a special software command sequence.

The integrated temperature sensor converts temperatures from -20°C to +125°C to a digital word and provides an accuracy of ±1°C (max.) in the temperature range +75°C to +95°C. The temperature sensor continuously monitors temperature and updates the data in the Temperature Register at least eight times per second. The temperature data is latched internally by the device and may be read by software via a bus Master at anytime (even when the Serial EEPROM is busy writing data to the memory).

The AT30TSE004A incorporates flexible user programmable internal registers to configure the temperature sensor's performance and response to over and under temperature conditions. The device contains flexible programmable high, low, and critical temperature limits. The $\overline{\text{EVENT}}$ pin is an active low output and can be configured to operate as an Interrupt or as a Comparator output. The Manufacturer and Device ID Registers provide the ability to confirm the identity of the device. The AT30TSE004A supports the industry standard 2-wire I^2C FM plus (Fast Mode +) serial interface allowing device communication to operate up to 1MHz. A bus timeout feature is supported for both temperature sensor and Serial EEPROM operations to help prevent system lock-ups. The AT30TSE004A is available in space saving 8-lead UDFN and WDFN packages.

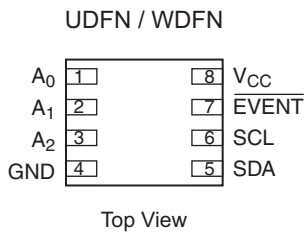
The UDFN is the recommended and preferred package.

2. Pin Descriptions and Pinouts

Table 2-1. Pin Descriptions

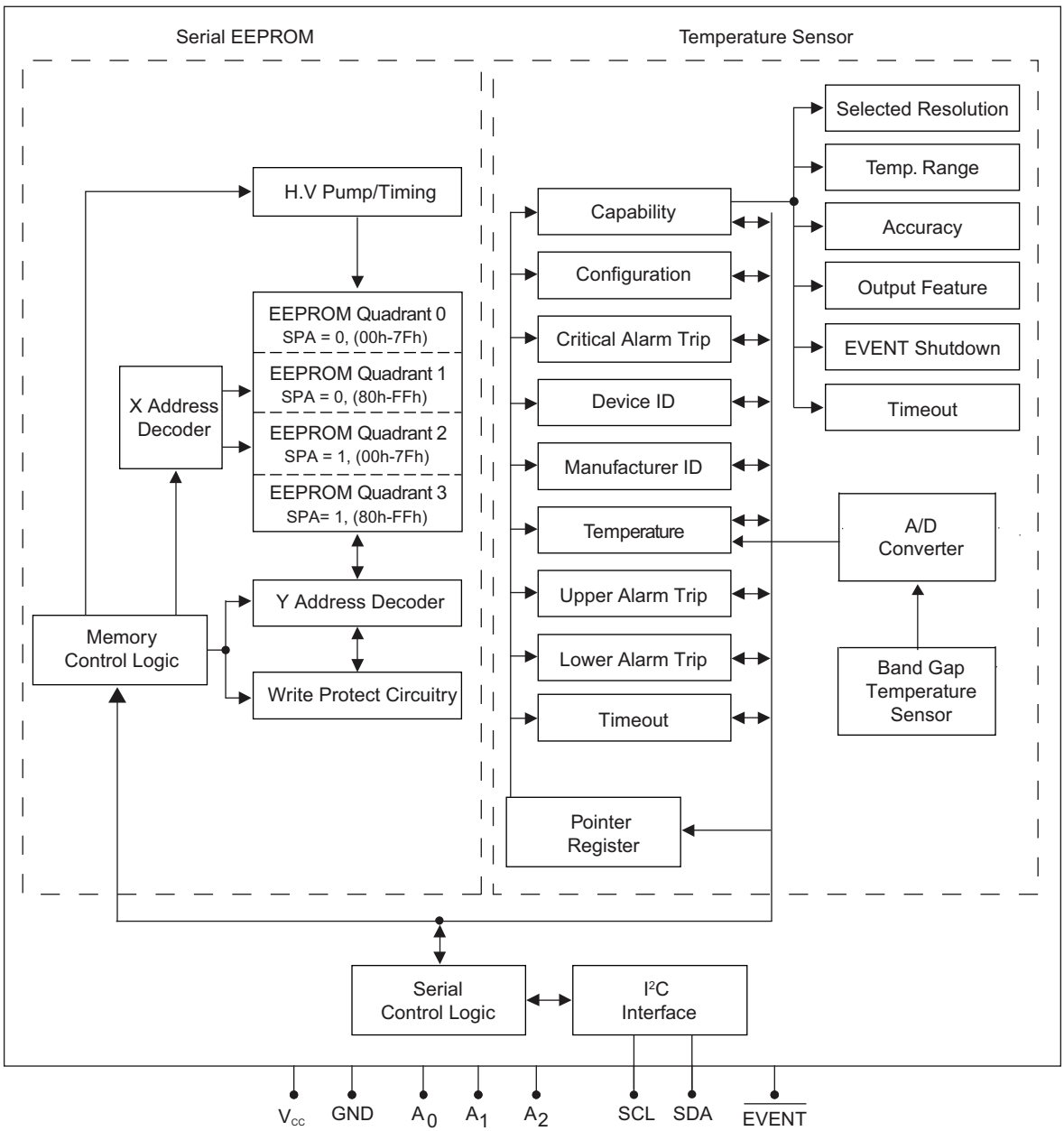
Symbol	Name and Function	Asserted State	Type
SCL	**Serial Clock:** The SCL pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is always clocked out on the falling edge of SCL. The SCL pin must either be forced high when the serial bus is idle or pulled-high using an external pull-up resistor.	—	Input
SDA	**Serial Data:** The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device. The SDA pin must be pulled-high using an external pull-up resistor (not to exceed 8KΩ in value) and may be wire-ORed with any number of other open-drain or open-collector pins from other devices on the same bus.	—	Input/ Output
$\overline{\text{EVENT}}$	**EVENT:** The $\overline{\text{EVENT}}$ pin is an open-drain output pin used to indicate when the temperature goes beyond the user-programmed temperature limits. The $\overline{\text{EVENT}}$ pin can be operated in one of three different modes; either Interrupt, Comparator, or Critical Alarm Modes. The ALERT pin must be pulled-high using an external pull-up resistor for proper operation.	—	Output
A_2, A_1, A_0	**Device Address Inputs:** The A_0, A_1, and A_2 pins are used to select the device address and corresponds to the three Least-Significant Bits (LSB) of the I^2C FM+ seven bit slave address. These pins can be directly connected to V_{CC} or GND in any combination, allowing up to eight devices on the same bus. The A_0 pin is also an overvoltage tolerant pin, allowing up to 10V to support the Reversible Software Write Protection (RSWP) feature (see Section 7.3 “Write Protection” on page 33).	—	Input
V_{CC}	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	—	Power
GND	**Ground:** The ground reference for the power supply. GND should be connected to the system ground.	—	Power

Figure 2-1. Pinout



Note: UDFN is the recommended and preferred package. The metal pad on the bottom of the UDFN/WDFN package is not internally connected to a voltage potential. This pad can be a “no connect” or connected to GND.

3. Block Diagram



4. Device Communication

The AT30TSE004A operates as a slave device and utilizes a simple 2-wire digital serial interface, compatible with the I^2C Fast Mode Plus (I^2C FM+) protocol, to communicate with a host controller, commonly referred to as the bus Master. The Master initiates and controls all Read and Write operations to the slave devices on the serial bus, and both the Master and the slave devices can transmit and receive data on the bus.

The serial interface is comprised of just two signal lines: the Serial Clock (SCL) and the Serial Data (SDA). The SCL pin is used to receive the clock signal from the Master, while the bidirectional SDA pin is used to receive command and data information from the Master, as well as, to send data back to the Master. Data is always latched into the AT30TSE004A on the rising edge of SCL and is always output from the device on the falling edge of SCL. Both the SCL and SDA pin incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise.

All command and data information is transferred with the Most-Significant Bit (MSB) first. During the bus communication, one data bit is transmitted every clock cycle, and after eight bits (one byte) of data has been transferred, the receiving device must respond with either an acknowledge (ACK) or a no-acknowledge (NACK) response bit during a ninth clock cycle (ACK/NACK clock cycle) generated by the Master; therefore, nine clock cycles are required for every one byte of data transferred. There are no unused clock cycles during any Read or Write operation so there must not be any interruptions or breaks in the data stream during each data byte transfer and ACK or NACK clock cycle.

During data transfers, data on the SDA pin must only change while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. Start and Stop conditions are used to initiate and end all serial bus communication between the Master and the slave devices.The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the Master.

In order for the serial bus to be idle, both the SCL and SDA pins must be in the Logic 1 state at the same time.

4.1 Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is stable in the Logic 1 state. The Master uses a Start condition to initiate any data transfer sequence, and the Start condition must precede any command. AT30TSE004A will continuously monitor the SDA and SCL pins for a Start condition, and the device will not respond unless one is given. Please refer to Figure 4-1 on page 8 for more details.

4.2 Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in the Logic 1 state. The Master uses the Stop condition to end a data transfer sequence to the AT30TSE004A which will subsequently return to the idle state. The Master can also utilize a repeated Start condition instead of a Stop condition to end the current data transfer if the Master will perform another operation. Please refer to Figure 4-1 on page 8 for more details.

4.3 Acknowledge (ACK)

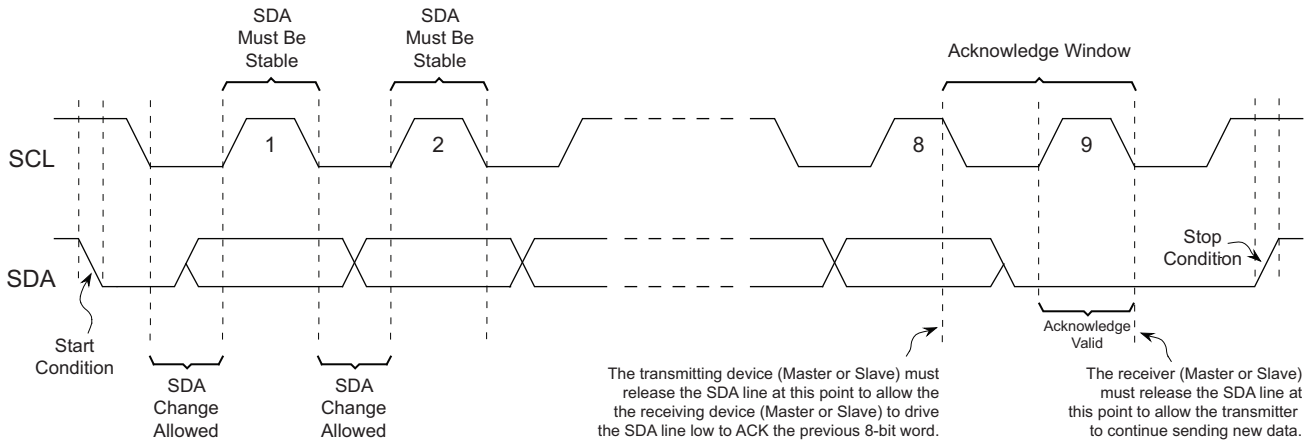
After every byte of data is received, AT30TSE004A must acknowledge to the Master that it has successfully received the data byte by responding with an ACK. This is accomplished by the Master first releasing the SDA line and providing the ACK/NACK clock cycle (a ninth clock cycle for every byte). During the ACK/NACK clock cycle, the AT30TSE004A must output a Logic 0 (ACK) for the entire clock cycle such that the SDA line must be stable in the Logic 0 state during the entire high period of the clock cycle. Please refer to Figure 4-1 on page 8 for more details.

4.4 No-Acknowledge (NACK)

When the AT30TSE004A is transmitting data to the Master, the Master can indicate that it is done receiving data and wants to end the operation by sending a NACK response to the AT30TSE004A instead of an ACK response. This is accomplished by the Master outputting a Logic 1 during the ACK/NACK clock cycle, at which point the AT30TSE004A will release the SDA line so that the Master can then generate a Stop condition.

In addition, the AT30TSE004A can use a NACK to respond to the Master instead of an ACK for certain invalid operation cases such as an attempt to Write to a read-only register (e.g. an attempt to Write to the Temperature Register).

Figure 4-1. Start, Stop, and ACK



4.5 Standby Mode

The AT30TSE004A incorporates a low-power Standby Mode which is enabled:

- Upon power-up *or*
- After the receipt of the Stop condition and the completion of any internal operations.

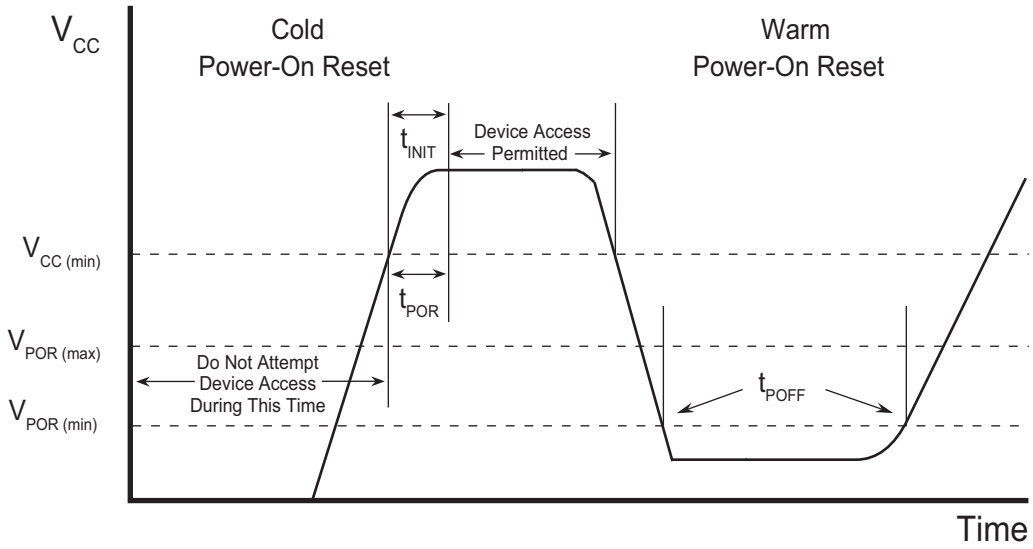
4.6 Device Reset and Initialization

The AT30TSE004A incorporates an internal Power-On Reset (POR) circuit to help prevent inadvertent operations during power-up and power-down cycles. On a cold power-up, the supply voltage must rise monotonically between $V_{POR(max)}$ and $V_{CC(min)}$ without any ring back to ensure a proper power-up (see Figure 4-2 on page 9). Once the supply voltage has passed the $V_{POR(min)}$ threshold, the device's internal reset process is initiated. Completion of the internal reset process occurs within the t_{INIT} time listed in Table 4.6.1 on page 9. Upon completion of the internal reset process, the device will have the following power-on default conditions:

- Temperature sensor starts monitoring temperature continuously.
- Pointer Register = 00h
- Upper Limit, Lower Limit, and Critical Alarm Registers are set to 0°C.
- $\overline{\text{EVENT}}$ pin is pulled high by the external pull up resistor.
- Operational mode is Comparator.
- Hysteresis level is set to 0°C.
- $\overline{\text{EVENT}}$ pin polarity is set low.
- $\overline{\text{EVENT}}$ output is disabled and not asserted.
- Serial EEPROM's SPA = 0.

Table 6-1 on page 13 shows the power-on register default values. The Upper Limit, Lower Limit, Critical Alarm, and Configuration Registers should be programmed to their user desired values before the temperature sensor can properly function. Before selecting the device and issuing protocol, a valid and stable supply voltage must be applied and no protocol should be issued to the device for the time specified by the t_{INIT} parameter. The supply voltage must remain stable and valid until the end of the protocol transmission, and for a Serial EEPROM Write instruction, until the end of the internal write cycle.

Figure 4-2. Power-Up Timing



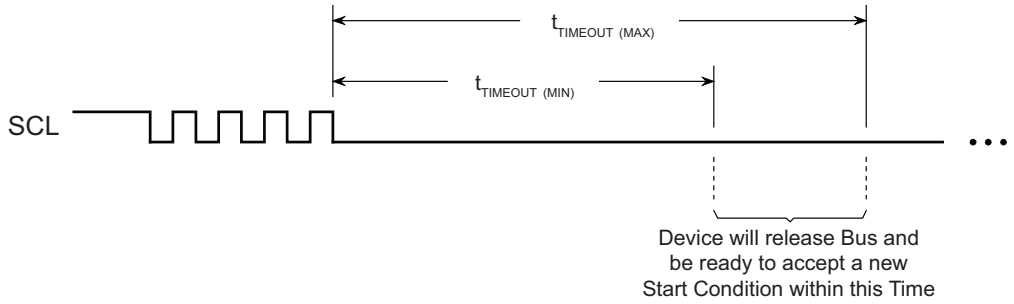
4.6.1 Power-Up Conditions

Symbol	Parameter	Min	Max	Units
t_{POR}	Power-on Reset Time		10.0	ms
v_{PON}	Power-on Reset Threshold	1.6		V
v_{POFF}	Power-off Threshold for Warm Power-on Cycle		0.9	V
t_{POFF}	Warm Power Cycle Off Time	1.0		ms
t_{INIT}	Time from Power-On to First Command	10.0		ms

4.7 Timeout

The AT30TSE004A supports the industry standard bus Timeout feature on both temperature sensor and Serial EEPROM operations to help prevent potential system bus hang-ups. The device resets its serial interface and will stop driving the bus (will let SDA float high) if the SCL pin is held low for more than the minimum Timeout (t_{OUT}) specification. The AT30TSE004A will be ready to accept a new Start condition before the maximum t_{OUT} has elapsed (see Figure 4-3). This feature does require a minimum SCL clock speed of 10kHz to avoid any timeout issues.

Figure 4-3. Timeout

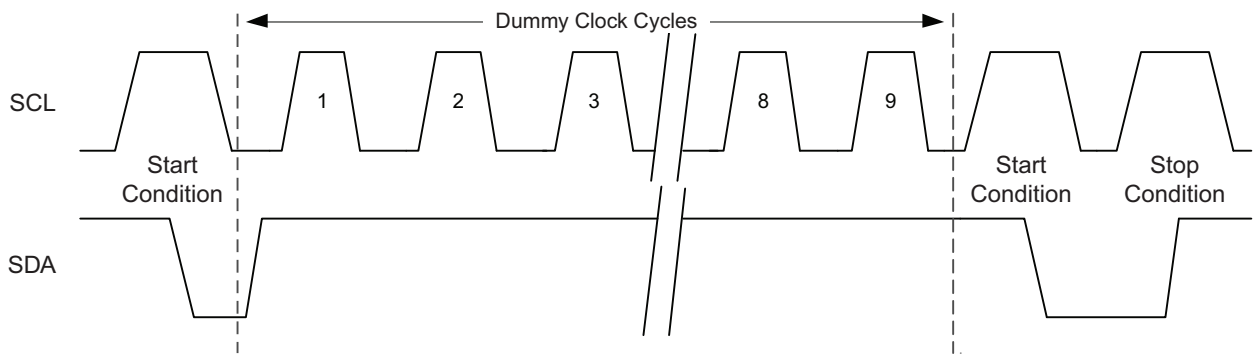


4.8 2-wire Software Reset

After an interruption in protocol, power loss, or system reset, any 2-wire part can be reset by following these steps:

1. Create a Start condition.
2. Clock nine cycles.
3. Create another Start condition followed by Stop condition as shown in Figure 4-4.

Figure 4-4. 2-wire Software Reset



5. Device Addressing

The AT30TSE004A is designed to allow the Serial EEPROM and the temperature sensor to operate in parallel while executing valid command protocol. For example, when the temperature sensor is busy during a temperature conversion cycle, it is possible to perform any Serial EEPROM operation during this time and vice versa.

The device requires a 7-bit device address and a Read/Write select bit following a Start condition from the Master to initiate communication with either the temperature sensor or the Serial EEPROM. The device address byte is comprised of a 4-bit device type identifier followed by three device address bits (A2, A1,and A0) and a R/$\overline{W}$ bit and is clocked by the Master on the SDA pin with the Most Significant Bit first (see Table 5-1).

The AT30TSE004A will respond to three unique device type identifiers. The device type identifier of `'1010'`(Ah) is necessary to select the device for reading or writing. The device type identifier of `'0110'`(6h) has multiple purposes. First, it is used to access the page address function which determines what the internal address counter is set to. For more information on accessing the page address function, please refer to Section 7.1.1 “Set Page Address and Read Page Address Commands” on page 27 The device type identifier of `'0110'`(6h) is also used to access the Software Write Protection feature of the device. Information on the Software Write Protection functionality can be found in Section 7.3 “Write Protection” on page 33.

Table 5-1. AT30TSE004A Device Address Byte

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Function	**Device Type Identifier**				**Device Address**			**Read/Write**
Serial EEPROM Read/Write	1	0	1	0	A2	A1	A0	R/$\overline{W}$
Serial EEPROM Write Protection and Page Address Functions	0	1	1	0	A2	A1	A0	R/$\overline{W}$
Temperature Sensor	0	0	1	1	A2	A1	A0	R/$\overline{W}$

The software device address bits (A2, A1, and A0) must match their corresponding hard-wired device address inputs (A_2, A_1 and A_0) allowing up to eight devices on the bus at the same time (see Table 5-2). The eighth bit of the address byte is the R/$\overline{W}$ operation selection bit. A Read operation is selected if this bit is a Logic 1, and a Serial EEPROM Write operation is selected if this bit is a Logic 0. Upon a compare of the device address byte, the AT30TSE004A will output an ACK during the ninth clock cycle; if a compare is not true, the device will output a NACK during the ninth clock cycle and return the device to the low-power Standby Mode.

Table 5-2. Device Address Combinations

Software Device Address Bits	Hard-wired Device Address Inputs		
A2, A1, A0	**A_2**	**A_1**	**A_0**
0 0 0	GND	GND	GND
0 0 1	GND	GND	V_{CC}
0 1 0	GND	V_{CC}	GND
0 1 1	GND	V_{CC}	V_{CC}
1 0 0	V_{CC}	GND	GND
1 0 1	V_{CC}	GND	V_{CC}
1 1 0	V_{CC}	V_{CC}	GND
1 1 1	V_{CC}	V_{CC}	V_{CC}

6. Temperature Sensor

6.1 Functional Description

The temperature sensor consists of a Delta-Sigma Analog to Digital Converter (ADC) with a band gap type temperature sensor that monitors and updates its temperature measurement at least eight times per second converting the temperature readings into digital data bits and latching them into the Temperature Register that can be read via the 2-wire I^2C FM+ serial interface.

The device communicates over a 2-wire I^2C FM+ interface with a Master consisting of a Serial Clock (SCL) and a Serial Bidirectional Data Bus (SDA) with clock frequencies up to 1MHz. The Master generates the SCL signal and is used by the AT30TSE004A to receive and send serial data on the SDA line with the Most Significant Bit transferred first. A pull-up resistor is required on the SDA pin since it has an open drain configuration.

6.1.1 $\overline{\text{EVENT}}$ Output

The $\overline{\text{EVENT}}$ pin has three operating modes depending on the configuration settings:

- Interrupt Mode
- Comparator Mode
- Critical Alarm (Crit_Alarm) Mode

While in Interrupt Mode, once a temperature reaches a boundary limit, the AT30TSE004A asserts the $\overline{\text{EVENT}}$ pin. The $\overline{\text{EVENT}}$ pin will remain asserted until the system clears the interrupt by writing a Logic 1 to the EVTCLR bit five in the Configuration Register. When the temperature drops below specified limits, the device returns back to either Interrupt or Comparator Mode as programmed in the Configuration Register's EVTMOD bit zero.

In Comparator Mode, the $\overline{\text{EVENT}}$ pin remains asserted until the error condition that caused the pin to be asserted no longer exists and the $\overline{\text{EVENT}}$ pin will clear itself. In the Crit_Alarm Mode, when the measured temperature exceeds Crit_Alarm limit, the $\overline{\text{EVENT}}$ pin will remain asserted until the temperature drops below the Crit_Alarm limit minus hysteresis (see Figure 6-1 on page 17). All event thresholds use hysteresis as programmed in the Configuration Register.

6.1.2 Alarm Window

The Alarm Window consists of the Upper Limit Register and Lower Limit Register. The Upper Limit Register holds the upper temperature trip point and the Lower Limit Register holds the lower temperature trip point. After the $\overline{\text{EVENT}}$ pin control is enabled, the $\overline{\text{EVENT}}$ output will be triggered upon entering and exiting from this window.

6.2 Register Descriptions

This section describes all the temperature sensor registers that are used in the AT30TSE004A. The AT30TSE004A contains several registers that are user accessible and/or programmable and utilized for latching the temperature readings, storing high, low, and critical temperature limits, configuring the temperature sensor performance, and reporting temperature sensor status.

These registers include a Capability Register, Configuration Register, Upper Limit Register, Lower Limit Register, Critical Alarm Register, Temperature Register, Manufacturer Identification Register, and a Device Identification/Device Revision Register.

The AT30TSE004A utilizes an 8-bit Pointer Register to access the 16-bit registers. Table 6-1 indicates the Write/Read access capability for each register.

Note: Reading from a Write-only register will result in reading Logic 0 data, and writing to a Read-only register will have no impact even though the Write sequence will be acknowledged by the device.

Table 6-1. Registers

Register	Address	Read/Write	Section	Power-On Default
Pointer Register	n/a	$\overline{W}$	6.2.1	00h
Capability Register	00h	R	6.2.2	00F7h
Configuration Register	01h	R/$\overline{W}$	6.2.3	0000h
Upper Limit Register	02h	R/$\overline{W}$	6.2.4	0000h
Lower Limit Register	03h	R/$\overline{W}$	6.2.5	0000h
Critical Alarm Register	04h	R/$\overline{W}$	6.2.6	0000h
Temperature Register	05h	R	6.2.7	N/A
Manufacturer I.D. Register	06h	R	6.2.8	1114h
Device I.D./Device Revision Register	07h	R	6.2.9	2200h
Reserved (1)	08h to 0Fh	R/$\overline{W}$	N/A	N/A

Note: 1. Write operations to reserve registers should be avoided as it may cause undesirable results.

6.2.1 Pointer Register (8-bit Write Only, Address = N/A)

The AT30TSE004A utilizes a Pointer Register to select and access all the data registers shown on Table 6-1. The Pointer Register is an 8-bit Write-only register (see Table 6-2). The power-on default value is 00h which is the address location for the Capability Register.

Table 6-2. Pointer Register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Symbol	Pointer Register Value							
R/W	W	W	W	W	W	W	W	W
Default Value	0	0	0	0	0	0	0	0

6.2.2 Capability Register (16-bit Read-only, Address = 00h)

This register is a 16-bit read-only register used to specify the functional capabilities of the temperature sensor. The AT30TSE004A is capable of measuring temperature with ±1°C over the active range and ±2°C over the monitor range. The Capability Register functions are described in Table 6-3 and Table 6-4.

Table 6-3. Capability Register Bit Distribution

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Symbol	RFU							
Default Value	0	0	0	0	0	0	0	0
R/W Access	R	R	R	R	R	R	R	R
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Symbol	EVSD	TMOUT	V_{HV}	TPRES		RANGE	SACC	ICAP
Default Value	1	1	1	1	0	1	1	1
R/W Access	R	R	R	R	R	R	R	R

Table 6-4. Capability Register Bit Description

Bit	Symbol	Description
15:8	RFU	***Reserved*** for ***Future Use*** and must be Logic 0.
7	EVSD	**Event Output Status During Shutdown Mode**: 1 = The $\overline{\text{EVENT}}$ pin output is deasserted (not driven) when entering Shutdown Mode and will remain deasserted upon exit from Shutdown Mode until the next temperature measurement sample is taken. In Interrupt Mode, the $\overline{\text{EVENT}}$ pin maybe asserted when existing Shutdown if a pending Interrupt has not be cleared.
6	TMOUT	Timeout: 1 = BusTimeout supported within the range 25 to 35ms.
5	V_{HV}	A_0 Pin High Voltage: 1 = The A_0 pin supports a maximum voltage up to 10V.
4:3	TPRES	Temperature Resolution: 10 =Supports 0.125°C (11-bit resolution).
2	RANGE	1 = Can read temperatures below 0°C and sets appropriate sign bit.
1	SACC	Supported Accuracy: 1 = Supports a B-grade accuracy of ±1°C over the active range (75°C to 95°C) and 2°C over the monitor range (40°C to 125°C).
0	ICAP	Interrupt Capability: 1 = Supports Interrupt capabilities.

6.2.3 Configuration Register (16-bit Read/Write, Address = 01h)

The AT30TSE004A incorporates a 16-bit Configuration Register allowing the user to set key operational features of the temperature sensor. The Configuration Register functions are described in Table 6-5 and Table 6-6.

Table 6-5. Configuration Register Bit Distribution

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Symbol	RFU					HYSTENB		SHTDWN
Default Value	0	0	0	0	0	0	0	0
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Symbol	CRTALML	WINLOCK	EVTCLR	EVTSTS	EVTOUT	CRITEVT	EVTPOL	EVTMOD
Default Value	0	0	0	0	0	0	0	0
R/W Access	R/W	R/W	W	R	R/W	R/W	R/W	R/W

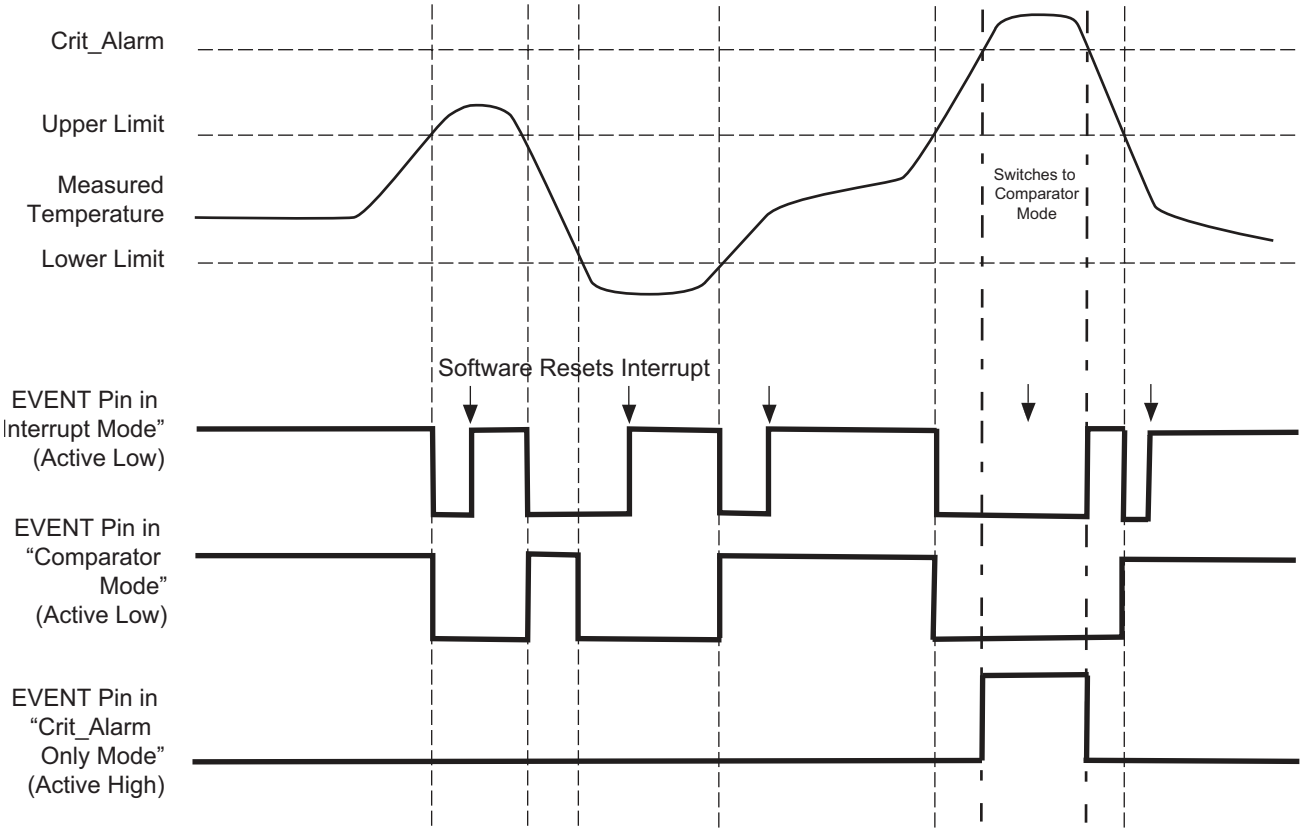
Table 6-6. Configuration Register Bit Description

Bit	Symbol	Description
15:11	RFU	***Reserved*** for ***Future Use*** and must be Logic 0.
10:9	HYSTENB	Hysteresis Enable: 00 = 0°C Disable hysteresis (Power-on default) 01 = 1.5°C Enable hysteresis 10 = 3.0°C Enable hysteresis 11 = 6.0°C Enable hysteresis The purpose of these bits is to control the hysteresis applied to the temperature limit trip point boundaries. The above hysteresis applies to all limits when temperature drops below the user specified temperature limit trip points. Note: Hysteresis applies to decreasing temperature only. Once the temperature is above a given threshold, the temperature must drop below the boundary limit minus hysteresis in order for a Comparator $\overline{\text{EVENT}}$ to be cleared. Example: If these two bits are set to '01' for 1.5°C and the Upper Limit is set to 85°C, as temperature rises above 85°C, bit 14 of the Temperature Register will be set to a Logic 1. Bit 14 will remain set until the temperature drops below the threshold (85°C) minus the hysteresis value(83.5°C). Note: Hysteresis is also applied to the $\overline{\text{EVENT}}$ pin functionality. This bit cannot be changed if the Crit_Alarm or Alarm Window Lock bits is set.
8	SHTDWN	Shutdown Mode: 0 = The temperature sensor is enabled for continuous conversion (power-on default). 1 = The temperature sensor is disabled. To save power in Shutdown Mode, the temperature sensor is not active and will not generate interrupts or update the temperature data. The $\overline{\text{EVENT}}$ pin is deasserted (not driven). This bit cannot be set to a Logic 1 if either of the Crit_Alarm or Alarm Window Lock bits is set, however, it can be cleared at any time. The device will respond to protocol commands and the bus timeout is active when in Shutdown Mode.

Table 6-6. Configuration Register Bit Description (Continued)

Bit	Symbol	Description
7	CRTALML	Crit_Alarm Lock bit: 0 = The Crit_Alarm Register can be updated (power-on default). 1 = The Crit_Alarm Register is locked and cannot be updated. This bit locks the Critical Alarm Register from being updated. Once set, it can only be cleared to a Logic 0 by an internal Power-On Reset.
6	WINLOCK	Alarm Window Lock bit: 0 = The Upper Limit and Lower Limit Registers can be updated (power-on default). 1 = The Upper and Lower Limit Registers are locked and cannot be updated. Once set, it can be only be cleared to a Logic 0 by an internal Power-On Reset.
5	EVTCLR	$\overline{\text{EVENT}}$ Clear: 0 = Has no effect (power-on default). 1 = Clears (releases) the active $\overline{\text{EVENT}}$ pin in Interrupt Mode. This bit will clear the $\overline{\text{EVENT}}$ pin after it has been enabled. This bit is a write-only bit and will read as a Logic 0 and is ignored when in Comparator Mode.
4	EVTSTS	$\overline{\text{EVENT}}$ Pin Output Status: 0 = The $\overline{\text{EVENT}}$ output is not asserted by the device (power-on default). 1 = The $\overline{\text{EVENT}}$ output is asserted due to a limit or alarm condition.
3	EVTOUT	$\overline{\text{EVENT}}$ Output Control: 0 = The $\overline{\text{EVENT}}$ output is disabled and will not generate interrupts (power-on default). 1 = The $\overline{\text{EVENT}}$ output is enabled. This bit cannot be altered if the Crit_Alarm or the Alarm Window Lock bits is set.
2	CRITEVT	Critical Temperature only: 0 = The $\overline{\text{EVENT}}$ output is asserted if the measured temperature is above the Upper Limit or Critical Alarm, or is below the Lower Limit (power-on default). 1 = The $\overline{\text{EVENT}}$ output is asserted only for a Critical Alarm violation when the temperature is greater then the Crit_Alarm. This bit cannot be altered if the Alarm Window Lock bit is set.
1	EVTPOL	$\overline{\text{EVENT}}$ Polarity: 0 = The $\overline{\text{EVENT}}$ pin is active low (power-on default). 1 = The $\overline{\text{EVENT}}$ pin is active high. This bit cannot be altered if the Crit_Alarm or the Alarm Window Lock bit is set. A pull-up resistor is required on this pin to achieve the Logic 1 state.
0	EVTMOD	$\overline{\text{EVENT}}$ Mode: 0 = The $\overline{\text{EVENT}}$ pin will operate in Comparator Mode (power-on default). 1 = The $\overline{\text{EVENT}}$ pin will operate in Interrupt Mode. This bit cannot be altered if the Crit_Alarm or the Alarm Window Lock bit is set.

Figure 6-1. $\overline{\text{EVENT}}$ Pin Mode Functionality



6.2.4 Upper Limit Register (16-bit Read/Write, Address = 02h)

The Upper Limit Register holds the user programmed upper temperature boundary trip point in 2's complement format (0.125°C resolution) that can be utilized to monitor the temperature in an operating window between the Upper Limit Register and the Lower Limit Register settings (see Table 6-7 and Table 6-9). When the temperature increases above this trip point, drops below, or is equal to the trip point (minus any hysteresis set), then the $\overline{\text{EVENT}}$ pin is asserted (if enabled). This register is read-only if the Alarm Window Lock (WINLOCK) bit six in the Configuration Register is set to a Logic 1.

Table 6-7. Upper Limit Register Bit Distribution

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Symbol	RFU			SIGN	ALMWINH			
Default Value	0	0	0	0	0	0	0	0
R/W Access	R	R	R	R/W	R/W	R/W	R/W	R/W
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Symbol	ALMWINH						RFU	
Default Value	0	0	0	0	0	0	0	0
R/W Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 6-8. Upper Limit Register Bit Description

Bit	Symbol	Description
15:13	RFU	***Reserved*** for ***Future Use***. Read as Logic 0.
12	SIGN	Sign bit: 0 = The temperature is greater than or equal to 0°C. 1= The temperature is less than 0°C.
11:2	ALMWINH	Upper Limit temperature bits: Represented in 2's complement format. Read-only access if Alarm Window is locked (Configuration Register bit 6 high). R/W access if the Alarm Window is unlocked.
0:1	RFU	***Reserved*** for ***Future Use***. Read as Logic 0.

6.2.5 Lower Limit Register (16-bit Read/Write, Address = 03h)

The Lower Limit Register holds the user programmed lower temperature boundary trip point in 2's complement format (0.125°C resolution) that can be utilized to monitor the temperature in an operating window (see Table 6-7 and Table 6-9). When the temperature decreases below this trip point minus any hysteresis set or increases to meet or exceed this trip point, then the $\overline{\text{EVENT}}$ pin is asserted (if enabled).

This register becomes read-only if the Alarm Window Lock (WINLOCK) bit six in the Configuration Register is set to a Logic 1.

Table 6-9. Lower Limit Register Bit Distribution

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Symbol	RFU			SIGN	ALMWINL			
Default Value	0	0	0	0	0	0	0	0
R/W Access	R	R	R	R/W	R/W	R/W	R/W	R/W
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Symbol	ALMWINL						RFU	
Default Value	0	0	0	0	0	0	0	0
R/W Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 6-10. Lower Limit Register Bit Description

Bit	Symbol	Description
15:13	RFU	***Reserved*** for ***Future Use***. Read as Logic 0.
12	SIGN	Sign bit: 0 = The temperature is greater than or equal to 0°C. 1 = The temperature is less than 0°C.
11:2	ALMWINL	Lower Limit temperature bits: Represented in 2's complement format. Read-only access if Alarm Window is locked (Configuration Register bit 6 high). R/W access if the Alarm Window is unlocked.
0:1	RFU	***Reserved*** for ***Future Use***. Read as Logic 0.

6.2.6 Critical Alarm Register (16-bit Read/Write, Address = 04h)

The Critical Alarm Register holds the user programmed Critical Alarm temperature boundary trip point in 2's complement format (0.125°C resolution) that can be utilized to monitor the temperature (see Table 6-11 and Table 6-12). When the temperature increases above this trip point, the $\overline{\text{EVENT}}$ pin will be asserted (if enabled). It will remain asserted until temperature decreases below or equal to the trip point minus any hysteresis set. This register becomes read-only if the Critical Alarm Lock Bit (CRTALML) bit seven in the Configuration Register is set to a Logic 1.

Table 6-11. Critical Alarm Register Bit Distribution

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Symbol	RFU			SIGN	CRITEVT			
Default Value	0	0	0	0	0	0	0	0
R/W Access	R	R	R	R/W	R/W	R/W	R/W	R/W
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Symbol	CRITEVT						RFU	
Default Value	0	0	0	0	0	0	0	0
R/W Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 6-12. Critical Alarm Register Bit Description

Bit	Symbol	Description
15:13	RFU	***Reserved*** for ***Future Use***. Read as Logic 0.
12	SIGN	Sign bit: 0 = The temperature is greater than or equal to 0°C. 1 = The temperature is less than 0°C.
11:2	CRITEVT	Critical Alarm temperature bits: Represented in 2's complement format. Read-only access if Alarm Window is locked (Configuration Register bit 6 high). R/W access if the Alarm Window is unlocked.
0:1	RFU	***Reserved*** for *Future Use*. Read as Logic 0.

6.2.7 Temperature Register (16-bit Read-only, Address = 05h)

The Temperature Register holds the internal temperature measurement data represented in 2's complement format allowing for resolution equal to 0.125°C (least significant bit). The upper three bits (15, 14, and 13) of the Temperature Register indicates the trip status of the current temperature and most important, are not affected by the status of the output of the $\overline{\text{EVENT}}$ pin (see Table 6-13 and Table 6-14).

Table 6-13. Temperature Register Bit Distribution

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Symbol	CRITHIGH	ALMHIGH	ALMLOW	SIGN	128°C	64°C	32°C	16°C
Default Value	0	0	0	0	0	0	0	0
R/W Access	R	R	R	R	R	R	R	R
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Symbol	8°C	4°C	2°C	1°C	0.5°C	0.25°C	0.125°C	RFU
Default Value	0	0	0	0	0	0	0	0
R/W Access	R	R	R	R	R	R	R	R

Table 6-14. Temperature Register Bit Description

Bit	Symbol	Description
15	CRITHIGH	0 = The temperature is less than the Critical Alarm Register setting. 1 = The temperature is greater than or equal to Critical Alarm Register setting. When this bit is set to a Logic 1, it will automatically clear once the measured temperature decreases below or is equal to the trip point minus any hysteresis set.
14	ALMHIGH	0 = The temperature is below the Upper Limit Register setting. 1 = The temperature is above the Upper Limit Register setting. When the bit is set to a Logic 1, it will automatically clear once the measured temperature decreases below or is equal to the trip point minus any hysteresis set.
13	ALMLOW	0 = The temperature is above the Lower Limit Register setting. 1 = The temperature is below the Lower Limit Register setting. When the bit is set to a Logic 1, it will automatically clear once the measured temperature increases above or is to equal to the trip point.
12	SIGN	Sign bit: 0 = The temperature is greater than or equal to 0°C. 1 = The temperature is less than 0°C.
11:1	TEMP	Temperature bits: Represented in 2's complement format. The encoding of bits B11 through B2 is the same as in the limit and alarm registers.
0	RFU	***Reserved*** for ***Future Use***. Read as Logic 0.

6.2.7.1 Temperature Register Format

This section will clarify the Temperature Register format and temperature bit value assignments utilized for temperature for the following registers: Upper Limit, Lower Limit, Critical Alarm, and Temperature Registers. The temperatures expressed in the Upper Limit, Lower Limit, Critical Alarm, and Temperature Registers are indicated in 2's complement format. In each of the temperature limit registers, bits 12 through bit two are utilized for temperature settings, or in the case of the Temperature Register, holds the internal temperature measurement with bits 12 through bit one allowing 0.125ºC resolution.

Table 6-15 indicates the Temperature Register's assigned bit values utilized for temperature and shows examples for the Temperature Register bit values for various temperature readings.

Table 6-15. Temperature Register Format

Position	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Value	SIGN	128°C	64°C	32°C	16°C	8°C	4°C	2°C	1°C	0.5°C	0.25°C	0.125°C	X

Table 6-16. Temperature Register Examples

Temperature Register Value Examples	
Temperature	**Binary (Bit 15 – Bit 0)**
+125°C	xxx0 0111 1101 00xx
+99.75°C	xxx0 0110 0011 11xx
+85°C	xxx0 0101 0101 00xx
+39°C	xxx0 0010 0111 00xx
+15.75°C	xxx0 0000 1111 11xx
+0.25°C	xxx0 0000 0000 01xx
0°C	xxx0 0000 0000 00xx
-0.25°C	xxx1 1111 1111 11xx
-1°C	xxx1 1111 1110 00xx
-20°C	xxx1 1110 1100 00xx

6.2.8 Manufacturer ID Register (16-bit Read-only, Address = 06h)

The Manufacturer ID Register contains the PCI SIG number assigned to Atmel (1114h) as shown in Table 6-17.

Table 6-17. Manufacturer ID Register Bit Distribution

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Symbol	Manufacturer ID							
Default Value	0	0	0	1	0	0	0	1
R/W Access	R	R	R	R	R	R	R	R
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Symbol	Manufacturer ID							
Default Value	0	0	0	1	0	1	0	0
R/W Access	R	R	R	R	R	R	R	R

6.2.9 Device ID Register (16-bit Read-only, Address = 07h)

The upper or high order byte is used to specify the device identification and the low byte is used to specify the device revision. The Device ID for the AT30TSE004A is 2200h (see Table 6-18).

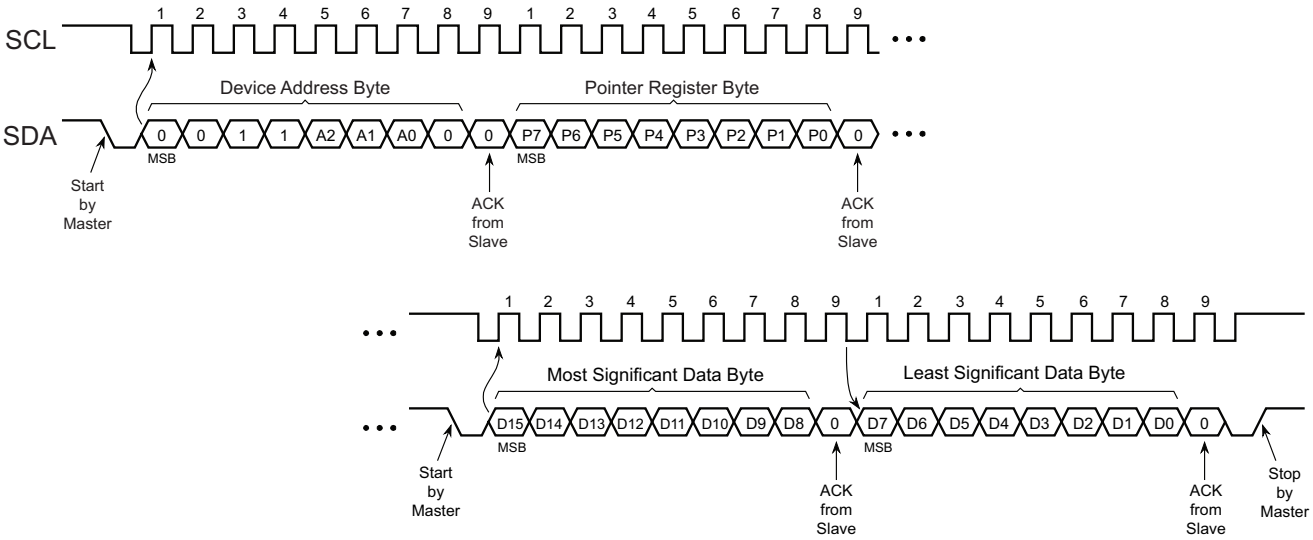
Table 6-18. Device ID Register Bit Distribution

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Symbol	Device ID							
Default Value	0	0	1	0	0	0	1	0
R/W Access	R	R	R	R	R	R	R	R
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Symbol	Device Revision							
Default Value	0	0	0	0	0	0	0	0
R/W Access	R	R	R	R	R	R	R	R

6.3 Temperature Sensor Write Operations

Writing to the Temperature Register of the AT30TSE004A is accomplished through a modified Write operation for two data bytes. To maintain 2-wire compatibility, the 16-bit registers are accessed through a Pointer Register requiring the TS Write sequence to include a Pointer Register byte following the device address byte to write the two data bytes. Figure 6-2 illustrates the entire Write transaction.

Figure 6-2. Temperature Sensor Register Write Operation



6.4 Temperature Sensor Read Operations

Reading data from the temperature sensor may be accomplished in one of two ways:

- If the location latched in the Pointer Register is correct (for normal operation, it is expected the same address will be read repeatedly to read the temperature from the Temperature Register), the Register Pointer Word Read sequence should be utilized as shown in Figure 6-3. To perform a Register Pointer Word Read, the Master transmits a Start condition followed by a device address byte with the R/$\overline{W}$ select bit to a Logic 1. The AT30TSE004A should respond with an ACK and will transmit the most significant data byte. The Master should send an ACK followed by the device transmitting the least significant data byte. To end the Read operation, the Master sends a NACK followed by a Stop condition.
- If it is desired to Read a Random Register or simply change to read a different register from the temperature sensor, then the Preset Pointer Register Word Read protocol sequence should be followed and is shown in Figure 6-4. The Preset Pointer Register Word Read sequence allows the Pointer Register to be preloaded with the correct register address to gain access to the desired register to be read. To perform a Preset Pointer Register Word Read, the Master transmits a Start condition followed by a device address byte (with the R/$\overline{W}$ select bit to a Logic 0) and a Pointer Register byte to the AT30TSE004A. Once the device address and Pointer Register bytes are clocked in and acknowledged by the AT30TSE004A, the Master must generate another Start condition. The Master transmits another device address byte (with the R/$\overline{W}$ select bit to a Logic 1) followed by an ACK by the AT30TSE004A and the device transmitting the most significant data byte. The Master should send a ACK followed by the device transmitting the least significant data byte. To end the Read operation, the Master should send a NACK followed by a Stop condition.

Figure 6-3. Register Pointer Word Read

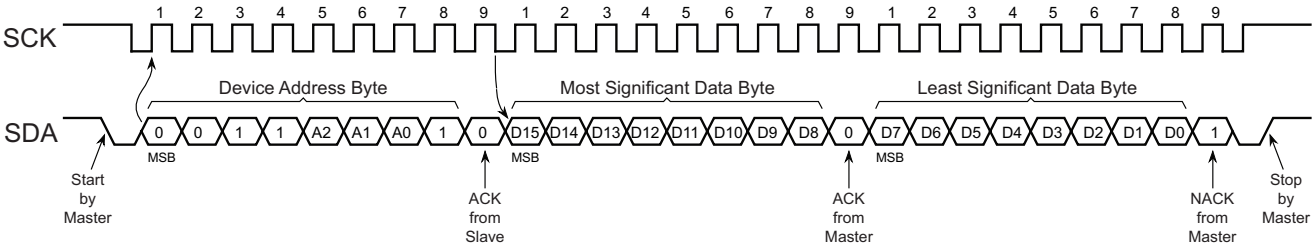
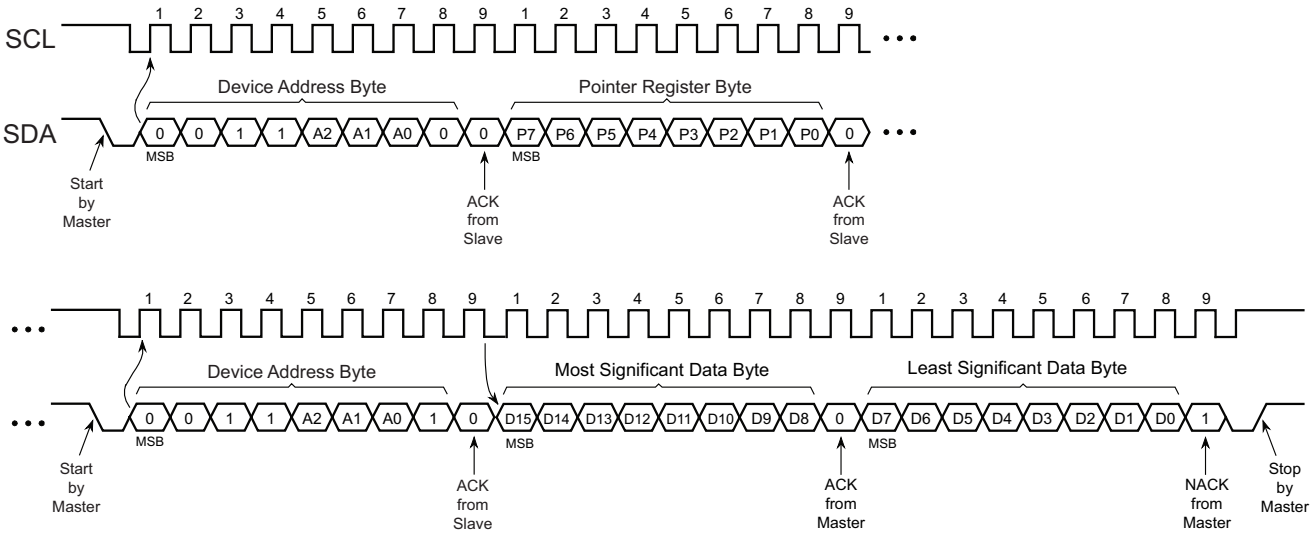


Figure 6-4. Preset Pointer Register Word Read



7. Serial EEPROM

7.1 Memory Organization

To provide the greatest flexibility and backwards compatibility with the previous generations of SPD devices, the AT30TSE004A memory organization is organized into two independent 2-Kbit memory arrays. Each 2-Kbit (256-byte) section is internally organized into two independent quadrants of 128 bytes with each quadrant comprised of eight pages of 16 bytes. Including both memory sections, there are four 128-byte quadrants totaling 512 bytes. The Memory Array organization details are shown in Section on page 6 and Table 7-1.

7.1.1 Set Page Address and Read Page Address Commands

The AT30TSE004A incorporates an innovative memory addressing technique that utilizes a Set Page Address (SPA) and Read Page Address (RPA) commands to select and verify the desired half of the memory is enabled to perform Write and Read operations.

Example: If SPA = 0, then the first-half or lower 256 bytes of the Serial EEPROM is selected allowing access to Quadrant 0 and Quadrant 1. Alternately, if SPA = 1, then the second-half or upper 256 bytes of the Serial EEPROM is selected allowing access to Quadrant 2 and Quadrant 3.

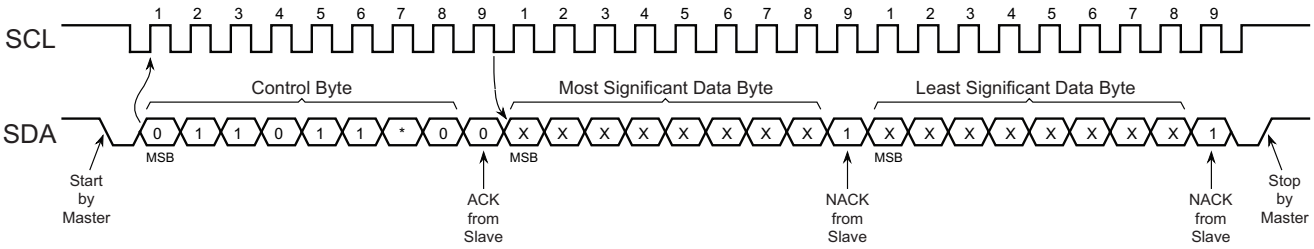
Table 7-1. Set Page Address and Memory Organization

Block	Set Page Address (SPA)	Memory Address Locations
Quadrant 0	0	00h to 7Fh
Quadrant 1	0	80h to FFh
Quadrant 2	1	00h to 7Fh
Quadrant 3	1	80h to FFh

Note: Due to the requirement for the A_0 pin to be driven to V_{HV}, the SPA and the RPA commands are fully supported in a single DIMM (isolated DIMM) end application or a single DIMM programming station only.

Setting the Set Page Address (SPA) value selects the desired half of the EEPROM for performing Write or Read operations. This is done by sending the SPA as seen in Figure 7-1. The SPA command sequence requires the Master to transmit a Start condition followed by sending a control byte of `'011011*0'` where the `'*'` in the bit 7 position will dictate which half of the EEPROM is being addressed. A `'0'` in this position (or 6Ch) is required to set the page address to the first half of the memory and a `'1'` (or 6Eh) is necessary to set the page address to the second half of the memory. After receiving the control byte, the AT30TSE004A should return an ACK and the Master should follow by sending two data bytes of don't care values. The AT30TSE004A responds with a NACK to each of these two data bytes although the JEDEC TSE2004av specification allows for either an ACK or NACK response. The protocol is completed by the Master sending a Stop condition to end the operation.

Figure 7-1. Set Page Address (SPA)



Bit * = 0: Indicates the page address is located in the first half of the memory.

Bit * = 1: Indicates the page address is located in the second half of the memory.

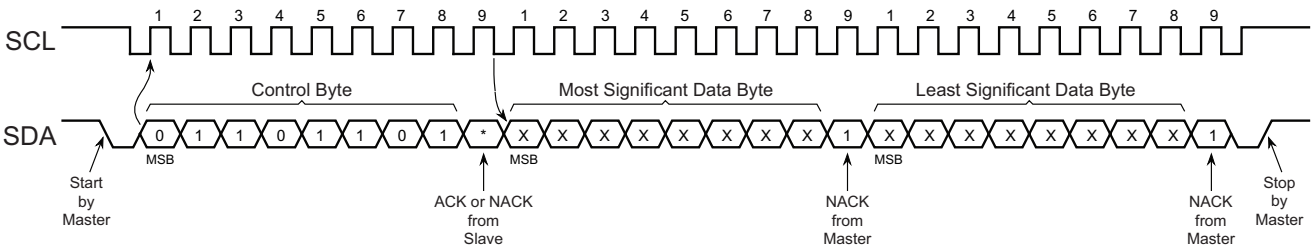
Reading the state of the SPA can be accomplished via the Read Page Address (RPA) command. The Master can issue the RPA command to determine if the AT30TSE004A's internal address counter is located in the first 2-Kbit section or the second 2-Kbit memory section based upon the device's ACK or NACK response to the RPA command.

The RPA command sequence requires the Master to transmit a Start condition followed by a control byte of '01101101'(6Dh). The device's current address counter (page address) is located in the first half of the memory if the AT30TSE004A responds with an ACK to the RPA command. Alternatively, if the device's response to the RPA command is a NACK, indicates the page address is located in the second half of the memory (see Figure 7-2). Following the control byte and the device's ACK or NACK response, the AT30TSE004A should transmit two data bytes of don't care values. The Master should NACK on these two data bytes followed by the Master sending a Stop condition to end the operation.

After power-up, the SPA is set to zero indicating internal address counter is located in the first half of the memory. Performing a software reset (see Section 4.8 "2-wire Software Reset" on page 10) will also set the SPA to zero.

The AT30TSE004A incorporates a Reversible Software Write Protect (RSWP) feature that allows the ability to selectively write protect data stored in any or all of the four Serial EEPROM 128-byte quadrants. See Section 7.3 "Write Protection" on page 33 for more information on the RSWP feature.

Figure 7-2. Read Page Address (RPA)



Bit * = 0: ACK indicates the device's internal address counter is located in the first half of the memory.

Bit * = 1: NACK indicates the device's internal address counter is located in the second half of the memory.

7.2 Serial EEPROM Write Operations

The 4-Kbit Serial EEPROM within the AT30TSE004A supports single Byte Write and Page Write operations up to the maximum page size of 16 bytes in one operation. The only difference between a Byte Write and a Page Write operation is the amount of data bytes loaded. Regardless of whether a Byte Write or Page Write operation is performed, the internally self-timed write cycle will take the same amount of time to write the data to the addressed memory location(s). Temperature sensor operations can be accessed during the write cycle to read the Temperature Register or perform any other temperature sensor function.

Caution: All Byte Write and Page Write operations should be preceded by the SPA and or RPA commands to ensure the internal address counter is located in the desired half of the memory.

If a Byte Write or Page Write operation is attempted to a protected quadrant, then the AT30TSE004A will respond (ACK or NACK) to the Write operation according to Table 7-2.

Table 7-2. Serial EEPROM Acknowledge Status When Writing Data or Defining Write Protection

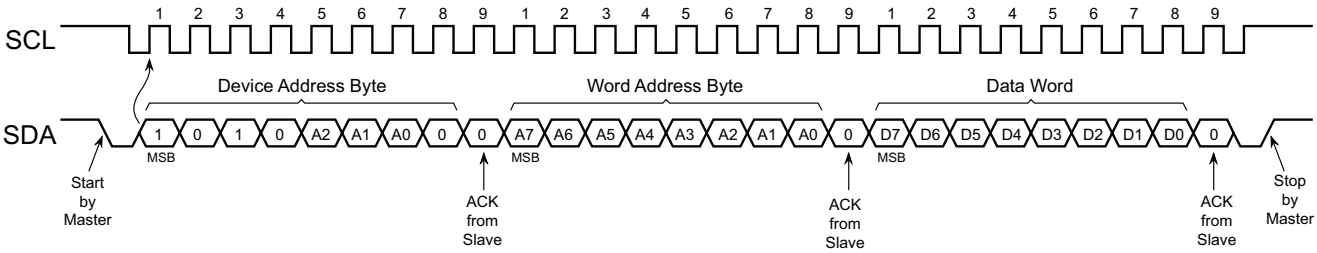
Quadrant Status	Instruction Sent	Instruction Response	Word Address Sent	Word Address Response	Data Word Sent	Data Word Response	Write Cycle
Write Protected with Set RSWP	Set RSWP	NACK	Don't Care	NACK	Don't Care	NACK	No
	Clear RSWP	ACK	Don't Care	ACK	Don't Care	ACK	Yes
	Byte Write or Page Write to Protected Quadrant	ACK	Word Address	ACK	Data	NACK	No
Not Protected	Set RSWP or Clear RSWP	ACK	Don't Care	ACK	Don't Care	ACK	Yes
	Byte Write or Page Write	ACK	Word Address	ACK	Data	ACK	Yes

7.2.1 Byte Write

Following the Start condition from the Master, the device type identifier (‘1010’), the device address bits and the R/$\overline{W}$ select bit (set to a Logic 0) are clocked onto the bus by the Master (see Figure 7-3). This indicates to the addressed device that the Master will follow by transmitting a byte with the word address. The AT30TSE004A will respond with an ACK during the ninth clock cycle. Then the next byte transmitted by the Master is the 8-bit word address of the byte location to be written into the Serial EEPROM. After receiving an ACK from the AT30TSE004A, the Master transmits the data word to be programmed followed by an ACK from the AT30TSE004A. The Master ends the Write sequence with a Stop condition during the 10th clock cycle to initiate the internally self-timed write cycle. A Stop condition issued during any other clock cycle during the Write operation will not trigger the internally self-timed write cycle. Once the write cycle begins, the pre-loaded data word will be programmed in the amount of time not to exceed the t_{WR} specification. The t_{WR} time is defined in more detail in Section 7.2.4 on page 32. During this time, the Master should wait a fixed amount of time set to the t_{WR} specification, or for time sensitive applications, an ACK polling routine can be implemented (see Figure 7-5 on page 32). All inputs are ignored by the Serial EEPROM during the write cycle and the Serial EEPROM will not respond until the write cycle is complete. The Serial EEPROM will increment its internal address counter each time a byte is written.

Note: The temperature sensor operations can be accessed during the write cycle to read the Temperature Register or perform any other temperature sensor function.

Figure 7-3. Byte Write to Serial EEPROM

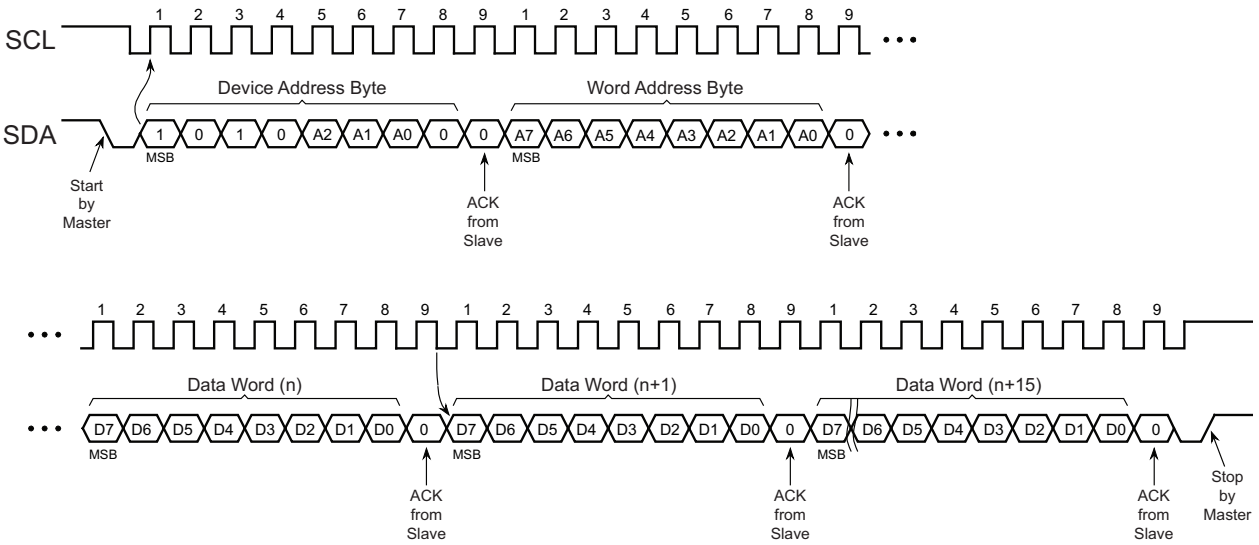


7.2.2 Page Write

The 4-Kbit Serial EEPROM is capable of writing up to 16 data bytes at a time executing the Page Write protocol sequence (see Figure 7-4). A partial or full Page Write operation is initiated the same as a Byte Write operation except that the Master does not send a Stop condition after the first data word is clocked in. Instead, after the Serial EEPROM has acknowledged receipt of the first data word, the Master can transmit up to fifteen more data words. The device will respond with an ACK after each data word is received. The lower four bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the internally generated word address reaches the page boundary, then the following data word is placed at the beginning of the same page. If more than sixteen data words are transmitted to the Serial EEPROM, the data word address will roll-over and the previous data will be overwritten. The address roll-over during a Write sequence is from the last byte of the current page to the first byte of the same page.

The Master ends the Page Write sequence with a Stop condition during the 10th clock cycle to initiate the internally self-timed write cycle. A Stop condition issued during any other clock cycle during the Write operation will not trigger the internally self-timed write cycle. Once the write cycle begins, the pre-loaded data words will be programmed in the amount of time not to exceed the t_{WR} specification. All inputs are ignored by the Serial EEPROM during the write cycle and the Serial EEPROM will not respond until the write cycle is complete. The t_{WR} time is defined in more detail in Section 7.2.4 on page 32. During this time, the Master should wait a fixed amount of time set to the t_{WR} specification, or for time sensitive applications, an ACK polling routine can be implemented (see Figure 7-5 on page 32).

Figure 7-4. Page Write to Serial EEPROM

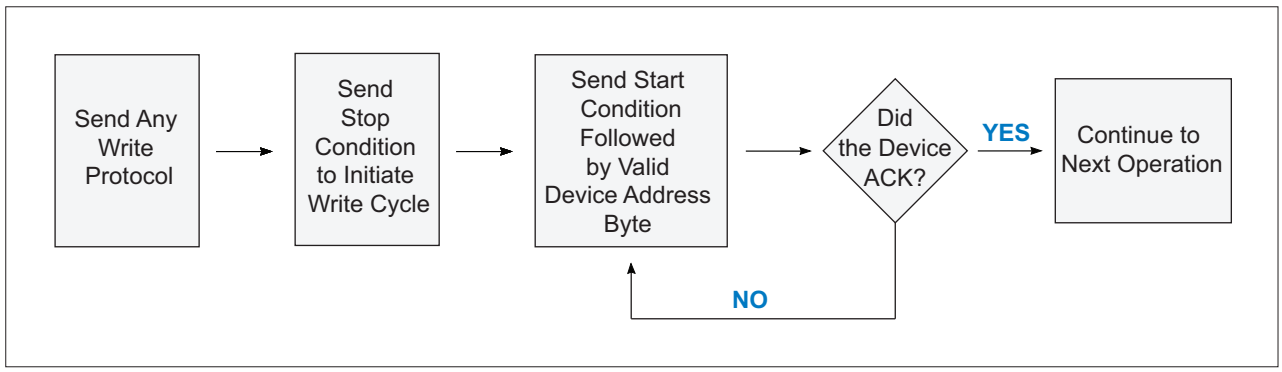


7.2.3 Acknowledge (ACK) Polling

An ACK polling routine can be implemented to optimize time sensitive applications that would not prefer waiting the fixed maximum write cycle time and would prefer to know immediately when the Serial EEPROM write cycle has completed to start a subsequent operation. Once the internally self timed write cycle has started (the Stop condition during the 10th clock cycle at the end of the Write sequence), the Serial EEPROM inputs are disabled and ACK polling can be initiated (see Figure 7-5). An ACK polling routine involves sending a valid Start condition followed by the device address byte. While the write cycle is in progress, the device will not respond with an ACK indicating the Serial EEPROM is busy writing data. Once complete, the device will ACK and the next device operation can be started.

Note: The temperature sensor operations can be accessed during the write cycle to read the Temperature Register or perform any other user desired temperature sensor operation.

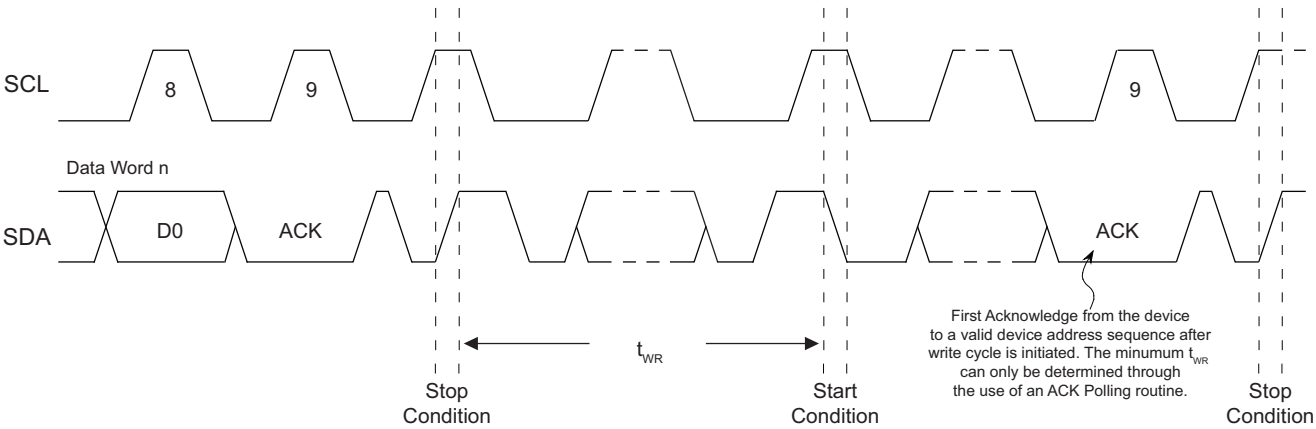
Figure 7-5. Acknowledge Polling Flow Chart



7.2.4 Write Cycle Timing

The length of the self timed write cycle, or t_{WR}, is defined as the amount of time from a valid Stop condition that begins the internal write sequence to the Start condition of the first device address byte sent to the AT30TSE004A that it subsequently responds to with an ACK. Figure 7-6 has been included to show this measurement.

Figure 7-6. Write cycle Timing



7.3 Write Protection

The AT30TSE004A incorporates a Reversible Software Write Protection (RSWP) feature that allows the ability to selectively write protect data stored in each of the four independent 128-byte Serial EEPROM quadrants. Table 7-3 identifies the memory quadrant identifier with its associated quadrant, SPA and memory address locations.

The AT30TSE004A has three RSWP software commands:

- Set RSWP command for setting the RSWP.
- Clear RSWP command for resetting all of the quadrants that are software write protected.
- Read RSWP command for reading the RSWP status.

Table 7-3. Serial EEPROM Memory Organization

Block	SPA	Address Locations	Memory Quadrant Identifier
Quadrant 0	0	00h to 7Fh	001
Quadrant 1	0	80h to FFh	100
Quadrant 2	1	00h to 7Fh	101
Quadrant 3	1	80h to FFh	000

7.3.1 Set RSWP

Setting the RSWP is enabled by sending the Set RSWP command, similar to a normal Write command to the device which programs the Write Protection to the target quadrant. The Set RSWP sequence requires sending a control byte of `'0110MMM0'` (where the `'M'` represents the memory quadrant identifier for the target quadrant to be write-protected) with the R/$\overline{W}$ bit set to a Logic 0. In conjunction with sending the protocol, the A_0 pin must be connected to V_{HV} for the duration of RSWP sequence (see Figure 7-7 and Section 8.2). The Set RSWP command acts on a single quadrant only as specified in the Set RSWP command and can only be reversed by issuing the Clear RSWP command and will unprotect all quadrants in one operation (see Table 7-4).

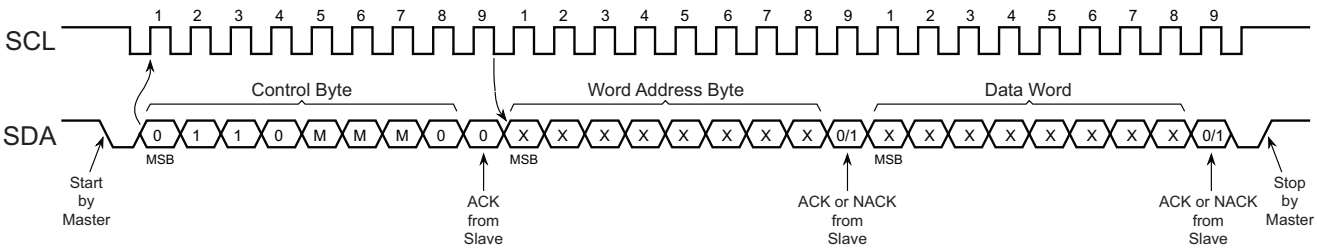
Example: If Quadrant 0 and Quadrant 3 are to be write-protected, two separate Set RSWP commands would be required; however, only one Clear RSWP command is needed to clear and unprotect both quadrants.

Table 7-4. Set RSWP and Clear RSWP

Function	Pin			Control Byte							
				Device Type Identifier				Memory Quadrant Identifier			R/$\overline{W}$
	A_2	A_1	A_0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Set RSWP, Quadrant 0	X	X	V_{HV}	0	1	1	0	0	0	1	0
Set RSWP, Quadrant 1	X	X						1	0	0	0
Set RSWP, Quadrant 2	X	X						1	0	1	0
Set RSWP, Quadrant 3	X	X						0	0	0	0
Clear RSWP	X	X						0	1	1	0

Notes:
1. X = Don't care but recommend to be hard-wired to V_{CC} or GND.
2. See Section 8.2 for the V_{HV} values.
3. Due to the requirement for the A_0 pin to be driven to V_{HV}, the Set RSWP and Clear RSWP commands are fully supported in a single DIMM (isolated DIMM) end application or single DIMM programming station only.

Figure 7-7. Set RSWP and Clear RSWP



M = Memory Quadrant Identifier

X = Don't care

7.3.2 Clear RSWP

Similar to the Set RSWP command, the reversible write protection on all quadrants can be reversed or unprotected by transmitting the Clear RSWP command. The Clear RSWP sequence requires the Master to send a Start condition followed by sending a control byte of '01100110' (66h) with the R/$\overline{W}$ bit set to a Logic 0. The AT30TSE004A should respond with an ACK. The Master transmits a word address byte and data bytes with don't care values. The AT30TSE004A will respond with either an ACK or NACK to both the word address and data word. In conjunction with sending the protocol, the A_0 pin must be connected to V_{HV} for the duration of the Clear RSWP command (see Figure 7-7 and Section 8.2). To end the Clear RSWP sequence, the Master sends a Stop condition.

Caution: The write protection of individual quadrants cannot be reversed separately, and executing the Clear RSWP command will clear the write protection on all four quadrants leaving all quadrants with no software write protection.

7.3.3 Read RSWP

The Read RSWP command allows the ability to check a quadrant's write protection status. To find out if the Software Write Protection has been set to a specific quadrant, the same procedure that was used to set the quadrant's write protection can be utilized except that the R/$\overline{W}$ select bit is set to a Logic 1, and the A_0 pin is not required to have V_{HV} (see Table 7-6).

The Read RSWP sequence requires sending a control byte of '0110MMM1' (where the 'M' represents the memory quadrant identifier for the quadrant to be read) with the R/$\overline{W}$ bit set to a Logic 1 (see Figure 7-8).

If the RSWP has not been set, then the AT30TSE004A responds to the control byte with an ACK, and responds to the word address byte and data word with a NACK. If the RSWP has been set, the AT30TSE004A responds to all three bytes (control, word address, and data bytes) with a NACK as shown in Table 7-5.

Table 7-5. Serial EEPROM Acknowledge When Reading Protection Status

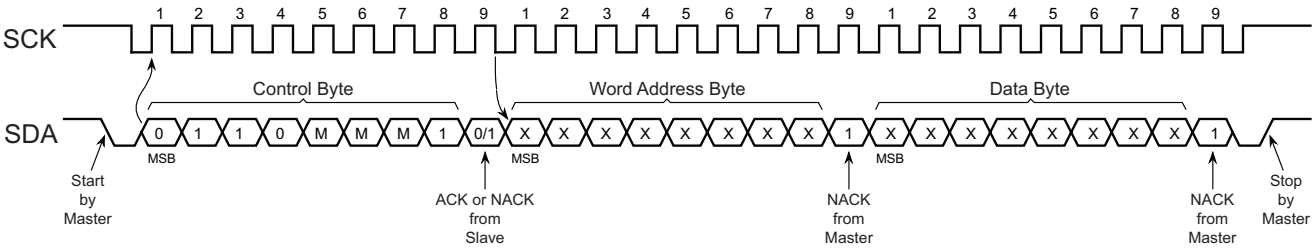
Quadrant Status	Instruction Sent	Instruction Response	Word Address Sent	Word Address Response	Data Word Sent	Data Word Response
Write Protected	Read RSWP	NACK	Don't Care	NACK	Don't Care	NACK
Not Protected	Read RSWP	ACK	Don't Care	NACK	Don't Care	NACK

Table 7-6. Read RSWP

Function	Pin			Control Byte							
				Device Type Identifier				Memory Quadrant Identifier			R/$\overline{W}$
	A_2	A_1	A_0	B7	B6	B5	B4	B3	B2	B1	B0
Read RSWP, Quadrant 0	X	X	0, 1 or V_{HV}	0	1	1	0	0	0	1	1
Read RSWP, Quadrant 1	X	X						1	0	0	1
Read RSWP, Quadrant 2	X	X						1	0	1	1
Read RSWP, Quadrant 3	X	X						0	0	0	1

Notes: 1. X= Don't care but recommend to be hard-wired to V_{CC} or GND.
2. See Section 8.2 for the V_{HV} values.

Figure 7-8. Read RSWP



M = Memory Quadrant Identifier
X = Don't care

7.4 Serial EEPROM Read Operations

All Read operations are initiated by the Master transmitting a Start bit, a device type identifier of '1010' (Ah), three software address bits (A2, A1, and A0) that match their corresponding hard-wired address pins (A_2, A_1, and A_0), and the R/$\overline{W}$ select bit with a Logic 1 state. In the following clock cycle, the device should respond with an ACK. The subsequent protocol depends on the type of Read operation desired. There are three Read operations:

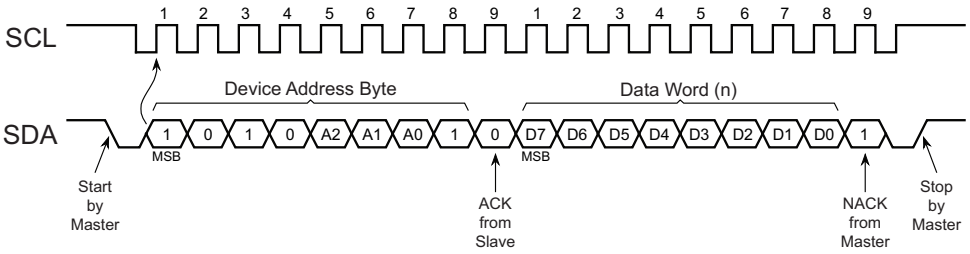
- Current Address Read
- Random Address Read
- Sequential Read

Caution: All Read operations should be preceded by the SPA and or RPA commands to ensure the desired half of the memory is selected. The reason this is important, for example, during a Sequential Read operation on the last byte in the first half of the memory (address FFh) with SPA=0 (indicating first half is selected), the internal address counter will roll-over to address 00h in the first half of memory as opposed to the first byte in the second half of the memory. For more information on the SPA and RPA commands, see Section 7.1.1 "Set Page Address and Read Page Address Commands" on page 27.

7.4.1 Current Address Read

Following a Start condition, the Master only transmits the device address byte with the R/$\overline{W}$ select bit set to a Logic 1 (see Figure 7-9). The AT30TSE004A should respond with an ACK and then serially transmits the data word addressed by the internal address counter. The internal data word address counter maintains the last address accessed during the last Read or Write operation, incremented by one. This address stays valid between operations as long as power to the device is maintained. The address roll-over during a Read is from the last byte of the last page to the first byte of the first page of the addressed 2-Kbit (depends on the current SPA setting). To end the command, the Master does not respond with an ACK but does generate a following Stop condition.

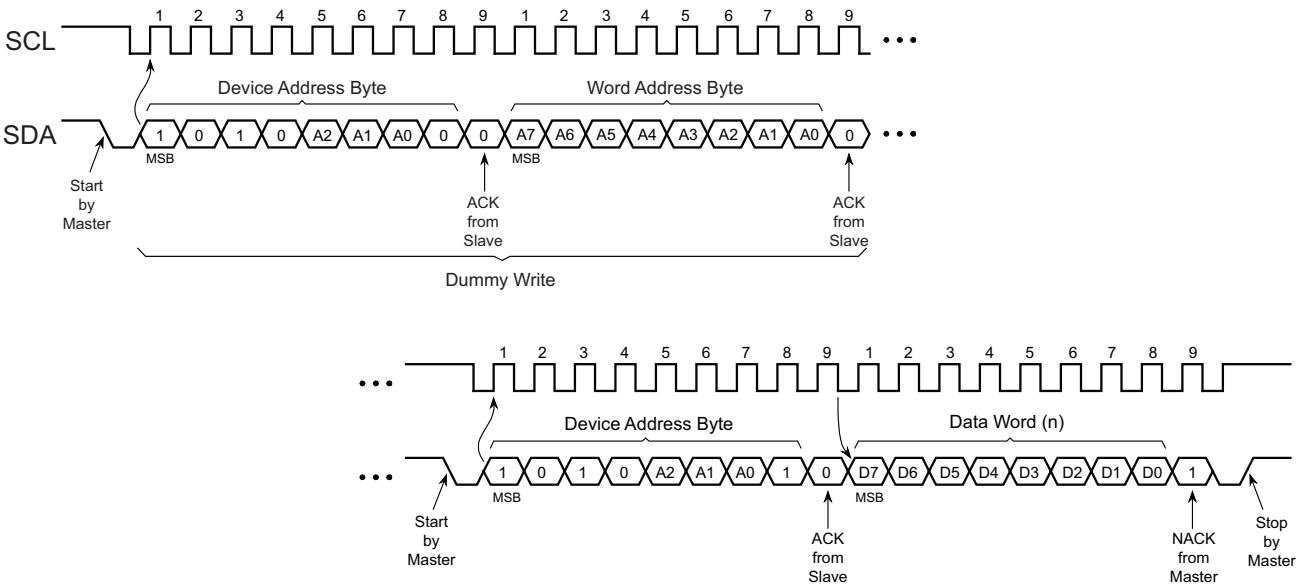
Figure 7-9. Current Address Read from Serial EEPROM



7.4.2 Random Read

A Random Read operation allows the Master to access any memory location in a random manner and requires a dummy write sequence to preload the starting data word address. To perform a Random Read, the device address byte and the word address byte are transmitted to the AT30TSE004A as part of the dummy Write sequence (see Figure 7-10). Once the device address byte and data word address are clocked in and acknowledged by the AT30TSE004A, the Master must generate another Start condition. The Master initiates a Current Address Read by sending another device address byte with the R/$\overline{W}$ select bit to a Logic 1. The AT30TSE004A acknowledges the device address byte, increments its internal address counter and serially clocks out the first data word. The device will continue to transmit sequential data words as long as the Master continues to ACK each data word. To end the sequence, the Master responds with a NACK and a Stop condition.

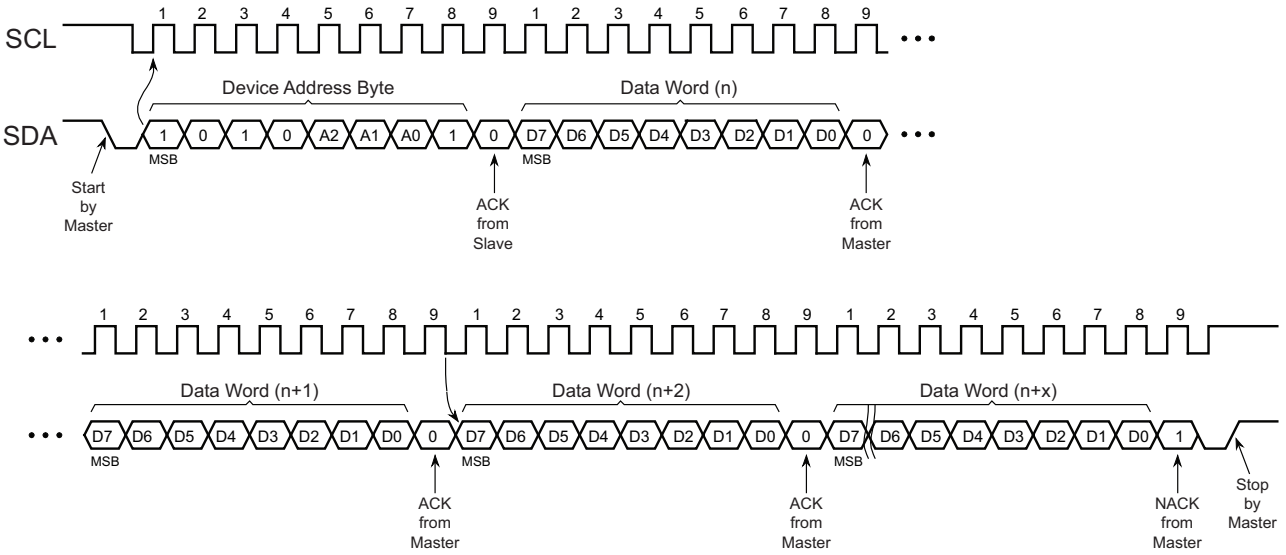
Figure 7-10. Random Read from Serial EEPROM



7.4.3 Sequential Read

A Sequential Read operation is initiated in the same way as a Random Read operation, except after the AT30TSE004A transmits the first data word, the Master responds with an ACK (instead of a NACK followed by a Stop condition). As long as the AT34TSE004A receives an ACK, it will continue to increment the data word address and serially clock out the sequential data words (see Figure 7-11). When the internal address counter is at the last byte of the last page, the data word address will roll-over to the beginning of the selected 2-Kbit array (depending on the SPA setting) starting at address zero, and the Sequential Read operation will continue. The Sequential Read operation is terminated when the Master responds with a NACK followed by a Stop condition.

Figure 7-11. Sequential Read from Serial EEPROM



8. Electrical Specifications

8.1 Absolute Maximum Ratings*

Temperature under Bias	-40°C to +125°C
Storage Temperature	-65°C to +150°C
Supply voltage with respect to ground	-0.5V to +4.3V
A_0 Pin	-0.5V to +12.0V
All other input voltages with respect to ground	-0.5V to V_{CC} + 0.5V
$\overline{EVENT}$ Pin	-0.5V to V_{CC} + 0.3V
All other output voltages with respect to ground	-0.5V to V_{CC} + 0.5V

*Notice: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these ratings or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Voltage extremes referenced in the "Absolute Maximum Ratings" are intended to accommodate short duration undershoot/overshoot conditions and does not imply or guarantee functional device operation at these levels for any extended period of time.

Pull-up voltages applied to the $\overline{EVENT}$ Pin that exceed the "Absolute Maximum Ratings" may forward bias the ESD protection circuitry. Doing so may result in improper device function and may corrupt temperature measurements.

8.2 DC Characteristics

Applicable over recommended operating range: T_{AI} = -20°C to +125°C, V_{CC} = 1.7V to 3.6V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.7		3.6	V
V_{CC2}	Supply Voltage			2.2		3.6	V
I_{CC1}	Supply Current(2)	V_{CC} = 3.6V	Read at 100kHz		0.4	1.0	mA
I_{CC2}	Supply Current(2)	V_{CC} = 3.6V	Write at 100kHz		1.5	3.0	mA
I_{CC3}	Temp Sensor	V_{CC} = 3.6V	EE Inactive		0.2	0.5	mA
I_{SB}	Standby Current(3)	V_{CC} = 1.7V	V_{IN} = V_{CC} or V_{SS}		1.6	3.0	µA
		V_{CC} = 3.6V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}			0.1	2.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}			0.1	2.0	µA
V_{IL}	Input Low Level(1)			-0.5		0.3 * V_{CC}	V
V_{IH}	Input High Level(1)			0.7 * Vcc		Vcc + 0.5	V
V_{OL1}	Low-Level Output Voltage Open-Drain	V_{CC} > 2V	I_{OL} = 3mA			0.4	V
V_{OL2}		V_{CC} ≤ 2V	I_{OL} = 2mA			0.2 * V_{CC}	V
I_{OL}	Low-Level Output Current	V_{OL} = 0.4V	Freq ≤ 400kHz	3.0			mA
		V_{OL} = 0.6V	Freq ≤ 400kHz	6.0			mA
		V_{OL} = 0.4V	Freq > 400kHz	20.0			mA
V_{HV}	A_0 Pin High Voltage	V_{HV} - V_{CC} ≥ 4.8V		7		10	V
V_{HYST1}	Input Hysteresis (SDA, SCL)	V_{CC} < 2V		0.10 * V_{CC}			V
V_{HYST2}	Input Hysteresis (SDA, SCL)	V_{CC} ≥ 2V		0.05 * V_{CC}			V

Notes:
1. V_{IL} min and V_{IH} max are reference only and are not tested.
2. TS in Shutdown mode.
3. Serial EEPROM inactive, TS in Shutdown mode.

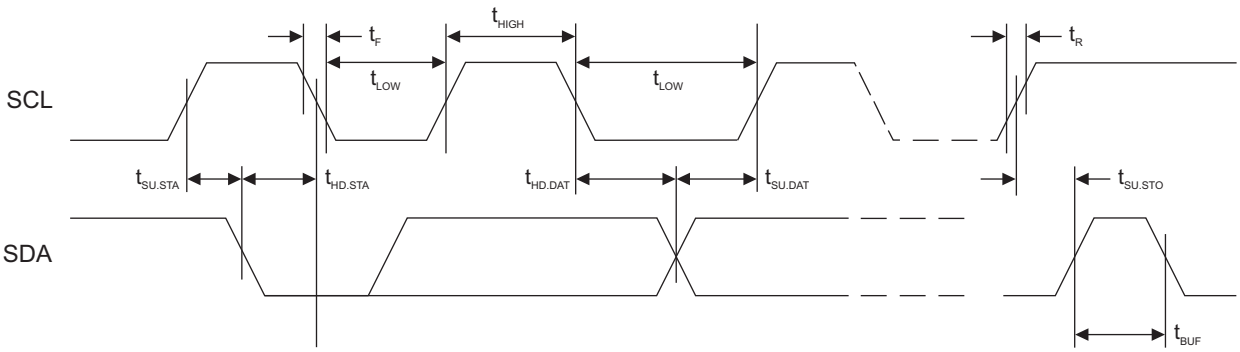
8.3 AC Characteristics

Applicable over recommended operating range: T_{AI} = -20°C to +125°C, V_{CC} = 1.7V to 3.6V, CL = 1 TTL Gate and 100µF (unless otherwise noted).

Symbol	Parameter	V_{CC} < 2.2V		V_{CC} ≥ 2.2V				Units
		100kHz		400kHz		1000kHz		
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL	10[2]	100	10[2]	400	10[2]	1000	kHz
t_{LOW}	Clock Pulse Width Low	4700		1300		500		ns
t_{HIGH}	Clock Pulse Width High	4000		600		260		ns
t_I	Noise Suppression Time		100		50		50	ns
t_{BUF}	Time the bus must be free before a new transmission can start[1]	4700		1300		500		ns
$t_{HD.STA}$	Start Hold Time	4000		600		260		ns
$t_{SU.STA}$	Start Set-up Time	4700		600		260		ns
$t_{HD.DI}$	Data In Hold Time	0		0		0		ns
$t_{SU.DAT}$	Data In Set-up Time	250		100		50		ns
t_R	Inputs Rise Time[1]		1000	20	300		120	ns
t_F	Inputs Fall Time[1]		300	20	300		120	ns
$t_{SU.STO}$	Stop Set-up Time	4000		600		260		ns
$t_{HD.DAT}$	Data Out Hold Time	200	3450	200	900	0	350	ns
t_{WR}	Write Cycle Time		5		5		5	ms
t_{OUT}	Timeout Time	25	35	25	35	25	35	ms
EEPROM Write Endurance	25°C, Page Mode[1]	1,000,000						Write Cycles

Notes: 1. This parameter is ensured by characterization only.
2. The minimum frequency is specified at 10kHz to avoid activating the timeout feature.

Figure 8-1. SCL: Serial Clock
SDA: Serial Data I/O



8.4 Temperature Sensor Characteristics

Applicable over recommended operating range: T_{AI} = -20°C to +125°C, V_{CC} = 1.7V to 3.6V (unless otherwise noted).

Symbol	Parameter	Test Condition	Freq. ≤ 400kHz			Freq. > 400kHz			Units
			Min	Typ	Max	Min	Typ	Max	
T_{ACC}	TS Accuracy (B-grade)	+75°C < Ta < +95°C		±0.5	±1.0		±0.5	±1.0	°C
		+40°C < Ta < +125°C		±1.0	±2.0		±1.0	±2.0	°C
		-20°C < Ta < +125°C		±2.0	±3.0		±2.0	±3.0	°C
T_{CONV}	TS Conversion Time			75.0	125.0		75.0	125.0	ms
T_{RES}	TS Resolution			0.125			0.125		°C

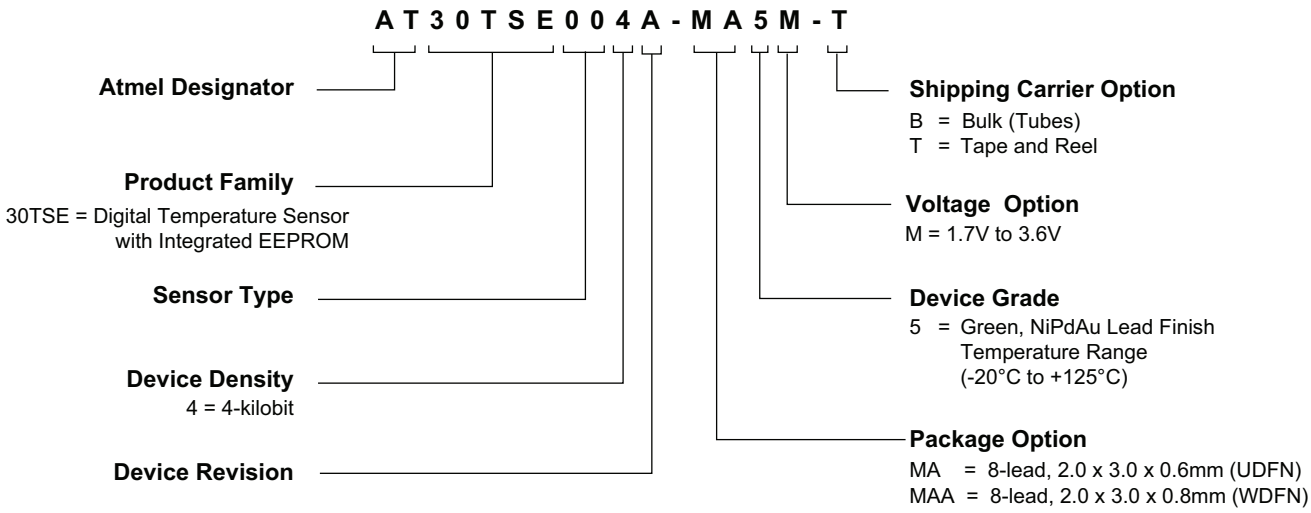
8.5 Pin Capacitance[1]

Applicable over recommended operating range from T_A = +25°C, f = 1MHz, V_{CC} = 1.7V – 3.6V.

Symbol	Test condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA, $\overline{EVENT}$)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is ensured by characterization only.

9. Ordering Code Detail



10. Ordering Information

Ordering Code[1]	Package	Lead Finish	Operating Voltage	Max. Frequency	Operational Range
AT30TSE004A-MA5M-T[2]	8MA2	NiPdAu	1.7V to 3.6V	1000kHz	–20°C to 125°C
AT30TSE004A-MAA5M-T[2]	8MAA				

Notes: 1. Consistent with the general semiconductor market trend, Atmel will supply devices with either gold or copper bond wires to increase manufacturing flexibility and ensure a long-term continuity of supply. There is no difference in product quality, reliability, or performance between the two variations.

2. T = Tape and Reel
   - UDFN and WDFN= 5K per reel

	Package Type
8MA2	8-lead, 2.0 x 3.0 x 0.6mm, Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead (UDFN)
8MAA	8-lead, 2.0 x 3.0 x 0.8mm, Thermally Enhanced Plastic Very Very Thin Dual Flat No Lead (WDFN)

11. Part Markings

AT30TSE004A: Package Marking Information

8-lead UDFN	8-lead WDFN
2.0 x 3.0 mm Body	2.0 x 3.0 mm Body
	

Note 1: ● Designates pin 1

Note 2: Package drawings are not to scale

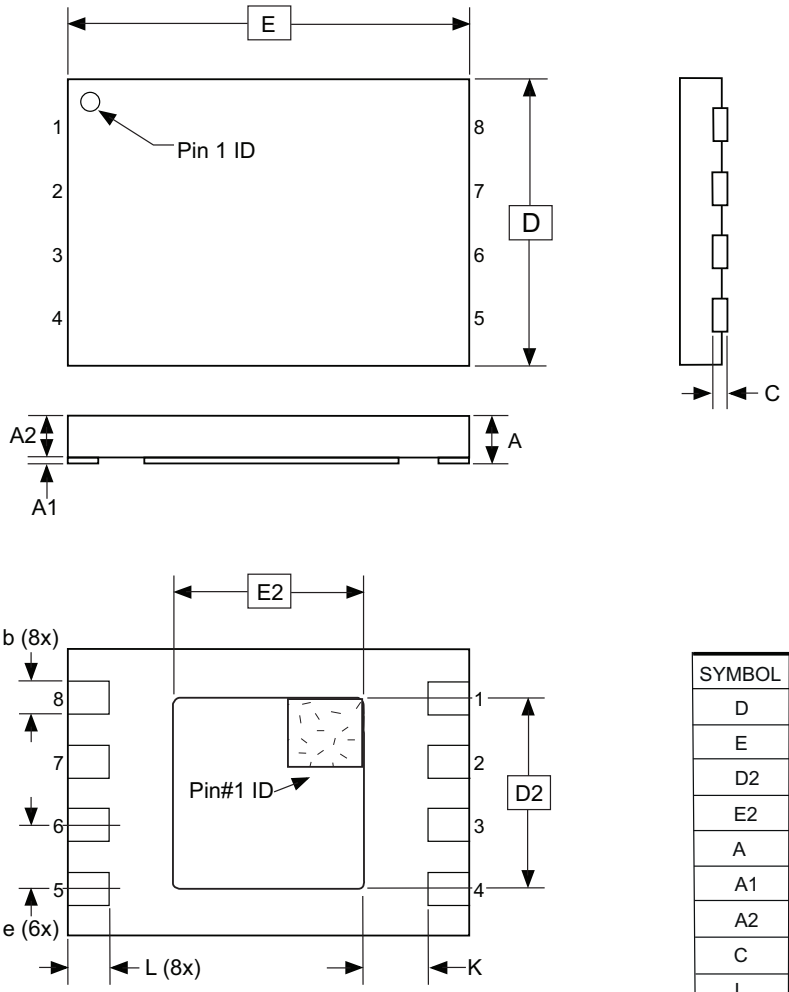
Catalog Number Truncation			
AT30TSE004A		Truncation Code ###: T8A	
Date Codes			**Voltages**
Y = Year	M = Month	WW = Work Week of Assembly	% = Minimum Voltage
2: 2012 6: 2016 3: 2013 7: 2017 4: 2014 8: 2018 5: 2015 9: 2019	A: January B: February ... L: December	02: Week 2 04: Week 4 ... 52: Week 52	M: 1.7V min
Country of Assembly	**Lot Number**		**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number		5: Industrial (-20°C to 125°C) NiPdAu
Trace Code			**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

3/8/13

Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	**TITLE** **30TSE004ASM**, AT30TSE004A Package Marking Information	**DRAWING NO.** 30TSE004A	**REV.** A

12. Package Drawings

12.1 8MA2 — 8-pad UDFN



COMMON DIMENSIONS
(Unit of Measure = mm)

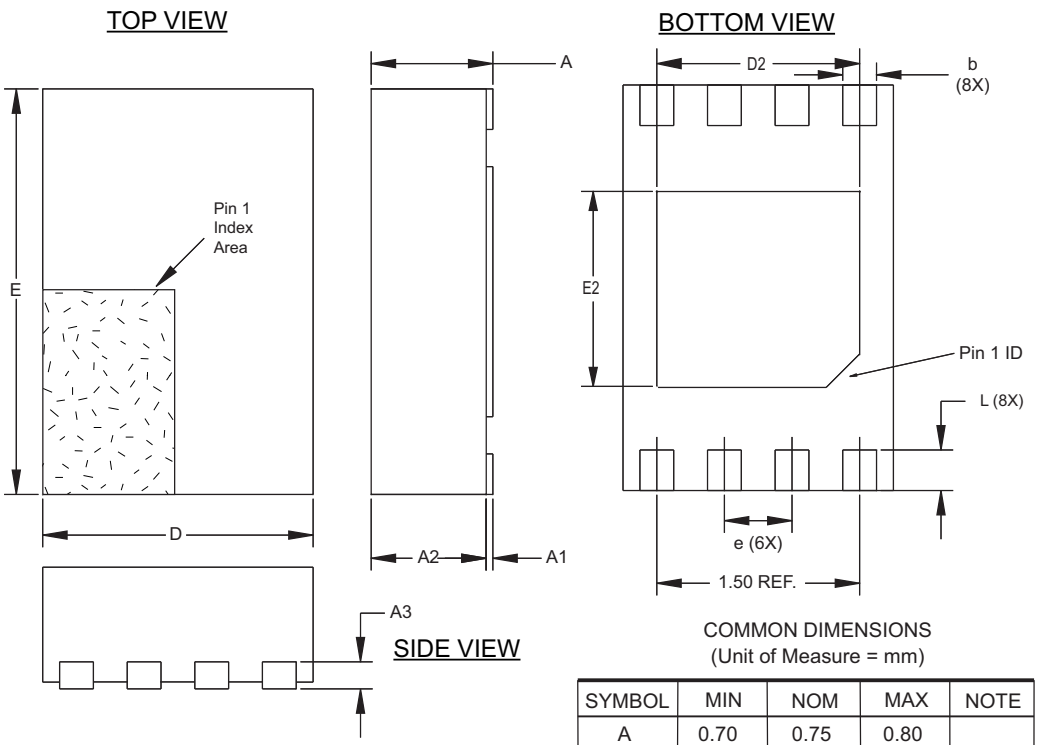
SYMBOL	MIN	NOM	MAX	NOTE
D	1.90	2.00	2.10	
E	2.90	3.00	3.10	
D2	1.40	1.50	1.60	
E2	1.20	1.30	1.40	
A	0.50	0.55	0.60	
A1	0.0	0.02	0.05	
A2	–	–	0.55	
C	0.152 REF			
L	0.30	0.35	0.40	
e	0.50 BSC			
b	0.18	0.25	0.30	3
K	0.20	–	–	

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. The terminal #1 ID is a laser-marked feature.
3. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.

9/6/12

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8MA2, 8-pad, 2 x 3 x 0.6 mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)	GPC YNZ	DRAWING NO. 8MA2	REV. C

12.2 8MAA — 8-pad WDFN



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.70	0.75	0.80	
A1	0.00	0.02	0.05	
A2	0.45	0.55	0.65	
A3		2.0 REF		
D	1.90	2.00	2.10	
D2	1.20	-	1.60	
E	2.90	3.00	3.10	
E2	1.20	-	1.60	
b	0.18	0.25	0.30	2
L	0.30	–	0.45	
e		0.50 BSC		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229, WCED-3, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
3. Soldering the large thermal pad is optional, but not recommended. No electrical connection is accomplished to the device through this pad, so if soldered it should be tied to ground

09/11/12

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8MAA, 8-pad 2.0 x 3.0mm Body, 0.50mm Pitch Very, Very Thin Dual No Lead Package (WDFN) (Sawn)	GPC YRV	DRAWING NO. 8MAA	REV. A

13. Revision History

Doc. Rev.	Date	Comments
8868C	12/2013	Updated Section, “Power-up Conditions” and Figure, “Power-up Timing”.
8868B	07/2013	Updated the Absolute Maximum Ratings.
8868A	04/2013	Initial document release.





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