ADE3700

Analog LCD Display Engine for XGA and SXGA Resolutions

TARGET SPECIFICATION

Feature Overview

- Programmable Context Sensitive™ Scaling
- High-quality Up-scaling and Down-scaling
- Integrated 9-bit ADC/PLL
- IQSync™ AutoSetup
- Integrated programmable Timing Controller
- Integrated Pattern Generator
- Perfect Picture™ Technology
- sRGB 3D Color Warp
- Integrated OSD
- Advanced EMI reduction features
- Framelock operation with Safety Mode™
- Serial I²C interface
- Low power 0.18 µm process technology

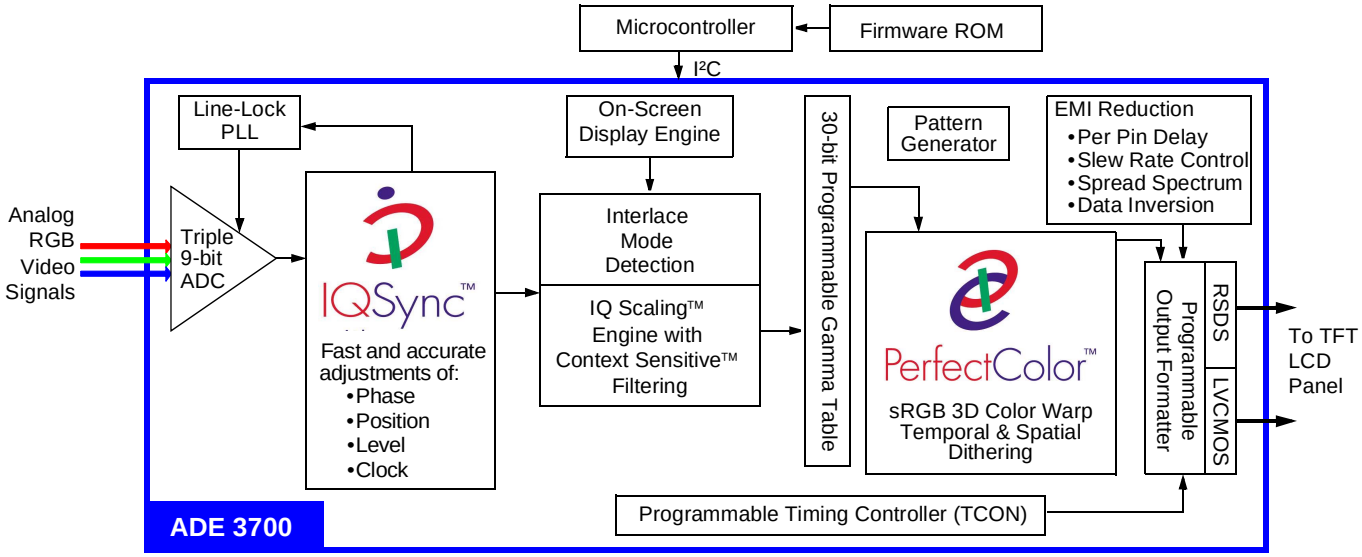
General Description

ADE3700 devices are a family of highly-integrated display engine ICs, enabling the most advanced, flexible, and cost-effective system-on-chip solutions for analog-only input LCD display applications.

The ADE3700 covers the full range of XGA and SXGA analog-only applications including Smart Panel designs.

The ADE3700 family is pin-to-pin compatible and comes in a low-cost, 128-pin LQFP package.

ADE3700 devices use the same software platform and are backward-compatible with the previous generation of ADE3xxx Scaling Engines.



LCD Scaler Product Selector

Product	Package	Output Format Support		Input Interface Support		
		Resolution	TCON	Analog	DVI	YUV
ADE3700X	128 LQFP	Up to XGA 75 Hz		Yes		
ADE3700XT	128 LQFP	Up to XGA 75 Hz	Yes	Yes		
ADE3700SX	128 LQFP	Up to SXGA 75 Hz		Yes		

This is preliminary information on a new product forseen to be developed. Details are subject to change without notice.

Third Generation Context Sensitive™ Scaler

- Sharper text with Edge Enhancement
- RAM based coefficients for unique customization
- 5:1 Upscale and 2:1 Downscale
- Independent X - Y axis zoom and shrink

Analog RGB input

- 140 MHz 9-bit ADC
- Ultra low jitter digital Line Lock PLL
- Composite Sync and Sync on Green support

IQsync™ AutoSetup

- AutoSetup configures phase, clock, level, and position
- Supports continuous calibration for reduced user intervention
- Automatically detects activity on input
- Compatible with all standard VESA and GTF modes

Perfect Picture™ Technology

- Programmable 3D Color Warp
- Digital brightness, contrast, hue, and saturation gamma controls for all inputs
- Simple white point control
- Compatible with sRGB standard
- Video & Picture windowing
- Supports up to 7 different windows
- Independent window controls for contrast brightness, saturation, hue and gamma

Perfect Color™ Technology

- True color dithering for 12- and 18-bit panels
- Temporal and spatial dithering
- 30-bit programmable gamma table

OSD Engine

- 256 RAM based 12x18 characters
- 1- and 4-bit per pixel color characters
- Bordering, shadowing, transparency, fade-in, and fade-out effects
- Supports font rotation
- Up to 4 sub windows
- 32-entry TrueColor LUT

Programmable Timing Controller (TCON)

- Highly programmable support for XGA SmartPanels
- Dual-function LVCMOS and RSDS outputs
- Supports 18-, 24-, 36-, and 48-bit RSDS outputs
- Advanced Flicker Detection and Reduction
- 12 programmable timing signals for row/ column control
- Wide range of drivers & TCON compatibility
- Simulation tools for easy programming
- Supports complex polarity generation for IPS panels

Advanced EMI Reduction Features

- Flexible data inversion / transition minimization, single, dual, and separate
- Per pin delay, 0 to 6ns in 0.4ns increments
- Adaptive Slew Rate control outputs
- Differential clock
- Spread spectrum -programmable digital FM modulation of the output clock with no external components

Output Format

- Supports resolutions up to SXGA @ 75Hz
- Supports 6- or 8-bit Panels
- Supports double or single pixel wide formats

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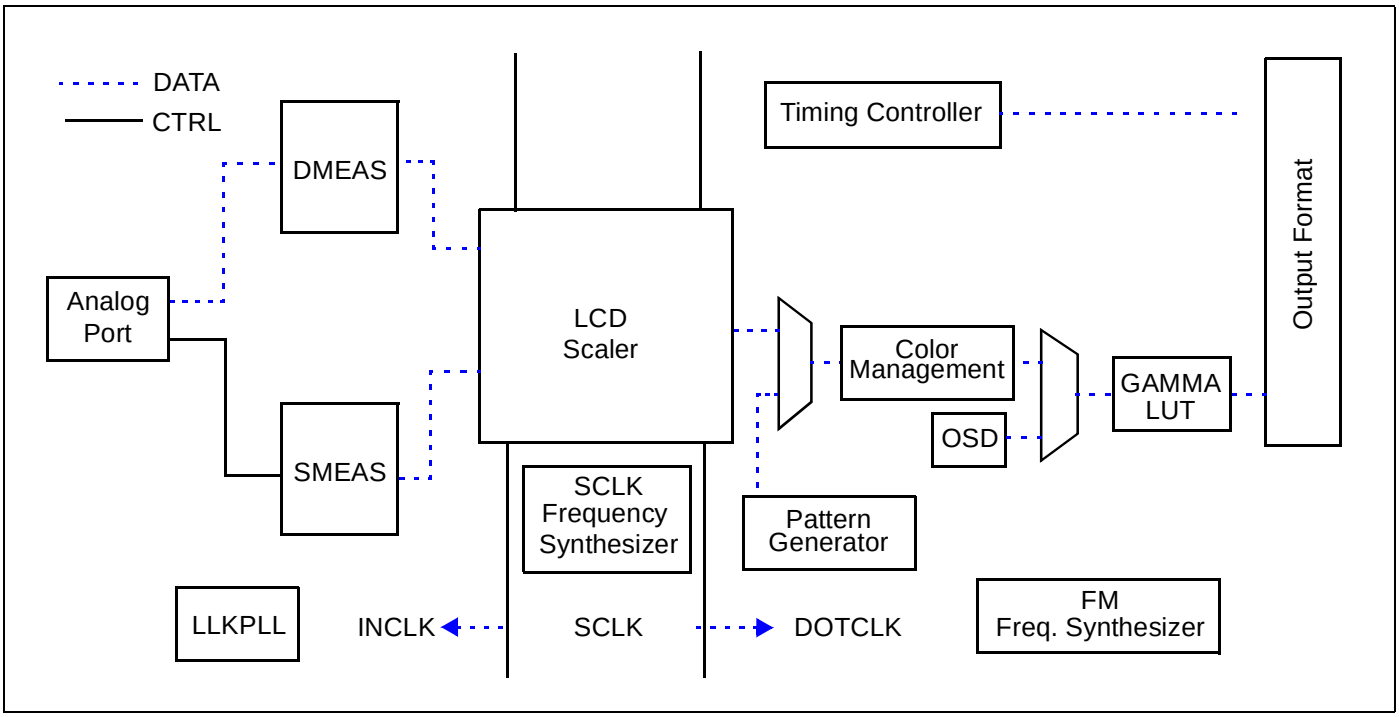
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1 General Information

The ADE3700 family of devices is capable of implementing all of the advanced features of today's LCD monitor products. For maximum flexibility, an external microcontroller (MCU) is used for controlling the ADE3700 and other monitor functions.

Figure 1: ADE3700 Block Diagram



The ADE3700 architecture unburdens the MCU from all data-intensive pixel manipulations, providing an optimal blend of features and code customizing without incurring the cost of a 16-bit processor or memory. The key interactions between the monitor MCU and the ADE3700 can be broken down into the features shown in the table below.

Table 1: ADE3700 Features (Sheet 1 of 2)

Feature	Description of ADE3700 Operation	Blocks Used	Pages
Power-up / Initialize	When power is first applied, the ADE3700 is asynchronously reset from a pin. The MCU typically programs the ADE3700 with a number of default values and sets up the ADE3700 to identify activity on any of the input pins. All pre-configured values and RAMs, such as DVI settings, line-lock PLL settings, OSD characters, LCD timing values (output sequencer), scale kernels, gamma curves, sRGB color warp, APC dithering, output pin configuration (OMUX), etc. can be pre-loaded into the ADE3700. The typical end state is that the ADE3700 is initialized into a low power mode, ready to turn active once the power button is pressed.	GLBL SMEAS LLK ADC OSD SCALER GAMMA SRGB OUTSEQ TCON APC OMUX	11 25 18 17 62 42 70 60 45 48 71 72
Activity Detect	When the monitor has been powered on, the inputs can be monitored for active video sources. Based on the activity monitors, the MCU chooses an input or power down state.	SMEAS	25

Table 1: ADE3700 Features (Sheet 2 of 2)

Feature	Description of ADE3700 Operation	Blocks Used	Pages
Sync / Timing Measurement	Once an input source is selected, all available information on frequencies and line/pixel counts is measured for the selected source and made available to the MCU.	SMEAS	25
Mode Set	Once the MCU has determined the matching video mode or calculated a video mode using a GTF algorithm, the datapath is programmed to drive the flat panel. Clock frequencies for the internal memory and datapath are also set at this time.	GLBL LLK SRT DMUX SMUX SCALER	11 18 23 37 32 42
Autotune	When the MCU calls for an autotune, the MCU sets up an iterative loop to search for the best phase, gain, offset, etc. At each step of the loop, the MCU kicks off a test in which the ADE3700 which performs extensive statistical analysis of the incoming data stream. The results of the analysis are made available to the MCU which is responsible for the optimization algorithm.	DMEAS LLK ADC SMUX SRT	47 18 17 32 23
Digital Contrast / Brightness	In response to user OSD control, the MCU can program single 8-bit registers that set brightness and contrast for each color channel independently.	SRGB	60
White Point Control	In response to user OSD control, the MCU can program three 8-bit registers that set the white point for the output.	SRGB	60
GAMMA Adjustment	The MCU can program the gamma RAMs to implement 10-bit accurate color transformations.	GAMMA	70
sRGB Control	The SRGB block allows simple, intuitive color control with just a few registers.	SRGB	60
Pattern Generation	For production testing, the ADE3700 can be programmed by the MCU to output a wide set of test patterns.	PGEN	54
Flicker Reduction	For Smart Panel applications, the MCU can set up the flicker detection block to report any correlation with the polarity inversion signal. The MCU can then change the polarity inversion to a non-correlating pattern to eliminate flicker.	FLICKER TCON	68 48
Backlight Control	The ADE3700 provides two PWM outputs for direct control of the power components in a typical backlight. The MCU sets up the registers and enables the function.	PWM	80
Low Power State	To enter a low power state, the MCU can gate of most of the clocks and put the analog blocks into a low power standby state.	GLBL	11

1.1 Pin Descriptions

Table 2: Pinout (Sheet 1 of 4)

LQFP128	Name	Type	Description
32	XVDD18	Power	Crystal Oscillator 1.8V VDD
31	XTAL_OUT	Output	Crystal Oscillator output
30	XTAL_IN	Input	Crystal Oscillator input
29	XGND	Power	Crystal Oscillator Ground
19	XCLK_EN	Input	Crystal clock output enable
18	XCLK	Output	Crystal clock buffered output
34	VSYNC	Input	Vertical Sync Input
21	TSTCLK	Input	Connect to Digital Ground
65	TST_SCAN	Input	Connect to Digital Ground
8	TCON7	Output	TCON Output 7
9	TCON6/OVS	Output	TCON Output 6/Output Vertical Sync
10	TCON5/OHS	Output	TCON Output 5/Output Horizontal Sync
11	TCON4/ODE	Output	TCON Output 4/Output Data Enable
12	TCON3	Input/Output	TCON Output 3
13	TCON2	Input/Output	TCON Output 2
14	TCON1	Input/Output	TCON Output 1
15	TCON0	Input/Output	TCON Output 0
17	SDA	Open Drain I/O	I2C Data
16	SCL	Input	I2C Clock
20	RESETN	Input	Reset input, Active Low
54	REFR	Passive	1% 15.0 kOhm resistor to Analog Ground
55	REFMR	Passive	Connect to Analog Ground
48	REFMG	Passive	Connect to Analog Ground
41	REFMB	Passive	Connect to Analog Ground
47	REFG	Passive	1% 15.0 kOhm resistor to Analog Ground
58	REFCR	Passive	100nF capacitor to Analog Ground
51	REFCG	Passive	100nF capacitor to Analog Ground
44	REFCB	Passive	100nF capacitor to Analog Ground
40	REFB	Passive	1% 15.0 kOhm resistor to Analog Ground
26	PVDD18	Power	PLL 1.8V VDD
28	PVDD18	Power	PLL 1.8V VDD
25	PGND	Power	PLL Ground
27	PGND	Power	PLL Ground
105	AVS	Output	Alternate Vertical Sync
126	ORB7	Input/Output	Output Port B: Red Data 7
127	ORB6	Input/Output	Output Port B: Red Data 6

Table 2: Pinout (Sheet 2 of 4)

LQFP128	Name	Type	Description
128	ORB5	Input/Output	Output Port B: Red Data 5
1	ORB4	Input/Output	Output Port B: Red Data 4
2	ORB3	Input/Output	Output Port B: Red Data 3
3	ORB2	Input/Output	Output Port B: Red Data 2
4	ORB1	Input/Output	Output Port B: Red Data 1
5	ORB0	Input/Output	Output Port B: Red Data 0
86	ORA7	Output	Output Port A: Red Data 7
87	ORA6	Output	Output Port A: Red Data 6
88	ORA5	Output	Output Port A: Red Data 5
89	ORA4	Output	Output Port A: Red Data 4
90	ORA3	Output	Output Port A: Red Data 3
95	ORA2	Output	Output Port A: Red Data 2
96	ORA1	Output	Output Port A: Red Data 1
97	ORA0	Output	Output Port A: Red Data 0
103	AHS	Output	Alternate Horizontal Sync
112	OGB7	Input/Output	Output Port B: Green Data 7
113	OGB6	Input/Output	Output Port B: Green Data 6
114	OGB5	Input/Output	Output Port B: Green Data 5
115	OGB4	Input/Output	Output Port B: Green Data 4
120	OGB3	Input/Output	Output Port B: Green Data 3
121	OGB2	Input/Output	Output Port B: Green Data 2
122	OGB1	Input/Output	Output Port B: Green Data 1
123	OGB0	Input/Output	Output Port B: Green Data 0
74	OGA7	Output	Output Port A: Green Data 7
75	OGA6	Output	Output Port A: Green Data 6
76	OGA5	Output	Output Port A: Green Data 5
77	OGA4	Output	Output Port A: Green Data 4
78	OGA3	Output	Output Port A: Green Data 3
79	OGA2	Output	Output Port A: Green Data 2
82	OGA1	Output	Output Port A: Green Data 1
83	OGA0	Output	Output Port A: Green Data 0
102	ADE	Output	Alternate Data Enable
104	OCLK	Output	Output Clock
98	OBB7	Input/Output	Output Port B: Blue Data 7
99	OBB6	Input/Output	Output Port B: Blue Data 6
100	OBB5	Input/Output	Output Port B: Blue Data 5
101	OBB4	Input/Output	Output Port B: Blue Data 4

Table 2: Pinout (Sheet 3 of 4)

LQFP128	Name	Type	Description
108	OBB3	Input/Output	Output Port B: Blue Data 3
109	OBB2	Input/Output	Output Port B: Blue Data 2
110	OBB1	Input/Output	Output Port B: Blue Data 1
111	OBB0	Input/Output	Output Port B: Blue Data 0
66	OBA7	Output	Output Port A: Blue Data 7
67	OBA6	Output	Output Port A: Blue Data 6
68	OBA5	Output	Output Port A: Blue Data 5
69	OBA4	Output	Output Port A: Blue Data 4
70	OBA3	Output	Output Port A: Blue Data 3
71	OBA2	Output	Output Port A: Blue Data 2
72	OBA1	Output	Output Port A: Blue Data 1
73	OBA0	Output	Output Port A: Blue Data 0
56	INR	Input	Analog Video Port: Red Channel input
49	ING	Input	Analog Video Port: Green Channel input
42	INB	Input	Analog Video Port: Blue Channel input
35	HSYNC	Input	Horizontal (or Composite) Sync Input
7	DVDD33	Power	Digital 3.3V VDD
64	DVDD33	Power	Digital 3.3V VDD
80	DVDD33	Power	Digital 3.3V VDD
91	DVDD33	Power	Digital 3.3V VDD
106	DVDD33	Power	Digital 3.3V VDD
119	DVDD33	Power	Digital 3.3V VDD
23	DVDD18	Power	Digital 1.8V VDD
62	DVDD18	Power	Digital 1.8V VDD
84	DVDD18	Power	Digital 1.8V VDD
93	DVDD18	Power	Digital 1.8V VDD
117	DVDD18	Power	Digital 1.8V VDD
124	DVDD18	Power	Digital 1.8V VDD
6	DGND	Power	Digital Ground
22	DGND	Power	Digital Ground
24	DGND	Power	Digital Ground
63	DGND	Power	Digital Ground
81	DGND	Power	Digital Ground
85	DGND	Power	Digital Ground
92	DGND	Power	Digital Ground
94	DGND	Power	Digital Ground
107	DGND	Power	Digital Ground

Table 2: Pinout (Sheet 4 of 4)

LQFP128	Name	Type	Description
116	DGND	Power	Digital Ground
118	DGND	Power	Digital Ground
125	DGND	Power	Digital Ground
33	CSYNC	Input	Composite Sync Input - for Sync On Green
36	AVDD33	Power	Analog 3.3V VDD
43	AVDD33	Power	Analog 3.3V VDD
50	AVDD33	Power	Analog 3.3V VDD
57	AVDD33	Power	Analog 3.3V VDD
46	AVDD18	Power	Analog 1.8V VDD
53	AVDD18	Power	Analog 1.8V VDD
60	AVDD18	Power	Analog 1.8V VDD
37	AGND	Power	Analog Ground
39	AGND	Power	Analog Ground
45	AGND	Power	Analog Ground
52	AGND	Power	Analog Ground
59	AGND	Power	Analog Ground
61	AGND	Power	Analog Ground
38	ADVDD18	Power	1.8V VDD

2 Functional Description

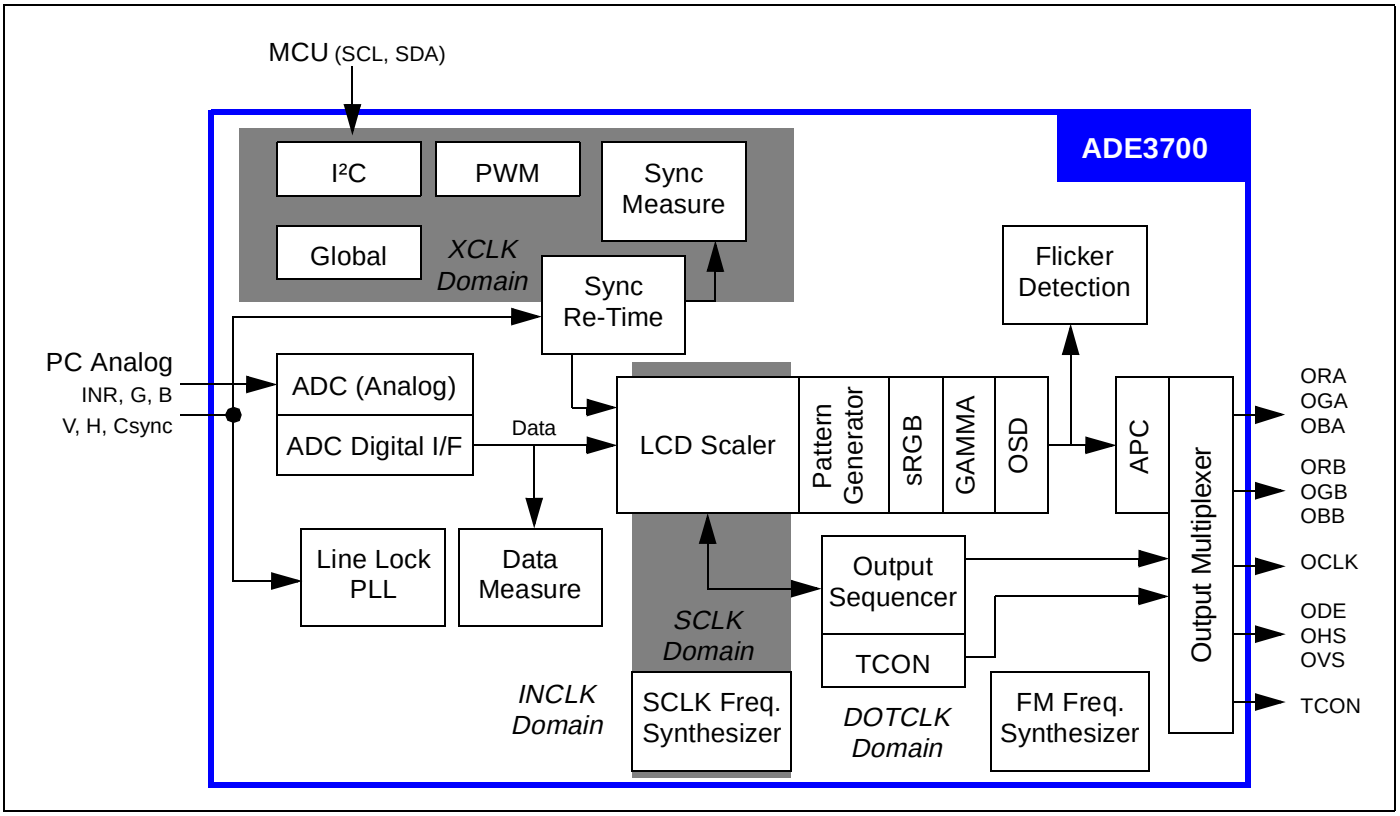
2.1 Global Control

The global control block is responsible for:

- selecting clock sources
- power control
- I²C control
- SCLK frequency synthesizer control
- block by block synchronous reset generation

The global control block runs on the XCLK clock domain which is required to be active for programming. The clock domains of all other blocks are set in the Global Control Block. For I²C access, the requested block must be driven with a valid clock frequency greater than 10 MHz. Clock domains are shown in Figure 2.

Figure 2: Global Control Block Diagram



To program the SCLK frequency synthesizer to a desired frequency (f_{OUT}, in MHz), the following equations apply.

Table 3: SCLK Frequency Synthesizer Programmable Values (Sheet 1 of 2)

Frequency Range	SDIV
$f_{OUT} < 8 \times f_{XCLK}$ AND $f_{OUT} \geq 4 \times f_{XCLK}$	0
$f_{OUT} < 4 \times f_{XCLK}$ AND $f_{OUT} \geq 2 \times f_{XCLK}$	1

Table 3: SCLK Frequency Synthesizer Programmable Values (Sheet 2 of 2)

Frequency Range	SDIV
$f_{OUT} < 2 \times f_{XCLK}$ AND $f_{OUT} \geq f_{XCLK}$	2
$f_{OUT} < f_{XCLK}$ AND $f_{OUT} \geq f_{XCLK} / 2$	3
$f_{OUT} < f_{XCLK}/2$ AND $f_{OUT} \geq f_{XCLK} / 4$	4
$f_{OUT} < f_{XCLK}/4$ AND $f_{OUT} \geq f_{XCLK} / 8$	5
$f_{OUT} < f_{XCLK}/8$ AND $f_{OUT} \geq f_{XCLK} / 16$	6
$f_{OUT} < f_{XCLK}/16$ AND $f_{OUT} \geq f_{XCLK} / 32$	7

$$MD = INT(f_{XCLK} \times (2^{(6 + NDIV - SDIV)}) / f_{OUT})$$

$$PE = INT((2^{15}) \times (MD + 1 - f_{XCLK} \times (2^{(6 + NDIV - SDIV)}) / f_{OUT}))$$

where f_{XCLK} is the external crystal frequency in MHz (typically 27). The maximum SCLK frequency generated by this block is $f_{XTAL} \times 2^{(2+NDIV)}$.

For the lowest power operation, all clock sources should be set to the “zero” setting and the analog power disables should be set. In this condition, only the crystal clock domain (XCLK) is running and blocks in INCLK or DOTCLK domains may not be accessible through the I²C interface.

The following modules can have their clocks disabled to reduce power consumption when the chip is in steady-state mode: FLK, OSD, PGEN, DFT, and DMEAS. Also, the clock to the TCON can be disabled for non-Smart Panel applications. Note that the OSD module has a special power bypass bit that must be enabled when the OSD clock is disabled.

Also, the clock to all I²C registers associated with modules in the INCLK and DOTCLK domains can be disabled after the chip is configured to reduce power in steady-state mode. Note that during chip configuration, all I²C clocks must be enabled.

An asynchronous clock enable override signal must be disabled to allow control of individual module clock signals.

Table 4: Global Registers (Sheet 1 of 4)

Register Name	Addr.	mode	Bits	Default	Description
GLBL_NULL_ADDR	0x0000	Read	[7:0]		Chip Revision ID
GLBL_CLK_SRC_SEL_0	0x0001		[7]	0x0	Reserved
		R/W	[6:4]	0x5	DOTCLK source 0x0: TESTCLK pin 0x1: SCLK freq synth 0x2: FM freq synth (normal) 0x3: INCLK source 0x4: CLKIN pin 0x5: crystal clock 0x6: 0 0x7: Reserved
		R/W	[3:0]	0xA	INCLK source 0x0: TESTCLK pin 0x1: nc 0x2: ADC clock red 0x3: ADC clock green 0x4: ADC clock blue 0x5: SCLK freq synth 0x6: nc 0x7: LLK PLL (ADC Input) 0x8: CLKIN pin 0x9: FM freq synth 0xA: crystal clock 0xB: 0 0xC - 0xF: Reserved
GLBL_CLK_SRC_SEL_2	0x0002		[7]	0x0	Reserved
		R/W	[6:4]	0x4	LLK CTRL CLK source 0x0: TESTCLK pin 0x1: SCLK freq synth 0x2: LLKPLL control clock (normal) 0x3: CLKIN pin 0x4: crystal clock 0x5: 0 0x6 - 0x7: Reserved
			[3]		Reserved
		R/W	[2:0]	0x4	LLK ZERO CLK source 0x0: TESTCLK pin 0x1: SCLK freq synth 0x2: LLKPLL zero clock (normal) 0x3: CLKIN pin 0x4: crystal clock 0x5: 0 0x6 - 0x7: Reserved

Table 4: Global Registers (Sheet 2 of 4)

Register Name	Addr.	mode	Bits	Default	Description
GLBL_CLK_INV	0x0003		[7:5]	0x0	Reserved
		R/W	[4]	0x0	Invert LLPLL control clock
		R/W	[3]	0x0	Invert LLPLL zero clock
		R/W	[2]	0x0	Invert ADC sample clock
		R/W	[1]	0x0	Invert DOT clock
		R/W	[0]	0x0	Invert input clock
GLBL_CLK_ENABLE_0	0x0004		[7:1]	0x0	Reserved
		R/W	[0]	0x1	Clock enable async override
GLBL_ANA_PWR	0x0005		[7:5]	0x0	Reserved
		R/W	[4]	0x1	Blue ADC power down
		R/W	[3]	0x1	Green ADC power down
		R/W	[2]	0x1	Red ADC power down
			[1:0]	0x0	Reserved
GLBL_XK_SRST	0x0006		[7:3]	0x0	Reserved
		R/W	[2]	0x0	SMEAS block reset, synchronous to XCLK
		R/W	[1]	0x0	SRT block reset, synchronous to XCLK
		R/W	[0]	0x0	Frame Sync block reset, synchronous to XCLK
GLBL_I2C_CTRL	0x0007		[7:3]	0x0	Reserved
		R/W	[2]	0x0	Disable I2C auto increment
		R/W	[1]	0x0	SDA PMOS enable
		R/W	[0]	0x0	bypass I2C filter
GLBL_XTAL_CTRL	0x0008		[7:1]	0x0	Reserved
		R/W	[0]	0x1	crystal oscillator enable
GLBL_SCLK_SYNTH_CTRL	0x0009		[7:5]	0x0	Reserved
		R/W	[4:3]	0x0	XTAL frequency multiplier NDIV 0x0: f_{XCLK} = 54MHz 0x1: f_{XCLK} = 27MHz (normal) 0x2: f_{XCLK} = 13.5MHz 0x3: Reserved
		R/W	[2]	0x0	SCLK frequency synthesizer EXT_PLL (normal operation = 0)
		R/W	[1]	0x0	SCLK frequency synthesizer PLL_SEL (normal operation = 1)
		R/W	[0]	0x1	SCLK freq synth control disable (normal operation = 0)

Table 4: Global Registers (Sheet 3 of 4)

Register Name	Addr.	mode	Bits	Default	Description
GLBL_SCLK_MD_SD	0x000A	R/W	[7:3]	0x0	SCLK frequency synthesizer MD, range is [16,31]
		R/W	[2:0]	0x0	SCLK frequency synthesizer SDIV, range is [0,7]
GLBL_SCLK_PE_L	0x000B	R/W	[7:0]	0x0	SCLK frequency synthesizer PE, range is [0, 32767]
GLBL_SCLK_PE_H	0x000C	R/W	[7:0]		
GLBL_TST_CTRL	0x000D		[7:1]	0x0	Reserved
		R/W	[0]	0x0	functional test mode enable
GLBL_COMP_PAD_CTRL	0x000E		[7:2]	0x0	Reserved
		R/W	[1]	0x0	Compensation pad TQ (test mode)
		R/W	[0]	0x1	Compensation pad EN (enable)
GLBL_SCLK_CTRL	0x0010		[7:5]	0x0	Reserved
		R/W	[4]	0x0	invert SCLK
			[3]	0x0	Reserved
		R/W	[2:0]	0x0	SCLK source select 0x0: TESTCLK pin 0x1: SCLK freq synth 0x2: FM freq synth (normal) 0x3: INCLK source 0x4: CLKIN pin 0x5: crystal clock 0x6: 0 0x7: Reserved
GLBL_BPAD_EN	0x0011	R/W	[3:0]	0x0	For each bit n (0 to 3) in the LS nibble, 0: TCON[n] pin is TCON output 1: TCON[n] pin is input for testing
		R/W	[4]	0x0	Port B input mode enable (production test only)
GLBL_IK_SRST	0x0020	R/W	[7]	0x0	Reserved
		R/W	[6]	0x0	DFT block reset synchronous to INCLK
		R/W	[5]	0x0	ADC block reset synchronous to INCLK
		R/W	[4]	0x0	SCALER block reset synchronous to INCLK
		R/W	[3]	0x0	Reserved
		R/W	[2]	0x0	Reserved
		R/W	[1]	0x0	DMEAS block reset synchronous to INCLK
		R/W	[0]	0x0	SMUX block reset synchronous to INCLK
GLBL_SHADOW_EN	0x0021		[7:1]	0x0	Reserved
		R/W	[0]	0x0	Shadow registers sync on frame boundary

Table 4: Global Registers (Sheet 4 of 4)

Register Name	Addr.	mode	Bits	Default	Description
GLBL_INCLK_GATE_CTRL	0x0022		[7:3]	0x0	Reserved
		R/W	[2]	0x1	Enable DFT clock
		R/W	[1]	0x1	Enable DMEAS clock
		R/W	[0]	0x1	Enable INCLK to I2C registers
GLBL_DK_SRST	0x0040		[7]	0x0	Reserved
		R/W	[6]	0x0	PGEN block reset synchronous to DOTCLK
		R/W	[5]	0x0	OMUX block reset synchronous to DOTCLK
		R/W	[4]	0x0	APC block reset synchronous to DOTCLK
		R/W	[3]	0x0	OSD block reset synchronous to DOTCLK
		R/W	[2]	0x0	GAMMA block reset synchronous to DOTCLK
		R/W	[1]	0x0	OSQ block reset synchronous to DOTCLK
		R/W	[0]	0x0	SCALE block reset synchronous to DOTCLK
GLBL_OSD_POWER_CTRL	0x0041		[7:1]	0x0	Reserved
		R/W	[0]	0x0	OSD bypass (when clock disabled)
GLBL_DOTCLK_GATE_CTRL	0x0042		[7:5]	0x0	Reserved
		R/W	[4]	0x1	Enable FLK clock
		R/W	[3]	0x1	Enable TCON clock
		R/W	[2]	0x1	Enable OSD clock
		R/W	[1]	0x1	Enable PGEN clock
		R/W	[0]	0x1	Enable DOTCLK to I2C registers

2.2 FM Frequency Synthesizer

The FM Frequency Synthesizer can create a clock up to eight times the crystal input clock using a digital frequency synthesizer. The modulation period and amplitude are directly controlled by I2C registers. The I2C interface runs in the LLK_CTRL clock domain, which must be active for access.

The relationship of the output frequency (f_{OUT}) to the 32-bit phase_rate value and the crystal frequency (f_{XCLK}) is:

$$f_{OUT} = f_{XCLK} * 2^{27+NDIV} / \text{phase_rate}$$

where f_{OUT} and f_{XCLK} are in MHz.

The maximum output frequency of the FM frequency synthesizer is $f_{XTAL} \times 2^{(2+NDIV)}$.

Note that native duty cycle of the FM frequency synthesizer is not 50/50, so it is recommended to either enable the divide-by-two in the fm synthesizer block for frequencies up to $f_{XCLK} \times 2^{(1+NDIV)}$ (typically 108 MHz) or set the output mux to a double wide output mode for pixel clocks above $f_{XCLK} \times 2^{(1+NDIV)}$. This will ensure a 50% duty clock on the output.

Table 5: FM Frequency Synthesizer Registers

Register Name	Addr	Mode	Bits	Default	Description
FM_FS_CTRL	0x0830		[7:4]		Reserved
		R/W	[3]	0x0	Clear the FM synthesizer
		R/W	[2]	0x0	Clear the fs accumulator
		R/W	[1]	0x0	Activate the frequency modulation
		R/W	[0]	0x0	Divide the output by 2
FM_FS_PR_0	0x0831	R/W	[7:0]	8000000	Phase Rate
FM_FS_PR_1	0x0832	R/W	[7:0]		
FM_FS_PR_2	0x0833	R/W	[7:0]		
FM_FS_PR_3	0x0834	R/W	[7:0]		
FM_FS_AMPLITUDE	0x0835	R/W	[7:0]	0x0	LSB = 72 ps
FM_FS_PERIODX64	0x0836	R/W	[7:0]	0x80	LSB = 1.185 us
FM_FS_PULSE_EXT	0x0837	R/W	[7]	0x0	Enable
			[6:3]		Reserved
		R/W	[2:0]	0x0	Value

2.3 Analog-to-Digital Converter (ADC)

The analog port consists of three 9-bit RGB ADCs with preamp, gain/offset adjustment and digital filtering. The I2C interface for the ADC block is in the INCLK clock domain which must be active for programming.

The relationship of input voltage, gain and offset register settings to output code is approximately as follows:

output_code_8b = 457 x offset / 2^8 + 181 x gain x input_mV / 2^{16} - 125 x gain x offset / 2^{16} - 219

Table 6: ADC Registers (Sheet 1 of 2)

Register	Addr.	Mode	Bits	Default	Description
ADC_DITHER	0x0324		[7]		Reserved
		R/W	[6]	0x0	Dither horizontally
		R/W	[5]	0x0	Dither vertically
		R/W	[4]	0x0	Dither temporally
		R/W	[3]	0x0	Force dither high
		R/W	[2]	0x0	Enable dither
			[1:0]	0x0	Reserved
ADC_OFFSET_R	0x0326	R/W	[7:0]	0x0	Offset Control, Red Channel
ADC_OFFSET_G	0x0328	R/W	[7:0]	0x0	Offset Control, Green Channel

Table 6: ADC Registers (Sheet 2 of 2)

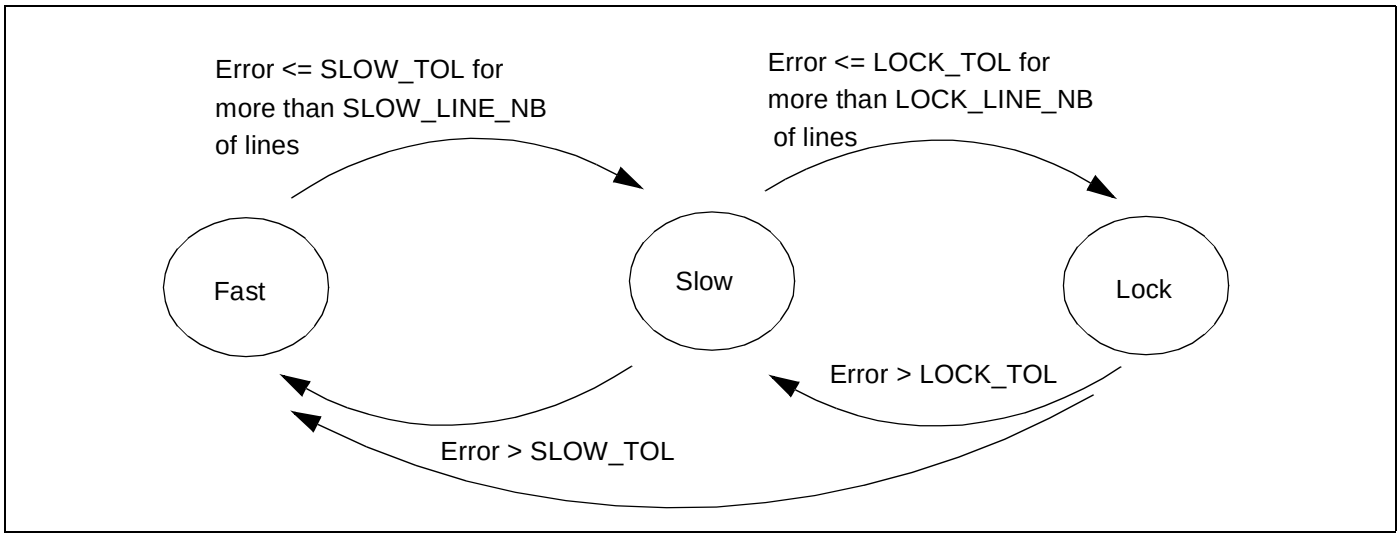
Register	Addr.	Mode	Bits	Default	Description
ADC_OFFSET_B	0x0329	R/W	[7:0]	0x0	Offset Control, Blue Channel
ADC_GAIN_R	0x032A	R/W	[7:0]	0x0	Gain Control, Red Channel
ADC_GAIN_G	0x032B	R/W	[7:0]	0x0	Gain Control, Green Channel
ADC_GAIN_B	0x032C	R/W	[7:0]	0x0	Gain Control, Blue Channel

2.4 Line Lock PLL

The Line Lock PLL recovers a sample clock from an incoming hsync source. The response characteristics of the line lock PLL can be adjusted for optimum response time and jitter filtering. The phase of the sample clock can be digitally adjusted in steps of 289 ps (with a 27-MHz crystal). The I2C interface of the line lock PLL is in the LLK_CTRL clock domain which must be active for programming.

The PLL filter has three ranges with independent filter parameters. When the phase detector error stays below a programmable threshold for a programmable number of input lines, the PLL filter coefficients are changed. Any phase detector error above the programmed threshold will return the filter to the appropriate level in one line. The operation is shown in Figure 3.

Figure 3: Line Lock PLL



The digital loop filter is controlled by three parameters: MFACTOR, A and B. M_FACTOR is the desired number of clocks per input line. The A and B parameters control the response of the 2nd order digital filter. A and B are composed of a linear and exponential component designated by the L and E suffix, respectively. The relationship of these numbers to the classic 2nd order damping and natural frequency are as follows:

$$\text{Damping} = AL \times 2^{(AE-12)} \times \text{SQRT}(5 \times M_FACTOR / (BL \times 2^{BE}))$$

$$\text{Natural Frequency} = \text{SQRT}(M_FACTOR \times 5 \times BL \times 2^{(BE-34)})$$

Table 7: Line Lock PLL Registers (Sheet 1 of 4)

Register Name	Addr	Mode	Bits	Default	Description
LLK_PLL_CLEAR	0x0800		[7:6]		Reserved
		R/W	[5]	0x0	master reset
		R/W	[4]	0x0	reset the PLL synthetic sync
		R/W	[3]	0x0	reset PLL offset
		R/W	[2]	0x0	reset PLL accumulator
		R/W	[1]	0x0	reset the low pass filter
		R/W	[0]	0x0	reset the PLL phase error
LLK_PLL_CTRL	0x0801	R/W	[7]		Reserved
		R/W	[6]	0x0	zero clock delay enable
		R/W	[5]	0x0	0: normal 1: diagnostic mode -- PLL uses only fine error
		R/W	[4]	0x0	0: normal 1: diagnostic -- coarse error is multiplied by 2
		R/W	[3]	0x0	input hsync edge selection 0: rising edge 1: falling edge
		R/W	[2]	0x0	sync on green input selection 0: composite sync (HSYNC pin) 1: sync on green (CSYNC pin)
		R/W	[1]	0x0	0: normal 1: divide PLL clock by 2
		R/W	[0]	0x0	0: normal 1: free-running mode
LLK_PLL_MFACTOR_L	0x0802	R/W	[7:0]	0x0280	number of clocks in a line
LLK_PLL_MFACTOR_H	0x0803	R/W	[7:0]		
LLK_PLL_HPERIOD_L	0x0804	R/W	[7:0]	0x0040	pulse width of synthetic hsync
LLK_PLL_HPERIOD_H	0x0805	R/W	[7:0]		
LLK_PLL_PHASE_RATE_INIT_0	0x0806	R/W	[7:0]	0x0	initial phase rate
LLK_PLL_PHASE_RATE_INIT_1	0x0807	R/W	[7:0]		fout = fxtal * $2^{27+NDIV}$ / phase_rate
LLK_PLL_PHASE_RATE_INIT_2	0x0808	R/W	[7:0]		
LLK_PLL_PHASE_RATE_INIT_3	0x0809	R/W	[7:0]		
LLK_PLL_PHASE_RATE_INIT_WR	0x080A	R/W	[7:1]		Reserved
			[0]		When written to 1, the pll phase rate is initialized with the initial phase rate register. Self clearing.

Table 7: Line Lock PLL Registers (Sheet 2 of 4)

Register Name	Addr	Mode	Bits	Default	Description
LLK_PLL_TC_AEF	0x080B		[7:4]		Reserved
		R/W	[3:0]	0xA	Fast Time Constant A Exponent
LLK_PLL_TC_BEF	0x080C		[7:4]		Reserved
		R/W	[3:0]	0xA	Fast Time Constant B Exponent
LLK_PLL_TC_ALF	0x080D		[7:6]		Reserved
		R/W	[5:0]	0x20	Fast Time Constant A Linear
LLK_PLL_TC_BLF	0x080E		[7:6]		Reserved
		R/W	[5:0]	0x20	Fast Time Constant B Linear
LLK_PLL_TC_AES	0x080F		[7:4]		Reserved
		R/W	[3:0]	0x6	Slow Time Constant A Exponent
LLK_PLL_TC_BES	0x0810		[7:4]		Reserved
		R/W	[3:0]	0x6	Slow Time Constant B Exponent
LLK_PLL_TC_ALS	0x0811		[7:6]		Reserved
		R/W	[5:0]	0x20	Slow Time Constant A Linear
LLK_PLL_TC_BLS	0x0812		[7:6]		Reserved
		R/W	[5:0]	0x20	Slow Time Constant B Linear
LLK_PLL_TC_AEK	0x0813		[7:4]		Reserved
		R/W	[3:0]	0x6	Lock Time Constant A Exponent
LLK_PLL_TC_BEK	0x0814		[7:4]		Reserved
		R/W	[3:0]	0x6	Lock Time Constant B Exponent
LLK_PLL_TC_ALK	0x0815		[7:6]		Reserved
		R/W	[5:0]	0x20	Lock Time Constant A Linear
LLK_PLL_TC_BLK	0x0816		[7:6]		Reserved
		R/W	[5:0]	0x20	Lock Time Constant B Linear
LLK_PLL_TC_SLOW_TOL	0x0817	R/W	[7:0]	0x80	More than slow_line_nb lines with a phase error less than the slow_tol will set the slow status bit, and the pll will work with the slow time constant. One or more lines with a phase error more than slow_tol will reset the slow status bit, and the pll will work with the fast time constant. LSB of slow tol is approx. 200ps.
LLK_PLL_TC_SLOW_LINE_NB	0x0818	R/W	[7:0]	0x10	

Table 7: Line Lock PLL Registers (Sheet 3 of 4)

Register Name	Addr	Mode	Bits	Default	Description
LLK_PLL_LOCK_TOL	0x0819	R/W	[7:0]	0x20	More than lock_line_nb lines with a phase error less than the lock_tol will set the lock status bit, and the pll will work with the lock time constant. One or more lines with a phase error more than lock_tol will reset the lock status bit, and the pll will work with the slow time constant. LSB of lock tol is approx. 200ps.
LLK_PLL_LOCK_LINE_NB	0x081A	R/W	[7:0]	0x30	
LLK_PLL_PH_OFFSET	0x081B	R/W	[7:0]	0x0	Phase adjustment. The maximum phase offset value is equal to phase_rate[31:21] or 0x40, whichever is higher.
LLK_PLL_PH_OFFSET_EN	0x081C	R/W	[7]	0x0	phase enable
			[6]		skip pulse
			[5]		skip pulse at every rising edge of hsync
			[4:0]		Reserved
LLK_PLL_PULSE_HIGH_EXT	0x081D	R/W	[7]	0x0	0: no pulse extend 1: extend pulse (normal)
			[6:3]		Reserved
		R/W	[2:0]	0x0	pulse extend amount 0x0: minimum 0x7: maximum (normal)
LLK_PLL_STAT_LINES_L	0x081E	R/W	[7:0]	0x10	Number of lines to statistically analyze.
LLK_PLL_STAT_LINES_H	0x081F	R/W	[7:0]		
LLK_PLL_STAT_ERROR_INC_LOW	0x0820		[7:0]		Reserved
LLK_PLL_FINE_ERROR_WAIT	0x0821		[7:4]		Reserved
		R/W	[3:0]	0x0	Wait this number of CTRL_CLK cycles before updating the PLL.
LLK_PLL_STAT_ON_VSYNC	0x0822		[7:2]		Reserved
		R/W	[1]	0x0	PLL statistic synchronize on falling edge of vsync
		R/W	[0]	0x0	PLL statistic synchronize on rising edge of vsync
LLK_PLL_MFACTOR_SHADOW_L	0x0823	R/W	[7:0]	0x80	Number of clocks in a line.
LLK_PLL_MFACTOR_SHADOW_U	0x0824	R/W	[7:0]	0x02	Registers 0x0803 and 0x0802 are transferred to those registers according to update_on_venab_fe.

Table 7: Line Lock PLL Registers (Sheet 4 of 4)

Register Name	Addr	Mode	Bits	Default	Description
LLK_PLL_UPDATE	0x0840	R	[7]		In free-running mode, toggles when status is updated. In one-shot mode, this bit is set when status is ready.
			[6:2]		Reserved
		R/W	[1]	0x0	0: free-running mode 1: one-shot mode
		R/W	[0]	0x0	update enable
LLK_PLL_STATUS	0x0841		[7:4]		Reserved
		R	[3]		llk overflow
		R	[2]		coarse error = 0
		R	[1]		in slow mode
		R	[0]		in lock mode
LLK_PLL_PH_ERROR_L	0x0842	R	[7:0]		phase error
LLK_PLL_PH_ERROR_H	0x0843	R	[7:0]		LSB = approx. 200ps
LLK_PLL_PHASE_RATE_0	0x0844	R	[7:0]		llk phase rate
LLK_PLL_PHASE_RATE_1	0x0845	R	[7:0]		fout = fxtal * $2^{27+NDIV}$ / phase_rate
LLK_PLL_PHASE_RATE_2	0x0846	R	[7:0]		
LLK_PLL_PHASE_RATE_3	0x0847	R	[7:0]		
LLK_PLL_PHASE_RATE_I_0	0x0848	R	[7:0]		integral phase rate
LLK_PLL_PHASE_RATE_I_1	0x0849	R	[7:0]		
LLK_PLL_PHASE_RATE_I_2	0x084A	R	[7:0]		
LLK_PLL_PHASE_RATE_I_3	0x084B	R	[7:0]		
LLK_PLL_STAT_ERROR_MEAN	0x084C	R	[7:0]		average phase error over stat_lines phase error LSB is approx. 200ps
LLK_PLL_STAT_ERROR_PP_L	0x084D	R	[7:0]		peak phase error over stat_lines
LLK_PLL_STAT_ERROR_PP_H	0x084E	R	[7:0]		phase error LSB is approx. 200ps
LLK_PLL_STAT_ERROR_ABS_L	0x084F	R	[7:0]		sum of absolute phase errors over stat_lines phase error LSB is approx. 200ps
LLK_PLL_STAT_ERROR_ABS_H	0x0850	R	[7:0]		
LLK_PLL_STAT_ERROR_GTX	0x0851		[7:0]		Reserved

2.5 Sync Retiming (SRT)

The Sync Retiming (SRT) block retimes incoming synchronization signals (H Sync, V Sync, etc) into the XCLK and INCLK domains.

For the XCLK domain, the SRT has the following functions:

- Retimes all sync signals going to SMEAS into the XCLK domain.
- Extracts the vertical sync signal from composite sync signals (AHSYNC and ACSYNC pins)
- Divides clocks by 1024 for activity detection purposes.
- Generates a delay-filtered version of vertical sync from a mux-selectable vertical sync source.
- Generates a coast signal in the XCLK domain for the LLPLL.

Table 8: Sync Retiming Registers (Sheet 1 of 2)

Register Name	Addr	Mode	Bits	Default	Description
SRTXK_CSYNC_INV	0x01E0		[7:3]	0x0	Reserved
		R/W	[2]	0x0	invert filtered vert sync signal
		R/W	[1]	0x0	invert composite sync signal
		R/W	[0]	0x0	invert SOG signal
SRTXK_SOG_THR_L	0x01E1	R/W	[7:0]	0x080	SOG vert sync extractor threshold [7:0]
SRTXK_SOG_THR_H	0x01E2	R/W	[7:4]		Reserved
			[3:0]		SOG vert sync extractor threshold [11:8]
SRTXK_CSYNC_THR_L	0x01E3	R/W	[7:0]	0x080	composite sync vertical sync extractor threshold [7:0]
SRTXK_CSYNC_THR_H	0x01E4	R/W	[7:4]		Reserved
			[3:0]		composite sync vertical sync extractor threshold [11:8]
SRTXK_VSYNC_SEL	0x01E5	R/W	[7:3]		Reserved
			[2:0]	0x0	filtered vert sync source select 0x0: avsync pin 0x1: vsync from composite ahsync pin 0x2: vsync from composite acsync pin 0x3: Reserved 0x4 - 0x7: Reserved
SRTXK_VSYNC_THR_L	0x01E6	R/W	[7:0]	0x080	filtered vert sync delay [7:0]
SRTXK_VSYNC_THR_H	0x01E7	R/W	[7:4]		Reserved
		R/W	[3:0]		filtered vert sync delay [11:8]

Table 8: Sync Retiming Registers (Sheet 2 of 2)

Register Name	Addr	Mode	Bits	Default	Description
SRTXK_COAST_VS_SEL	0x01E8		[7:4]	0x0	Reserved
		R/W	[3]	0x0	coast signal trigger edge 0: posedge of selected vertical 1: negedge of selected vertical
		R/W	[2:0]	0x0	source select for coast vert sync trigger 0x0: avsync pin 0x1: vsync from ahsync pin 0x2: vsync from acsync pin 0x3: Reserved 0x4: nc 0x5: nc 0x6: srt vsync (filtered vsync) 0x7: Reserved
SRTXK_COAST_RISE_L	0x01E9	R/W	[7:0]	0x0	rising edge of coast, in XCLKs from vsync trigger
SRTXK_COAST_RISE_M	0x01EA	R/W	[7:0]	0x0	
SRTXK_COAST_RISE_H	0x01EB	R/W	[7:0]	0x0	
SRTXK_COAST_FALL_L	0x01EC	R/W	[7:0]	0x0	falling edge of coast, in XCLKs from vsync trigger
SRTXK_COAST_FALL_M	0x01ED	R/W	[7:0]	0x0	
SRTXK_COAST_FALL_H	0x01EE	R/W	[7:0]	0x0	
SRTIK_HS_CTRL	0x01F0		[7:3]	0x0	Reserved
		R/W	[2]	0x0	Resample clock edge to transfer hsync into the INCLK domain; depends on LLK phase offset value. 0: posedge INCLK 1: negedge INCLK
		R/W	[1:0]	0x0	horz sync source select for resampling into the INCLK domain 0x0: LLPLL lock sync (normal) 0x1: ahsync pin 0x2: acsync pin 0x3: Reserved
SRTIK_VS_SEL	0x01F1		[7:2]	0x0	Reserved
		R/W	[1:0]	0x0	vert sync source select for resampling 0x0: avsync pin 0x1: vsync from ahsync pin 0x2: vsync from acsync pin 0x3: srt vsync (filtered vsync)

2.6 Sync Measurement

The Input Sync Measurement (SMEAS) block continuously detects activity from all video sources. The module can measure the characteristics of the sync signals on any input port. The sync measurement module reports the results of the measurements to the system microcontroller.

This portion of the sync measurement is fully synchronous on the crystal clock (XCLK). Another block, the Sync Retiming Block (SRT), handles the asynchronous signal transfer of the incoming sync signals.

Input Sync Functions:

- Activity Detection
- Sync Management
- Measurement

Table 9: Sync Measurement (Sheet 1 of 8)

Register Name	Addr	Mode	Bits	Default	Description
SMEAS_ACT_CTRL	0x0100		[7:4]	0x0	Reserved
		R/W	[3]	0x0	Enable activity detection in free-running mode.
		R/W	[2]	0x0	Freeze results in free-running mode. No meaning in one shot mode. 0: Do not freeze the results. New result will be available on the next and subsequent toggle of the polling bit. 1: Freeze the current results. The polling bit will still toggle and the block continues to free-run; however, results will not be updated.
		R/W	[1]	0x0	activity detection start. In one-shot mode it triggers the start of a measurement and is reset to zero when the measurement is complete.
		R/W	[0]	0x0	activity detection mode control 0: free-running 1: one shot
SMEAS_ACT_H_SMPTM_L	0x0101	R/W	[7:0]	0x0	Sample time value for clock or hsync activity. In units of XCLK_period*256
SMEAS_ACT_H_SMPTM_H	0x0102	R/W	[7:0]	0x0	
SMEAS_ACT_V_SMPTM_L	0x0103	R/W	[7:0]	0x0	Sample time value for vsync activity in units of XCLK_period*256. jj Note: this number MUST be larger than hsync sample time.
SMEAS_ACT_V_SMPTM_H	0x0104	R/W	[7:0]	0x0	
SMEAS_ACT_H_MINEDGE	0x0105	R/W	[7:0]	0x0	Minimum edge count value for clk or hsync activity.
SMEAS_ACT_V_MINEDGE	0x0106	R/W	[7:0]	0x0	Minimum edge count value for vsync activity.
SMEAS_H_TMOT_L	0x0107	R/W	[7:0]	0x4000	timeout counter value for clk or horizontal measurement in XCLKs
SMEAS_H_TMOT_H	0x0108	R/W	[7:0]		

Table 9: Sync Measurement (Sheet 2 of 8)

Register Name	Addr	Mode	Bits	Default	Description
SMEAS_V_TMOT_L	0x0109	R/W	[7:0]	0x1600	timeout counter value for vertical measurement in units of XCLK/256
SMEAS_V_TMOT_H	0x010A	R/W	[7:0]		
SMEAS_CLEAR	0x0110		[7:3]		Reserved
		R/W	[2]	0x0	clear sticky status bits
		R/W	[1]	0x0	clear all out-of-range event counters
		R/W	[0]	0x0	clear all result registers
SMEAS_H_CTRL	0x0111		[7]	0x0	Reserved
		R/W	[6]	0x0	Enable hsync filter -- all hsync pulses less than SMEAS_FILTER_HS_WIDTH will be ignored.
		R/W	[5]	0x0	measure hsync in the absence of vsync
		R/W	[4]	0x0	enable horizontal measurement in free-running mode
		R/W	[3]	0x0	horizontal event edge select 0: positive edge 1: negative edge
		R/W	[2]	0x0	Freeze horizontal measurements results during free-running mode. No meaning in one shot mode. 0: Do not freeze measurement results. New result will be available on the next and subsequent toggle of the polling bit. 1: Freeze the current results. The polling bit will still toggle and the block continues to free-running; however, results will not be updated.
		R/W	[1]	0x0	horizontal measurement start In one-shot mode setting this bit triggers the start of a measurement. The bit is reset to zero when the measurement is complete.
		R/W	[0]	0x0	horizontal measurement mode 0: free-running 1: one shot

Table 9: Sync Measurement (Sheet 3 of 8)

Register Name	Addr	Mode	Bits	Default	Description
SMEAS_V_CTRL	0x0112		[7:5]		Reserved
		R/W	[4]	0x0	Enable Vertical Measurement in Free-running mode
		R/W	[3]	0x0	Vertical Event Edge Select 0: positive edge 1: negative edge
		R/W	[2]	0x0	Freeze vertical measurement results during free-running mode. No meaning in one shot mode. 0: Do not freeze the results. New result will be available on the next and subsequent toggle of the polling bit. 1: Freeze the current results in free-running mode. The polling bit will still toggle and the block continues to free run; however, results will not be updated.
		R/W	[1]	0x0	Vertical Measurement Start In one-shot mode setting this bit triggers the start of a measurement. The bit is reset to zero when the measurement is complete.
		R/W	[0]	0x0	Vertical Measurement Mode 0: free-running 1: one shot
SMEAS_H_SEL	0x0113		[7:4]		Reserved
		R/W	[3:0]	0x0	Select a horizontal sync, enable or clock for measurement. 0x0: Analog hsync 0x1: Hsync generated from LLPLL 0x2: SOG from csync pin 0X3: NC 0X4: NC 0X5: NC 0X6: NC 0X7: NC 0X8: NC 0x9: TCON hsync 0xA: TCON data enable 0xB: INCLK div1k 0xC: DOTCLK div1k 0xD-0xF: Reserved

Table 9: Sync Measurement (Sheet 4 of 8)

Register Name	Addr	Mode	Bits	Default	Description
SMEAS_V_SEL	0x0114	R/W	[7:4]	0x0	Selects a vertical signal for measurement of the high pulse width. 0x0: Analog vsync 0x1: Composite vsync 0x2: SOG vsync 0x3: nc 0x4: nc 0x5: nc 0x6: nc 0x7: TCON vsync 0x8 - 0xF: Reserved
		R/W	[3:0]	0x0	Selects a vertical signal for measurement of period and polarity. 0x0: Analog vsync 0x1: Composite vsync 0x2: nc 0x3: nc 0x4: nc 0x5: nc 0x6: nc 0x7: TCON vsync
SMEAS_STATUS_MASK	0x0119	R/W	[7]	0x0	Mask bit for hsync polarity check 0: ignore 1: check
		R/W	[6]	0x0	Mask bit for vsync polarity check 0: ignore 1: check
			[5:4]		Reserved
		R/W	[3]	0x0	Mask bit for vert pulse width check 0: ignore 1: check
		R/W	[2]	0x0	Mask bit for h per v check 0: ignore 1: check
		R/W	[1]	0x0	Mask bit for h period check 0: ignore 1: check
		R/W	[0]	0x0	Mask bit for v period check 0: ignore 1: check
SMEAS_H_NUM_LINES	0x011A	R/W	[7:0]	0x0	Number of lines to measure for Horizontal period. Valid range is 1 to 255.
SMEAS_H_SKIP_L	0x011B	R/W	[7:0]	0x0	Number of lines to skip before starting a horizontal measurement. The skip counter counts from the chosen vertical source and edge. [7:0]

Table 9: Sync Measurement (Sheet 5 of 8)

Register Name	Addr	Mode	Bits	Default	Description
SMEAS_H_SKIP_H	0x011C	R/W	[7:4]		Reserved
			[3:0]		Number of lines to skip before starting a horizontal measurement. The skip counter counts from the chosen vertical source and edge. [11:8]
SMEAS_SKEW_CTRL	0x011D		[7:3]	0x0	Reserved
		R/W	[2]	0x0	1 = delay vsync a number of XCLKs specified in SMEAS_DELAY_VSYNC
			[1]	0x0	Reserved
		R/W	[0]	0x0	Write a rising edge to start the hv-skew measurement.
SMEAS_SKEW_THRES	0x011E	R	[7:0]	0x5	Test skew limit in XCLKs. If the skew is less than this test limit, the SMEASE_SKEW_STATUS register will report an error condition. SMEAS_DELAY_VSYNC should be reprogrammed until the skew is large enough to prevent vcount ambiguity.
SMEAS_DELAY_VSYNC	0x011F	R/W	[7:0]	0x3	Number of XCLKs to delay vsync.
SMEAS_REF_XK_PER_H_L	0x0120	R/W	[7:0]	0x0	Reference value for XCLKs per horizontal event actual value = programmed value + 1
SMEAS_REF_XK_PER_H_M	0x0121	R/W	[7:0]	0x0	
SMEAS_REF_XK_PER_H_H	0x0122	R/W	[7:0]	0x0	
SMEAS_REF_XK_PER_V_L	0x0123	R/W	[7:0]	0x0	Reference value for XCLKs per vertical event actual value = programmed value + 2
SMEAS_REF_XK_PER_V_M	0x0124	R/W	[7:0]	0x0	
SMEAS_REF_XK_PER_V_H	0x0125	R/W	[7:0]	0x0	
SMEAS_REF_H_PER_V_L	0x0126	R/W	[7:0]	0x0	Reference value for horizontal events per vertical event
SMEAS_REF_H_PER_V_H	0x0127	R/W	[7:0]	0x0	
SMEAS_REF_XK_V_PER_HI_L	0x0128	R/W	[7:0]	0x0	Reference value for vertical pulse width measurement result in XCLKs. actual value = programmed value + 1
SMEAS_REF_XK_V_PER_HI_M	0x0129	R/W	[7:0]	0x0	
SMEAS_REF_XK_V_PER_HI_H	0x012A	R/W	[7:0]	0x0	
SMEAS_REF_POLARITY	0x012B		[7:2]	0x0	Reserved
		R/W	[1]	0x0	Reference value for Hsync polarity. 0: active low 1: active high
		R/W	[0]	0x0	Reference value for Vsync polarity. 0: active low 1: active high
SMEAS_XK_HTOL_EXP	0x012C	R/W	[7:4]	0x0	Reserved
			[3:0]	0x0	Horizontal tolerance; $\pm 2^n$ XCLKs
SMEAS_XK_VTOL_EXP	0x012D		[7:4]	0x0	Reserved
		R/W	[3:0]	0x0	Vertical tolerance; $\pm 2^n$ XCLKs

Table 9: Sync Measurement (Sheet 6 of 8)

Register Name	Addr	Mode	Bits	Default	Description
SMEAS_HSYNC_VTOL	0x012E		[7:4]	0x0	Reserved
		R/W	[3:0]	0x0	Horizontal per vertical tolerance, ± 2^n
SMEAS_FILTR_HS_WIDTH	0x012F	R/W	[7:0]	0x1	Refer to register 0x0111
SMEAS_ACT_POLLING	0x013F		[7:1]	0x0	Reserved
		R	[0]	0x0	Toggle on activity status update in free-running mode. No function in one-shot mode.
SMEAS_ANA_ACT	0x0140		[7:5]	0x0	Reserved
		R	[4]	0x0	Composite sync is active
		R	[3]	0x0	Vsync from SOG separator is active
		R	[2]	0x0	Comp vsync from composite sync separator is active
		R	[1]	0x0	Analog hsync is active
		R	[0]	0x0	Analog vsync is active
SMEAS_ANA_STUCK	0x0143		[7:5]	0x0	Reserved
		R	[4]	0x0	Comp sync is stuck at 1(high)/0(low)
		R	[3]	0x0	Vsync from SOG separator is stuck at 1(high)/0(low)
		R	[2]	0x0	Comp vsync from separator is stuck at 1(high)/0(low)
		R	[1]	0x0	Analog hsync is stuck at 1(high)/0(low)
		R	[0]	0x0	Analog vsync is stuck at 1(high)/0(low)
SMEAS_XK_PER_H_L	0x0146	R	[7:0]	0x0	XCLKs per horizontal event - 1
SMEAS_XK_PER_H_M	0x0147	R	[7:0]	0x0	
SMEAS_XK_PER_H_H	0x0148	R	[7:0]	0x0	
SMEAS_XK_PER_V_L	0x0149	R	[7:0]	0x0	XCLKs per vertical event - 1
SMEAS_XK_PER_V_M	0x014A	R	[7:0]	0x0	
SMEAS_XK_PER_V_H	0x014B	R	[7:0]	0x0	
SMEAS_H_PER_V_L	0x014C	R	[7:0]	0x0	Horizontal events per vertical event
SMEAS_H_PER_V_H	0x014D	R	[7:0]	0x0	
SMEAS_SK_V_HI_L	0x014E	R	[7:0]	0x0	Vertical high time in XCLKs - 1
SMEAS_SK_V_HI_M	0x014F	R	[7:0]	0x0	
SMEAS_SK_V_HI_H	0x0150	R	[7:0]	0x0	
SMEAS_TIMEOUT_STATUS	0x0151		[7:2]	0x0	Reserved
		R	[1]	0x0	Indicates that the horizontal measurement timed out.
		R	[0]	0x0	Indicates that the vertical measurement timed out.

Table 9: Sync Measurement (Sheet 7 of 8)

Register Name	Addr	Mode	Bits	Default	Description
SMEAS_STATUS_RANGE	0x0152	R	[7]	0x0	In free-running mode any of the status bits can change at the end of each measurement. In one shot mode any of the status bits can change at the completion of the measurement. The MEAS_STICKY_STATUS bit is a bitwise OR of bits[3:0] (before the bitwise OR, the mask in SMEAS_STATUS_MASK is AND in) and is sticky. The only way to reset it is for software to write a zero into this bit. This bit goes to the scaler to blank the scaler output. A write to this reg will reset it to 0.
		R	[6]	0x0	Indicates that one of the measured polarities does not match the reference value.
		R	[5]	0x0	Hsync (selected by SMEAS_H_SEL) polarity. 0: active low 1: active high
		R	[4]	0x0	Vsync (selected by SMEAS_V_SEL) polarity. 0: active low 1: active high
		R	[3]	0x0	Indicates that the vertical pulse width measurement exceeded the reference ± tolerance range.
		R	[2]	0x0	Indicates that the horizontal per vertical measurement exceeded the reference ± tolerance range.
		R	[1]	0x0	Indicates that the XCLKs per horizontal measurement exceeded the reference ± tolerance range.
		R	[0]	0x0	Indicates that the XCLKs per vertical measurement exceeded the reference ± tolerance range.
SMEAS_MEAS_POLLING	0x0153		[7:2]	0x0	Reserved
		R	[1]	0x0	Toggle on h meas free-running mode, at end of each meas. No function on one-shot mode.
		R	[0]	0x0	Toggle on v meas free-running mode, at end of each meas. No function on one-shot mode.
SMEAS_SKEW_STATUS	0x0154		[7:2]	0x0	Reserved
		R	[1]	0x0	0: hsync to vsync skew above threshold 1: hsync to vsync skew below threshold
		R	[0]	0x0	0: skew measurement running 1: skew measurement finished

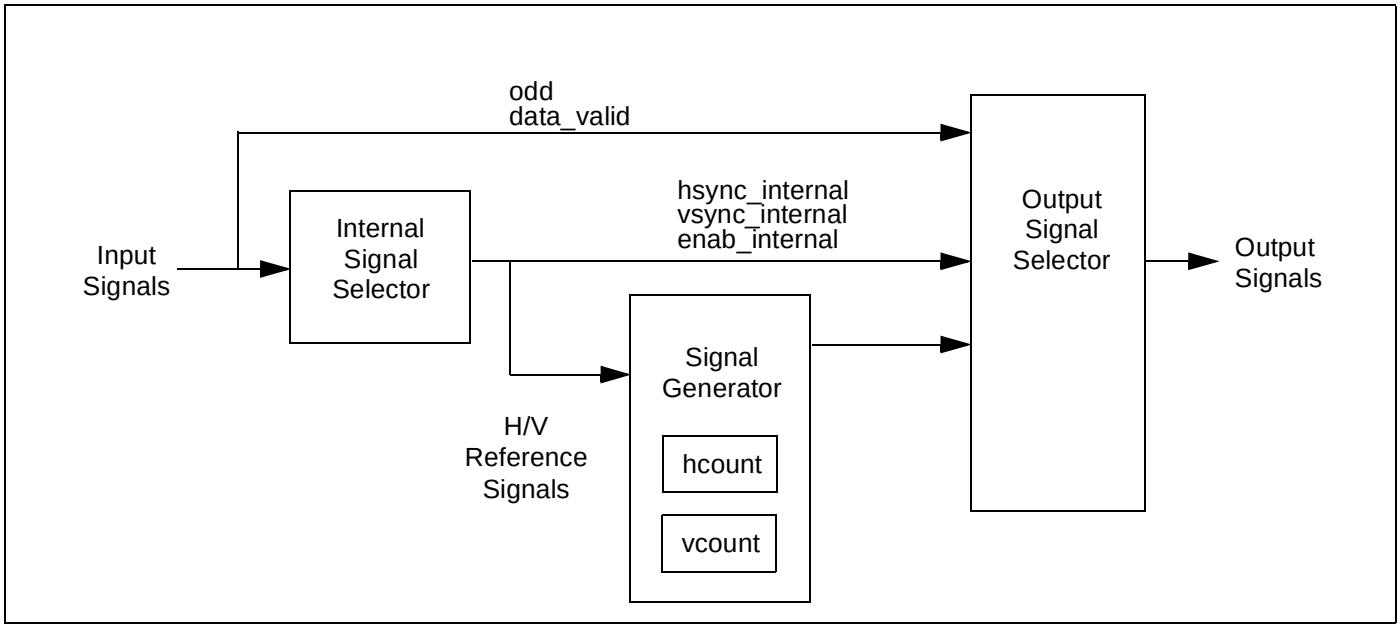
Table 9: Sync Measurement (Sheet 8 of 8)

Register Name	Addr	Mode	Bits	Default	Description
SMEAS_V_OUTOF_RNG	0x0155	R	[7:0]	0x0	The number of times the XCLKs per vertical reference/meas comparison has been out of range. Maximum is 240. Clear by setting SMEAS_CLEAR[1].
SMEAS_H_OUTOF_RNG	0x0156	R	[7:0]	0x0	The number of times the XCLKs per horizontal reference/meas comparison has been out of range. Maximum is 240. Clear by setting SMEAS_CLEAR[1].
SMEAS_HV_OUTOF_RNG	0x0157	R	[7:0]	0x0	The number of times the horizontal per vertical reference/meas comparison has been out of range. Maximum is 240. Clear by setting SMEAS_CLEAR[1].
SMEAS_VHI_OUTOF_RNG	0x0158	R	[7:0]	0x0	The number of times the vertical pulse width in XCLKs reference/meas comparison has been out of range. Maximum is 240. Clear by setting SMEAS_CLEAR[1].
SMEAS_HPOL_OUTOF_RNG	0x0159	R	[7:0]	0x0	The number of times the horizontal polarity reference/meas comparison has been out of range. Maximum is 240. Clear by setting SMEAS_CLEAR[1].
SMEAS_VPOL_OUTOF_RNG	0x015A	R	[7:0]	0x0	The number of times the vertical polarity reference/meas comparison has been out of range. Maximum is 240. Clear by setting SMEAS_CLEAR[1].

2.7 Sync Multiplexer (SMUX)

The Synchronization Multiplexer (SMUX) selects a set of sync signals from the input sources and provides them to the scaler. It generates signals that are missing, depending on the capability. The MCU can select the output sync signals between the input sources and the generated signals.

Figure 4: Sync Multiplexer Block Diagram



2.7.1 Functional Description

The internal signal selector selects which of the input sources are to be used for the internal hsync, vsync and enab signals and is controlled by I2C register SMUX_CTRL0.

The signal generator contains a horizontal and a vertical counter that are resynced using a horizontal and vertical reference signals respectively. The selection of the H/V references and the resync edge (either rising or falling) are programmed via SMUX_CTRL1[3:0]. The signal generator requires both references to be defined, or else the counters will not run properly and the generated signals (other than venab) will be invalid.

The output signal selector can be programmed to output any of the internal syncs, bypassed signals such as odd and data_valid, or the generated versions of all the signals (hsync, vsync, enab, odd, valid). Vertical enable (venab) and clamp are always generated.

The following table summarizes programming for typical modes.

Table 10: Sync Multiplexer Programming Table

Mode	Valid Inputs	Output Source for						
		Hsync	Vsync	Enab	Valid	Odd	Venab	Clamp
Analog Line Lock	LLK_HSYNC LLK_VSYNC	LLK	LLK	GEN	GEN	NA	GEN	GEN
Analog Ext. Clock	VGA_HSYNC LLK_VSYNC TESTCLK	VGA	LLK	GEN	GEN	NA	GEN	GEN

Other sources (such as composite sync) are simple variations on these basic configurations.

The programmed timing values of the generated signals (such as clamp) are relative to the reference signal and edge selected. For example, if the LLK_HSYNC falling edge is selected as the horizontal reference, then all horizontal programming values are relative to it.

Three signals are generated using programmable set/reset values: clamp and the two components that make up the input enable signal (horizontal and vertical enables). The henab and venab signals define the video window that the scaler operates on. The difference between the reset and set quantities is the number of pixels (h) or lines (v) in the input image. Clean wraparound is supported: the henab_set can be greater than the henab_rst.

The clamp pulse should be located outside the active video area, i.e. both programmed values should be in the horizontal blanking region, typically in backporch of the incoming sync.

All set/reset programming values for clamp and henab must be less than the input horizontal total. Both set/reset programming values for venab must be less than the input vertical total. The updates for the enable registers can occur in four modes:

1. No Shadowing
2. Simple Shadowing: updates occur when the upper byte of _rst is written
3. Shadowing + Blank Update: updates occur only in the next blanking region after rst_u is written
4. Shadowing + Vblank Update: updates occur in the next vblank region after rst_u is written.

   This mode also advances or retards the frame trigger to the scaler to prevent glitches. It takes one frame to write H and two frames to write the V-position. With large position changes, a glitch will show up. For small changes (e.g. ±1) no glitch is created.

The written position values are instantly available by read back, independent of shadow mode. The actual values being used by the hardware at a given time can also be read back using separate I²C addresses.

When hsync and/or vsync is generated (e.g. when enab is the only input), the relative position of the generated pulse can be set either before or after the reference edge between -128 and +127 pixels per line.

2.7.2 Example

ADC input using line lock clock:

omux_ctrl0 = 0x09 // select llk hsync and vsync
omux_ctrl1 = 0x0F // choose incoming hsync and vsync as references, choose rising edges
omux_ctrl2 = 0x0C // select the original hsyncs and vsyncs, along with the generated
// enab and valid signals

henab_set = hsync_width + hback_porch
henab_rst = hsync_width + hback_porch + in_hpixel
venab_set = vsync_width + vback_porch
venab_rst = vsync_width + vback_porch + in_vpixel
clamp_set = hsync_width + hback_porch + in_hpixel + 4 // clamp is turned on 4 after last pixel
clamp_rst = hsync_width + hback_porch -4 // clamp is turned off 4 pixels before the 1st pixel

Table 11: Sync Multiplexer Registers (Sheet 1 of 4)

Register Name	Addr	Mode	Bits	Default	Description
SMUX_CTRL0	0x0200		[7:6]	0x0	Reserved
		R/W	[5:3]	0x0	Vsync_internal select 0x0 = Reserved 0x1 = llk/VGA vsync 0x2 = Reserved 0x3 = composite sync decoder 0x4 = Reserved
		R/W	[2:0]	0x0	Hsync_internal select 0x0 = Reserved 0x1 = llk synthesized hsync 0x2 = Reserved 0x3 = raw VGA hsync (jitter) 0x4 = Reserved

Table 11: Sync Multiplexer Registers (Sheet 2 of 4)

Register Name	Addr	Mode	Bits	Default	Description
SMUX_CTRL1	0x0201	R/W	[7]	0x0	venab out select 0: derived from enab out 1: generated internally
		R/W	[6]	0x0	0: simple reset of hcount by href 1: self reset of hcount, used when the chosen href is intermittent, e.g. generating hsync from henab source.
		R/W	[5]	0x0	Vsync_out invert
		R/W	[4]	0x0	Hsync_out invert
		R/W	[3]	0x0	V_reference edge select 0: falling 1: rising
		R/W	[2]	0x0	V_reference select 0: venab_generated 1: vsync_internal
		R/W	[1]	0x0	H_reference edge select 0: falling 1: rising
		R/W	[0]	0x0	H_reference select 0: enab_internal 1: hsync_internal
SMUX_CTRL2	0x0202	R	[7]	0x0	V_reference toggle output.
		R/W	[6]	0x0	Software odd set (for testing odd params on the bench)
		R/W	[5:4]	0x0	Odd_out select 0x0: Reserved 0x1: vsync toggle 0x2: SMUX_CTRL2[6] 0x3: Reserved
		R/W	[3]	0x0	Valid_out select 0: Reserved 1: valid_generated
		R/W	[2]	0x0	Enab_out select 0: enab_internal 1: enab_generated
		R/W	[1]	0x0	Vsync_out select 0: vsync_internal 1: hsync_generated
		R/W	[0]	0x0	Hsync_out select 0: hsync_internal 1: hsync_generated

Table 11: Sync Multiplexer Registers (Sheet 3 of 4)

Register Name	Addr	Mode	Bits	Default	Description
SMUX_CTRL3	0x0203	R	[7:6]		venab pending state 0x0: idle 0x1: venab pending frame 1 0x2: venab pending frame 2 Wait until 0 to write venab again if in henab or venab shadow mode.
		R	[5]		henab pending
			[4]		Reserved
		R/W	[3:2]	0x0	vtrigger reference 2'bx0: trigger ref = venab 2'b01: last pixel w/ anti-glitch 2'b11: first pixel w/ anti-glitch Anti-glitch modes work only with venab shadow mode. First/last pixel must be consistent with out_seq in this mode.
		R/W	[1:0]	0x0	0x0: no shadow 0x1: simple shadow. When henab_rst_u is written, henab_set_l, henab_set_u, henab_rst_l take effect. When venab_rst_u is written, venab_set_l, venab_set_u, venab_rst_l take effect. 0x2: henab shadow. Wait for next available blank period to update positions after henab_rst_u or venab_rst_u is written. 0x3: venab shadow. Wait for next available vblank period to update positions after henab_rst_u or venab_rst_u is written. Venab update takes two frames. State can be watched in ctrl3[7:5].
SMUX_CLAMP_SET_L	0x0204	R/W	[7:0]	0x0	ADC clamp signal rising edge [11:0], relative to selected H reference signal, in INCLKS (pixels)
SMUX_CLAMP_SET_U	0x0205	R/W	[3:0]	0x0	ADC clamp signal MSBs
SMUX_CLAMP_RST_L	0x0206	R/W	[7:0]	0x0	ADC clamp falling edge
SMUX_CLAMP_RST_U	0x0207	R/W	[3:0]	0x0	ADC clamp falling edge
SMUX_HENAB_SET_L	0x0208	R/W	[7:0]	0x0	Horizontal enable start [11:0] (left edge of image) relative to the selected H reference edge in INCLKS (pixels)
HENAB _SET_U	0x0209	R/W	[3:0]	0x0	horizontal enable start MSBs
HENAB _RST_L	0x020A	R/W	[7:0]	0x00	horizontal enable end LSBs
HENAB _RST_U	0x020B	R/W	[3:0]	0x0	horizontal enable end MSBs
VENAB_SET_L	0x020C	R/W	[7:0]	0x00	vertical enable start (top edge of image) relative to the selected vertical reference edge in lines
VENAB _SET_U	0x020D	R/W	[3:0]	0x0	vertical enable start MSBs
VENAB _RST_L	0x020E	R/W	[7:0]	0x00	vertical enable end LSBs
VENAB _RST_U	0x020F	R/W	[3:0]	0x0	vertical enable end MSBs

Table 11: Sync Multiplexer Registers (Sheet 4 of 4)

Register Name	Addr	Mode	Bits	Default	Description
HSYNC_PHASE	0x0210	R/W	[7:0]	0x00	number of horizontal pixels/INCLKS that the generated hsync edge is from the reference edge. 2's complement [-128,127]
VSYNC_PHASE	0x0211	R/W	[7:0]	0x00	number of vertical lines that the generated vsync edge is from the reference edge. 2's complement [-128,127]
HENAB_SET_HW_L	0x0212	R	[7:0]		Actual value used by hardware post shadowing.
HENAB _SET_HW _U	0x0213	R	[3:0]		Actual value used by hardware post shadowing.
HENAB _RST_HW _L	0x0214	R	[7:0]		Actual value used by hardware post shadowing.
HENAB _RST_HW _U	0x0215	R	[3:0]		Actual value used by hardware post shadowing.
VENAB_SET_HW _L	0x0216	R	[7:0]		Actual value used by hardware post shadowing.
VENAB _SET_HW _U	0x0217	R	[3:0]		Actual value used by hardware post shadowing.
VENAB _RST_HW _L	0x0218	R	[7:0]		Actual value used by hardware post shadowing.
VENAB _RST_HW _U	0x0219	R	[3:0]		Actual value used by hardware post shadowing.

2.8 Data Multiplexer

The Data Multiplexer provides the following functions:

- Debug modes (e.g. bit order swap, color swap)

Table 12: Data Mux Registers

Register Name	Addr.	Mode	Bits	Default	Description
DMUX_CHANSEL	0x0280		[7]	0x0	Reserved
		R/W	[6]	0x0	0: Normal 1: MSB/LSB byte flip
		R/W	[5:3]	0x0	If enabled by [2] 0x0: Reserved 0x1: R & G bytes are swapped 0x2: B & G bytes are swapped 0x3: R => G, G => B, B => R 0x4: R & B bytes are swapped 0x5: R => B, G => R, B => G 0x0, 0x6-0x7: Reserved
		R/W	[2]	0x0	0: normal 1: enable color swap
		R/W	[1:0]	0x0	video source select 0x0: ADC data 0x1: nc 0x2: nc 0x3: for test only

2.9 Data Measurement (DMEAS)

The Data Measurement (DMEAS) module measures several characteristics of the data and sync signals. Data measurements are taken over a programmable window as defined by an upper left (mix_x, min_y) and a lower right (max_x, max_y), which may be the whole frame. Measurements are programmable either per color channel or over all color channels.

This module computes all measurements of sync and data format that are done in the INCLK domain. The Sync Measurement module does measurements in the XCLK domain. The INCLKS per DE measurement does not use the window feature. It measures the number of INCLK per DE and returns the result for every line.

All unused or reserved bits will return as zero.

Windows are relative to Sync pulses. A window defined from (0,0) - (0xFFF, 0xFFF) would go from sync to sync. The reference edge to use, rising or falling, is also programmable per X and Y coordinates. SMUX should be configured to provide a positive polarity sync to the DMEAS block. All window enables are reset to 0 and will always be reset on the rising or falling edge of the sync pulse.

Most algorithms can be run over separate or all color channels. Most algorithms also contain a threshold value to zero out noise and/or amplify edges. Algorithm, Color, Threshold, or Window Control changes are accepted at the end of a valid measurement so that they do not affect the current measurement in progress.

Software can request measurements in one of two ways:

1. All measurements, except DE_Size, are performed in One-shot mode, which is synchronous in respect the microcontroller.
2. The DE_Size measurement can be set either to One-shot or Free-running modes. Free-running mode is asynchronous in respect to the microcontroller.

In **One-shot mode**, the block should indicate that the measurement is valid through an auto clear of the start condition.

In **Free-running mode**, the block should indicate that the measurement is valid through a polling bit. In Free-running mode, a Freeze bit is provided to freeze the results. Measurements still continue with the polling bit active, however, they are not updated if the Freeze bit is set.

2.9.1 Edge Intensity

The Edge Intensity measurement is the sum of the absolute value of the delta between adjacent pixels. A programmable threshold is applied to zero out noise and amplify edges. Equation:

```
Delta_val = abs(pixelA - pixelB) - threshold;
Delta_val = Delta_val < 0? 0: Delta_val;
Sum += Delta_val;
```

For all 3 color channels: Sum += Delta_val on Red channel + Delta_val on Green channel + Delta_val on Blue channel

2.9.2 Pixel Sum

The Pixel Sum is the sum of all selected pixels for either a specific color channel or all color channels within the window specified.

2.9.3 Minimum/Maximum Pixel

This function reports the minimum and maximum pixel found within the specified window.

2.9.4 Pixel Cumulative Distribution (PCD)

The Pixel Cumulative Distribution (PCD) function reports the total number of pixels greater than (or less than) a programmable threshold.

To switch between pixels greater than or pixels less than the threshold, a control bit is provided in the DMM_Mode register when requesting a measurement.

2.9.5 Horizontal Position

The Horizontal Position measures the start and end of video data in INCLKS clock cycles relative to the posedge of hsync.

The Data Horizontal Start is defined as the number of INCLKS clock cycles between posedge of hsync and the “first data pixel”.

First data pixel is either:

1. First pixel greater than the programmable threshold value
2. First pixel with the absolute value (current pixel - previous pixel) is greater than the programmable threshold value

The Data Horizontal End is defined as the number of INCLKS clock cycles between posedge of hsync and the “last data pixel plus one”. The search for the last pixels ends at the end of a window.

Last data pixel plus one is either:

1. Pixel after the last pixel that is greater than the programmable threshold value
2. Last pixel with the absolute value (current pixel - previous pixel) is greater than the programmable threshold value

To switch between the two threshold methods used in the first and last pixel, a control bit is provided in the DMM_Mode register when requesting a measurement.

The first and last pixels are measured for each line, and the earliest first and latest last for the selected pixel area are reported out at the end of the measurement. The intention is for “last data pixel plus one” minus “first data pixel” is to equal the horizontal width of the video format.

2.9.6 Vertical Position

The Vertical Position measures the start and end of video data in hsyncs relative to the posedge of vsync.

The Data Vertical Start is defined as the number of hsyncs signals between the positive edge of the vsync signal and the “first data pixel line”.

First data pixel line definition is the first line with at least one pixel that is greater then the programmable threshold.

The Data Vertical End is defined as the number of hsyncs between posedge of vsync and the “first blanking line after data plus one”. The first blanking line is detected then confirmed that each subsequent line contains no data pixels. The confirmation of the first blanking line measurement ends at the posedge of vsync.

The first blanking line after data definition is the row after the last row with at least one pixel greater than the programmable threshold.

The first and last data pixel lines are measured within a frame and the earliest first and latest last for the selected pixel area are reported out at the end of the measurement. The intention is for “data vertical end plus one” minus “data vertical start” is to equal the vertical height of the video format.

2.9.7 DE Size

The DE Size measures the number of INCLKS clock cycles per data enable. It is useful for DVI inputs to exactly measure the input image horizontal size.

At the end of the measurement (DE falling edge), the measured value is compared to a programmed expected value ± a programmed threshold. If the expected value is within the threshold, the DE_size_mismatch flag is not set. If the measured size is outside of the threshold, the DE_size_mismatch flag is set.

In Free-running mode, the results are updated every line. The DE_size_mismatch flag is set at DE falling edge and reset at DE rising edge.

In One-shot mode, the results are updated once and stay that way until they are cleared by software. The DE_size_mismatch flag can only be cleared when the reset flag bit is set by software.

Table 13: DMEAS Output Register Mapping

	ALG_SEL = 00	ALG_SEL = 01	ALG_SEL = 10	ALG_SEL = 11
DMEAS_DATA_0	EDGE_OUT[7:0]	MIN_OUT[7:0]	HPOS_MIN[7:0]	DE_SIZE_OUT [7:0]
DMEAS_DATA_1	EDGE_OUT[15:8]	MAX_OUT[7:0]	HPOS_MIN[11:8]	DE_SIZE_OUT [15:8]
DMEAS_DATA_2	EDGE_OUT[23:16]	PCD_OUT[7:0]	HPOS_MAX[7:0]	DE_MISMATCH_FLAG
DMEAS_DATA_3	EDGE_OUT[31:24]	PCD_OUT[15:8]	HPOS_MAX[11:8]	8'h00
DMEAS_DATA_4	PSUM_OUT[7:0]	PCD_OUT[23:16]	VPOS_MIN[7:0]	8'h00
DMEAS_DATA_5	PSUM_OUT[15:8]	8'h00	VPOS_MIN[11:8]	8'h00
DMEAS_DATA_6	PSUM_OUT[23:16]	8'h00	VPOS_MAX[7:0]	8'h00
DMEAS_DATA_7	PSUM_OUT[31:24]	8'h00	VPOS_MAX[11:8]	8'h00

Table 14: Data Measurement Registers (Sheet 1 of 3)

Register Name	Addr	Mode	Bits	Default	Description
DMEAS_AEC_CTRL	0x0900		[7:6]	0x0	color select 00: all 01: red 10: green 11: blue
		R/W	[5]	0x0	vsync edge select 0: rising edge 1: falling edge
		R/W	[4]	0x0	hsync edge select 0: rising edge 1: falling edge
		R/W	[3]	0x0	interlace mode enable
		R/W	[2]	0x0	0: use data valid (tv mode only) 1: use data enable for data valid
		R/W	[1:0]	0x0	algorithm select 00 = Edge Intensity & Pixel Sum 01 = Min / Max & PCD 10 = H position and V position 11 = DE size

Table 14: Data Measurement Registers (Sheet 2 of 3)

Register Name	Addr	Mode	Bits	Default	Description
DMEAS_MODE_CTRL	0x0901	R/W	[7]	0x0	Reset the DE mismatch flag
		R/W	[6]	0x0	DE_freeze enable
		R/W	[5]	0x0	DE_one shot mode enable
		R/W	[4]	0x0	0: Listen to odd frame only 1: Listen to even frame only
		R/W	[3]	0x0	Threshold Mode Bit
		R/W	[1]	0x0	Polling Bit
		R/W	[0]	0x0	Data Measurement Start
DMEAS_THRESHOLD	0x0902	R/W	[7:0]	0x0	Threshold value for selected algorithm
DMEAS_WIN_MIN_X_L	0x0903	R/W	[7:0]	0x0	Min. X window [7:0] (bits[3:0] read back ‘0’.
DMEAS_WIN_MIN_X_H	0x0904		[7:4]		Reserved
		R/W	[3:0]		Min. X window [11:8] (relative to hsync)
DMEAS_WIN_MAX_X_L	0x0905	R/W	[7:0]	0xFFF	Max. X window [7:0] (bits[3:0] read back ‘0’.
DMEAS_WIN_MAX_X_H	0x0906		[7:4]		Reserved
		R/W	[3:0]		Max. X window [11:8] Relative to hsync, must be less than input horizontal total (LLK_LINELEN for analog input).
DMEAS_WIN_MIN_Y_L	0x0907	R/W	[7:0]	0x0	Min. Y window [7:0] (bits[3:0] read back ‘0’.
DMEAS_WIN_MIN_Y_H	0x0908		[7:4]		Reserved
		R/W	[3:0]		Min. Y window [11:8] (relative to vsync)
DMEAS_WIN_MAX_Y_L	0x0909	R/W	[7:0]	0xFFF	Max. Y window [7:0] (bits[3:0] read back ‘0’.
DMEAS_WIN_MAX_Y_H	0x090A		[7:4]		Reserved
		R/W	[3:0]		Max. Y window [11:8] (relative to vsync)
DMEAS_DE_REF_L	0x090B	R/W	[7:0]	0x0	DE_size expected result [7:0]
DMEAS_DE_REF_L	0x090C	R/W	[7:0]	0x0	DE_size expected result [15:8]
DMEAS_DE_TOL	0x090D	R/W	[7:0]	0x0	DE_tolerance value
DMEAS_DATA_0	0x090E	R	[7:0]	0x0	For details, refer to Table 13.
DMEAS_DATA_1	0x090F	R	[7:0]	0x0	
DMEAS_DATA_2	0x0910	R	[7:0]	0x0	
DMEAS_DATA_3	0x0911	R	[7:0]	0x0	
DMEAS_DATA_4	0x0912	R	[7:0]	0x0	
DMEAS_DATA_5	0x0913	R	[7:0]	0x0	
DMEAS_DATA_6	0x0914	R	[7:0]	0x0	
DMEAS_DATA_7	0x0915	R	[7:0]	0x0	

Table 14: Data Measurement Registers (Sheet 3 of 3)

Register Name	Addr	Mode	Bits	Default	Description
DMEAS_SCR_PAD_0	0x0934	R	[7:0]	0x0	Scratch Pad Registers
DMEAS_SCR_PAD_1	0x0916	R/W	[7:0]		
DMEAS_SCR_PAD_2	0x0917	R/W	[7:0]		
DMEAS_SCR_PAD_3	0x0918	R/W	[7:0]		
DMEAS_SCR_PAD_4	0x0919	R/W	[7:0]		
DMEAS_SCR_PAD_5	0x091A	R/W	[7:0]		
DMEAS_SCR_PAD_6	0x091B	R/W	[7:0]		
DMEAS_SCR_PAD_7	0x091C	R/W	[7:0]		
DMEAS_SCR_PAD_8	0x091E	R/W	[7:0]		
DMEAS_SCR_PAD_9	0x091F	R/W	[7:0]		
DMEAS_SCR_PAD_10	0x0920	R/W	[7:0]		
DMEAS_SCR_PAD_11	0x0921	R/W	[7:0]		
DMEAS_SCR_PAD_12	0x0922	R/W	[7:0]		
DMEAS_SCR_PAD_13	0x0923	R/W	[7:0]		
DMEAS_SCR_PAD_14	0x0924	R/W	[7:0]		
DMEAS_SCR_PAD_15	0x0925	R/W	[7:0]		

2.10 LCD Scaler

The LCD Scaler module resizes images from one resolution to another. It employs a 3x3 non-separable scaling filter which performs a dot product of the input pixel values with a weighting vector that is computed from the chosen filtering function. To sharpen text without introducing excessive artifacts, the output pixel's contrast level is adjusted based on the context value measured over a 3x3 grid in the relevant area of the source image.

For proper scaler operation, the SCLK frequency must be set greater than the max of DCLK and IN_HPIXEL x DCLK_FREQ / (DEST_HPIXEL x PIXEL_AVG).

Table 15: LCD Scaler Registers (Sheet 1 of 3)

Register Name	Addr	Mode	Bits	Default	Description
SCL_SRC_HPIX_L	0x0A01	R/W	[7:0]	0x0	Input Horizontal Resolution Bits [3:0] must be set to zero.
SCL_SRC_HPIX_H	0x0A02	R/W	[7:0]		
SCL_SRC_VPIX_L	0x0A03	R/W	[7:0]	0x0	Input Vertical Resolution Bits[3:0] must be set to 0.
SCL_SRC_VPIX_H	0x0A04	R/W	[7:0]		
SCL_SCALEFACH_L	0x0A05	R/W	[7:0]	0x0	17-bit Horizontal Scale Factor = (in_hpixel << 16) / dest_hpixel + 0.5
SCL_SCALEFACH_M	0x0A06	R/W	[7:0]	0x0	
SCL_SCALEFACH_H	0x0A07	R/W	[0]	0x0	
SCL_SCALEFACV_L	0x0A08	R/W	[7:0]	0x0	16-bit Vertical Scale Factor = (in_vpixel << 15) / dest_vpixel + 0.5
SCL_SCALEFACV_H	0x0A09	R/W	[7:0]	0x0	

Table 15: LCD Scaler Registers (Sheet 2 of 3)

Register Name	Addr	Mode	Bits	Default	Description
SCL_ORIGHPOS_0	0x0A0A	R/W	[7:0]	0x0	2's complement, signed number 27-bit horizontal position of the first output pixel =(-dest_hpos * scalefactor_h) >> 5
SCL_ORIGHPOS_1	0x0A0B	R/W	[7:0]	0x0	
SCL_ORIGHPOS_2	0x0A0C	R/W	[7:0]	0x0	
SCL_ORIGHPOS_3	0x0A0D	RW	[2:0]	0x0	
SCL_ORIGVPOS_E_0	0x0A0E	R/W	[7:0]	0x0	2's complement, signed number 27-bit vertical position of the first output pixel of the even frame = (-dest_vpos_e * scalefactor_v) >> 5
SCL_ORIGVPOS_E_1	0x0A0F	R/W	[7:0]		
SCL_ORIGVPOS_E_2	0x0A10	R/W	[7:0]	0x0	
SCL_ORIGVPOS_E_3	0x0A11	R/W	[2:0]		
SCL_THRES_SLOPE	0x0A16		[7:6]	0x0	Reserved
		R/W	[5:0]	0x28	Slope of the contrast amplification function
SCL_THRES_OFFSET_L	0x0A17	R/W	[7:0]	0x40	Offset of the contrast amplification function [7:0]
SCL_THRES_OFFSET_H	0x0A18		[7:2]	0x0	Reserved
		R/W	[1:0]	0x2	Offset of the contrast amplification function [9:8]
SCL_CBBYPASS	0x0A19	R/W	[7:2]	0x0	Reserved
			[1]	0x0	0: Normal 1: TCON control of contrast amplification
		R/W	[0]	0x0	0: Contrast Amplification enabled 1: Bypass Contrast Amplification
SCL_CON_CAL_SEL	0x0A1A		[7:1]		Reserved
		R/W	[0]	0x0	0: Context = max of RGB pk-pk 1: Context = sum of RGB pk-pk
SCL_TESTCON	0x0A1B		[7:2]		6-bit contrast amplification test data
		R/W	[1:0]	0x0	0x0, 0x3: normal 0x1: force input data into the contrast amplification function to bits [7:2] 0x2: force the output context data to be bits [5:2]
SCL_LUT1	0x0A1C	R/W	[7:0]	0xFA	Sigmoidal Function LUT Entry 1, 8-bit 2's complement
SCL_LUT2	0x0A1D	R/W	[7:0]	0xF7	Sigmoidal Function LUT Entry 2, 8-bit 2's complement
SCL_LUT3	0x0A1E	R/W	[7:0]	0xF7	Sigmoidal Function LUT Entry 3, 8-bit 2's complement
SCL_LUT4	0x0A1F	R/W	[7:0]	0xFC	Sigmoidal Function LUT Entry 4, 8-bit 2's complement
SCL_LUT5	0x0A20	R/W	[7:0]	0x2	Sigmoidal Function LUT Entry 5, 8-bit 2's complement
SCL_LUT6	0x0A21	R/W	[7:0]	0x0D	Sigmoidal Function LUT Entry 6, 8-bit 2's complement

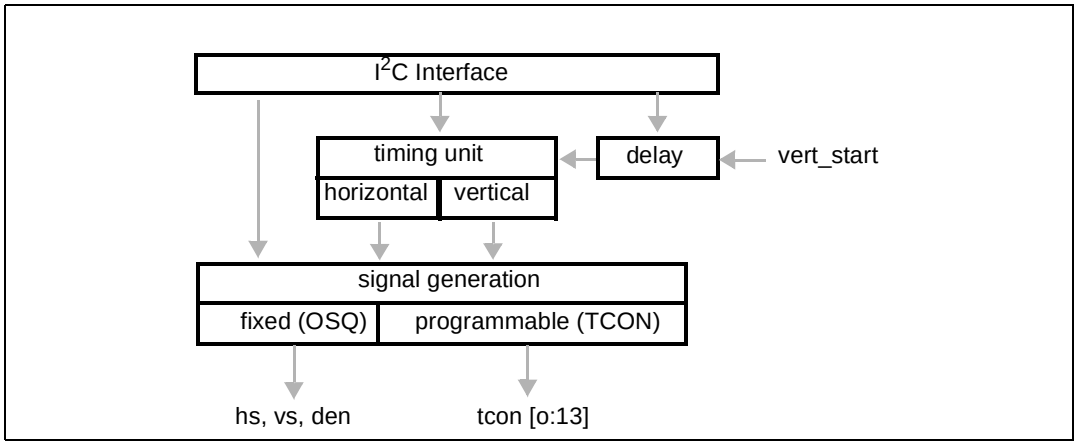
Table 15: LCD Scaler Registers (Sheet 3 of 3)

Register Name	Addr	Mode	Bits	Default	Description
SCL_LUT7	0x0A22	R/W	[7:0]	0x17	Sigmoidal Function LUT Entry 7, 8-bit 2's complement
SCL_LUT8	0x0A23	R/W	[7:0]	0x21	Sigmoidal Function LUT Entry 8, 8-bit 2's complement
SCL_LUT9	0x0A24	R/W	[7:0]	0x28	Sigmoidal Function LUT Entry 9, 8-bit 2's complement
SCL_LUT10	0x0A25	R/W	[7:0]	0x2C	Sigmoidal Function LUT Entry 10, 8-bit 2's complement
SCL_LUT11	0x0A26	R/W	[7:0]	0x2C	Sigmoidal Function LUT Entry 11, 8-bit 2's complement
SCL_LUT12	0x0A27	R/W	[7:0]	0x28	Sigmoidal Function LUT Entry 12, 8-bit 2's complement
SCL_LUT13	0x0A28	R/W	[7:0]	0x21	Sigmoidal Function LUT Entry 13, 8-bit 2's complement
SCL_LUT14	0x0A29	R/W	[7:0]	0x17	Sigmoidal Function LUT Entry 14, 8-bit 2's complement
SCL_LUT15	0x0A2A	R/W	[7:0]	0x0C	Sigmoidal Function LUT Entry 15, 8-bit 2's complement
SCL_BGCOLOR_R	0x0A2B	R/W	[7:0]	0x0	Red Component of background color
SCL_BGCOLOR_G	0x0A2C	R/W	[7:0]	0x0	Green Component of background color
SCL_BGCOLOR_B	0x0A2D	R/W	[7:0]	0x0	Blue Component of background color
SCL_BCOLOR_CTRL	0x0A2E	R/W	[7]	0x0	0: Normal 1: Force image to background color
		R/W	[6]	0x0	Top & Bottom Border Control 0: pixel replicating 1: background color blending
		R/W	[5]	0x0	Left & Right Border Control: 0: pixel replicating 1: background color blending
		R/W	[4]	0x0	Force output data as described in bit [1] when the maximum output vertical is reached.
		R/W	[3]	0x0	Force output data as described in bit [1] when an abnormal condition is detected by the sync measurement module.
		R/W	[2]	0x0	When the scaler is not running, force the output data to black if this bit is 0 or to the background color if the bit is 1.
		R/W	[1]	0x0	If an abnormality is detected in the sync measurement module or if the maximum output vertical total has been reached, force the output data to black if this bit is 0 or to white if this bit is 1.
		R/W	[0]	0x0	During blanking, force output data to black if this bit is 0 or to the background color if this bit is 1.

2.11 Output Sequencer

The Output Sequencer module synchronizes timing for the output video interface. It allows sufficient flexibility to support a broad range of Smart Panel applications as well using the Output Timing Controller (TCON) module, refer to Section 2.12 for more details. The timing unit is based on horizontal and vertical counters, which are locked with the input video stream.

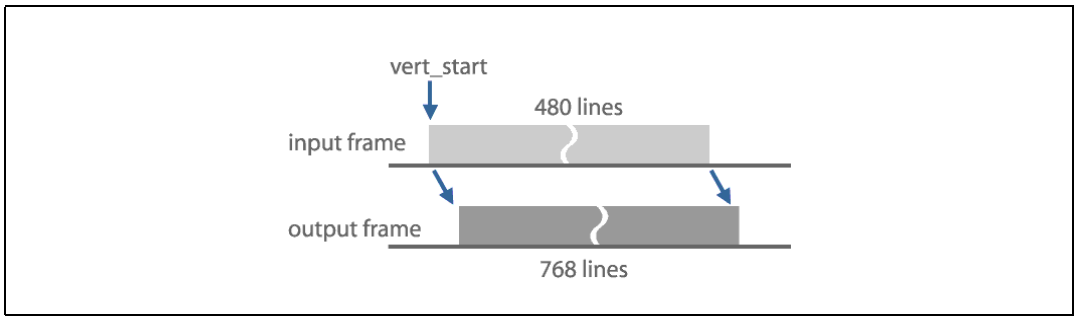
Figure 5: Output Sequencer and Timing Controller Block Diagram



2.11.1 Frame Synchronization

Due to the limited pixel memory of the chip, the output active video needs to be perfectly synchronized with the input active video. This mode of operation is called *Frame Lock*.

Figure 6: Frame Lock Operation



2.11.2 Timing Unit

The Timing Unit consists of a 12-bit horizontal and 12-bit vertical counter. It is synchronized with the input video stream.

2.11.3 Signal Generation

The Signal Generation unit can generate all fixed control signals like hsync, vsync and data enable as well as those required to run the internal data path. The fixed control signals appear on the

alternate output sync pins (AHS, AUS, ADE) for applications that do not require the more sophisticated timing control provided by the programmable TCON module.

Table 16: Output Sequencer Registers (Sheet 1 of 2)

Register Name	Addr	Mode	Bits	Default	Description
OSQ_CONTROL	0x0BC1	R	[7]		OUT_VMAX detected, sticky bit
		R/W	[6]	0x0	OUT_VMAX detect reset
		R/W	[5]	0x0	Interlace Enable
		R/W	[4]	0x0	Fractional Line Extend 0: +1 1: +2
		R/W	[3]	0x0	Frame Lock Reference 0: Last Input Pixel 1: First Input Pixel
		R/W	[2]	0x0	Frame Lock Selection 0: Last Line Variable 1: Fixed Line Length
		R	[1]		Shutdown ready - current frame has completed, panel can now be shut down
		R/W	[0]	0x0	Run sequencer when 1, otherwise stop at the end of the frame and set shutdown ready flag (bit [1])
OSQ_CLOCK_FRAC	0x0BC2	R/W	[7:0]	0x0	The fraction of lines (/256) that are extended
OSQ_OUT_HTOTAL_L	0x0BC3	R/W	[7:0]	0x0	Nominal Output Horizontal Total [7:0]
OSQ_OUT_HTOTAL_H	0x0BC4		[7:4]		Reserved
		R/W	[3:0]	0x0	Nominal Output Horizontal Total [11:8]
OSQ_OUT_VTOTAL_MIN_L	0x0BC5	R/W	[7:0]	0x0	minimum output vertical total, used to rearm for vert_enab trigger [7:0]
OSQ_OUT_VTOTAL_MIN_H	0x0BC6		[7:4]		Reserved
		R/W	[3:0]	0x0	Minimum Output Vertical Total, used to rearm for vert_enab triggers [11:8]
OSQ_VTOTAL_MAX_L	0x0BC7	R/W	[7:0]	0x0	Maximum Output Vertical Total, prevents panel burn with loss of vert_enab trigger [7:0]
OSQ_VTOTAL_MAX_H	0x0BC8		[7:4]		Reserved
		R/W	[3:0]	0x0	Maximum Output Vertical Total, prevents panel burn with loss of vert_enab triggers [11:8]
OSQ_VERTEN_DLY_E_L	0x0BC9	R/W	[7:0]	0x0	Delay of the VERT_ENAB signal to the reset of the horizontal and vertical counters, even and non-interlaced modes [15:0]
OSQ_VERTEN_DLY_E_M	0x0BCA	R/W	[7:0]	0x0	
OSQ_VERTEN_DLY_E_H	0x0BCB		[7:4]		Reserved
		R/W	[3:0]	0x0	Delay of the VERT_ENAB signal to the reset of the horizontal and vertical counters, even and non-interlaced [19:16]

Table 16: Output Sequencer Registers (Sheet 2 of 2)

Register Name	Addr	Mode	Bits	Default	Description
OSQ_VERTEN_DLY_O_L	0x0BCC	R/W	[7:0]	0x0	Delay of the VERT_ENAB signal to the reset of the horizontal and vertical counters, odd frame in interlace mode only [15:0]
OSQ_VERTEN_DLY_O_M	0x0BCD	R/W	[7:0]	0x0	
OSQ_VERTEN_DLY_O_H	0x0BCE		[7:4]	0x0	Reserved
		R/W	[3:0]	0x0	Delay of the VERT_ENAB signal to the reset of the horizontal and vertical counters, odd frame in interlace mode only [19:16]
OSQ_VSYNC_SET_L	0x0BCF	R/W	[7:0]	0x0	Vertical count at which VSYNC goes high [7:0]
OSQ_VSYNC_SET_H	0x0BD0		[7:4]	0x0	Reserved
		R/W	[3:0]	0x0	vertical count at which VSYNC goes high [11:8]
OSQ_VSYNC_RST_L	0x0BD1	R/W	[7:0]	0x0	Vertical count at which VSYNC goes low [7:0]
OSQ_VSYNC_RST_H	0x0BD2		[7:4]	0x0	Reserved
		R/W	[3:0]	0x0	Vertical count at which VSYNC goes low [11:8]
OSQ_HSYNC_SET_L	0x0BD3	R/W	[7:0]	0x0	Horizontal count at which HSYNC goes high [7:0]
OSQ_HSYNC_SET_H	0x0BD4		[7:4]	0x0	Reserved
		R/W	[3:0]		Horizontal count at which HSYNC goes high [11:8]
OSQ_HSYNC_RST_L	0x0BD5	R/W	[7:0]	0x0	Horizontal count at which HSYNC goes low [7:0]
OSQ_HSYNC_RST_H	0x0BD6		[7:4]	0x0	Reserved
		R/W	[3:0]	0x0	Horizontal count at which HSYNC goes low [11:8]
OSQ_HENAB_SET_L	0x0BD7	R/W	[7:0]	0x0	Horizontal count at which ENAB goes high [7:0]
OSQ_HENAB_SET_H	0x0BD8		[7:4]	0x0	Reserved
		R/W	[3:0]	0x0	Horizontal count at which ENAB goes high [11:8] value must be greater than 0x01C
OSQ_HENAB_RST_L	0x0BD9	R/W	[7:0]	0x0	Horizontal count at which ENAB goes low [7:0]
OSQ_HENAB_RST_H	0x0BDA		[7:4]	0x0	Reserved
		R/W	[3:0]	0x0	Horizontal count at which ENAB goes low [11:8]
OSQ_VENAB_SET_L	0x0BDB	R/W	[7:0]	0x0	Vertical count at which ENAB goes high [7:0]
OSQ_VENAB_SET_H	0x0BDC		[7:4]	0x0	Reserved
		R/W	[3:0]	0x0	Vertical count at which ENAB goes high [11:8]
OSQ_VENAB_RST_L	0x0BDD	R/W	[7:0]	0x0	Vertical count at which ENAB goes low [7:0]
OSQ_VENAB_RST_H	0x0BDE		[7:4]	0x0	Reserved
		R/W	[3:0]	0x0	Vertical count at which ENAB goes low [11:8]
OSQ_OUT_VCOUNT	0x0BDF	R	[7:0]	0x0	Vertical Counter /16 indicating the current frame position

2.12 Timing Controller (TCON)

The Output Timing Controller module provides timing for Smart Panel applications and other applications that are sensitive to output synchronization timing. The timing unit is based on horizontal and vertical counters, which are locked with the output video stream. A set of programmable comparators provides all necessary time events to generate the signals for the driver interface.

Please refer to the Programming Tool User's Manual and to the "Using TCON Outputs" application note for more details.

Table 17: TCON Registers (Sheet 1 of 7)

Register Name	Addr.	Mode	Bits	Default	Description
TCON_CONTROL	0x0B00		[7:3]		Reserved
		R/W	[2]	0x0	0: no TCON pipe delay matching 1: TCON pipe delay enabled (normal)
		R/W	[1]	0x0	Initialize SRTDs
		R/W	[0]	0x0	Enable TCON
TCON_COMP_0_L	0x0B10	R/W	[7:0]	0x0	count comparison value [7:0]
TCON_COMP_0_H	0x0B11	R/W	[7:5]		Reserved
		R/W	[4]		0: horizontal count compare 1: vertical count compare
		R/W	[3:0]		count comparison value [11:8]
TCON_COMP_1_L	0x0B12	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_1_H	0x0B13	R/W	[7:0]	0x0	
TCON_COMP_2_L	0x0B14	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_2_H	0x0B15	R/W	[7:0]	0x0	
TCON_COMP_3_L	0x0B16	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_3_H	0x0B17	R/W	[7:0]	0x0	
TCON_COMP_4_L	0x0B18	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_4_H	0x0B19	R/W	[7:0]	0x0	
TCON_COMP_5_L	0x0B1A	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_5_H	0x0B1B	R/W	[7:0]	0x0	
TCON_COMP_6_L	0x0B1C	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_6_H	0x0B1D	R/W	[7:0]	0x0	
TCON_COMP_7_L	0x0B1E	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_7_H	0x0B1F	R/W	[7:0]	0x0	
TCON_COMP_8_L	0x0B20	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_8_H	0x0B21	R/W	[7:0]	0x0	
TCON_COMP_9_L	0x0B22	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_9_H	0x0B23	R/W	[7:0]	0x0	

Table 17: TCON Registers (Sheet 2 of 7)

Register Name	Addr.	Mode	Bits	Default	Description
TCON_COMP_10_L	0x0B24	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_10_H	0x0B25	R/W	[7:0]	0x0	
TCON_COMP_11_L	0x0B26	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_11_H	0x0B27	R/W	[7:0]	0x0	
TCON_COMP_12_L	0x0B28	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_12_H	0x0B29	R/W	[7:0]	0x0	
TCON_COMP_13_L	0x0B2A	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_13_H	0x0B2B	R/W	[7:0]	0x0	
TCON_COMP_14_L	0x0B2C	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_14_H	0x0B2D	R/W	[7:0]	0x0	
TCON_COMP_15_L	0x0B2E	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_15_H	0x0B2F	R/W	[7:0]	0x0	
TCON_COMP_16_L	0x0B30	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_16_H	0x0B31	R/W	[7:0]	0x0	
TCON_COMP_17_L	0x0B32	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_17_H	0x0B33	R/W	[7:0]	0x0	
TCON_COMP_18_L	0x0B34	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_18_H	0x0B35	R/W	[7:0]	0x0	
TCON_COMP_19_L	0x0B36	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_19_H	0x0B37	R/W	[7:0]	0x0	
TCON_COMP_20_L	0x0B38	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_20_H	0x0B39	R/W	[7:0]	0x0	
TCON_COMP_21_L	0x0B3A	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_21_H	0x0B3B	R/W	[7:0]	0x0	
TCON_COMP_22_L	0x0B3C	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_22_H	0x0B3D	R/W	[7:0]	0x0	
TCON_COMP_23_L	0x0B3E	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_23_H	0x0B3F	R/W	[7:0]	0x0	
TCON_COMP_24_L	0x0B40	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_24_H	0x0B41	R/W	[7:0]	0x0	
TCON_COMP_25_L	0x0B42	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_25_H	0x0B43	R/W	[7:0]	0x0	
TCON_COMP_26_L	0x0B44	R/W	[7:0]	0x0	v to TCON_COMP_0 for definition
TCON_COMP_26_H	0x0B45	R/W	[7:0]	0x0	

Table 17: TCON Registers (Sheet 3 of 7)

Register Name	Addr.	Mode	Bits	Default	Description
TCON_COMP_27_L	0x0B46	R/W	[7:0]	0x0	Refer to TCON_COMP_0 for definition
TCON_COMP_27_H	0x0B47	R/W	[7:0]	0x0	
TCON_SRTD_0	0x0B50		[7:4]	0x0	Reserved
		R/W	[3]	0x0	SRTD initialization state
		R/W	[2:0]	0x0	0x0: f (A&B,&C&D,0,0) 0x1: f (A&B,&C&D,0,0) 0x2: f (A&B,&C&D,0,0) 0x3: f (0,0,A&B,0) 0x4: f (0,0,0,A&B) 0x5: f (0,0,0,A|B) 0x6: f (0,0,0,A^B) 0x7: f (0,0,0,!(A&B)) where f(Set, Reset, Toggle, Dflop) is a programmable logic/flop element
TCON_SRTD_1	0x0B51	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_2	0x0B52	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_3	0x0B53	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_4	0x0B54	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_5	0x0B55	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_6	0x0B56	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_7	0x0B57	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_8	0x0B58	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_9	0x0B59	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_10	0x0B5A	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_11	0x0B5B	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_12	0x0B5C	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_13	0x0B5D	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_14	0x0B5E	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_15	0x0B5F	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_16	0x0B60	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_17	0x0B61	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_18	0x0B62	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_19	0x0B63	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_20	0x0B64	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_21	0x0B65	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_22	0x0B66	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_23	0x0B67	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_24	0x0B68	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_25	0x0B69	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.

Table 17: TCON Registers (Sheet 4 of 7)

Register Name	Addr.	Mode	Bits	Default	Description
TCON_SRTD_26	0x0B6A	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_27	0x0B6B	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_28	0x0B6C	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_29	0x0B6D	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_30	0x0B6E	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_SRTD_31	0x0B6F	R/W	[7:0]	0x0	Refer to TCON_SRTD_0 for definition.
TCON_X_0	0x0B80		[7:6]		Reserved
		R/W	[5:0]	0x0	input selection for SRTD_0.A
TCON_X_1	0x0B81	R/W	[7:0]	0x0	input selection for SRTD_0.B (Refer to Table 18 for definition)
TCON_X_2	0x0B82	R/W	[7:0]	0x0	input selection for SRTD_1.A (Refer to Table 18 for definition)
TCON_X_3	0x0B83	R/W	[7:0]	0x0	input selection for SRTD_1.B (Refer to Table 18 for definition)
TCON_X_4	0x0B84	R/W	[7:0]	0x0	input selection for SRTD_2.A (Refer to Table 18 for definition)
TCON_X_5	0x0B85	R/W	[7:0]	0x0	input selection for SRTD_2.B (Refer to Table 18 for definition)
TCON_X_6	0x0B86	R/W	[7:0]	0x0	input selection for SRTD_3.A (Refer to Table 18 for definition)
TCON_X_7	0x0B87	R/W	[7:0]	0x0	input selection for SRTD_3.B (Refer to Table 18 for definition)
TCON_X_8	0x0B88	R/W	[7:0]	0x0	input selection for SRTD_4.A (Refer to Table 18 for definition)
TCON_X_9	0x0B89	R/W	[7:0]	0x0	input selection for SRTD_4.B (Refer to Table 18 for definition)
TCON_X_10	0x0B8A	R/W	[7:0]	0x0	input selection for SRTD_5.A (Refer to Table 18 for definition)
TCON_X_11	0x0B8B	R/W	[7:0]	0x0	input selection for SRTD_5.B (Refer to Table 18 for definition)
TCON_X_12	0x0B8C	R/W	[7:0]	0x0	input selection for SRTD_6.A (Refer to Table 18 for definition)
TCON_X_13	0x0B8D	R/W	[7:0]	0x0	input selection for SRTD_6.B (Refer to Table 18 for definition)
TCON_X_14	0x0B8E	R/W	[7:0]	0x0	input selection for SRTD_7.A (Refer to Table 18 for definition)
TCON_X_15	0x0B8F	R/W	[7:0]	0x0	input selection for SRTD_7.B (Refer to Table 18 for definition)
TCON_X_16	0x0B90	R/W	[7:0]	0x0	input selection for SRTD_8.A (Refer to Table 18 for definition)
TCON_X_17	0x0B91	R/W	[7:0]	0x0	input selection for SRTD_8.B (Refer to Table 18 for definition)

Table 17: TCON Registers (Sheet 5 of 7)

Register Name	Addr.	Mode	Bits	Default	Description
TCON_X_18	0x0B92	R/W	[7:0]	0x0	input selection for SRTD_9.A (Refer to Table 18 for definition)
TCON_X_19	0x0B93	R/W	[7:0]	0x0	input selection for SRTD_9.B (Refer to Table 18 for definition)
TCON_X_20	0x0B94	R/W	[7:0]	0x0	input selection for SRTD_10.A (Refer to Table 18 for definition)
TCON_X_21	0x0B95	R/W	[7:0]	0x0	input selection for SRTD_10.B (Refer to Table 18 for definition)
TCON_X_22	0x0B96	R/W	[7:0]	0x0	input selection for SRTD_11.A (Refer to Table 18 for definition)
TCON_X_23	0x0B97	R/W	[7:0]	0x0	input selection for SRTD_11.B (Refer to Table 18 for definition)
TCON_X_24	0x0B98	R/W	[7:0]	0x0	input selection for SRTD_12.A (Refer to Table 18 for definition)
TCON_X_25	0x0B99	R/W	[7:0]	0x0	input selection for SRTD_12. (Refer to Table 18 for definition)
TCON_X_26	0x0B9A	R/W	[7:0]	0x0	input selection for SRTD_13.A (Refer to Table 18 for definition)
TCON_X_27	0x0B9B	R/W	[7:0]	0x0	input selection for SRTD_13.B (Refer to Table 18 for definition)
TCON_X_28	0x0B9C	R/W	[7:0]	0x0	input selection for SRTD_14.A (Refer to Table 18 for definition)
TCON_X_29	0x0B9D	R/W	[7:0]	0x0	input selection for SRTD_14.B (Refer to Table 18 for definition)
TCON_X_30	0x0B9E	R/W	[7:0]	0x0	input selection for SRTD_15.A (Refer to Table 18 for definition)
TCON_X_31	0x0B9F	R/W	[7:0]	0x0	input selection for SRTD_15.B (Refer to Table 18 for definition)
TCON_X_32	0x0BA0	R/W	[7:0]	0x0	input selection for SRTD_16.A (Refer to Table 18 for definition)
TCON_X_33	0x0BA1	R/W	[7:0]	0x0	input selection for SRTD_16.B (Refer to Table 18 for definition)
TCON_X_34	0x0BA2	R/W	[7:0]	0x0	input selection for SRTD_17.A (Refer to Table 18 for definition)
TCON_X_35	0x0BA3	R/W	[7:0]	0x0	input selection for SRTD_17.B (Refer to Table 18 for definition)
TCON_X_36	0x0BA4	R/W	[7:0]	0x0	input selection for SRTD_18.A (Refer to Table 18 for definition)
TCON_X_37	0x0BA5	R/W	[7:0]	0x0	input selection for SRTD_18.B (Refer to Table 18 for definition)
TCON_X_38	0x0BA6	R/W	[7:0]	0x0	input selection for SRTD_19.A (Refer to Table 18 for definition)
TCON_X_39	0x0BA7	R/W	[7:0]	0x0	input selection for SRTD_19.B (Refer to Table 18 for definition)

Table 17: TCON Registers (Sheet 6 of 7)

Register Name	Addr.	Mode	Bits	Default	Description
TCON_X_40	0x0BA8	R/W	[7:0]	0x0	input selection for SRTD_20.A (Refer to Table 18 for definition)
TCON_X_41	0x0BA9	R/W	[7:0]	0x0	input selection for SRTD_20.B (Refer to Table 18 for definition)
TCON_X_42	0x0BAA	R/W	[7:0]	0x0	input selection for SRTD_21.A (Refer to Table 18 for definition)
TCON_X_43	0x0BAB	R/W	[7:0]	0x0	input selection for SRTD_21.B (Refer to Table 18 for definition)
TCON_X_44	0x0BAC	R/W	[7:0]	0x0	input selection for SRTD_22.A (Refer to Table 18 for definition)
TCON_X_45	0x0BAD	R/W	[7:0]	0x0	input selection for SRTD_22.B (Refer to Table 18 for definition)
TCON_X_46	0x0BAE	R/W	[7:0]	0x0	input selection for SRTD_23.A (Refer to Table 18 for definition)
TCON_X_47	0x0BAF	R/W	[7:0]	0x0	input selection for SRTD_23.B (Refer to Table 18 for definition)
TCON_X_48	0x0BB0	R/W	[7:0]	0x0	input selection for SRTD_24.A (Refer to Table 18 for definition)
TCON_X_49	0x0BB1	R/W	[7:0]	0x0	input selection for SRTD_24.B (Refer to Table 18 for definition)
TCON_X_50	0x0BB2	R/W	[7:0]	0x0	input selection for SRTD_25.A (Refer to Table 18 for definition)
TCON_X_51	0x0BB3	R/W	[7:0]	0x0	input selection for SRTD_25.B (Refer to Table 18 for definition)
TCON_X_52	0x0BB4	R/W	[7:0]	0x0	input selection for SRTD_26.A (Refer to Table 18 for definition)
TCON_X_53	0x0BB5	R/W	[7:0]	0x0	input selection for SRTD_26.B (Refer to Table 18 for definition)
TCON_X_54	0x0BB6	R/W	[7:0]	0x0	input selection for SRTD_27.A (Refer to Table 18 for definition)
TCON_X_55	0x0BB7	R/W	[7:0]	0x0	input selection for SRTD_27.B (Refer to Table 18 for definition)
TCON_X_56	0x0BB8	R/W	[7:0]	0x0	input selection for SRTD_28.A (Refer to Table 18 for definition)
TCON_X_57	0x0BB9	R/W	[7:0]	0x0	input selection for SRTD_28.B (Refer to Table 18 for definition)
TCON_X_58	0x0BBA	R/W	[7:0]	0x0	input selection for SRTD_29.A (Refer to Table 18 for definition)
TCON_X_59	0x0BBB	R/W	[7:0]	0x0	input selection for SRTD_29.B (Refer to Table 18 for definition)
TCON_X_60	0x0BBC	R/W	[7:0]	0x0	input selection for SRTD_30.A (Refer to Table 18 for definition)
TCON_X_61	0x0BBD	R/W	[7:0]	0x0	input selection for SRTD_30.B (Refer to Table 18 for definition)

Table 17: TCON Registers (Sheet 7 of 7)

Register Name	Addr.	Mode	Bits	Default	Description
TCON_X_62	0x0BBE	R/W	[7:0]	0x0	input selection for SRTD_31.A (Refer to Table 18 for definition)
TCON_X_63	0x0BBF	R/W	[7:0]	0x0	input selection for SRTD_31.B (Refer to Table 18 for definition)

Table 18: Input Selection Values

Value	Description	Value	Description
0x00	0	0x39	2 frame + 2 line + 1 pixel toggle
0x01	1	0x3A	HCOUNT[0]
0x02	External TCON input pin	0x3B	HCOUNT[1]
0x03	I2C SRTD init bit	0x3C	VCOUNT[0]
0x04 - 0x1F	comp0 - comp27	0x3D	VCOUNT[1]
0x20 - 0x37	SRTD8 - SRTD31	0x3E	FCOUNT[0]
0x38	2 frame + 1 line + 2 pixel toggle	0x3F	FCOUNT[1]

2.13 Pattern Generator

The integrated Pattern Generator gives the ability to display a set of graphic patterns to help debugging systems and test LCD panels. It is located ahead of the color management block, so all generated colors are subject to further transforms.

The screen can be split into a programmable grid of up to 8x8 areas. In each of these areas, it is possible to display one of two independent programmable patterns.

2.13.1 Screen Split

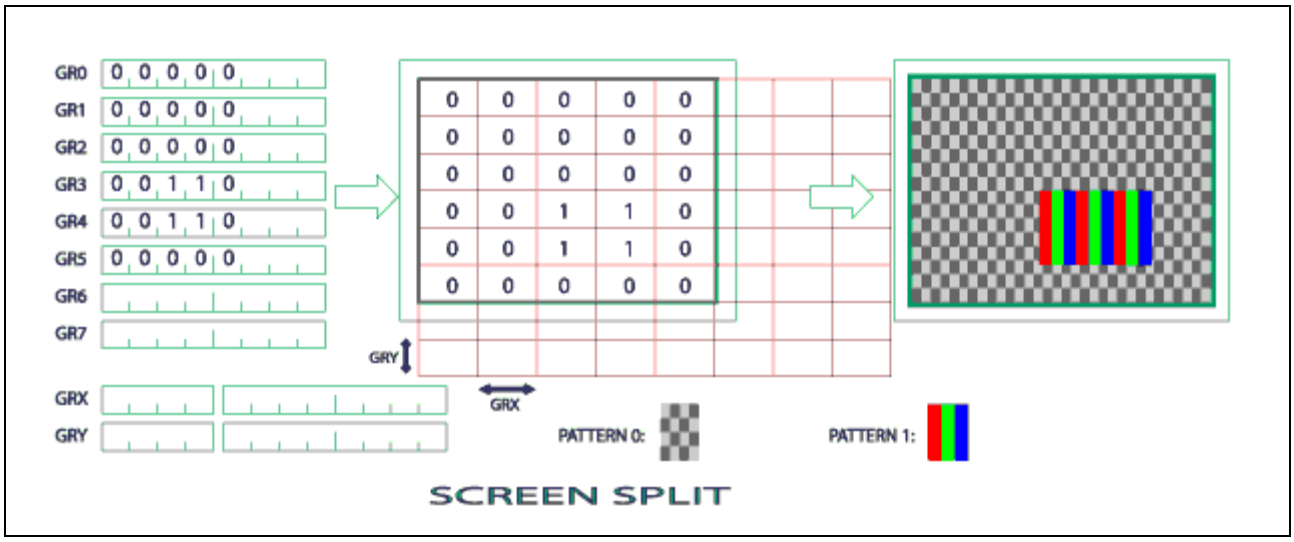
A set of eight Grid registers ***grid0 - grid7*** with eight bits each represents a block map of the grid of 8x8 blocks. Each bit of the Grid registers represents one rectangular (gridX)x(gridY) block of pixels which covers the LCD screen display area. Within these registers, a 0 selects Pattern 0 (defined below) and a 1 selects Pattern 1.

All cells have the same size, defined by one horizontal and one vertical grid block size registers ***gridX and gridY***.

When the programmed block size is such that the complete 8x8 grid is larger than the total screen area, only the blocks or part of blocks that are included in the output screen space are rendered. The 8x8 block set is upper left justified, such that all blocks on the right and bottom sides that are outside of the total display area are not rendered.

When the programmed block size is such that the complete 8x8 grid is smaller than the total screen area, the part of the screen area which is outside the 8x8 grid is forced to black.

Figure 7: Pattern Generator (Screen Split)



2.13.2 Pattern Engine

In order to display two patterns simultaneously on the LCD screen, the Pattern Generator has two pattern display engines. Each engine can display horizontal or vertical bicolor stripes, bicolor checkers, color bars, gray scales or color scales. It is also possible to select the video stream from the scaler as a pattern.

The pattern engine displays a bi-directional x-y symmetric pattern. Two 24-bit colors, C0 and C1, are alternately displayed with a horizontal period of Width and vertical period of Height. Programming a large Width and a small Height generates horizontal bars whereas the opposite will generate vertical bars. Programming small numbers for Width and Height generates checker patterns.

Each of the two patterns is also given X and Y offset attributes, so that it is possible to center the pattern inside the grid blocks.

A gradient effect can be applied independently on each of the two patterns, to either or both horizontal and vertical directions. The gradient effect takes two parameters: STEP and DELTA that define a ramp.

2.13.3 Borders

The Border Generator adds a single pixel width border to the whole display area. Each of the four sides of the display can be one of 8 independent colors.

Table 19: PGEN Registers (Sheet 1 of 5)

Register Name	Addr	Mode	Bits	Default	Description
PGEN_PGEN_ENAB	0x0600		[7:1]		Reserved
		R/W	[0]	0x0	0 = disable PGEN block 1 = enable PGEN block
PGEN_GRID0	0x0601	R/W	[7:0]	0x0	Grid Row 0
PGEN_GRID1	0x0602	R/W	[7:0]	0x0	Grid Row 1
PGEN_GRID2	0x0603	R/W	[7:0]	0x0	Grid Row 2

Table 19: PGEN Registers (Sheet 2 of 5)

Register Name	Addr	Mode	Bits	Default	Description
PGEN_GRID3	0x0604	R/W	[7:0]	0x0	Grid Row 3
PGEN_GRID4	0x0605	R/W	[7:0]	0x0	Grid Row 4
PGEN_GRID5	0x0606	R/W	[7:0]	0x0	Grid Row 5
PGEN_GRID6	0x0607	R/W	[7:0]	0x0	Grid Row 6
PGEN_GRID7	0x0608	R/W	[7:0]	0x0	Grid Row 7
PGEN_GRID_X_L	0x0609	R/W	[7:0]	0x0	width of a grid block in pixels [7:0]
PGEN_GRID_X_H	0x060A		[7:4]		Reserved
		R/W	[3:0]	0x0	width of a grid block in pixels [11:8]
PGEN_GRID_Y_L	0x060B	R/W	[7:0]	0x0	height of a grid block in pixels [7:0]
PGEN_GRID_Y_H	0x060C		[7:4]		Reserved
		R/W	[3:0]	0x0	height of a grid block in pixels [11:8]
PGEN_GRID_X_OFFSET_X_L	0x060D	R/W	[7:0]	0x0	grid block horizontal offset in pixels [7:0]
PGEN_GRID_X_OFFSET_X_H	0x060E		[7:4]		Reserved
		R/W	[3:0]	0x0	Grid Block Horizontal Offset in pixels [11:8]
PGEN_GRID_Y_OFFSET_Y_L	0x060F	R/W	[7:4]	0x0	Grid Block Vertical Offset in pixels
PGEN_GRID_Y_OFFSET_Y_H	0x0610	R/W	[3:0]		
PGEN_P0_MODE	0x0611	R/W			Pattern 0 Control
		R/W	[7:5]	0x0	number of bars in C0
		R/W	[4:2]	0x0	number of bars in C1
		R/W	[1]	0x0	0: pattern continues to progress across block boundaries 1: block boundaries cause the pattern to restart
		R/W	[0]	0x0	0: normal mode 1: C0 = video bypass
PGEN_P1_MODE	0x0612				Pattern 1 Control
		R/W	[7:5]	0x0	number of bars in C0
		R/W	[4:2]	0x0	number of bars in C1
		R/W	[1]	0x0	0: pattern continues to progress across block boundaries 1: block boundaries cause the pattern to restart
		R/W	[0]	0x0	0: normal mode 1: C0 = video bypass
PGEN_P0_WIDTH_X_L	0x0613	R/W	[7:0]	0x0	Pattern 0 Bar Width [7:0]
PGEN_P0_WIDTH_X_H	0x0614		[7:4]		Reserved
		R/W	[3:0]	0x0	Pattern 0 Bar Width [11:8]
PGEN_P0_WIDTH_X_OFFSET_L	0x0615	R/W	[7:0]	0x0	Pattern 0 Horizontal Offset [7:0]

Table 19: PGEN Registers (Sheet 3 of 5)

Register Name	Addr	Mode	Bits	Default	Description
PGEN_P0_WIDTH_X_OFFSET_H	0x0616		[7:4]		Reserved
		R/W	[3:0]	0x0	Pattern 0 Horizontal Offset [11:8]
PGEN_P0_HEIGHT_Y_L	0x0617	R/W	[7:0]	0x0	Pattern 0 Bar Height [7:0]
PGEN_P0_HEIGHT_Y_H	0x0618	R/W	[7:4]	0x0	Pattern 0 Vertical Sequence Increment
		R/W	[3:0]	0x0	Pattern 0 Bar Height [11:8]
PGEN_P0_HEIGHT_Y_OFFSET_L	0x0619	R/W	[7:0]	0x0	Pattern 0 Vertical Offset [7:0]
PGEN_P0_HEIGHT_Y_OFFSET_H	0x061A		[7:4]		Reserved
		R/W	[3:0]	0x0	Pattern 0 Vertical Offset [11:8]
PGEN_P1_WIDTH_X_L	0x061B	R/W	[7:0]	0x0	Pattern 1 Bar Width [7:0]
PGEN_P1_WIDTH_X_H	0x061C		[7:4]		Reserved
		R/W	[3:0]	0x0	Pattern 1 Bar Width [11:8]
PGEN_P1_WIDTH_X_OFFSET_L	0x061D	R/W	[7:0]	0x0	Pattern 1 Horizontal Offset [7:0]
PGEN_P1_WIDTH_X_OFFSET_H	0x061E		[7:4]		Reserved
		R/W	[3:0]	0x0	Pattern 1 Horizontal Offset [11:8]
PGEN_P1_HEIGHT_Y_L	0x061F	R/W	[7:0]	0x0	Pattern 1 Bar Height [7:0]
PGEN_P1_HEIGHT_Y_H	0x0620	R/W	[7:4]	0x0	Pattern 1 Vertical Sequence Increment
		R/W	[3:0]	0x0	Pattern 1 Bar Height [11:8]
PGEN_P1_HEIGHT_Y_OFFSET_L	0x0621	R/W	[7:0]	0x0	Pattern 1 Vertical Offset [7:0]
PGEN_P1_HEIGHT_Y_OFFSET_H	0x0622		[7:4]		Reserved
		R/W	[3:0]	0x0	Pattern 1 Vertical Offset [11:8]
PGEN_P0_COLOR_R_C0	0x0623	R/W	[7:0]	0x0	Pattern 0 Color C0 - Red
PGEN_P0_COLOR_G_C0	0x0624	R/W	[7:0]	0x0	Pattern 0 Color C0 - Green
PGEN_P0_COLOR_B_C0	0x0625	R/W	[7:0]	0x0	Pattern 0 Color C0 - Blue
PGEN_P0_COLOR_R_C1	0x0626	R/W	[7:0]	0x0	Pattern 0 Color C1 - Red
PGEN_P0_COLOR_G_C1	0x0627	R/W	[7:0]	0x0	Pattern 0 Color C1 - Green
PGEN_P0_COLOR_B_C1	0x0628	R/W	[7:0]	0x0	Pattern 0 Color C1 - Blue
PGEN_P1_COLOR_R_C0	0x0629	R/W	[7:0]	0x0	Pattern 1 Color C0 - Red
PGEN_P1_COLOR_G_C0	0x062A	R/W	[7:0]	0x0	Pattern 1 Color C0 - Green
PGEN_P1_COLOR_B_C0	0x062B	R/W	[7:0]	0x0	Pattern 1 Color C0 - Blue
PGEN_P1_COLOR_R_C1	0x062C	R/W	[7:0]	0x0	Pattern 1 Color C1 - Red
PGEN_P1_COLOR_G_C1	0x062D	R/W	[7:0]	0x0	Pattern 1 Color C1 - Green
PGEN_P1_COLOR_B_C1	0x062E	R/W	[7:0]	0x0	Pattern 1 Color C1 - Blue
PGEN_P0_GRADDELTA_R	0x062F	R/W	[7:0]	0x0	Pattern 0 Gradient Delta On Red
PGEN_P0_GRADDELTA_G	0x0630	R/W	[7:0]	0x0	Pattern 0 Gradient Delta On Green
PGEN_P0_GRADDELTA_B	0x0631	R/W	[7:0]	0x0	Pattern 0 Gradient Delta On Blue

Table 19: PGEN Registers (Sheet 4 of 5)

Register Name	Addr	Mode	Bits	Default	Description
PGEN_P0_GRADSTEP_X	0x0632	R/W	[7:0]	0x0	Pattern 0 Gradient Horizontal Step
PGEN_P0_GRADSTEP_Y	0x0633	R/W	[7:0]	0x0	Pattern 0 Gradient Vertical Step
PGEN_P1_GRADDELTA_R	0x0634	R/W	[7:0]	0x0	Pattern 1 Gradient Delta On Red
PGEN_P1_GRADDELTA_G	0x0635	R/W	[7:0]	0x0	Pattern 1 Gradient Delta On Green
PGEN_P1_GRADDELTA_B	0x0636	R/W	[7:0]	0x0	Pattern 1 Gradient Delta On Blue
PGEN_P1_GRADSTEP_X	0x0637	R/W	[7:0]	0x0	Pattern 1 Gradient Horizontal Step
PGEN_P1_GRADSTEP_Y	0x0638	R/W	[7:0]	0x0	Pattern 1 Gradient Vertical Step
PGEN_P0_SEQ_COL0_COL1	0x0639		[7]		Reserved
		R/W	[6:4]	0x0	Pattern 0 Bar 1 Color
			[3]		Reserved
		R/W	[2:0]	0x0	Pattern 0 Bar 0 Color
PGEN_P0_SEQ_COL2_COL3	0x063A		[7]		Reserved
		R/W	[6:4]	0x0	Pattern 0 Bar 3 Color
			[3]		Reserved
		R/W	[2:0]	0x0	Pattern 0 Bar 2 Color
PGEN_P0_SEQ_COL4_COL5	0x063B		[7]		Reserved
		R/W	[6:4]	0x0	Pattern 0 Bar 5 Color
			[3]		Reserved
		R/W	[2:0]	0x0	Pattern 0 Bar 4 Color
PGEN_P0_SEQ_COL6_COL7	0x063C		[7]		Reserved
		R/W	[6:4]	0x0	Pattern 0 Bar 7 Color
			[3]		Reserved
		R/W	[2:0]	0x0	Pattern 0 Bar 6 Color
PGEN_P1_SEQ_COL0_COL1	0x063D		[7]		Reserved
		R/W	[6:4]	0x0	Pattern 1 Bar 1 Color
			[3]		Reserved
		R/W	[2:0]	0x0	Pattern 1 Bar 0 Color
PGEN_P1_SEQ_COL2_COL3	0x063E		[7]		Reserved
		R/W	[6:4]	0x0	Pattern 1 Bar 3 Color
			[3]		Reserved
		R/W	[2:0]	0x0	Pattern 1 Bar 2 Color
PGEN_P1_SEQ_COL4_COL5	0x063F		[7]		Reserved
		R/W	[6:4]	0x0	Pattern 1 Bar 5 Color
			[3]		Reserved
		R/W	[2:0]	0x0	Pattern 1 Bar 4 Color

Table 19: PGEN Registers (Sheet 5 of 5)

Register Name	Addr	Mode	Bits	Default	Description
PGEN_P1_SEQ_COL6_COL7	0x0640		[7]		Reserved
		R/W	[6:4]	0x0	Pattern 1 Bar 7 Color
			[3]		Reserved
		R/W	[2:0]	0x0	Pattern 1 Bar 6 Color
PGEN_B_TOP_BOTTOM	0x0641	R/W	[7]	0x0	Top Border Enable
		R/W	[6]	0x0	Top Border Red; 0 = Off, 1= On
		R/W	[5]	0x0	Top Border Green; 0 = Off, 1= On
		R/W	[4]	0x0	Top Border Blue; 0 = Off, 1= On
		R/W	[3]	0x0	Bottom Border Enable
		R/W	[2]	0x0	Bottom Border Red; 0 = Off, 1= On
		R/W	[1]	0x0	Bottom Border Green; 0 = Off, 1= On
		R/W	[0]	0x0	Bottom Border Blue; 0 = Off, 1= On
PGEN_B_LEFT_RIGHT	0x0642	R/W	[7]	0x0	Left Border Enable
		R/W	[6]	0x0	Left Border Red; 0 = Off, 1= On
		R/W	[5]	0x0	Left Border Green; 0 = Off, 1= On
		R/W	[4]	0x0	Left Border Blue; 0 = Off, 1= On
		R/W	[3]	0x0	Right Border Enable
		R/W	[2]	0x0	Right Border Red; 0 = Off, 1= On
		R/W	[1]	0x0	Right Border Green; 0 = Off, 1= On
		R/W	[0]	0x0	Right Border Blue; 0 = Off, 1= On
PGEN_X_TOTAL_L	0x0643	R/W	[7:0]	0x0	Total Horizontal Size [7:0]
PGEN_X_TOTAL_H	0x0644		[7:4]		Reserved
		R/W	[3:0]	0x0	Total Horizontal Size [11:8]
PGEN_Y_TOTAL_L	0x0645	R/W	[7:0]	0x0	Total Vertical Size [7:0]
PGEN_Y_TOTAL_H	0x0646		[7:4]		Reserved
		R/W	[3:0]	0x0	Total Vertical Size [11:8]

2.14 sRGB

The sRGB block performs two primary functions:

1. Parametric gamma correction on multiple windows or full screen, used for video enhancement in a window and digital contrast/brightness control. The window coordinates are set by TCON registers.
2. 3D color cube warping RGB color space.

2.14.1 Parametric Gamma, Digital Contrast / Brightness on Multiple Windows

The function can be applied to the entire window by programming the window control to full screen. Each color channel acts independently. Simple digital contrast and brightness can be programmed using this hardware function. The desired window coordinates are programmed into the TCON.

2.14.2 Color Space Warp

The 8 corners of the color cube are independently controlled in 3D space with smooth interpolation of intermediate colors. Registers are 2's complement color delta's. For example, to make WHITE more like RED, program SRGB_WHITE_R to a small positive value.

Figure 8: Color Space Warp

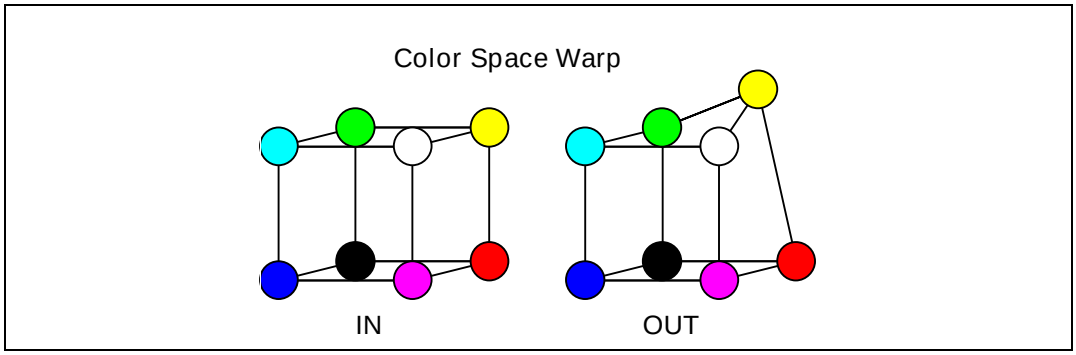


Table 20: sRGB Registers (Sheet 1 of 3)

Register Name	Addr	Mode	Bits	Default	Description
SRGB_CTRL	0x0D00	R/W	[7:6]	0x0	Reserved
		R/W	[5:4]	0x0	gamma_b control 0x0: disable 0x1: full screen 0x2: windowed 0x3: Reserved
		R/W	[3:2]	0x0	gamma_a control 0x0: disable 0x1: full screen 0x2: windowed 0x3: Reserved
		R/W	[1:0]	0x0	sRGB control 0x0: disabled 0x1: full screen 0x2: windowed 0x3: Reserved
SRGB_BLACK_R	0x0D01	R/W	[7:0]	0x0	Black Point Red Delta

Table 20: sRGB Registers (Sheet 2 of 3)

Register Name	Addr	Mode	Bits	Default	Description
SRGB_BLACK_G	0x0D02	R/W	[7:0]	0x0	Black Point Green Delta
SRGB_BLACK_B	0x0D03	R/W	[7:0]	0x0	Black Point Blue Delta
SRGB_RED_R	0x0D04	R/W	[7:0]	0x0	Red Point Red Delta
SRGB_RED_G	0x0D05	R/W	[7:0]	0x0	Red Point Green Delta
SRGB_RED_B	0x0D06	R/W	[7:0]	0x0	Red Point Blue Delta
SRGB_GREEN_R	0x0D07	R/W	[7:0]	0x0	Green Point Red Delta
SRGB_GREEN_G	0x0D08	R/W	[7:0]	0x0	Green Point Green Delta
SRGB_GREEN_B	0x0D09	R/W	[7:0]	0x0	Green Point Blue Delta
SRGB_BLUE_R	0x0D0A	R/W	[7:0]	0x0	Blue Point Red Delta
SRGB_BLUE_G	0x0D0B	R/W	[7:0]	0x0	Blue Point Green Delta
SRGB_BLUE_B	0x0D0C	R/W	[7:0]	0x0	Blue Point Blue Delta
SRGB_YELLOW_R	0x0D0D	R/W	[7:0]	0x0	Yellow Point Red Delta
SRGB_YELLOW_G	0x0D0E	R/W	[7:0]	0x0	Yellow Point Green Delta
SRGB_YELLOW_B	0x0D0F	R/W	[7:0]	0x0	Yellow Point Blue Delta
SRGB_CYAN_R	0x0D10	R/W	[7:0]	0x0	Cyan Point Red Delta
SRGB_CYAN_G	0x0D11	R/W	[7:0]	0x0	Cyan Point Green Delta
SRGB_CYAN_B	0x0D12	R/W	[7:0]	0x0	Cyan Point Blue Delta
SRGB_MAGENTA_R	0x0D13	R/W	[7:0]	0x0	Magenta Point Red Delta
SRGB_MAGENTA_G	0x0D14	R/W	[7:0]	0x0	Magenta Point Green Delta
SRGB_MAGENTA_B	0x0D15	R/W	[7:0]	0x0	Magenta Point Blue Delta
SRGB_WHITE_R	0x0D16	R/W	[7:0]	0x0	White Point Red Delta
SRGB_WHITE_G	0x0D17	R/W	[7:0]	0x0	White Point Green Delta
SRGB_WHITE_B	0x0D18	R/W	[7:0]	0x0	White Point Blue Delta
SRGB_GAMMA_A_RED_A	0x0D19	R/W	[7:0]	0x0	Parametric A Gamma A Red, Gamma
SRGB_GAMMA_A_RED_B	0x0D1A	R/W	[7:0]	0x0	Parametric A Gamma B Red, Contrast
SRGB_GAMMA_A_RED_C	0x0D1B	R/W	[7:0]	0x0	Parametric A Gamma C Red, Brightness
SRGB_GAMMA_A_GREEN_A	0x0D1C	R/W	[7:0]	0x0	Parametric A Gamma A Green, Gamma
SRGB_GAMMA_A_GREEN_B	0x0D1D	R/W	[7:0]	0x0	Parametric A Gamma B Green, Contrast
SRGB_GAMMA_A_GREEN_C	0x0D1E	R/W	[7:0]	0x0	Parametric A Gamma C Green, Brightness
SRGB_GAMMA_A_BLUE_A	0x0D1F	R/W	[7:0]	0x0	Parametric A Gamma A Blue, Gamma
SRGB_GAMMA_A_BLUE_B	0x0D20	R/W	[7:0]	0x0	Parametric A Gamma B Blue, Contrast
SRGB_GAMMA_A_BLUE_C	0x0D21	R/W	[7:0]	0x0	Parametric A Gamma C Blue, Brightness
SRGB_GAMMA_B_RED_A	0x0D22	R/W	[7:0]	0x0	Parametric B Gamma A Red, Gamma
SRGB_GAMMA_B_RED_B	0x0D23	R/W	[7:0]	0x0	Parametric Gamma B Red, Contrast
SRGB_GAMMA_B_RED_C	0x0D24	R/W	[7:0]	0x0	Parametric Gamma C Red, Brightness

Table 20: sRGB Registers (Sheet 3 of 3)

Register Name	Addr	Mode	Bits	Default	Description
SRGB_GAMMA_B_GREEN_A	0x0D25	R/W	[7:0]	0x0	Parametric Gamma A Green, Gamma
SRGB_GAMMA_B_GREEN_B	0x0D26	R/W	[7:0]	0x0	Parametric Gamma B Green, Contrast
SRGB_GAMMA_B_GREEN_C	0x0D27	R/W	[7:0]	0x0	Parametric Gamma C Green, Brightness
SRGB_GAMMA_B_BLUE_A	0x0D28	R/W	[7:0]	0x0	Parametric Gamma A Blue, Gamma
SRGB_GAMMA_B_BLUE_B	0x0D29	R/W	[7:0]	0x0	Parametric Gamma B Blue, Contrast
SRGB_GAMMA_B_BLUE_C	0x0D2A	R/W	[7:0]	0x0	Parametric Gamma C Blue, Brightness

2.15 On-Screen Display (OSD)

The integrated On-Screen Display (OSD) controller is a character-based overlay with a high level of features and over 100 kbits of on-board dedicated RAM storage.

- 15 row by 30 column character-mapped display
- Four user-definable windows
- 12x18-pixel characters with optional horizontal and vertical doubling on a row-by-row basis
- Two 16-entry 24-bit RGB user-definable color maps
- 192 RAM-based monochrome 1 bpp characters
- 64 RAM-based graphics 4 bpp characters
- Text character attributes: foreground/background color, blinking
- Graphics character attributes: per-pixel color, vertical/horizontal mirroring
- Row attributes: double width, double height
- Window attributes: window visibility, position, size, border shadow, color table
- Global attributes: OSD visibility, OSD screen position, alpha fade in/fade out, global size doubling, rotation in ninety-degree increments
- Single-bit enable/disable

For information on OSD programming, see the OSD Programming Manual.

2.15.1 OSD Access via I2C

The OSD uses a dedicated memory space that is accessed through an I2C port. The data stream sent to the OSD register starts with two header bytes. These specify the type of transfer and the row/column position for screen map transfers, the character index for font definition transfers, or the color index for color map transfers.

A stream of OSD writes to the OSD I2C register can fill in a segment of the OSD memory space with an internal auto-incrementing index register. The protocol is as follows:

1. Issue a start sequence with the R/W bit set to W.
2. Write to the OSD register. The first byte transferred is the index of the first internal OSD register to be written. The next byte contains the data to be written to that register. Subsequent bytes are written to successive internal OSD registers.
3. Continue writing data bytes until the desired range of OSD internal registers has been written (the ADE3700 device will issue an ACK on each transfer).
4. Issue an I2C stop sequence.

Character Display

There are two 96-character monochrome fonts and two 32-character four-bit color fonts, a total of 256 characters. The four bits of color are an index into one of two 16 entry color lookup tables. Entries in the color lookup table specify a 24-bit RGB color. All fonts and the color look-up table are RAM-based and must be downloaded to the OSD's internal RAM before use. Font addressing is as follows: character indexes 0x00-0x1F refer to color font 0, 0x20-0x7F refer to monochrome font 0, 0x80-0x9F refer to color font 1 and 0xA0-0xFF refer to monochrome font 1.

Screen Map

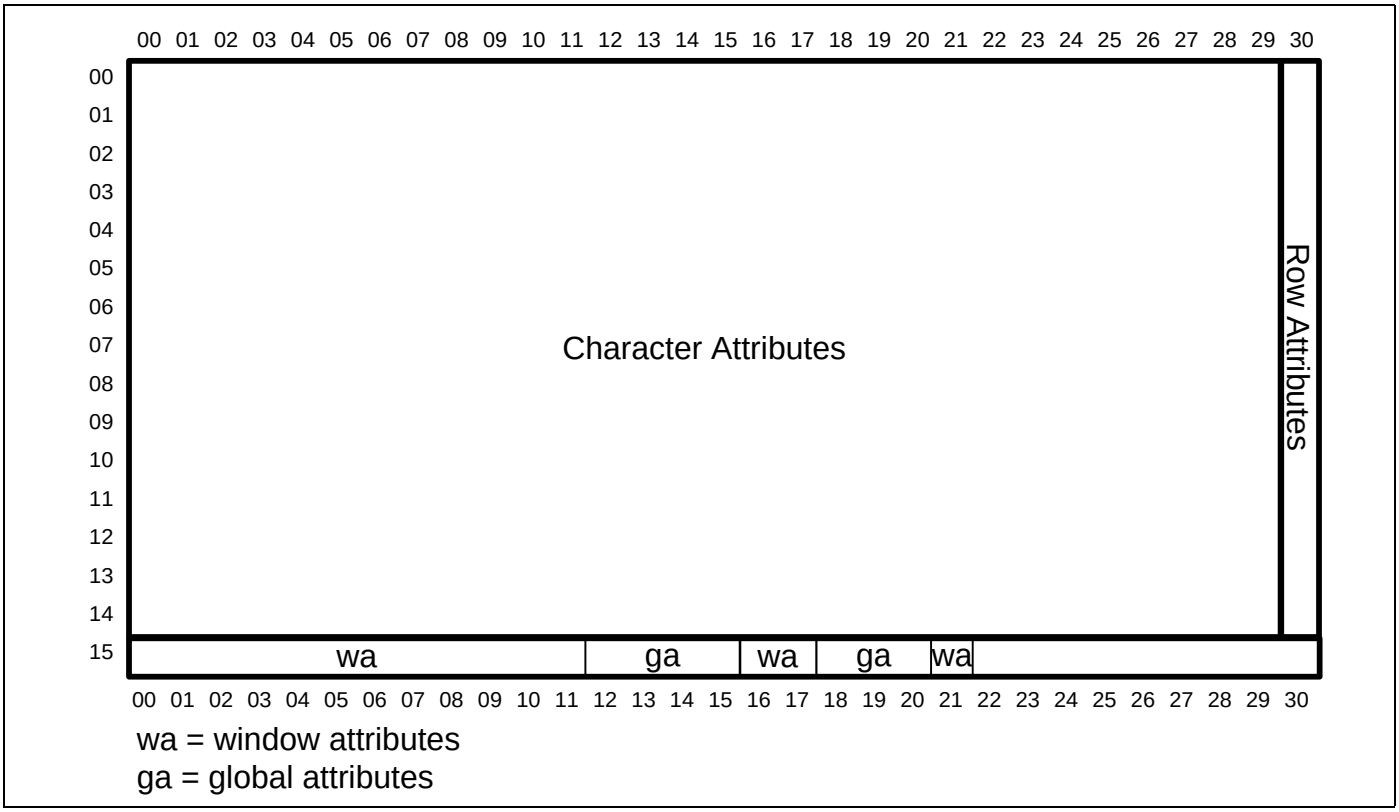
The OSD uses a character map of 15 rows x 30 columns. Each character occupies one byte. The value of each byte indicates the character to display.

The OSD character map is addressed by specifying the row and column as part of the data transfer.

Attribute Map

The attribute map is defined as 16 rows by 31 columns. It has an extra row and an extra column compared to the screen map.

Figure 9: Character Attribute Map



The values corresponding to printable row/column addresses provide character attributes. Each character on the screen has an attribute byte specifying (in the case of monochrome fonts) three bits of background color, four bits of foreground color, and a blink on/off bit.

Blinking, when enabled, has a period of 100 frames (50 frames on, 50 frames off).

Column 31 of each row contains row attributes. These include the fourth bit of the background color and two bits controlling double-height and double-width text.

Row 15 contains global attributes, including vertical and horizontal OSD position on the screen, alpha blending, shadow/bordering, OSD rotation, color map selection, and normal/double size. Alpha blending allows the OSD display to be mixed with the incoming video signal for transparency

effects. An alpha value of 255 makes the OSD opaque, while a value of 0 makes the OSD invisible, with a linear ramp of transparency between these two endpoints. Separate registers control alpha for foreground and background pixels.

A fade-in/fade-out feature ramps the alpha values every six frames, starting from their current value and going up or down the sequence: 0, 16, 32, 64, 128, 192, 224, 240, 255.

Row 15 also contains definitions for the four display windows. These windows define regions on the screen to which borders and shadows can be applied. (They are not analogous to windows in a GUI display, in that they do not represent four independent data displays. There is only one character map. The windows essentially define an area around which a border can be drawn or to which attributes can be assigned.) Windows also determine which of the two color tables will be used for the characters inside. Windows have a fixed precedence: Window 0 has the highest precedence and Window 3 the lowest. When windows overlap, the precedence determines which borders will be displayed and which color tables will be used in the overlapping area.

Monochrome and color fonts are affected differently by attribute bytes. Monochrome characters are affected by shadows and borders, and have their color specified by the foreground/background attributes. Color characters interpret the attribute byte differently than monochrome characters, using it to define blinking and 90-degree rotations rather than blinking, foreground color, and background color.

Color Tables

There are two color tables, each containing sixteen entries by three bytes each, giving a 24-bit RGB value for each entry. Entry 0 is used for the shadow color for monochrome characters and borders. Color-table selection is made on a window-by-window basis.

When writing the color table, the “row” value in the first header byte is interpreted as the color table index, while the “column” value in the second header byte encoded to select the color table (0 or 1) and the primary color (red, green, or blue). The data byte following the second header byte is written to the selected (table, index, primary) location.

Font Data

Font data is sent to the OSD through burst transfers. The first header byte selects the transfer type and provides three bits of the character index, while the second header byte selects transfer type “C” and gives the remaining five bits of offset. The data bytes for the character follow, given from top to bottom and left to right in the character cell.

A monochrome character is 27 bytes long, with two scan-lines occupying three bytes. A color character is four times as long as a monochrome character (108 bytes), with each byte containing two four-bit pixels. Both color and monochrome fonts are 12 pixels wide and 18 high.

Transfer Formats

The transfer format consists of two header bytes and a variable number of data bytes. The header bytes determine the type of transfer (character, attribute, monochrome font, color font, or color table). Addressing is by row and column in the case of character or attribute transfers, and by character index in the case of font transfers.

When writing to the color table, the “column” field determines the color table and R/G/B selection.

Table 21: OSD Access Header Definition

Header Byte	Bits	Description
First	[7:4]	Type of data transfer. Valid values are: 0x8: screen map 0x9: color LUT 0xA: attribute map 0xC: font data all others: Reserved
	[3:0]	For screen map or attribute map access, this is the row index. For color LUT access, this is the color index. For font data access, bits [2:0] are the MSB's of the character index.
Second	[7:6]	Type of data burst: 0x0: A/B modes: Only one data byte follows this header byte. 0x1: C mode: All bytes following this header byte are data bytes until the serial interface indicates an end-of-transmission. The OSD internally auto-increments after each byte. In screen and attribute map access modes the column number is incremented after each byte, wrapping to the beginning of the next row once column 29 is passed and wrapping to row 0 if row 14 is passed. Either mode may be used for display and character attribute modes, except for the off-screen attributes in column 15 and row 30, which must use mode A/B. Font definition mode must use mode C.
	[5]	must be set to zero
	[4:0]	In screen and attribute map access modes, this is the column number. In font data access mode, this gives the 5 lsb's of the character index. In color LUT access mode, it selects the table number and color to be written: 0x0: LUT 0, red 0x1: LUT 0, green 0x2: LUT 0, blue 0x3: LUT 1, red 0x4: LUT 1, green 0x5: LUT 1, blue 0x6 - 0x7: Reserved

Table 22: OSD Attribute Map Definition (Sheet 1 of 4)

Row	Column	Bits	Description
15	12	[7:0]	Vertical OSD position / 4
15	13	[7:0]	Horizontal OSD position / 5

Table 22: OSD Attribute Map Definition (Sheet 2 of 4)

Row	Column	Bits	Description
15	15	[7]	0: OSD off 1: OSD on
		[6:5]	0x0: plain characters 0x1: border characters 0x2: shadow characters 0x3: Reserved
		[4:3]	Reserved
		[2]	0: normal 1: flip OSD
		[1]	0: fade off 1: fade on
		[0]	0: normal size 1: double size
15	19	[7:0]	Foreground Alpha Blending
15	20	[7:0]	Background Alpha Blending
15	0	[7:4]	Window 0 Row Start
		[3:0]	Window 0 Row End
15	3	[7:4]	Window 1 Row Start
		[3:0]	Window 1 Row End
15	6	[7:4]	Window 2 Row Start
		[3:0]	Window 2 Row End
15	9	[7:4]	Window 3 Row Start
		[3:0]	Window 3 Row End
15	1	[7:3]	Window 0 Column Start
		[2]	Window 0 Visibility 0: Off 1: On
		[1]	Reserved
		[0]	Window 0 Shadow Enable
15	4	[7:3]	Window 1 Column Start
		[2]	Window 1 Visibility 0: Off 1: On
		[1]	Reserved
		[0]	Window 1 Shadow Enable

Table 22: OSD Attribute Map Definition (Sheet 3 of 4)

Row	Column	Bits	Description
15	7	[7:3]	Window 2 Column Start
		[2]	Window 2 Visibility 0: Off 1: On
		[1]	Reserved
		[0]	Window 2 Shadow Enable
15	10	[7:3]	Window 3 Column Start
		[2]	Window 3 Visibility 0: Off 1: On
		[1]	Reserved
		[0]	Window 3 Shadow Enable
15	2	[7:3]	Window 0 Column End
		[2:0]	Reserved
15	5	[7:3]	Window 1 Column End
		[2:0]	Reserved
15	8	[7:3]	Window 2 Column End
		[2:0]	Reserved
15	11	[7:3]	Window 3 Column End
		[2:0]	Reserved
15	16	[7:6]	Window 3 Shadow Width
		[5:4]	Window 2 Shadow Width
		[3:2]	Window 1 Shadow Width
		[1:0]	Window 0 Shadow Width
15	17	[7:6]	Window 3 Shadow Height
		[5:4]	Window 2 Shadow Height
		[3:2]	Window 1 Shadow Height
		[1:0]	Window 0 Shadow Height
15	21	[7:4]	Reserved
		[3]	window 3 color LUT select
		[2]	window 2color LUT select
		[1]	window 1 color LUT select
		[0]	window 0 color LUT select

Table 22: OSD Attribute Map Definition (Sheet 4 of 4)

Row	Column	Bits	Description
0 to 14	30	[7:3]	Reserved
		[2]	MSB of background color for the row
		[1]	double high enable for the row
		[0]	double wide enable for the row
0 to 14	0 to 29	[7:5]	3 LSBs of background color for 1bpp chars no function for 4bpp color chars
		[4]	blink enable
		[3:0]	foreground color for 1bpp chars for 4bpp color chars [3:2]: Reserved [1]: flip vertical [0]: flip horizontal

Table 23: OSD Register

Register Name	Addr	Mode	Bits	Default (hex)	Description
OSD_PORT	0x0C02	R/W	[7:0]	0	OSD Access Port

2.16 Flicker

The Flicker block computes correlations of the image data with potential inversion patterns of the LCD which in turn allows the microcontroller to modify the polarity signal to cancel large areas of flicker. This function is only useful in SmartPanel applications.

The incoming image is scored against 8 vertical Walsh functions. All patterns are considered vertically, while horizontally the pixels are assumed to be alternating RGB components.

The scores (0 to 7) are 32-bit unsigned quantities that reflect the correlation of the programmed window area with the 8 Walsh functions.

The horizontal inversion of the LCD drivers must be programmed into FLICKER_CTRL0[2:0]. The most common setting is +-+ or -+- (RGB).

A calculation is completed after the number of frames programmed into the FRAME_CNT_MAX register (0xCA03). With each frame the calculation is performed on only a vertical strip. The width of that strip (in pixels) is determined by the value programmed in the HBLOCK_SIZE register (0xCA02) with the following relation: strip width = 2 ^ (3 + HBLOCK_SIZE).

The free_run/freeze_scores bit (FLICKER_CTRL0[4]) enables the final calculation to be captured easily by the MCU. The internal flicker calculation continues to run -- only the update of the I2C registers is blocked when this bit is set to prevent corruption during readout.

Refer to the Flicker Programming Guide for more details.

Table 24: Flicker Registers (Sheet 1 of 2)

Register Name	Addr	Mode	Bits	Default	Description
FLK_CTRL	0x0CA1	R/W	[7:6]	0x0	Reserved
		R/W	[5]	0x1	0: straight line uniform function 1: straight line hill function (normal)
		R/W	[4]	0x0	0: free-running 1: freeze scores Set to a 1 when the microcontroller is reading multibyte scores to prevent update corruption.
		R/W	[2:0]	0x5	horizontal subpixel polarity inversion pattern of LCD (even/odd pixels) 0x0: -R-G-B / +R+G+B 0x1: -R-G+B / +R+G-B 0x2: -R+G-B / +R-G+B (Default) 0x3: -R+G+B / +R-G-B 0x4: +R-G-B / -R+G+B 0x5: +R-G+B / -R+G-B 0x6: +R+G-B / -R-G+B 0x7: +R+G+B / -R-G-B
FLK_HBLOCK_SIZE	0x0CA2	R/W	[7:4] [3:0]	0x0	Reserved width in pixels of the per frame scored area = 2 ^ (3+ hblock_size)
FLK_FRAME_CNT_MAX	0x0CA3	R/W	[7:0]	0x8	number of frames to complete one measurement total number of pixels in a line is: frame_cnt_max * (2 ^ (3+hblock_size)) example: hblock_size = 4; frame_cnt_max = 8; In each frame only one portion of the image is being scored. The width of that portion is 2 ^ (3 + hblock_size) = 128 pixels and the height is the full height of the image. Thus the total scored area after 8 frames is 128*8 = 1024 pixels wide.
FLK_MEAS0_0	0x0CB1	R/W	[7:0]	0x0	Score for Pattern 0
FLK_MEAS0_1	0x0CB2	R/W	[7:0]		
FLK_MEAS0_2	0x0CB3	R/W	[7:0]		
FLK_MEAS0_3	0x0CB4	R/W	[7:0]		
FLK_MEAS1_0	0x0CB5	R/W	[7:0]	0x0	Score for Pattern 1
FLK_MEAS1_1	0x0CB6	R/W	[7:0]		
FLK_MEAS1_2	0x0CB7	R/W	[7:0]		
FLK_MEAS1_3	0x0CB8	R/W	[7:0]		
FLK_MEAS2_0	0x0CB9	R/W	[7:0]	00x	Score for Pattern 2
FLK_MEAS2_1	0x0CBA	R/W	[7:0]		
FLK_MEAS2_2	0x0CBB	R/W	[7:0]		

Table 24: Flicker Registers (Sheet 2 of 2)

Register Name	Addr	Mode	Bits	Default	Description
FLK_MEAS2_3	0x0CBC	R/W	[7:0]		
FLK_MEAS3_0	0x0CBD	R/W	[7:0]	0x0	Score for Pattern 3
FLK_MEAS3_1	0x0CBE	R/W	[7:0]		
FLK_MEAS3_2	0x0CBF	R/W	[7:0]		
FLK_MEAS3_3	0x0CC0	R/W	[7:0]		
FLK_MEAS4_0	0x0CC1	R/W	[7:0]	0x0	Score for Pattern 4
FLK_MEAS4_1	0x0CC2	R/W	[7:0]		
FLK_MEAS4_2	0x0CC3	R/W	[7:0]		
FLK_MEAS4_3	0x0CC4	R/W	[7:0]		
FLK_MEAS5_0	0x0CC5	R/W	[7:0]	0x0	Score for Pattern 5
FLK_MEAS5_1	0x0CC6	R/W	[7:0]		
FLK_MEAS5_2	0x0CC7	R/W	[7:0]		
FLK_MEAS5_3	0x0CC8	R/W	[7:0]		
FLK_MEAS6_1	0x0CC9	R/W	[7:0]	0x0	Score for Pattern 6
FLK_MEAS6_2	0x0CCA	R/W	[7:0]		
FLK_MEAS6_3	0x0CCB	R/W	[7:0]		
FLK_MEAS6_4	0x0CCC	R/W	[7:0]		
FLK_MEAS7_0	0x0CCD	R/W	[7:0]	0x0	Score for Pattern 7
FLK_MEAS7_1	0x0CCE	R/W	[7:0]		
FLK_MEAS7_2	0x0CCF	R/W	[7:0]		
FLK_MEAS7_3	0x0CD0	R/W	[7:0]		

2.17 Gamma

The Gamma block performs an 8-bit to 10-bit lookup table on the 3 x 8 bits (R, G, B) color data coming from the LCD Scaler. The lookup table (LUT RAM) contains the corresponding 10-bit output corrected color for each 8-bit input color.

The RAMs are individually programmable (read and write) using I2C access. The memory map is as follows:

I2C address 0x1000 to 0x11FF: Red RAM

I2C address 0x1200 to 0x13FF: Green RAM

I2C address 0x1400 to 0x15FF: Blue RAM

Even addresses are the 8-bit LSBs of the 10-bit gamma value. Odd addresses are the 2 MSBs.

Table 25: Gamma Registers

Register Name	Addr	Mode	Bits	Default	Description
GAMMA_CTRL	0x0C10	R/W	[7:4]	0x0	Reserved
			[3]	0x0	0: normal 1: disable RAM access
			[2]	0x0	0: normal 1: test mode
			[1:0]	0x0	Gamma Mode Select 0x0: 10-bit linear bypass 0x1: 8-bit->10-bit gamma table (normal) 0x2: 8-bit linear bypass (no interpolation) 0x3: 8-bit->10-bit gamma table (normal)

2.18 APC

APC (formerly known as Arithmos Perfect Color) dithers an input 10 bit video stream down to 4-8 output bits. The dithering is done in space and time in such a way that the eye does not perceive objectionable artifacts such as:

- Fixed dither patterns
- Contours
- Flickering pixels
- Phase correlated flickering, which creates wave patterns known as “swimming”

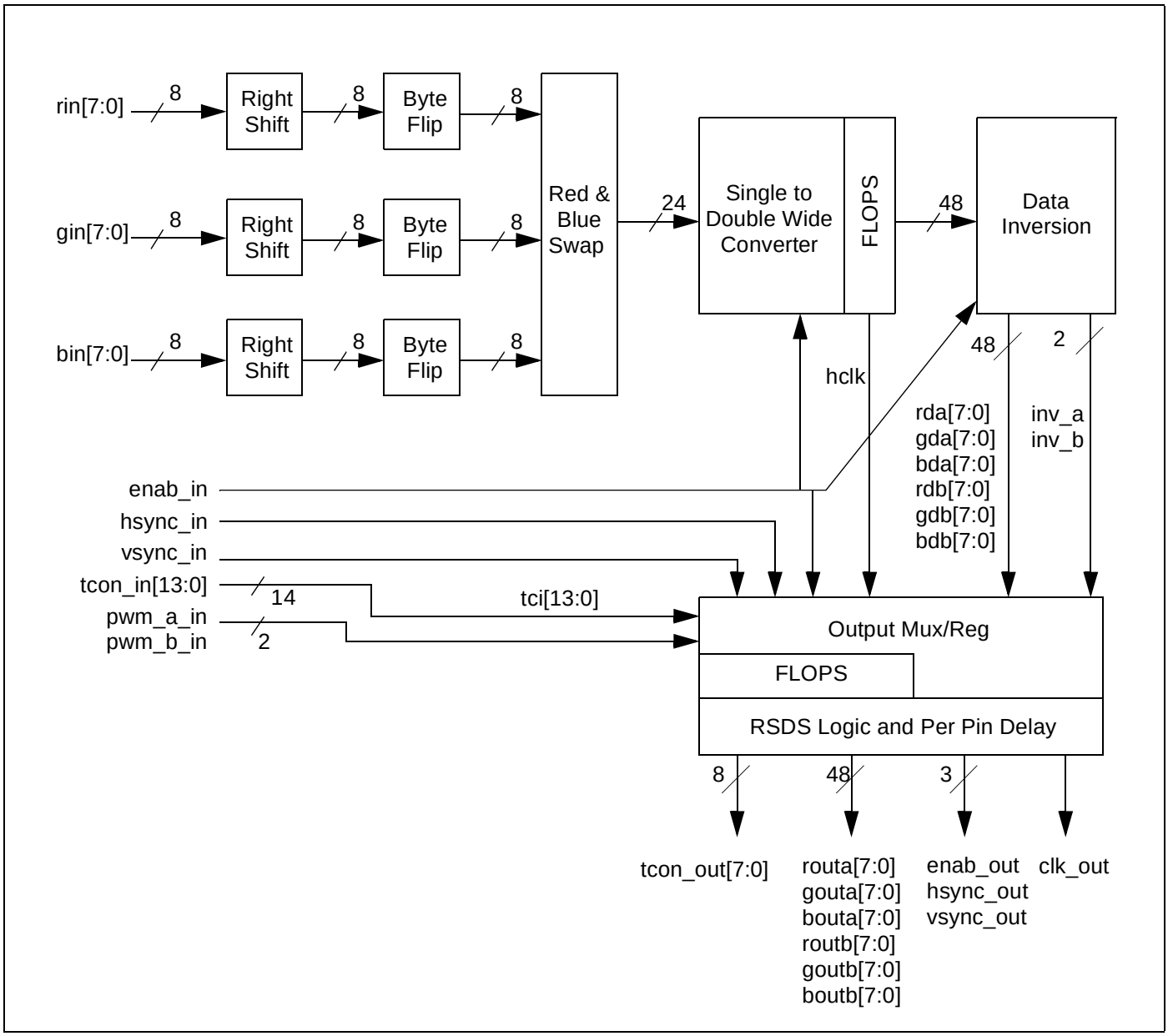
Table 26: APC Registers

Register Name	Addr	Mode	Bits	Default	Description
APC_APC0	0x0C20		[7]		Reserved
		R/W	[6:5]	0x0	Frame Modulation Period - 1
		R/W	[4:1]	0x0	0x0 - 0x3: 8-bit out 0x4: 4b out 0x5: 5b out 0x6: 6b out 0x7: 7b out 0x8: 8-bit out
		R/W	[0]	0x0	0: normal 1: disable APC -- truncate LSBs
APC_APC1	0x0C21		[7:2]		Reserved
		R/W	[1]	0x0	Offset the phase LUT
		R/W	[0]	0x0	Offset the dither LUT

2.19 Output Multiplexer

The Output Multiplexer formats the single wide data stream from the output of the APC block into a single or double wide data path for the flat panel. The architecture is shown in Figure 10.

Figure 10: Output Mux Block Diagram



Latency is not important, as long as the timing relationship between hsync, vsync, enab and data is preserved at the output. In Double Wide mode, the first pixel must be properly aligned even if the number of pixels in blanking or active are odd. The divide-by-2 circuit can be set to resync per line (based on data_enab and hsync_in edge) and per frame (based on vsync_in edge). The most reliable timing is when hsync and vsync are in the “low” counts of the timing core counters (i.e. hsync_set and hsync_rst are both below the active data region start/end counts). In the event that hsync and vsync are in the “high” (after active region) counts, the device should be set to sync to data_enab_re.

The Per Pin Delay and RSDS logic occur after the last latch and are implemented on all channels to maintain delay balance between signals that go into RSDS mode (data and clk/hsync) and those that do not (de/vsync and tcon).

2.19.1 Sub Block Function

2.19.1.1 Right Shift

- shifts right from 0 to 4 positions, fills from the top with zeroes
- out_mux_ctrl1[2:0]

2.19.1.2 Byte Flip

- flips data bits in a byte from LSB to MSB, i.e. out[7:0] = in[0:7]
- out_mux_ctrl0[4]

2.19.1.3 Red & Blue Swap

- swaps red and blue channels, i.e. out[23:0] = {in[7:0],in[15:8],in[23:16]}
- out_mux_ctrl0[3]

2.19.1.4 Single to Double Wide Converter

- in Single Wide mode (out_mux_ctrl0[1] = 0)
  - — flops all data into either A or B channels depending on out_mux_ctrl0[2]
  - — either inv_a or inv_b is active depending on active channel
- in Double Wide mode (out_mux_ctrl0[1] = 1)
  - — flops data into A/B or B/A positions depending on out_mux_ctrl0[2].
  - — divides clock by 2 (hclk = half speed DCLK), resyncing each line with data enable
  - — output data transitions as posedge/negedge as set in out_mux_ctrl0[5]
  - — can handle odd output htotal (i.e. all divide by 2's and state machines must be resynced per line)

2.19.1.5 Data Inversion

- resyncs at the end of each line to inactive state with data enable falling edge –
- invert is possible on the first pixel – compares 1st pixel to blanking value
- compares subsequent 24-bit/48-bit data to the last output; if more bits flip (i.e. hamming distance > active_bit_width/2), invert data word and toggle invert pin
- counts only active bits in hamming distance as determined by right shift and bit flip settings; zeroes out non active data signals at output
- controls:
  - — out_mux_ctrl1[4]
    - A and B channels have separate independent
    - A and B channels treated as one 48-bit channel, inv_a = inv_b
  - — out_mux_ctrl1[5]
    - data invert output polarity
  - — out_mux_ctrl1[6]
    - data invert enable
- data invert pins can also be driven by tcon srtd[26] and srtd[27] for panel balancing (out_mux_ctrl2[6] and out_mux_ctrl2[7])
- data can be inverted at the front end of the data inversion detection using tcon signals, either separate or combined channels (out_mux_ctrl3[0])

2.19.1.6 Output Mux / Reg

- combines all signals to form the desired outputs

- last point the data is flopped with DCLK before the pins
- gated clock available from tcon_srtd[12] in tcon mode
- see tables 2.2 - 2.5 for configurations.

Table 27: Output Mux Specification (Sheet 1 of 2)

Enable Data	OUT_MUX_CTRL0[0]	0	0	1	1	1	1	1	1	1	1	1
Enable TCON	OUT_MUX_CTRL1[3]	0	0	X	X	1	1	1	1	1	1	1
AB or BA	OUT_MUX_CTRL0[2]	X	X	0	1	X	X	0	1	X	X	X
Double	OUT_MUX_CTRL0[1]	X	X	0	0	1	1	0	0	1	1	1
Right Shift	OUT_MUX_CTRL1[2:0]	X	X	X	X	>0	>0	X	X	0	>0	>0
Byte Flip	OUT_MUX_CTRL0[4]	X	X	X	X	0	1	X	X	X	0	1
PWM enable	OUT_MUX_CTRL3[1]	0	1	1	1	1	1	0	0	0	0	0
PWM mux mode	OUT_MUX_CTRL3[2]	X	1	1	1	1	1	X	X	X	X	X
	OBA7	0	0	BDA7	BDA7	PWMA	BDA7	BDA7	BDA7	BDA7	BDA7	BDA7
	OBA6	0	0	BDA6	BDA6	BDA6	BDA6	BDA6	BDA6	BDA6	BDA6	BDA6
	OBA5	0	0	BDA5	BDA5	BDA5	BDA5	BDA5	BDA5	BDA5	BDA5	BDA5
	OBA4	0	0	BDA4	BDA4	BDA4	BDA4	BDA4	BDA4	BDA4	BDA4	BDA4
	OBA3	0	0	BDA3	BDA3	BDA3	BDA3	BDA3	BDA3	BDA3	BDA3	BDA3
	OBA2	0	0	BDA2	BDA2	BDA2	BDA2	BDA2	BDA2	BDA2	BDA2	BDA2
	OBA1	0	0	BDA1	BDA1	BDA1	BDA1	BDA1	BDA1	BDA1	BDA1	BDA1
	OBA0	0	0	BDA0	BDA0	BDA0	PWMA	BDA0	BDA0	BDA0	BDA0	BDA0
	OGA7	0	0	GDA7	GDA7	PWMB	GDA7	GDA7	GDA7	GDA7	GDA7	GDA7
	OGA6	0	0	GDA6	GDA6	GDA6	GDA6	GDA6	GDA6	GDA6	GDA6	GDA6
	OGA5	0	0	GDA5	GDA5	GDA5	GDA5	GDA5	GDA5	GDA5	GDA5	GDA5
	OGA4	0	0	GDA4	GDA4	GDA4	GDA4	GDA4	GDA4	GDA4	GDA4	GDA4
	OGA3	0	0	GDA3	GDA3	GDA3	GDA3	GDA3	GDA3	GDA3	GDA3	GDA3
	OGA2	0	0	GDA2	GDA2	GDA2	GDA2	GDA2	GDA2	GDA2	GDA2	GDA2
	OGA1	0	0	GDA1	GDA1	GDA1	GDA1	GDA1	GDA1	GDA1	GDA1	GDA1
	OGA0	0	0	GDA0	GDA0	GDA0	PWMB	GDA0	GDA0	GDA0	GDA0	GDA0
	ORA7	0	0	RDA7	RDA7	RDA7	RDA7	RDA7	RDA7	RDA7	TCI11	RDA7
	ORA6	0	0	RDA6	RDA6	RDA6	RDA6	RDA6	RDA6	RDA6	RDA6	RDA6
	ORA5	0	0	RDA5	RDA5	RDA5	RDA5	RDA5	RDA5	RDA5	RDA5	RDA5
	ORA4	0	0	RDA4	RDA4	RDA4	RDA4	RDA4	RDA4	RDA4	RDA4	RDA4
	ORA3	0	0	RDA3	RDA3	RDA3	RDA3	RDA3	TCI11	RDA3	RDA3	RDA3
	ORA2	0	0	RDA2	RDA2	RDA2	RDA2	RDA2	TCI10	RDA2	RDA2	RDA2
	ORA1	0	0	RDA1	PWMA	RDA1	RDA1	RDA1	TCI9	RDA1	RDA1	RDA1

Table 27: Output Mux Specification (Sheet 2 of 2)

	ORA0	0	0	RDA0	PWMB	RDA0	RDA0	RDA0	TCI8	RDA0	RDA0	TCI11
	OBB7	0	0	PWMA	BDB7	BDB7	BDB7	BDB7	BDB7	BDB7	TCI10	BDB7
	OBB6	0	0	PWMB	BDB6	BDB6	BDB6	BDB6	BDB6	BDB6	BDB6	BDB6
	OBB5	0	0	BDB5	BDB5	BDB5	BDB5	BDB5	BDB5	BDB5	BDB5	BDB5
	OBB4	0	0	BDB4	BDB4	BDB4	BDB4	BDB4	BDB4	BDB4	BDB4	BDB4
	OBB3	0	0	BDB3	BDB3	BDB3	BDB3	BDB3	BDB3	BDB3	BDB3	BDB3
	OBB2	0	0	BDB2	BDB2	BDB2	BDB2	BDB2	BDB2	BDB2	BDB2	BDB2
	OBB1	0	0	BDB1	BDB1	BDB1	BDB1	BDB1	BDB1	BDB1	BDB1	BDB1
	OBB0	0	0	BDB0	BDB0	BDB0	BDB0	BDB0	BDB0	BDB0	BDB0	TCI10
	OGB7	0	0	GDB7	GDB7	GDB7	GDB7	GDB7	GDB7	GDB7	TCI9	GDB7
	OGB6	0	0	GDB6	GDB6	GDB6	GDB6	GDB6	GDB6	GDB6	GDB6	GDB6
	OGB5	0	0	GDB5	GDB5	GDB5	GDB5	GDB5	GDB5	GDB5	GDB5	GDB5
	OGB4	0	0	GDB4	GDB4	GDB4	GDB4	GDB4	GDB4	GDB4	GDB4	GDB4
	OGB3	0	0	GDB3	GDB3	GDB3	GDB3	GDB3	GDB3	GDB3	GDB3	GDB3
	OGB2	0	0	GDB2	GDB2	GDB2	GDB2	GDB2	GDB2	GDB2	GDB2	GDB2
	OGB1	0	0	GDB1	GDB1	GDB1	GDB1	GDB1	GDB1	GDB1	GDB1	GDB1
	OGB0	0	0	GDB0	GDB0	GDB0	GDB0	GDB0	GDB0	GDB0	GDB0	TCI9
	ORB7	0	0	RDB7	RDB7	RDB7	RDB7	RDB7	RDB7	RDB7	TCI8	RDB7
	ORB6	0	0	RDB6	RDB6	RDB6	RDB6	RDB6	RDB6	RDB6	RDB6	RDB6
	ORB5	0	0	RDB5	RDB5	RDB5	RDB5	RDB5	RDB5	RDB5	RDB5	RDB5
	ORB4	0	0	RDB4	RDB4	RDB4	RDB4	RDB4	RDB4	RDB4	RDB4	RDB4
	ORB3	0	0	RDB3	RDB3	RDB3	RDB3	TCI11	RDB3	RDB3	RDB3	RDB3
	ORB2	0	0	RDB2	RDB2	RDB2	RDB2	TCI10	RDB2	RDB2	RDB2	RDB2
	ORB1	0	0	RDB1	RDB1	RDB1	RDB1	TCI9	RDB1	RDB1	RDB1	RDB1
	ORB0	0	0	RDB0	RDB0	RDB0	RDB0	TCI8	RDB0	RDB0	RDB0	TCI8

tci13 = tcon_in13, orb7 = output red B channel bit 7, rda3 = red A channel bit 3, etc. pwma = pwm_a input.

Table 28: CLK_OUT Mux Specification

enable data	OUT_MUX_CTRL0[0]	0	1	1	1	1
double	OUT_MUX_CTRL0[1]	X	0	0	1	1
clk invert	OUT_MUX_CTRL0[5]	X	0	1	0	1
	CLK_OUT	0	DOTCLK	!DOTCLK	HCLK	!HCLK

Table 29: Sync Mux Specification

enable data	OUT_MUX_CTRL0[0]	0	1	1
enable tcon	OUT_MUX_CTRL1[3]	0	0	1
	ENAB_OUT	0	ENI	INV_A
	HSYNC_OUT	0	HSI	TCI_GATED_CLK
	VSYNC_OUT	0	VSI	INV_B

eni = enab_in, hsi = hsync_in, vsi = vsync_in.

Table 30: TCON Mux Specification

enable tcon	OUT_MUX_CTRL1[3]	X	X	0
enable PWM	OUT_MUX_CTRL3[1]	0	1	1
PWM mux mode	OUT_MUX_CTRL3[2]	X	0	1
	TCON_OUT7	TCI7	TCI7	TCI7
	TCON_OUT6	TCI6	TCI6	TCI6
	TCON_OUT5	TCI5	TCI5	TCI5
	TCON_OUT4	TCI4	TCI4	TCI4
	TCON_OUT3	TCI3	TCI3	TCI3
	TCON_OUT2	TCI2	TCI2	TCI2
	TCON_OUT1	TCI1	PWM_A	TCI1
	TCON_OUT0	TCI0	PWM_B	TCI0

2.19.2 RSDS

In RSDS mode, clk and hsync outputs are the differential clock pair. All 48 data ports are combined into neighboring pairs (e.g. orb0 and orb1 are differential pairs in RSDS mode). the lower index is the positive sense differential output. TCON, data_enab and vsync outputs are unchanged. data_enab and vsync can be used to output LVCMOS data inversion signals independent of RSDS mode.

The following table indicates the pin, timing and data relationships in RSDS mode.

Table 31: RSDS Mode Specifications

RSDS Time	clk_o	hsync_o	o[r,g,b][a,b](2n)	o[r,g,b][a,b](2n+1)
t	0	1	bit from 2n	!bit from 2n
t+1	1	0	bit from 2n+1	!bit from 2n+1

Table 31: RSDS Mode Specifications (Continued)

RSDS Time	clk_o	hsync_o	o[r,g,b][a,b](2n)	o[r,g,b][a,b](2n+1)
t+2	0	1	bit from 2n	!bit from 2n
t+3	1	0	bit from 2n+1	!bit from 2n+1

Note: hsync_o is the positive clock signal according to the RSDS definition.

2.19.3 Per Pin Delay

Each of the 60 outputs has a per pin programmable delay. The delay is calibrated on the fly to the XCLK period, which is assumed to be 37ns. Each pin can be delayed by up to 6ns in 0.4ns increments. Code 0x0 is the least delay, code 0xF is the maximum delay. The setting is accurate to ±0.8ns across PVT. The calibration and resetting is done once per frame after the falling edge of vertical enable to prevent glitches from delay mux changes in the active data period. The delays are active in RSDS and normal output modes if enabled in the OUT_MUX_CTRL2 register.

Table 32: Output Mux Registers (Sheet 1 of 4)

Register Name	Addr	Mode	Bits	Default	Description
OMUX_CTRL_0	0x0C30	R/W	[7]	0x0	in 2 ppc, 0: data invert for A+B comb. 1: data invert A/B separate
		R/W	[6:4]	0x0	0x0 - 0x4: right shift per 8-bit R/G/B 0x5 - 0x7: Reserved
		R/W	[3]	0x0	0: normal 1: flip msbs to lsbs
		R/W	[2]	0x0	0: normal 1: swap R and B data
		R/W	[1]	0x0	0: in 1 ppc, A channel active 0: in 2 ppc, Left on A, Right on B 1: in 1 ppc, B channel active 1: 2ppc, Left on B, Right on A
		R/W	[0]	0x0	0: single wide, one pix/clk (ppc) 1: double wide, two pix/clk
OMUX_CTRL_1	0x0C31	R/W	[7]	0x0	Vsync Output Polarity
		R/W	[6]	0x0	Hsync Output Polarity
		R/W	[5]	0x0	Data Enable Output Polarity
		R/W	[4]	0x0	Clock Output Invert
		R/W	[3]	0x0	Data Invert Output Polarity
		R/W	[2]	0x0	Data Invert Enable
		R/W	[1]	0x0	0: TCON outputs set to zero 1: TCON outputs active
		R/W	[0]	0x0	0: all data outputs set to zero 1: output enabled

Table 32: Output Mux Registers (Sheet 2 of 4)

Register Name	Addr	Mode	Bits	Default	Description
OMUX_CTRL_2	0x0C32	R/W	[7]	0x0	Separate TCON driven invert enable
		R/W	[6]	0x0	TCON driven invert pin enable
		R/W	[5]	0x0	RSDS enable
		R/W	[4]	0x0	Per Pin Delay Enable
		R/W	[3]	0x0	Resync on Vsync Falling Edge
		R/W	[2]	0x0	Resync on Vsync Rising Edge
		R/W	[1]	0x0	Resync on Hsync Falling Edge
		R/W	[0]	0x0	Resync on Hsync Rising Edge
OMUX_DLY_BA0	0x0C50	R/W	[7:4]	0x0	Delay for OBA1
		R/W	[3:0]	0x0	Delay for OBA0
OMUX_ DLY_BA2	0x0C4F	R/W	[7:4]	0x0	Delay for OBA3
		R/W	[3:0]	0x0	Delay for OBA2
OMUX_ DLY_BA4	0x0C4E	R/W	[7:4]	0x0	Delay for OBA5
		R/W	[3:0]	0x0	Delay for OBA4
OMUX_ DLY_BA6	0x0C4D	R/W	[7:4]	0x0	Delay for OBA7
		R/W	[3:0]	0x0	Delay for OBA6
OMUX_ DLY_GA0	0x0C4C	R/W	[7:4]	0x0	Delay for OGA1
		R/W	[3:0]	0x0	Delay for OGA0
OMUX_ DLY_GA2	0x0C4B	R/W	[7:4]	0x0	Delay for OGA3
		R/W	[3:0]	0x0	Delay for OGA2
OMUX_ DLY_GA4	0x0C4A	R/W	[7:4]	0x0	Delay for OGA5
		R/W	[3:0]	0x0	Delay for OGA4
OMUX_ DLY_GA6	0x0C49	R/W	[7:4]	0x0	Delay for OGA7
		R/W	[3:0]	0x0	Delay for OGA6
OMUX_ DLY_RA0	0x0C48	R/W	[7:4]	0x0	Delay for ORA1
		R/W	[3:0]	0x0	Delay for ORA0
OMUX_ DLY_RA2	0x0C47	R/W	[7:4]	0x0	Delay for ORA3
		R/W	[3:0]	0x0	Delay for ORA2
OMUX_ DLY_RA4	0x0C46	R/W	[7:4]	0x0	Delay for ORA5
		R/W	[3:0]	0x0	Delay for ORA4
OMUX_ DLY_RA6	0x0C45	R/W	[7:4]	0x0	Delay for ORA7
		R/W	[3:0]	0x0	Delay for ORA6
OMUX_ DLY_BB0	0x0C44	R/W	[7:4]	0x0	Delay for OBB1
		R/W	[3:0]	0x0	Delay for OBB0

Table 32: Output Mux Registers (Sheet 3 of 4)

Register Name	Addr	Mode	Bits	Default	Description
OMUX_ DLY_BB2	0x0C43	R/W	[7:4]	0x0	Delay for OBB3
		R/W	[3:0]	0x0	Delay for OBB2
OMUX_ DLY_BB4	0x0C42	R/W	[7:4]	0x0	Delay for OBB5
		R/W	[3:0]	0x0	Delay for OBB4
OMUX_ DLY_BB6	0x0C41	R/W	[7:4]	0x0	Delay for OBB7
		R/W	[3:0]	0x0	Delay for OBB6
OMUX_ DLY_GB0	0x0C40	R/W	[7:4]	0x0	Delay for ORB1
		R/W	[3:0]	0x0	Delay for ORB0
OMUX_ DLY_GB2	0x0C3F	R/W	[7:4]	0x0	Delay for ORB3
		R/W	[3:0]	0x0	Delay for ORB2
OMUX_ DLY_GB4	0x0C3E	R/W	[7:4]	0x0	Delay for ORB5
		R/W	[3:0]	0x0	Delay for ORB4
OMUX_ DLY_GB6	0x0C3D	R/W	[7:4]	0x0	Delay for ORB7
		R/W	[3:0]	0x0	Delay for ORB6
OMUX_ DLY_RB0	0x0C3C	R/W	[7:4]	0x0	Delay for ORB1
		R/W	[3:0]	0x0	Delay for ORB0
OMUX_ DLY_RB2	0x0C3B	R/W	[7:4]	0x0	Delay for ORB3
		R/W	[3:0]	0x0	Delay for ORB2
OMUX_ DLY_R_B4	0x0C3A	R/W	[7:4]	0x0	Delay for ORB5
		R/W	[3:0]	0x0	Delay for ORB4
OMUX_ DLY_R_B6	0x0C39	R/W	[7:4]	0x0	Delay for ORB7
		R/W	[3:0]	0x0	Delay for ORB6
OMUX_ DLY_TCON_0	0x0C38	R/W	[7:4]	0x0	Delay for TCON1
		R/W	[3:0]	0x0	Delay for TCON0
OMUX_ DLY_TCON_2	0x0C37	R/W	[7:4]	0x0	Delay for TCON3
		R/W	[3:0]	0x0	Delay for TCON2
OMUX_ DLY_TCON_4	0x0C36	R/W	[7:4]	0x0	Delay for TCON5
		R/W	[3:0]	0x0	Delay for TCON4
OMUX_ DLY_TCON_6	0x0C35	R/W	[7:4]	0x0	Delay for TCON7
		R/W	[3:0]	0x0	Delay for TCON6
OMUX_ DLY_VS_ENAB	0x0C34	R/W	[7:4]	0x0	Delay for VSYNC
		R/W	[3:0]	0x0	Delay for ENAB
OMUX_ DLY_CLK_HS	0x0C33	R/W	[7:4]	0x0	Delay for CLK
		R/W	[3:0]	0x0	Delay for HSYNC

Table 32: Output Mux Registers (Sheet 4 of 4)

Register Name	Addr	Mode	Bits	Default	Description
OMUX_CTRL_3	0x0C51	R/W	[7:3]		Reserved
		R/W	[2]	0x0	PWM mux mode
		R/W	[1]	0x0	PWM enable
		R/W	[0]	0x0	TCON data invert enable, with computed data invert pin.
OMUX_REFCOUNT	0x0C52		[7:6]		Reserved
		R	[5:0]	0x0	Returns a value that indicates the ADE gate speed -- a function of temp and voltage higher = faster logic

2.20 Pulse Width Modulation (PWM)

The PWM block generates two signals that can be used to control backlight inverter switching power components directly. It is derived from XCLK and can be powered up independently of the DOTCLK and INCLK domains. The frequency, duty cycle, polarity and overlap/non-overlap are programmable. The output frequency can be free-running or locked to the output vsync signal.

Table 33: PWM Registers (Sheet 1 of 2)

Register Name	Addr	Mode	Bits	Default	Description
PWM_CTRL0	0x01A0	R	[7]	0x0	PWM status 0: unlocked 1: locked
		R/W	[6]	0x0	0: lock to CYCLES_PER_FRAME from the free-running state machine 1: lock to CYCLES_PER_FRAME register setting
		R/W	[5]	0x0	PWM_A polarity 0: active low 1: active high
		R/W	[4]	0x0	PWM_B polarity 0: active low 1: active high
		R/W	[3]	0x0	0: normal operation 1: force PWM outputs to polarity settings
		R/W	[2]	0x0	0: change period or duty cycle at the end of the current cycle 1: smooth change, period or duty cycle increment/decrement every PWM_STEP_DELAY cycle
		R/W	[1]	0x0	0: free-running 1: lock to out_vsync
		R/W	[0]	0x0	0: disable PWM output 1: enable PWM output

Table 33: PWM Registers (Sheet 2 of 2)

Register Name	Addr	Mode	Bits	Default	Description
PWM_CTRL1	0x01A1	R/W	[7:4]	0x0	Lock 2nd order gain (power of 2) 0x0 = max 0x3 = typical 0xF = min.
		R/W	[3:0]	0x0	Lock gain (power of 2) 0x0 = max 0x6 = typical 0xF = min.
PWM_PERIOD_L	0x01A2	R/W	[7:0]	0x0	Period-2 in free-running mode, in XCLKs
PWM_PERIOD_H	0x01A3	R/W	[7:0]		
PWM_DUTY_L	0x01A4	R/W	[7:0]	0x0	Duty cycle of PWM in XCLKs
PWM_DUTY_H	0x01A5	R/W	[7:0]		
PWM_OVERLAP_L	0x01A6	R/W	[7:0]	0x0	Non-overlap of PWMs in XCLKs
PWM_OVERLAP_H	0x01A7	R/W	[7:0]		
PWM_STEP_DELAY	0x01A8	R/W	[7:0]	0x0	In smooth change mode, the number of cycles skipped before the period/duty registers are incremented/decremented
PWM_CYCLES_PER_FRAME_L	0x01A9	R/W	[7:0]	0x0	The number of cycles per frame in frame lock mode when not using the internally generated cycles per frame from a previous free-running mode
PWM_CYCLES_PER_FRAME_H	0x01AA	R/W	[7:0]		

2.21 DFT Block

Table 34: DFT Registers (Sheet 1 of 3)

Register Name	Addr	Mode	Bits	Default	Description
DFT_TEST_MODE	0x0F00		[7:4]		Reserved
		R/W	[3]	0x0	trigger video bus MFSR
		R/W	[2]	0x0	enable output pin MFSR
		R/W	[1]	0x0	clear output pin MFSR
		R/W	[0]	0x0	output pin test override
DFT_MUX_OUT_MODE	0x0F01		[7:6]		Reserved
		R/W	[5:0]	0x0	mux selector for output porta/b and syncs
DFT_FLOP_OUT_MODE	0x0F02		[7:6]		Reserved
		R/W	[5:0]	0x0	mux selector for synchronous digital debug bus
DFT_CLK_0UT_MODE	0x0F03	R/W	[7:6]	0x0	divide-by selector for clocks to OCLK pin fout = selected clock / (2 ^ value)
		R/W	[5:0]	0x0	mux selector for clocks to OCLK pin
DFT_CLK_1_MODE	0x0F04	R/W	[7:6]	0x0	divide-by selector for clocks to CLKOUT pin fout = selected clock / (2 ^ value)

Table 34: DFT Registers (Sheet 2 of 3)

Register Name	Addr	Mode	Bits	Default	Description
DFT_CLK_2_MODE	0x0F05	R/W	[5:0]	0x0	mux selector for clocks to CLKOUT pin
DFT_OUT_DISAB_0	0x0F06	R/W	[7:0]	0x0	Disable Port A Red Output in Test Mode
DFT_OUT_DISAB_1	0x0F07	R/W	[7:0]	0x0	Disable Port A Green Output in Test Mode
DFT_OUT_DISAB_2	0x0F08	R/W	[7:0]	0x0	Disable Port A Blue Output in Test Mode
DFT_OUT_DISAB_3	0x0F09	R/W	[7:0]	0x0	Disable Port B Red Output in Test Mode
DFT_OUT_DISAB_4	0x0F0A	R/W	[7:0]	0x0	Disable Port B Green Output in Test Mode
DFT_OUT_DISAB_5	0x0F0B	R/W	[7:0]	0x0	Disable Port B Blue Output in Test Mode
DFT_OUT_DISAB_6	0x0F0C	R/W	[7:3]	0x0	Disable TCON Bits [4:0] in Test Mode
		R/W	[2]	0x0	Disable Vert Sync Output in Test Mode
		R/W	[1]	0x0	Disable Data Enab Output in Test Mode
		R/W	[0]	0x0	Disable Horz Sync Output in Test Mode
DFT_OUT_DISAB_7	0x0F0D		[7:5]		Reserved
		R/W	[4]	0x0	Disable CLKOUT Output In Test Mode
		R/W	[3]	0x0	Disable OCLK Output in Test Mode
		R/W	[2:0]	0x0	Disable TCON Bits [7:5] in Test Mode
DFT_STIM_CTRL	0x0F0E		[7:6]		Reserved
		R/W	[0]	0x0	Internal Stimulus Bus Enable
DFT_STIM_EN_0	0x0F0F	R/W	[7]	0x0	SCL Test Stimulus Enable
		R/W	[6:2]		Reserved
		R/W	[1]	0x0	ADC Test Stimulus Enable
		R/W	[0]	0x0	NC
DFT_STIM_EN_1	0x0F10		[7:6]		Reserved
		R/W	[5]	0x0	TCON test bypass
		R/W	[4]	0x0	OMUX test stimulus enable
		R/W	[3]	0x0	APC test stimulus enable
		R/W	[2]	0x0	OSD test stimulus enable
		R/W	[1]	0x0	SCL bypass
		R/W	[0]	0x0	PGEN test stimulus enable
DFT_BIST_STATUS	0x0F11		[7:6]		Reserved
		R	[5]		Gamma RAM BIST end
		R	[4]		OSD CS RAM BIST end
		R	[3]		OSD DRB RAM BIST
		R	[2]		OSD MB RAM BIST end
		R	[1]		SCL coeff. RAM BIST end
		R	[0]		SCL line buffer RAM BIST end

Table 34: DFT Registers (Sheet 3 of 3)

Register Name	Addr	Mode	Bits	Default	Description
DFT_BIST_RESULT_0	0x0F12		[7:6]		Reserved
		R	[5]		SCL coeff RAM 2 BIST fail
		R	[4]		SCL coeff RAM 1 BIST fail
		R	[3]		SCL line buffer 4 BIST fail
		R	[2]		SCL line buffer 3 BIST fail
		R	[1]		SCL line buffer 2 BIST fail
		R	[0]		SCL line buffer 1 BIST fail
DFT_BIST_RESULT_1	0x0F13		[7]		Reserved
		R	[6]		Gamma blue RAM BIST fail
		R	[5]		Gamma green RAM BIST fail
		R	[4]		Gamma red RAM BIST fail
		R	[3]		OSD CS RAM1 BIST fail
		R	[2]		OSD CS RAM 2 BIST fail
		R	[1]		OSD DRB RAM BIST fail
		R	[0]		OSD MB RAM BIST fail
DFT_MFSR_DONE	0x0F14		[7:1]		Reserved
		R	[0]		done signal
DFT_MFSR_SIG_0	0x0F15	R	[7:0]	0x0	video bus MFSR
DFT_MFSR_SIG_1	0x0F16	R	[7:0]		
DFT_MFSR_SIG_2	0x0F17	R	[7:0]		
DFT_MFSR_SIG_3	0x0F18	R	[7:0]		

2.22 I²C RAM Addresses

Table 35: I²C RAM Addresses

Name	Start Addr	End Addr	Description
GAM_RED	0x1000	11FF	Gamma LUT, Red, LSB0,MSB0,LSB1,... (256x10)
GAM_GREEN	0x1200	13FF	Gamma LUT, Green, (256x10)
GAM_BLUE	0x1400	15FF	Gamma LUT, Blue, (256x10)
OSD_MB	0x1700	175F	OSD Color LUTs (32x24)
OSD_CS	0x3000	5F3F	OSD Character Map (1344x36x2 copies)
OSD_DRB	0x6000	647F	OSD Screen Map (1152x8)
SCL_COEFF	0x9000	98FF	Scaler coefficient RAM (256x36x2 copies)
SCL_LINE1	0x9900	A7FF	Scaler line buffer 1 (1280x24)
SCL_LINE2	0xA800	B6FF	Scaler line buffer 2 (1280x24)
SCL_LINE3	0xB700	C5FF	Scaler line buffer 3 (1280x24)
SCL_LINE4	0xC600	D4FF	Scaler line buffer 4 (1280x24)

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD18 DVDD18 XVDD18 LVDD18	Supply voltage			1.95	V
AVDD33 DVDD33	Supply voltage			3.6	V
VIN	Max voltage on 5 volt tolerant input pins			6.1	V
T_{STG}	Storage temperature	-40		+150	°C

3.2 Power Consumption Matrices

Table 36: ADE3700x

Symbol	Parameter	Min	Typ*	Max**	Unit
	Supply Current (Analog Input, XGA@75Hz, 78.75MHz)				
I_{AVDD18}	1.8V analog supply (I_{AVDD18})		195	203	mA
I_{DVDD18}	1.8V digital supply (I_{DVDD18})		228	257	mA
I_{AVDD33}	3.3V analog supply ($_{IAVDD33}$)		102	105	mA
I_{DVDD33}	3.3V digital supply (I_{DVDD33})		44	51	mA
P_{TOTANA}	Total Power Consumption (Analog Input, XGA@75Hz, 78.75MHz)		1.25	1.48	W

* *Measured at nominal voltage supplies*

** *Measured at +10% voltage supplies*

Table 37: ADE3700xs

Symbol	Parameter	Min	Typ*	Max**	Unit
	Supply Current (Analog Input, XGA@75Hz, 135MHz)				
I_{AVDD18}	1.8V analog supply (I_{AVDD18})		200	207	mA
I_{DVDD18}	1.8V digital supply (I_{DVDD18})		351	401	mA
I_{AVDD33}	3.3V analog supply ($_{IAVDD33}$)		104	108	mA
I_{DVDD33}	3.3V digital supply (I_{DVDD33})		68	80	mA
P_{TOTANA}	Total Power Consumption (Analog Input, XGA@75Hz, 135MHz)		1.56	1.89	W

* *Measured at nominal voltage supplies*

** *Measured at +10% voltage supplies*

3.3 Nominal Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD18 DVDD18 XVDD18 LVDD18	Supply Voltage	1.71	1.8	1.89	V
AVDD33 DVDD33	Supply Voltage	3.135	3.3	3.465	V
f_{XTAL}	Crystal Frequency		27		MHz
T_{OPER}	Ambient Operating Temperature	0		+70	°C

3.4 Preliminary Thermal Data

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_{thJA}	Junction-to-Ambient Thermal Resistance, 144-pin package			25	°C/W
R_{thJA}	Junction-to-Ambient Thermal Resistance, 128-pin package			35	°C/W

3.5 Preliminary DC Specifications

Test Conditions: DVDD33 = AVDD33 = 3.3V, DVDD18 = AVDD18 = XVDD18 = LVDD18 = 1.8V and T_{AMB} = 25°C

3.5.1 LVTTL 5 Volt Tolerant Inputs With Hysteresis

YUV[0:7], YUVCLK, HSYNC, VSYNC, CSYNC, TCON_IN, SCL, RESETN

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{HYST}	Schmitt Trigger Hysteresis		0.4			V

3.5.2 LVTTL 5 Volt Tolerant Inputs

XCLK_EN

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V

3.5.3 LVTTL 5 Volt Tolerant I/O With Hysteresis

SDA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{HYST}	Schmitt Trigger Hysteresis		0.4			V

3.5.4 LVTTL Outputs

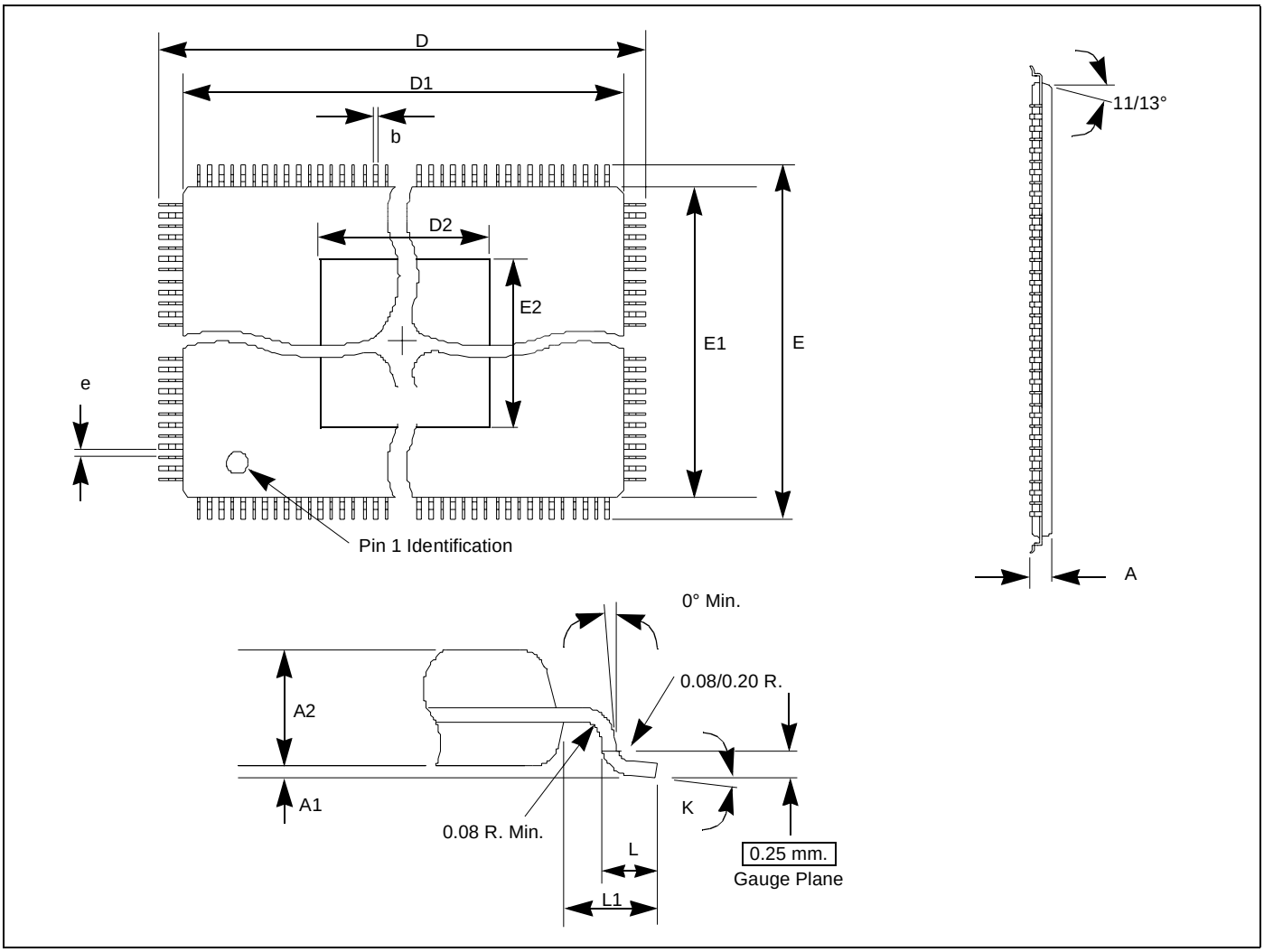
OBA[0:7], OGA[0:7], ORA[0:7], OBB[0:7], OGB[0:7], ORB[0:7], OHS, OVS, ODE, OCLK

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IH}	High Level Input Current	VIN = VDD			-10	µA
I_{IL}	Low Level Input Current	VIN = 0V			10	µA

3.6 Preliminary AC Specifications

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Vrsds_diff	RSDS Differential Output Voltage	RSDS mode	100	200	400	mV
Vrsrs_cm	RSDS Common Mode Output Voltage	680 ohm + 50 ohm external termination to 1.3V	1.1	1.3	1.5	V
Trise, Tfall	RSDS Transition Time To 90%	CL = 30pF			3	ns
INL	ADC Integral Nonlinearity (9-bit)			1.5		LSB
DNL	ADC Differential Nonlinearity (9-bit)	no missing codes		1.5		LSB
Vadc_in	ADC Input Voltage Range		0.5		1	Vp-p
ENOB	ADC Effective Number Of Bits	135 MSPS Input = 65 MHz sine at 95% FS		7.5		bits
Radc_in	ADC Input Resistance			200		Kohms
Cadc_in	ADC Input Capacitance				8	pF
Fadc	ADC Sample Frequency		20		140	MHz
ADC gain step	ADC Gain Step Size			0.05		dB
ADC offset step	ADC Offset Step Size			4		mV
Cadc_ext	ADC External AC Coupling Cap			0.1		uF

4 Package Mechanical Data



	Dimensions (mm)			Dimensions (inches)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.600			0.063
A1			0.150			0.006
A2	1.400	1.350	1.450	0.055	0.053	0.057
b	0.220	0.170	0.270	0.009	0.007	0.011
D	22.000			0.866		
D1	20.000			0.787		
D2						
E	16.000			0.623		
E1	14.000			0.551		
E2						
e	0.500			0.020		
L	0.600	0.450	0.750	0.024	0.0178	0.030
L1	1.000			0.040		
K		0.000	7.000		0.000	0.275

5 Revision History

Table 38: Summary of Modifications

Date	Version	Description
12 August 2002	0.1	First Draft
23 August 2002	0.2	Addition of diagram on Cover. Modification of Description and Product Selector info on 1st page. Modification of Section 2.7.1: Functional Description (SMUX) and Table 11: Sync Multiplexer Registers. Modification of Table 7: Line Lock PLL Registers, Table 14: Data Measurement Registers, Table 15: LCD Scaler Registers and Table 24: Flicker Registers.
17 October 2002	0.3	Device named changed from ADE3700X to ADE3700. Modification of block diagram and table on cover.
26 Nov 2002	0.4	Modification of registers SMEAS_V_CTRL and GLBL_INCLK_GATE_CTRL
4 Dec 2002	0.5	Modification of package data (128-pin LQFP).
9 Jan 2003	0.6	Changes to Pin Description information. Update of Timing Controller information.
10 July 2003	0.7	Inclusion of Section 3.2: Power Consumption Matrices on page 84.

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