ADC32RF80 Dual-Channel, 14-Bit, 3.0-GSPS, RF Sampling Wideband Receiver and Feedback IC

1 Features

- Dual-Channel
- Maximum Clock Rate: 3.0-GSPS
- 14-Bit
- Noise Floor: –155 dBFS/Hz
- RF Input Supports Up to 4.0 GHz
- Aperture Jitter: 70 f_S
- Channel Isolation: 80 dB at f_{IN} = 1.8 GHz
- Spectral Performance (f_{IN} = 900 MHz):
  - SNR: 60.6 dBFS
  - SFDR: 65 dBc HD2, HD3
  - SFDR: 75 dBFS Non HD2, HD3
- Spectral Performance (f_{IN} = 1.78 GHz):
  - SNR: 58.0 dBFS
  - SFDR: 63 dBc HD2, HD3
  - SFDR: 72 dBFS Non HD2, HD3
- On-Chip Digital Down-Converters:
  - Up to 4 DDCs (Dual-Band Mode)
  - Up to 3 Independent NCOs per DDC
- On-Chip Input Clamp for Overvoltage Protection
- Programmable On-Chip Power Detectors with Alarm Pins for AGC Support
- On-Chip Dither
- On-Chip, 50-Ω Input Termination
- Input Full-Scale: 1.35 V_{PP}
- Support for Multi-Chip Synchronization
- JESD204B Interface:
  - Subclass 1-Based Deterministic Latency
  - 4 Lanes Per ADC at 12.3 Gbps
- Power Supply:
  - 1.9 V (Analog), 1.2 V (Analog), 1.15 V (Digital)
- Power Dissipation: 3.2 W/Ch at 3.0 GSPS
- 72-Pin VQFN Package (10 mm × 10 mm)

2 Applications

- Multi-Band, Multi-Mode 2G, 3G, 4G Cellular Receivers
- Multi-Carrier Multi-Mode Cellular Infrastructure Base Stations
- Telecommunications Receiver
- Telecom DPD Observation Receiver

3 Description

The ADC32RF80 is a 14-bit, 3.0-GSPS, dual-channel, telecom receiver and feedback IC that supports RF sampling with input frequencies up to 4 GHz and beyond. Designed for high signal-to-noise ratio (SNR), the ADC32RF80 delivers a noise spectral density of –155 dBFS/Hz as well as excellent dynamic range and channel isolation over a large input frequency range. The buffered analog input with on-chip termination provides uniform input impedance across a wide frequency range and minimizes sample-and-hold glitch energy.

Each ADC channel is connected to a dual-band, digital down-converter (DDC) with up to three independent, 16-bit numerically-controlled oscillators (NCOs) per DDC for phase-coherent frequency hopping. Additionally, the ADC is equipped with front-end peak and RMS power detectors and alarm functions to support external automatic gain control (AGC) algorithms.

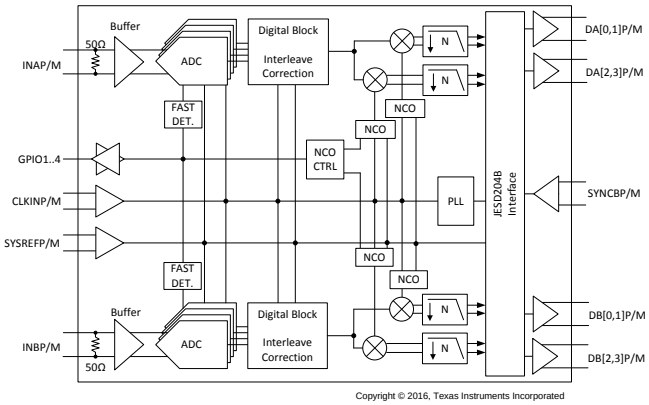
The ADC32RF80 supports the JESD204B serial interface with subclass 1-based deterministic latency using data rates up to 12.3 Gbps with up to four lanes per channel. The device is offered in a 72-pin VQFN package (10 mm × 10 mm) and supports the industrial temperature range (–40°C to +85°C).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC32RF80	VQFN (72)	10.00 mm × 10.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



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PRODUCT PREVIEW

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCT PREVIEW Information. Product in design phase of development. Subject to change or discontinuance without notice.

4 Device and Documentation Support

4.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

4.2 Trademarks

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4.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PRODUCT PREVIEW

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC32RF80IRMPR	PREVIEW	VQFN	RMP	72	1500	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 85	AZ32RF80	
ADC32RF80IRMPT	PREVIEW	VQFN	RMP	72	250	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 85	AZ32RF80	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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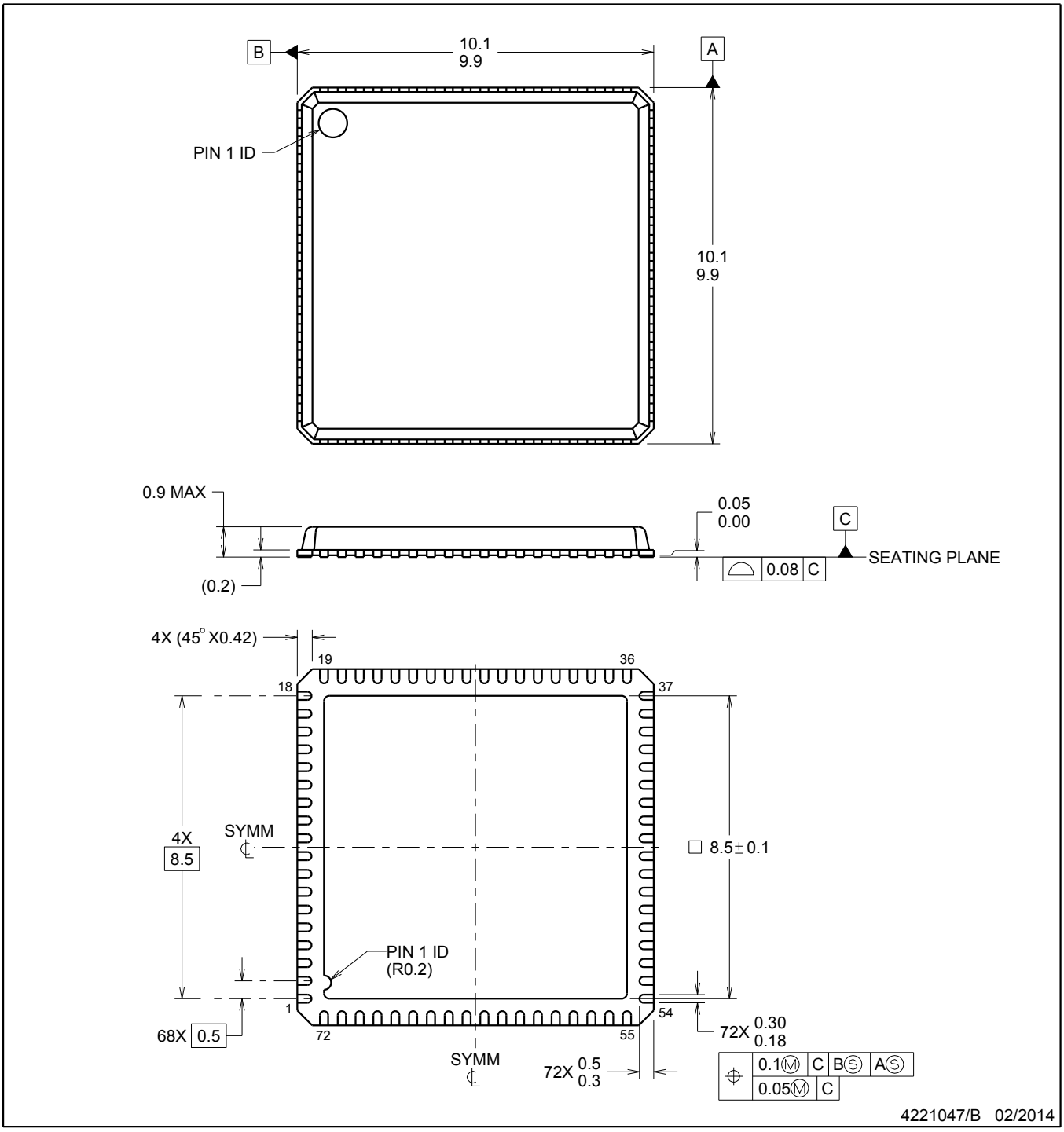
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PACKAGE OUTLINE

RMP0072A

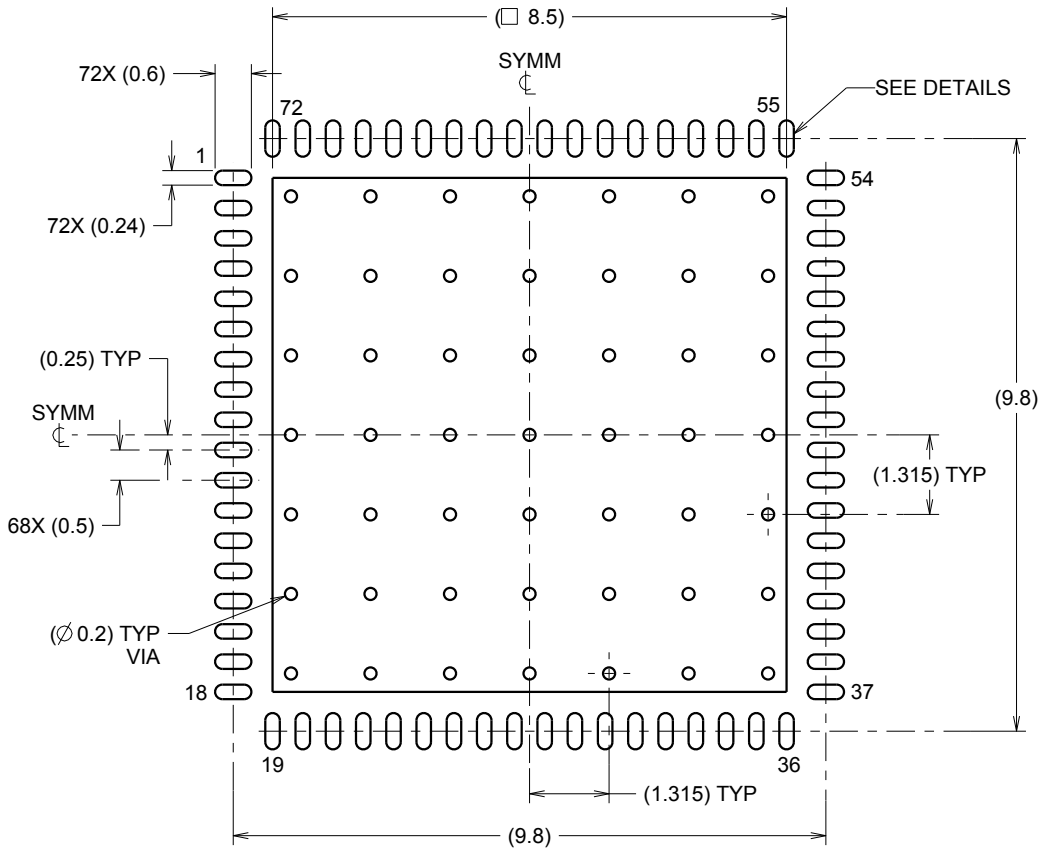
VQFN - 0.9 mm max height

VQFN

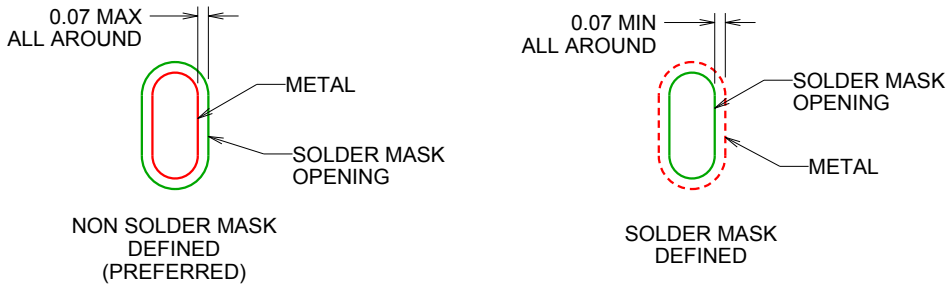


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X

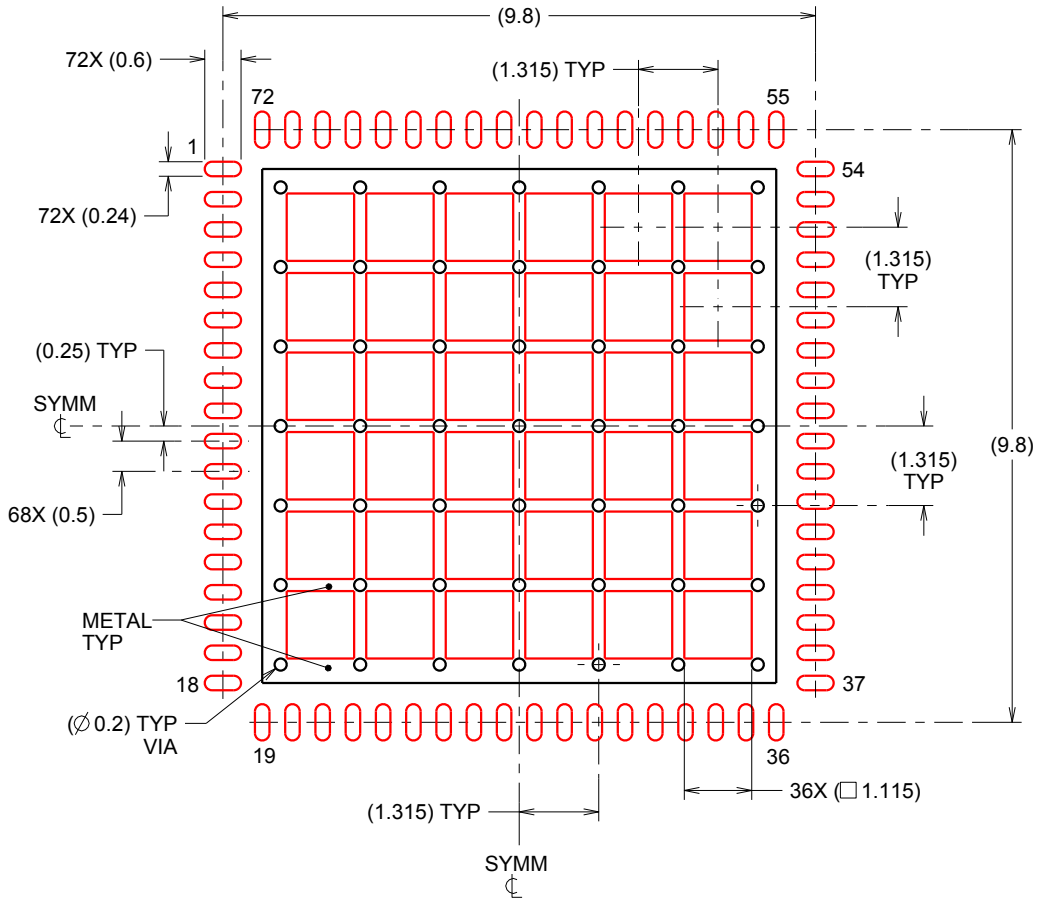


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
62% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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